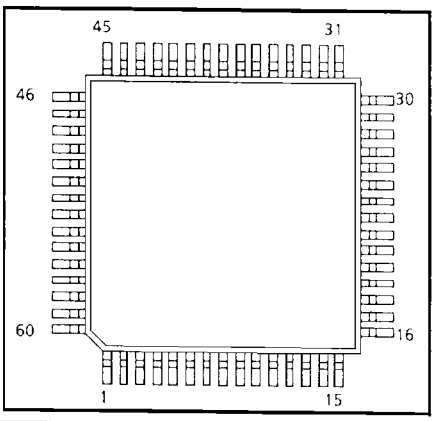
TC8605F

Floppy Disk Mechanism Controller

1. GENERAL DESCRIPTION

TC8605F is a single chip C-MOS LSI for the floppy disk drive digital control logic, consisting of a 4 bit CPU and required random logic. This LSI has input terminal for direct reception of the floppy disk drive system interface terminal inputs, such controls as step-motor, etc, which are the internal mechanisms of floppy disk drive, and read/write circuit control signal inputs, and the digital control board in the present floppy disk drive can be replaced by this LSI.

TC8605F has a firmware already mounted to the ROM of the built-in CPU and therefore, is readily usable for 3.5inch floppy disk drive.



NO.	IO	PIN NAME	NO	IO	PIN NAME
1	I	-DIR	31	I	LEDSEL
2	I	-SISEL	32	O	EJTON
3	I	-DCR	33	O	DSOUT
4	I	-DS	34	O	RWFTR
5	I	-RDDPI	35	O	SMPS
6	O	HD0	36	O	LED
7	O	-ERA	37	O	RWPWR
8	O	-WE	38	O	PWRON
9	O	SWFTR1	39	O	LEDSCN
10	I	TEST	40	O	MTREN
11	I	XIN	41	O	PHASE1
12	O	XOUT	42	O	PHASE2
13	I	-CLR	43	O	PHASE3
14	I	-EJECT	44	O	PHASE4
15	I	WPSNS	45	G	VSS
16	I	-TZSNS	46	O	DSKCHG
17	I	IXSNS	47	O	TRK00
18	I	-EJSW	48	O	INDEX
19	I	-DISNS	49	O	READY
20	I	PHRATE	50	O	WP
21	I	DRT0	51	O	RDDPO
22	I	FWSEL0	52	O	HLDRDY
23	V	VDD	53	V	VDD
24	G	VSS	54	G	VSS
25	I	FWSEL1	55	I	-HACTV
26	I	FWSEL2	56	I	-INUSE
27	I	MECNT	57	I	-WG
28	I	DRT1	58	I	HDMODE
29	I	TMODE	59	I	-MTRON
30	I	AUTORZ	60	I	-STEP

2. FEATURES

- Low power consumption by the Si-gate CMOS technology
- Fully compatible with TLCS-47 4 bit CPU
- System interface directly connected input terminals (TTL compatible threshold)
- Various specifications on 3.5inch floppy disk drive
- Various application for stepping motor driver
- Built-in R/W IC control circuit
- FDD aging function
- Built-in sensor (Photo-diode) input
- 60PIN mini FP

3. TC8605F and APPLICATION SYSTEM

3.1 OUTLINE

TC8605F is a floppy disk mechanism controller (FDMC) provided with the various option selecting functions for 3.5 inch floppy disk drive (FDD). By means of replacing the internal CPU of the TC8601F or the TC8603F, which is the conventional type of the FDMC for 3.5 inch disk, with the CPU having the doubled performance (processing speed and firmware capacity), the TC8605F is made possible to control functions with higher precision and the abundant selecting functions. Through selecting the functions, the standard 3.5 inch FDD can be fabricated with the functions shown below.

3.1.1 DISK TYPE SELECT

(1) 1.0M byte and 500K byte drive

These types are of the FDD construction which can fabricate the 1.0M byte and the 500K byte drives by means of employing the 1-phase/1-track or 2-phase/1-track as the stepping motor phase shifting mode through using the same structural parts except the R/W head.

1.0M byte mode :	Rotation speed 300 rpm Data transfer rate 250 Kbps Number of tracks 80
500K byte mode :	Rotation speed 300 rpm Data transfer rate 250 Kbps Number of tracks 40

(2) 1.0M byte/1.6M byte compatible drive

This is the user programmable drive type with the external input of the drive.

1.0M byte mode :	Rotation speed 300 rpm Data transfer rate 250 Kbps Number of tracks 80
1.6M byte mode :	Rotation speed 360 rpm Data transfer rate 500 Kbps Number of tracks 77

These modes are changed over during the normal operation.

☐ 1.0M byte/2.0M byte compatible drive

This is also user programmable drive type with the external input of the drive. 2M byte drive is the so-called doubled-double density recording FDD of the unformat 2M byte capacity.

1.0M byte mode :	Rotation speed 300 rpm Data transfer rate 250 Kbps Number of tracks 80
2.0M byte mode :	Rotation speed 300 rpm Data transfer rate 500 Kbps Number of tracks 80

These modes are changed over during the normal operation.

3.2 SYSTEM OUTLINE

The position of the FDMC in the FDD (Floppy Disk Drive) is shown in FIG.3.2. The TC8605F receives the control signal from the host to control the drive digitally. While the read/write signal of the FDD is processed by the R/W IC, the timing of the write enable and the erase enable are properly controlled by the TC8605F. As the structural parts of FDD, the stepping motor for head positioning and the spindle motor for media rotating are provided. The TC8605F generates the signals necessary for controlling these structural parts.

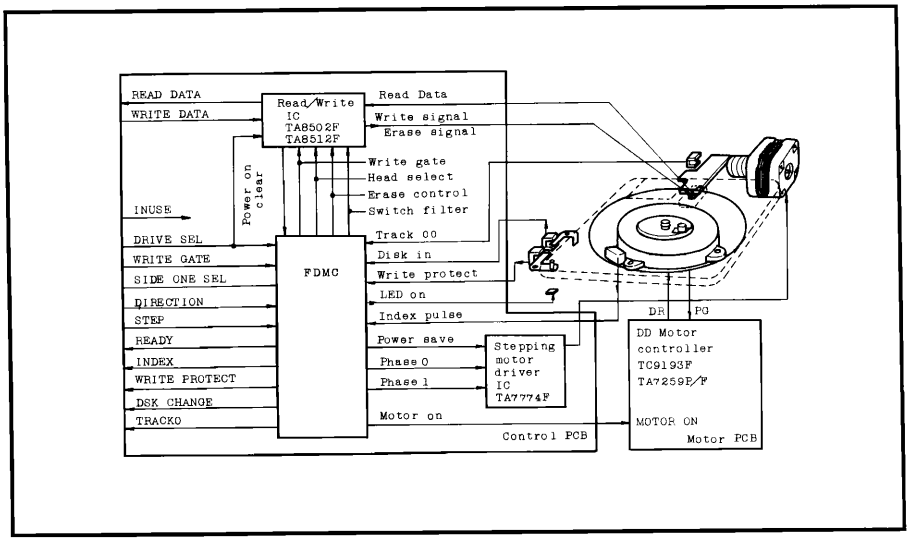


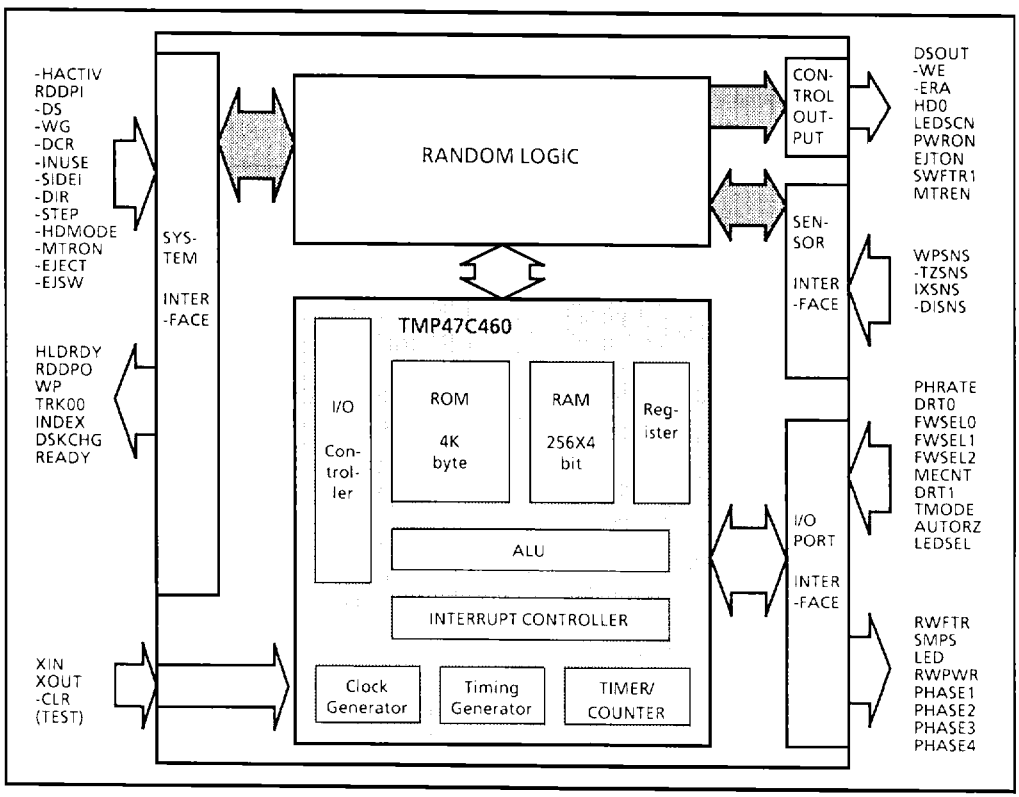
FIG.3.2 FDD SYSTEM DIAGRAM

3.2.1 OUTLINE of SYSTEM OPERATION

The initializing operation and the normal operation are available as the system operation using the TC8605F. By the initializing operation, the function selection input is read to select the various functions and the initialization of the structural parts is performed. As the initialization of the structural parts, the operation (re-calibration) is available which moves the head to the track 0 to make the track counter is the TC8605F matched to the physical position of the head.

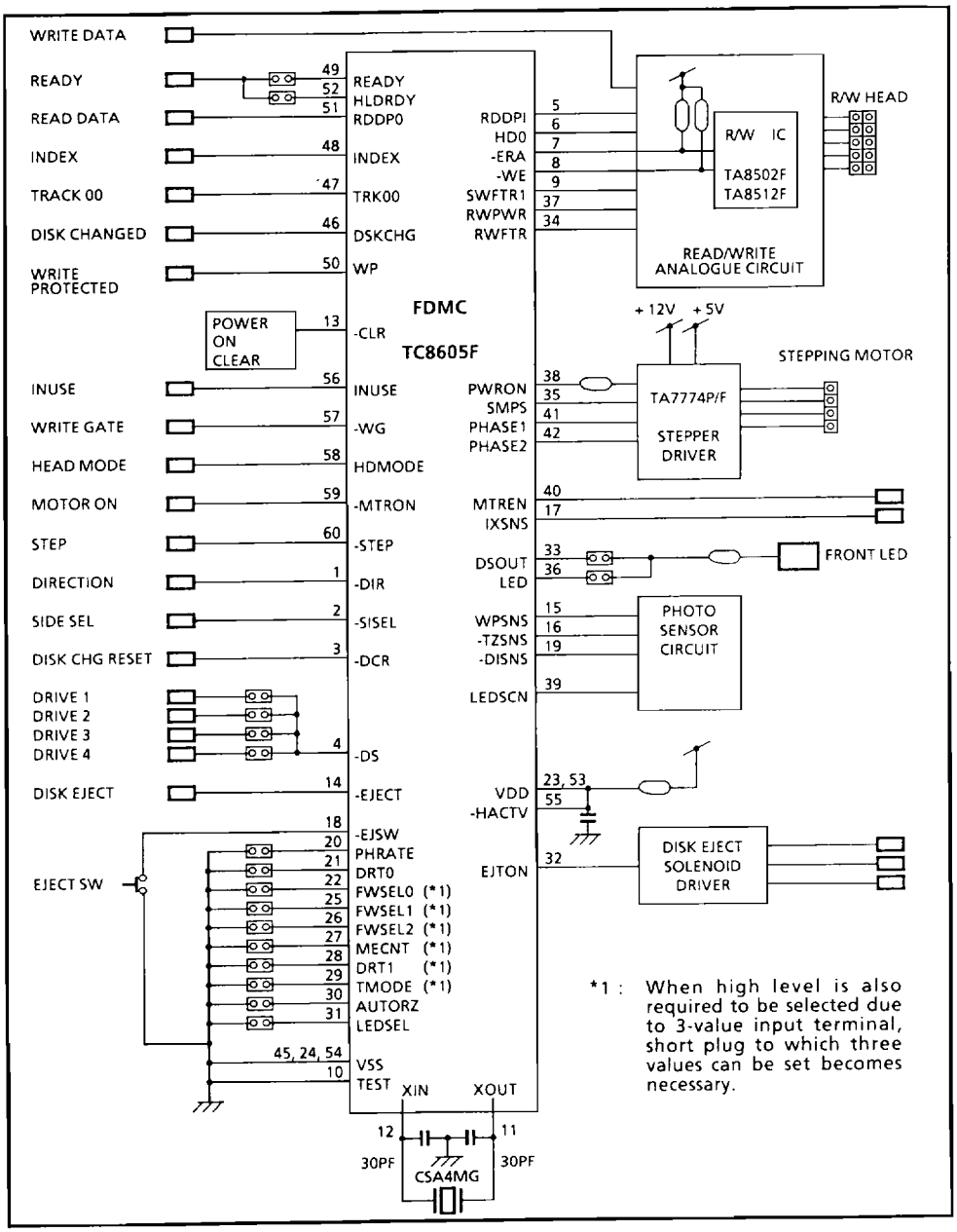
The operation of the stepping motor with the external step pulse, the generation of the ready signal with the index pulse detection, the automatic chucking operation with the disk-in detection and the processing of the write enable (WE) and erase generated depending on the write signal from the system are available as the normal operations. In these processing, the parameters for various timings are available, of which values are determined by the value that is read during the initializing operation and the state of the program terminal which is repeatedly by the polling loop during the normal operation.

3.3 BLOCK DIAGRAM



TC8605F BLOCK DIAGRAM

3.4 EXAMPLE of SYSTEM STRUCTURE



*1 : When high level is also required to be selected due to 3-value input terminal, short plug to which three values can be set becomes necessary.

4. PIN DESCRIPTION

NO.	PIN NAME	IO	FUNCTION
1	-DIR	I	Connect to DIRECTION terminal of system interface.
2	-SISEL	I	Connect to SIDE SELECT terminal of system interface.
3	-DCR	I	Connect to DISK CHANGE RESET terminal of system interface.
4	-DS	I	Connect to DRIVE SELECT terminals of system interface.
5	RDDPI	I	Input for READ DATA output of read/write IC.
6	HD0	O	R/W circuit control signal. Head 0 select signal.
7	-ERA	O	R/W circuit control signal. The delayed erase signal for tunnel erase head is supplied in negative logic. Open drain output.
8	-WE	O	R/W circuit control signal. Write enable signal for head is supplied in negative logic. Open drain output.
9	SWFTR1	O	R/W circuit control signal. Output for controlling the parameter of read/write circuit with relation to track position. This signal will be activated when the track position is inner than 44 track (60 track is also selectable).
10	TEST	I	Test pin of LSI which is normally kept at low level.
11	XIN	I	Ceramic oscillating resonator connection pin.
12	XOUT	O	Ceramic oscillating resonator connection pin.
13	-CLR	I	System reset pin of LSI. Low level signal is needed for the initialization of LSI when power is on application.
14	-EJECT	I	Connect to EJECT terminal of system interface.
15	WPSNS	I	Sensor input. Signal, which becomes high level in state the disk is protected, is input.
16	-TZSNS	I	Sensor input. Signal, which becomes low level in state the head is located on 0 track, is input.
17	IXSNS	I	Sensor input. Index signal is input in positive logic.
18	-EJSW	I	Input of eject switch signal of drive. Latched by internal FF at falling edge, eject timer starts.
19	-DISNS	I	Sensor input. Signal, which becomes low level in state the disk is inserted, is input.
20	PHRATE	I	Phase-rate selection input terminal of stepper. When this terminal is set at high level, phase rate becomes 1.5m sec and at low level, 30m sec.
21	DRT0	I	Program input for function selection.
22	FWSEL0	I	Program input for function selection. 3-valued threshould input terminal.
23	[VDD]	I	Power supply input of LSI. + 5V is supplied.

NO.	PIN NAME	IO	FUNCTION
24	[VSS]	I	Power supply input of LSI. Connection to GND of FDD circuit.
25	FWSEL1	I	Program input for function selection. 3-valued threshould input terminal.
26	FWSEL2	I	Program input for function selection. 3-valued threshould input terminal.
27	MECNT	I	[MTREN] output control input. 3-valued threshould input terminal.
28	DRT1	I	Program input for function selection. 3-valued threshould input terminal.
29	TMODE	I	Program input for determining operation mode of FDD.
30	AUTORZ	I	Program input for function selection.
31	LEDSEL	I	Input for selecting the requirements for controlling the lighting of front panel LED.
32	EJTON	O	Eject Timer output. Since falling edge of [-EFJECT] or [-EJSW], high level is output for 500ms.
33	DSOUT	O	Positive logic output of [-DS] input of system interface. When [-CLR] is at high level and [-DS] is at low level at the same time, output becomes high level.
34	RWFTR	O	R/W circuit control signal. Filter constant selection signal. This output becomes low level when [ODE] input is high level, otherwise becomes high level.
35	SMPS	O	This output pin will be activated to High level when the system cut off the + 12V power supply to stepping motor.
36	LED	O	Front panel LED control output.
37	RWPWR	O	R / W head drive circuit control signal.
38	PWRON	O	Power supply control output for stepping motor.
39	LEDSCN	O	Sensor LED lighting control output. In standby state, low level is output so as to reduce power consumption.
40	MTREN	O	Spindle motor control output. Used at high level with spindle motor set to on. Controlled by [-MTRON] of system interface input and auto chucking function.
41	PHASE1	O	Stepping motor phase control output. 1st phase.
42	PHASE2	O	Stepping motor phase control output. 2nd phase.
43	PHASE3	O	Output to be determined by function selection program terminal.
44	PHASE4	O	Output to be determined by function selection program terminal.
45	[VSS]	I	Power supply pin of LSI. Connected to GND of FDD circuit.
46	DSKCHG	O	Connect to -DISK CHANGE terminal of system interface.
47	TRK00	O	Connect to -TRACK0 terminal of system interface.
48	INDEX	O	Connect to -INDEX terminal of system interface.

NO.	PIN NAME	IO	FUNCTION
49	READY	O	Connect to -READY terminal of system interface.
50	WP	O	Connect to -WRITE PROTECTED terminal of system interface.
51	RDDPO	O	AND output of READ DATA from read/write IC and DRIVE SELECT of system interface.
52	HLDRDY	O	Hold ready/high density output terminal. Function either of ready/high density is selected by the function selection program terminal. Though the preparing condition for hold ready is the same as that for READY, once the ready state is obtained, the active state is maintained until the power supply is turned off or the disk is pulled out. By the high density function, the signal which is input to HDMODE is input to the system interface.
53	[VDD]	I	Power supply pin of LSI. + 5V is supplied.
54	[VSS]	I	System ground pin of LSI.
55	-HACTV	I	Output mode of each output terminal of [WP], [TRK00], [INDEX], [DSKCHG], [READY], [HLDRDY] or [RDDPO] is controlled. When this terminal is at low level, each output terminal is turned into the mode in which each terminal is connected to the system interface terminal via the open collector inverting buffer. When this terminal is at high level, each output terminal is turned into the mode in which each output terminal is directly connected to system interface terminal.
56	-INUSE	I	Connect to INUSE terminal of system interface.
57	-WG	I	Connect to WRITE GATE terminal of system interface.
58	HDMODE	I	Program input terminal for function selection.
59	-MTRON	I	Connect to MOTOR-ON terminal of system interface.
60	-STEP	I	Connect to STEP terminal of system interface.

5. FUNCTIONAL SPECIFICATION

5.1 FUNCTION SELECTION

5.1.1 DRIVE MODE SELECTION

The TC8605F is provided with ten kinds of function selection terminals (DRT0, DRT1, FWSEL0, FWSEL1, FWSEL2, MECNT, PHRATE, TMODE, AUTORZ and LEDSEL). Among them, two input of HDMODE and LEDSLO are repeatedly evaluated during the normal operation, however, the other eight input are evaluated only once when LSI's power is on (after -CLR is released from low level to high level).

The function selection performs the control at the index interval (ready preparing requirement) effective for each drive model as shown in TABLE 5.1.1a by the three terminals of DRT0, DRT1 and HDMODE. Also at of high density/low density compatible drive mode, the erase delay timing is set to make read/write possible in both modes. TABLE 5.1.1b shows the erase delay timings determined by the function selection terminals (DRT0, DRT1 and HDMODE).

TABLE 5.1.1a FUNCTION SELECTION MAP 1

DRT0	DRT1	HDMODE	FDD MODEL *1, *2	MODEL MODE	NUMBER OF TRACKS	Spindle Rotational Frequency*3	Rotation MODE	INDEX INTERVAL
H	H	H	2/1MB	2.0MB	80	300rpm	300rpm	160-240ms
H	H	L	2/1MB	1.0MB	80	300rpm	300rpm	160-240ms
H	L	H	1.6/1MB	1.6MB	77	300/360rpm	360rpm	126-240ms
H	L	L	1.6/1MB	1.0MB	80	300/360rpm	300rpm	160-240ms
H	Z*4	H	1MB	1.0MB	80	300rpm	300rpm	160-240ms
H	Z*4	L	500KB	500KB	40	300rpm	300rpm	160-240ms
L	H	H	2/1MB	2.0MB	80	300rpm	300rpm	160-240ms
L	H	L	2/1MB	1.0MB	80	300rpm	300rpm	160-240ms
L	L	H	1.6/1MB	1.6MB	77	300/360rpm	360rpm	126-240ms
L	L	L	1.6/1MB	1.0MB	80	300/360rpm	300rpm	160-240ms
L	Z*4	H	1MB	1.0MB	80	300rpm	300rpm	160-240ms
L	Z*4	L	500KB	500KB	40	300rpm	300rpm	160-240ms

*1 : 2/1MB means a type of FDD which can be modified 2M byte or 1M byte in using same mechanism. The FDD of so-called doubled-double density, which transfers the data at 500Kbps with the spindle rotation of 300rpm, is considered for the 2M byte drive.

*2 : 1.6/1MB means a type of FDD which can be modified 1.6M byte or 1M byte in using same mechanism.

*3 : Rotation speed prepared for the drive is indicated.

*4 : Open circuit.

TABLE 5.1.1b FUNCTION SELECTION MAP 2

DRT0	DRT1	HDMODE	FDD MODEL *1, *2	MODEL MODE	ERASE TIMING (μs)		GAP of HEAD	AUTORZ SPSEEK *3	Rotation Mode
					ON DELAY	OFF DELAY			
H	H	H	2/1MB	2.0MB	176-188	508-520	300μm	AUTORZ	300rpm
H	H	L	2/1MB	1.0MB	144-156	676-688	300μm	AUTORZ	300rpm
H	L	H	1.6/1MB	1.6MB	176-188	508-520	350μm	AUTORZ	360rpm
H	L	L	1.6/1MB	1.0MB	160-172	724-736	350μm	AUTORZ	300rpm
H	Z*4	H	1MB	1.0MB	320-332	932-944	600μm	Selection	300rpm
H	Z*4	L	500KB	500KB	320-332	932-944	600μm	Selection	300rpm
L	H	H	2/1MB	2.0MB	216-228	564-576	350μm	SPSEEK	300rpm
L	H	L	2/1MB	1.0MB	160-172	724-736	350μm	SPSEEK	300rpm
L	L	H	1.6/1MB	1.6MB	192-204	532-544	400μm	SPSEEK	360rpm
L	L	L	1.6/1MB	1.0MB	176-188	772-784	400μm	SPSEEK	300rpm
L	Z*4	H	1MB	1.0MB	440-452	1068-1080	700μm	Selection	300rpm
L	Z*4	L	500KB	500KB	440-452	1068-1080	700μm	Selection	300rpm

*1 : 2/1MB means a type of FDD which can be modified 2M byte or 1M byte in using same mechanism.
*2 : 1.6/1MB means a type of FDD which can be modified 1.6M byte or 1M byte in using same mechanism.
*3 : Selection either of the automatic return to zero function or the special seek function is indicated.
*4 : Open circuit.

5.1.2 FUNCTIONAL SELECTION by MECNT and TMODE

By the function selection input MECNT and TMODE, the condition that a spindle motor starts rotating, the spindle motor off-delay and the FDD operation mode are determined as shown in TABLE 5.1.2. If the spindle motor off-delay is being selected, the MTREN output is disabled after the delay of ten seconds when the condition for the spindle motor-off is met. For the operation sequences of the aging mode and the drive test mode shown in the column of the operation mode, refer to FIG.5.1.2a or FIG.5.1.2b. 1PHASE/1TRACK mode is used for the adjustment of track 0 position in the drive of 2PHASE/1TRACK mode, and also is used for 1M byte and 500K byte FDD.

TABLE 5.1.2 FUNCTION SELECTION MAP 3

MECNT	TMODE	SPINDLE MOTOR ENABLE CONDITION	OFF DELAY	OPERATION MODE
H	H	–	–	Aging mode
H	L	DI × MTRON	with	1PHASE/1TRACK mode
H	Z*1	DI × MTRON	with	Normal operation
L	H	–	–	Drive test mode
L	L	MTRON	without	1PHASE/1TRACK mode
L	Z*1	MTRON	without	Normal operation
Z*1	H	DS × DI × MTRON	with	Normal operation
Z*1	L	DI × MTRON	without	1PHASE/1TRACK mode
Z*1	Z*1	DI × MTRON	without	Normal operation

*1 : Open circuit

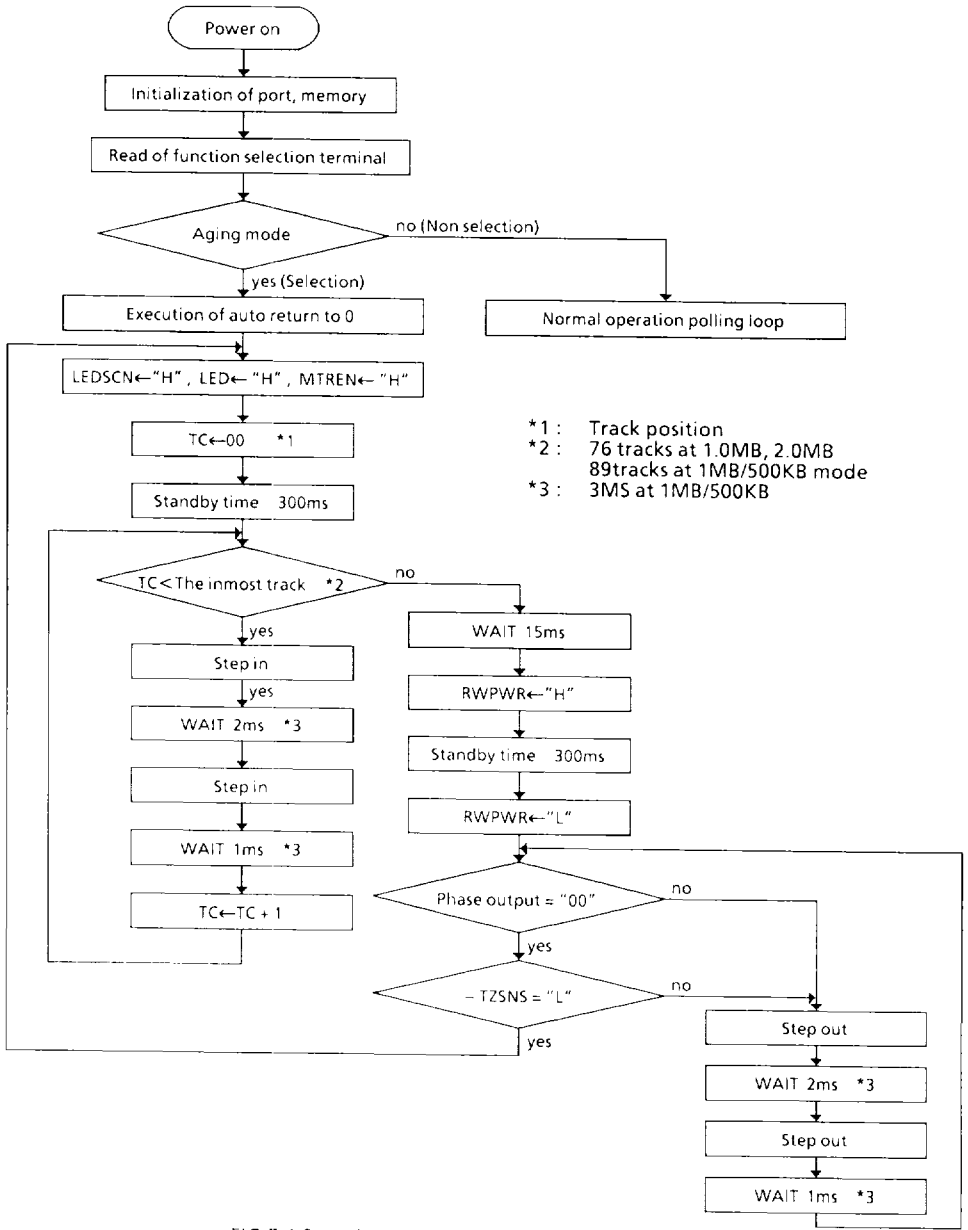


FIG.5.1.2a AGING MODE OPERATION SEQUENCE

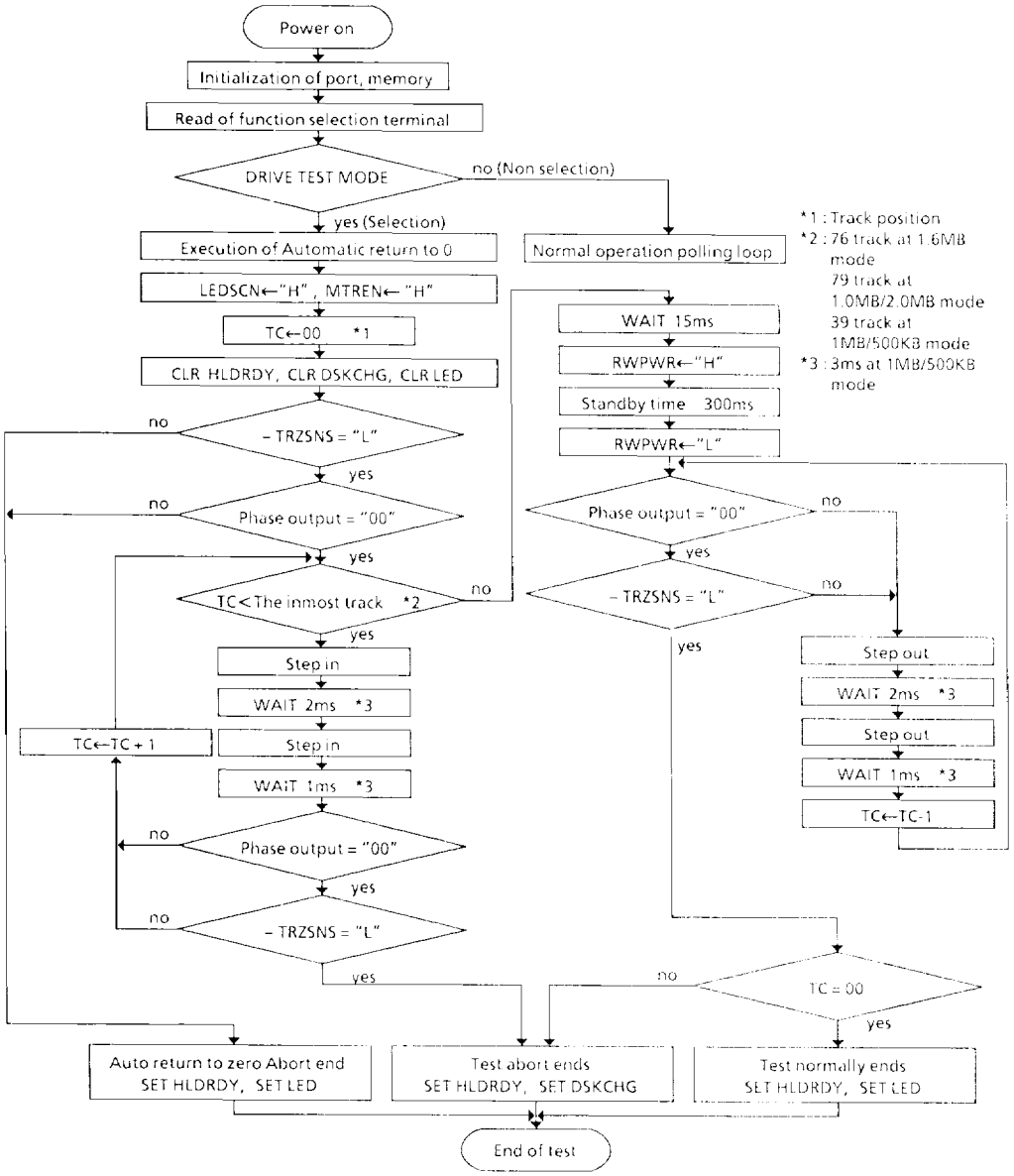


FIG.5.1.2b DRIVE TEST OPERATION SEQUENCE

5.1.3 FUNCTION SELECTION at DRT1 = HIGH or LOW

Functions below are selected by each input of FWSEL0, FWSEL1, FWSEL2 or AUTORZ.

TABLE 5.1.3a FUNCTION SELECTION MAP 4

FWSEL2	FWSEL1	EXCITATION MODE	PHASE3 OUTPUT	PHASE4 OUTPUT	HLDRDY OUTPUT
H	H	1 PHASE	PHASE3	PHASE4	HLDRDY
H	L	1 PHASE	PHASE3	PHASE4	HIDEN
H	Z	2 PHASE	SMPS15	PRDY	HLDRDY
L	H	1-2 PHASE	PHASE3	PHASE4	HLDRDY
L	L	1-2 PHASE	PHASE3	PHASE4	HIDEN
L	Z	2 PHASE	SMPS15	HIPS	HIDEN
Z	H	2 PHASE	SMPS15	HIPS	HLDRDY
Z	L	2 PHASE	XORPHS	PRDY	HIDEN
Z	Z	2 PHASE	XORPHS	PRDY	HLDRDY

TABLE 5.1.3b FUNCTION SELECTION MAP 5

AUTORZ	FWSEL0	STANDBY CONDITION	STANDBY MODE	SWITCH FILTER CHANGEOVER POSITION
H	H	MTRON	MODE 1	44 TRACK
H	L	MTRON	MODE 1	60 TRACK
H	Z	MTRON	MODE 2	44 TRACK
L	H	DS × MTRON	MODE 2	44 TRACK
L	L	DS × MTRON	MODE 1	60 TRACK
L	Z	DS × MTRON	MODE 2	60 TRACK

5.1.4 FUNCTION SELECTION at DRT1 = Z (OPEN)

TABLE 5.1.4a FUNCTION SELECTION MAP 6

AUTORZ	FWSEL0	ARZ/SPSEEK	AUTO CHUCKING	Excitation MODE	PHASE3	PHASE4
H	H	AUTORZ	with	2 PHASE	SMPS15	INUSE
H	L	AUTORZ	without	2 PHASE	SMPS15	INUSE
H	Z	SPSEEK	without	2PHASE	SMPS15	INUSE
L	H	SPSEEK	with	2PHASE	SMPS15	INUSE
L	L	SPSEEK	without	2PHASE	XORPHS	INUSE
L	Z	SPSEEK	without	1-2PHASE	PHASE3	PHASE4

TABLE 5.1.4b FUNCTION SELECTION MAP 7

FWSEL2	FWSEL1	STANDBY CONDITION	STANDBY MODE	SWITCH FILTER CHANGEOVER POSITION
H	H	MTRON	MODE 2	44 TRACK
H	L	DS × MTRON	MODE 2	44 TRACK
H	Z	MTRON	MODE 2	60 TRACK
L	H	DS × MTRON	MODE 2	60 TRACK
L	L	DS × MTRON	MODE 1	60 TRACK
L	Z	MTRON	MODE 1	60 TRACK
Z	*	–	–	–

PHASE3 : Stepping motor phase control output. 3rd phase.
PHASE4 : Stepping motor phase control output. 4th phase.
HIDEN : High density output (Refer to chapter 6.2.5)
SMPS15 : Stepping motor power control output. (Refer to chapter 5.2.1)
PRDY : Pre-ready output (Refer to chapter 5.2.2)
XORPHS : Low level is output at the 1st phase at 2PHASE/1TRACK mode.
HIPS : High level is output at 360rpm of spindle motor. (Refer to chapter 5.2.12)
MODE 1 : SMPS output is not made low level in standby mode control. (Refer to chapter 5.3.3)
MODE 2 : All the stepper control signals are made low level in standby mode control. (Refer to chapter 5.3.3)

5.1.5 SELECTION FUNCTION of FRONT PANEL LED CONTROL

The condition for lighting the front panel LED can be selected by the [LEDSEL] input as shown in TABLE 5.1.5.

TABLE 5.1.5 SELECTION FUNCTION of FRONT PANEL LED

LEDSEL	LED OUTPUT
High	DS or INUSE is output.
Low	Latched INUSE (*1) is output.

*1 : Signal which latch [-INUSE] input at falling edge of [-DS] input

5.1.6 OTHER FUNCTION SELECTION BY AUTORZ, AUTOCK

In case of DRT1 = Z (open), as shown in TABLE 5.1.4a with or without of the automatic chucking function, the automatic return-to-zero function or the special seek function is selected. When DRT = High or Low, the automatic chucking function and is selected either of the automatic return-to-zero function or the special seek function.

AUTOMATIC RETURN-TO-ZERO FUNCTION

The automatic return-to-zero function is a kind of initializing operation which performs re-calibration of track position. This sequence is divided two parts that is, power-on-step-in and return-to-zero seek.

POWER-ON-STEP-IN OPERATION

In this operation, for the first time, the track zero sensor input is evaluated and if the evaluation result is active (ACTIVE means that [TZSNS] input is low level), then FDMC executes inner seek step by step until track-zero sensor is non active. 12 steps (24 phases) are passed over at maximum with the seek rate of 3ms per track. After the track-zero sensor is non active, even if before first time of stepping operation, FDMC goes to next procedure, (the return to zero operation) starts after settling time of 15m seconds for head assembly.

RETURN-TO-ZERO OPERATION

In this operation, FDMC executes outer seek operation until the stepping motor phase becomes 00 (PHASE1, PHASE2, are both at high level) with the track-zero sensor being active. The seeking is performed 100 tracks (200phases) at maximum. After 100 tracks seek is done, the operation ends even if the head does not reach the track-zero position.

The power on step in sequence is for the safe operation in such a drive that has elastic carriage stopper at the track zero position, so as to keep precisioness avoiding mechanical collision. But using such mechanism causes wrong track recalibration, in case that head is located outer track 0, even if start at negative track position by the residue of former status of disk drive.

SPECIAL SEEK FUNCTION

The special seek is a funciton that postpones the recalibrate funciton at power on time, so as to avoid rush current through the all drives by doing the recalibrate operation. This funciton is suitable for battery operation type personal computer. If this function is eslected the FDMC do nothing when the power is on. But theFDMC memorized the status for executing special seek operation when the FDMC receives first step pulse. In that case, when the FDMC receives first step pulse after power is up, the FDMC examines TRACK0 status and if it is active (ACTIVE means on track 0), the FDMC transfer motor phase toward inner direction even if [DIR] input was outer seek. This operation will continue until detecting non track 0 in each operaiton. This function is same as the step in sequence in the automatic return to zero. And because of the first step pulse applied for disk drive is outer direction issued by floppy disk controller, the recalibrate operation completes preisely.

At changing the direction with the special seek function for waiting 15ms settling time, the step pulse which is input during this time is neglected.

AUTOMATIC CHUCKING FUNCITON

The FDMC has a function that rotates spindle motor instantaneously when disk is inserted, so as to get correct chucking of diskette holing mechanism. The spindle motor rotaiton sustains until detecting internal READY or till one second passed.

5.2 CONTROL FUNCTION

5.2.1 STEPPING MOTOR CONTROL

As the type of the stepping motor, either of the type of 1 phase excitaiton, 2 phase excitation, 2-1 phase excitation can be selected (Refer to TABLE 5.1.3a and TABLE 5.1.4a). FDMC outputs the positive phase signal of each phase is output to [PHASE1], [PHASE 2], [PHASE 3] or [PHASE 4]. This signal is turned into the actual driving signal for the stepping motor by using the external current driveing IC.
The step pulse signal [-STEP] from the system interface and the direction signal [-DIR] are sampled at the rising edge timing by the internal circuit. The internal CPU receives these signals as the interruption and starts the renewal process of the phase control signal of hte motor phase output. The step motor power-save output [SMPS], which is used for reducing the driveing current to the step motor at standby time, is connected to the power supply selection terminal of the current driving IC. By this signal, the 12V system or the 5V system of the power supply for the step motor driving is selected. Before the renewal process of the phase control signal, the FDMC negates [SMPS] output if the it is active (it is active during the power-saving). When a specified time (30ms or 15ms) has passed after the completion of the phase renewal operation, the [SMPS] output is made again active by the internal timer (power-save state). FIG.5.2.1a, b shows these timings. In the operaiton of 2 phase/1 track seeking, after the output of hte 1st phase, the 2nd phase is automatically output at programmed phase rate.

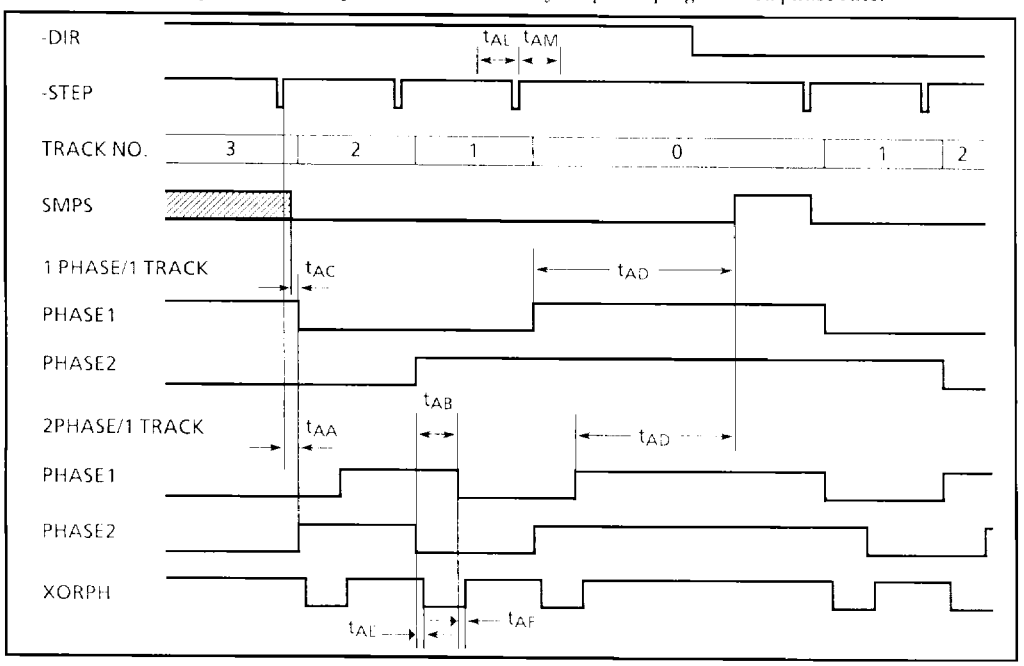


FIG.5.2.1a STEPPING MOTOR CONTROL (2PHASE EXCITATION SYSTEM)

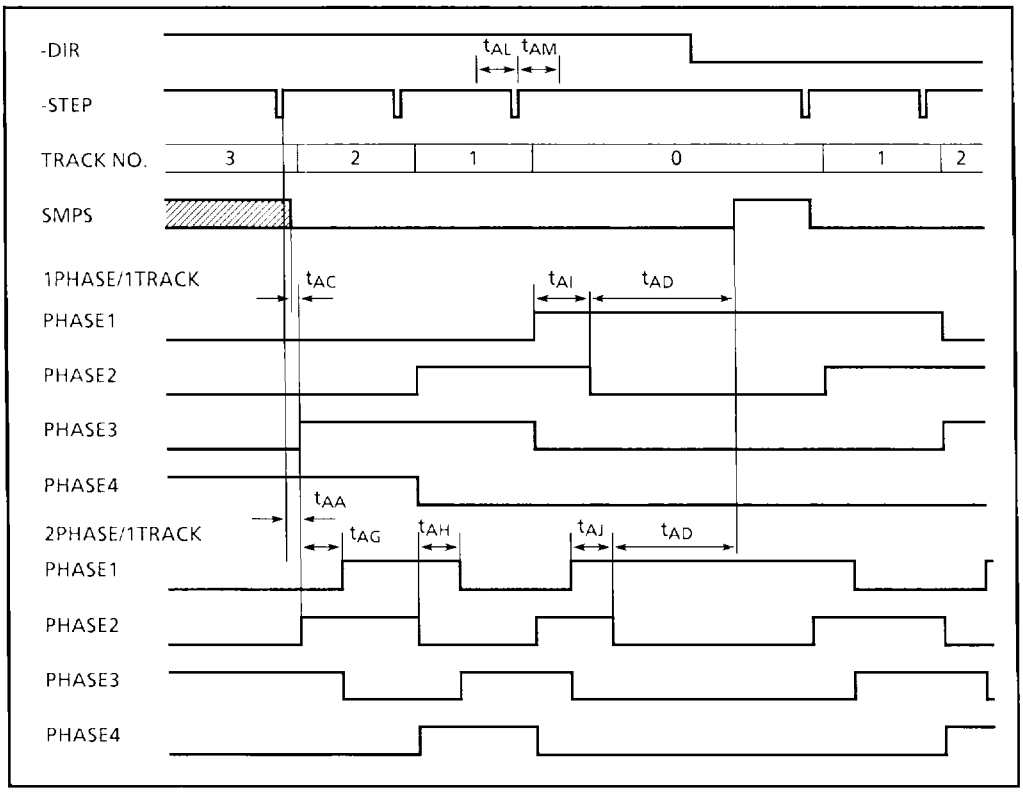


FIG.5.2.1b STEPPING MOTOR CONTROL (2-1 PHASE EXCITATION SYSTEM)

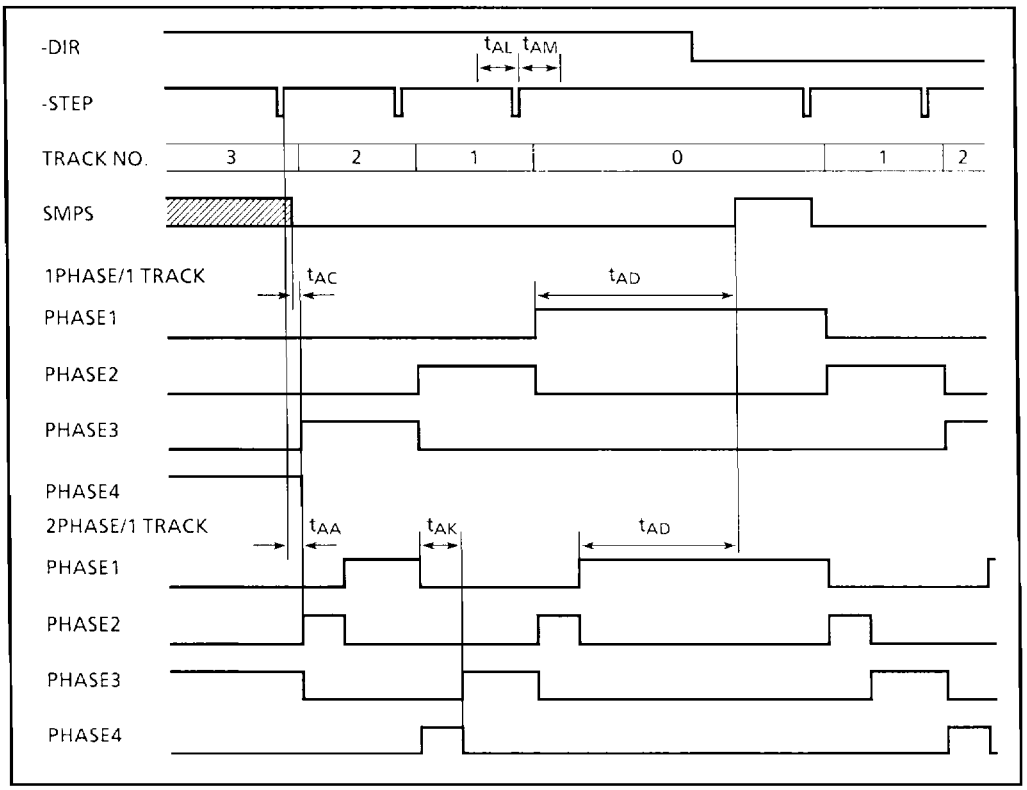


FIG.5.2.1c STEPPING MOTOR CONTROL (1 PHASE EXCITAITON SYSTEM)

TABLE 5.2.1 STEPPING MOTOR CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{AA}	STEP to Phase Shift Delay	160	180	400	μs	
t_{AB}	2nd Phase Starting Delay	1.62	1.80	2.04	ms	Phase Rate = 1.5ms
		2.64	2.80	3.07	ms	Phase Rate = 3.0ms
t_{AC}	SMPS Negate to Phase Shift	70		112	μs	
t_{AD}	Phase Shift to SMPS on	29	30	31	ms	
		14	15	16	ms	SMPS15 OUTPUT
t_{AE}	Phase Shift to XORPH on	30		46	μs	
t_{AF}	Phase Shift to XORPH off	38		48	μs	
t_{AG}	2nd Phase Starting Delay	1.20	1.24	1.30	ms	Phase Rate = 1.5ms
		2.64	2.80	3.05	ms	Phase Rate = 3.0ms
t_{AH}	2nd Phase Starting Delay	1.62	1.78	2.03	ms	Phase Rate = 1.5ms
		2.64	2.80	3.05	ms	Phase Rate = 3.0ms
t_{AI}	Phase to 1Phase Exciting	3.58	3.72	3.98	ms	
t_{AJ}	Phase to 1Phase Exciting	3.02	3.16	3.39	ms	Phase Rate = 1.5ms
		4.04	4.18	4.42	ms	Phase Rate = 3.0ms
t_{AK}	2nd Phase Starting Delay	1.60	1.76	2.00	ms	Phase Rate = 1.5ms
		2.62	2.78	3.03	ms	Phase Rate = 3.0ms
t_{AL}	Set up Time for Direction			200	ns	
t_{AM}	Hold Time for Direction			200	ns	

5.2.2 READY TIMING CONTROL

The internal ready signal is generated by evaluating the interval of the index pulse which is input from the [+IXSNS].

- READY-ON CONDITION

  When FDMC detects succesive two times of the specified interval in the state of disk-in and motor-on.

- READY-OFF CONDITION

  1. When the disk is out or the motor-of state is made.
  2. When the index pulse is not input within the specifed index interval.
  3 When the index pulse is input five times succesively at the interval shorter than the specified index interval.

The specified index intervals are as shown in TABLE 5.2.2a.

Once the ready state is obtained, the [HLDRDY] output keeps its active state until the power supply is turned off or the disk is pulled out. The [PRDY] output is of the same characteristic as the [READY] output excepting the condition which makes the [PRDY] output active. FDMC detects a specified interval of index pulse once, then makes [PRDY] active.

TABLE 5.2.2a SPECIFIED INDEX INTERVAL

SPINDLE MOTOR ROTATIONAL FREQUENCY	MIN.	TYP.	MAX.	UNIT	REMARKS
300rpm	162		239	ms	
360rpm	128		239	ms	

TABLE 5.2.2b INVALID INDEX INTERVAL

SPINDLE MOTOR ROTATIONAL FREQUENCY	MIN.	TYP.	MAX.	UNIT	REMARKS
300rpm	244		157	ms	
360rpm	244		122	ms	

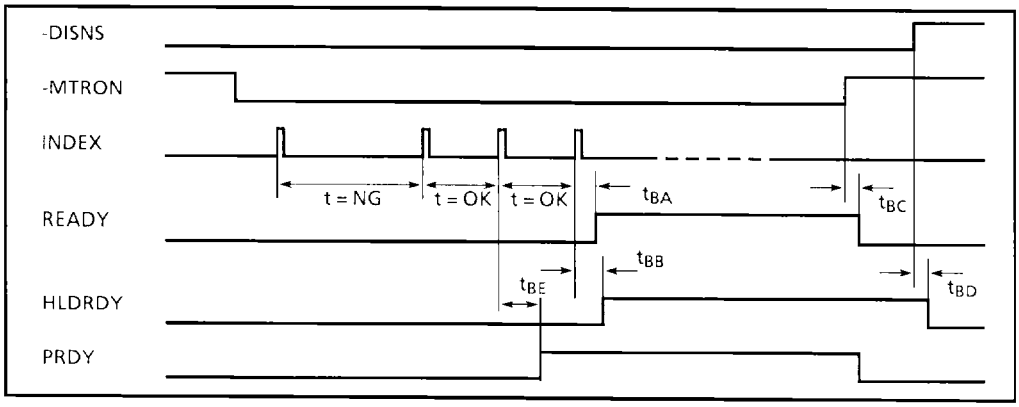


FIG. 5.2.2 READY TIMING CONTROL

TABLE 5.2.2c READY TIMING CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{BA}	INDEX Sensor to READY		0.5	2.5	ms	
t_{BB}	INDEX Sensor to HLDRDY		0.5	2.5	ms	
t_{BC}	MTRON off to READY/PRDY off		0.5	2.5	ms	
t_{BD}	DISNS off to HLDRDY off		0.5	2.5	ms	
t_{BE}	INDEX Sensor to PRDY on	46	47	54	ms	

5.2.3 TRACK-ZERO OUTPUT CONTROL

The [TRK00] outputs the logical AND of the three conditions shown below.

- The track 00 sensor input [-TZSNS] is at low level.
- The step motor output is "00" phase (both PHASE 1 and PHASE 2 are at high level).
- The input [-DS] is at low level.

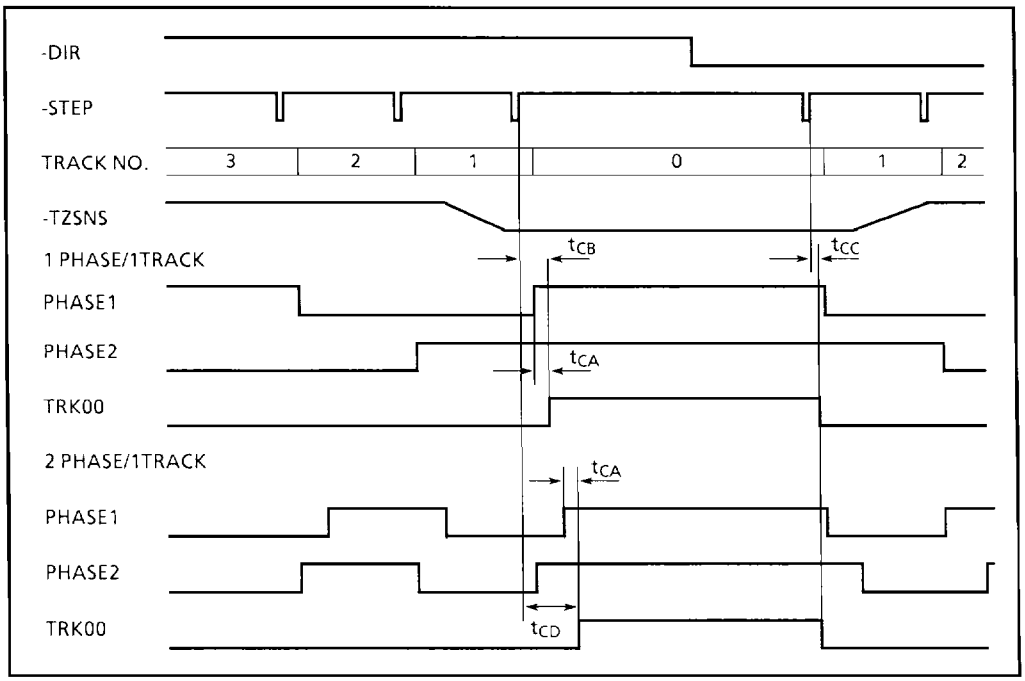


FIG.5.2.3a TRACK-ZERO TIMING (2 PHASE EXCITATION SYSTEM)

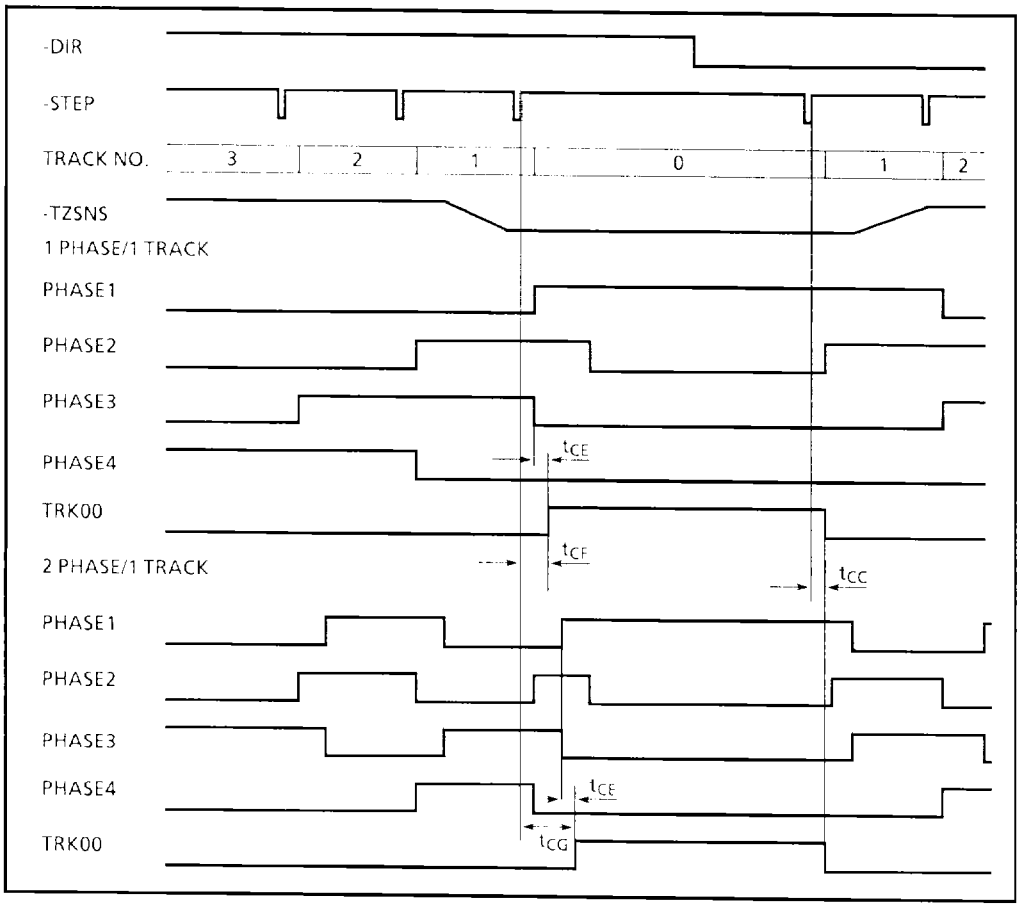


FIG.5.2.3b TRACK-ZERO TIMING (2-1 PHASE EXCITATION SYSTEM)

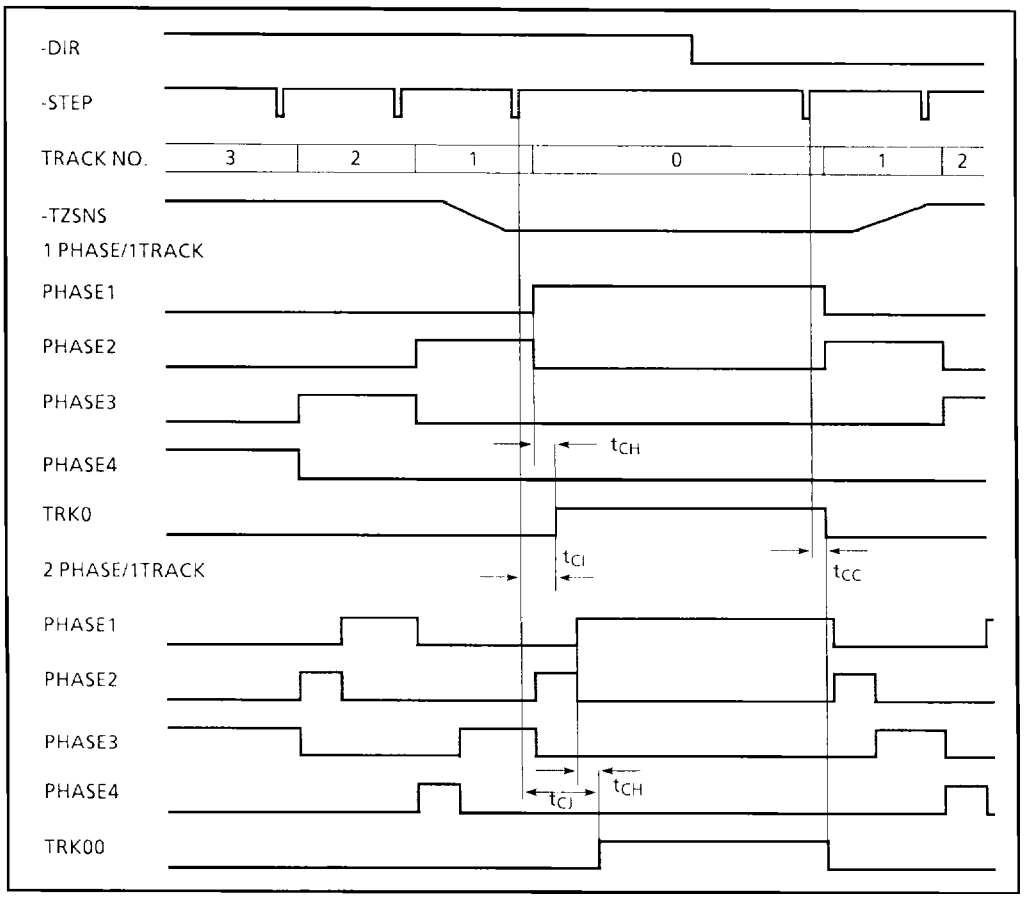


FIG.5.2.3c TRACK-ZERO TIMING (1 PHASE EXCITATION SYSTEM)

TABLE 5.2.3 TRACK-ZERO TIMING

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{CA}	Phase Shift to TRK00 on	60	70	95	μs	
t_{CB}	Step to TRK00 on	220	240	495	μs	1PHASE/1TRACK
t_{CC}	Step to not TRK00	120	140	200	μs	
t_{CD}	STEP to TRK00 on	1.84	2.00	2.50	ms	PHASE RATE = 1.5ms
		2.84	3.00	3.53	ms	PHASE RATE = 3.0ms
t_{CE}	Phase Shift to TRK00 on	60	64	70	μs	
t_{CF}	Step to TRK00 on	220	240	470	μs	1PHASE/1TRACK
t_{CG}	STEP to TRK00 on	1.84	2.00	2.46	ms	PHASE RATE = 1.5ms
		2.86	3.00	3.48	ms	PHASE RATE = 3.0ms
t_{CH}	Phase Shift to TRK00 on	60	64	70	μs	
t_{CI}	Step to TRK00 on	220	240	470	μs	1PHASE/1TRACK
t_{CJ}	STEP to TRK00 on	1.82	2.00	2.43	ms	PHASE RATE = 1.5ms
		2.84	3.00	3.46	ms	PHASE RATE = 3.0ms

5.2.4 ERASE TIMING PROCESS

The erase delay timing for the tunnel erase head is programmed. Since the adequate values are required individually for the disk format, the data transfer rate and the disk rotation speed in this timing, some useful parameters are prepared. The value for each function selection is shown in TABLE 5.1.1B.

In high density/low density compatible drive mode, the erase delay timing can be set evaluating [HDMODE] input to make read/write possible in each density mode.

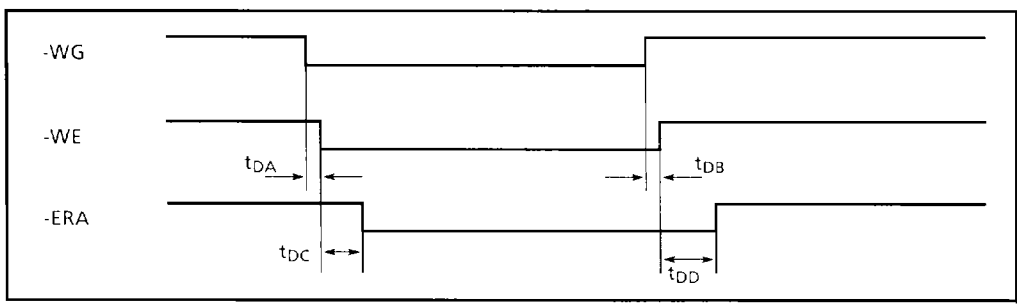


FIG.5.2.4 ERASE TIMING

TABLE 5.2.4 ERASE TIMING

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{DA}	Write Gate on to WE on			200	ns	
t_{DB}	Write Gate off to WE off			500	ns	Ro = 3.3K
t_{DC}	ON DELAY TIME	Refer to TABLE 5.1.1b				
t_{DD}	OFF DELAY TIME					

5.2.5 READ WRITE FILTER/HIGH DENSITY OUTPUT CONTROL

In high density/low density compatible drive mode, the [HDMODE] input can switch some FDMC's parameters from one density's to another. For this case, R/W analog circuit also need to change its AC characteristics. Helping R/W circuit keep compatibility in each density use, [RWFTR] is prepared. The antiphase of the [HDMODE] input is output to the [RWFTR]. When DRT1 = High or Low, the [HLDRDY] output can be used as the [HIDEN] output as shown in TABLE 5.1.3a. The [HIDEN] becomes active when [HDMODE] input is high level.

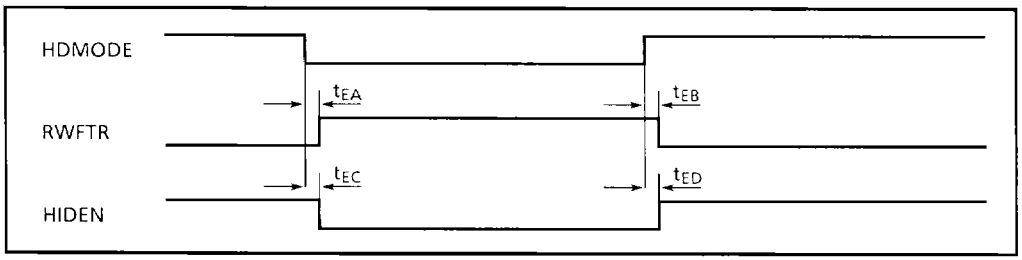


FIG.5.2.5 RWFTR, HIDEN TIMING

TABLE 5.2.5 READ WRITE FILTER/HIGH DENSITY OUTPUT CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{EA}	HDMODE fall to RWFTR Delay		0.5	2.5	ms	
t_{EB}	HDMODE rise to RWFTR Delay		0.5	2.5	ms	
t_{EC}	HDMODE fall to HIDEN Delay		0.5	2.5	ms	
t_{ED}	HDMODE rise to HIDEN Delay		0.5	2.5	ms	

5.2.6 SPINDLE MOTOR CONTROL

The spindle motor is controlled by the [MTREN] output. This output [MTREN] output high level for rotating the spindle motor. The cases in which the spindle motor starts rotating, are the execution of automatic chucking function and the case in which the requirements determined in the TABLE 5.1.2 are satisfied. As shown in TABLE 5.1.2, the spindle motor off-delay can be selected. In the off-delay operation, when the requirements for the spindle motor-off are satisfied, the [MTREN] output becomes low level ten seconds later. Even in this case, when the media is pulled out, [MTREN] output turns low level immediately without any off-delay.

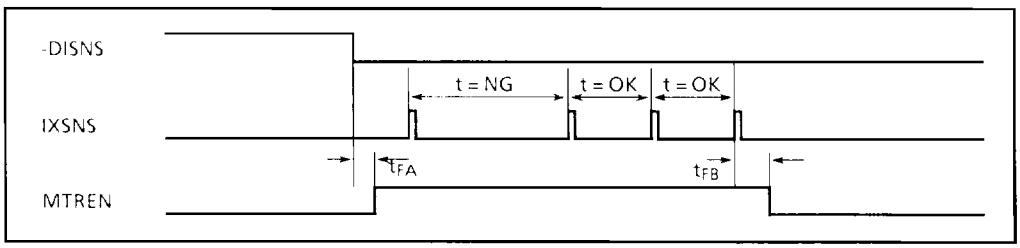


FIG.5.2.6a AUTO-CHUCKING OPERATION TIMING

TABLE 5.2.6a AUTO-CHUCKING OPERATION TIMING

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{FA}	DISNS on to MTREN on	0.2	0.5	3.0	ms	
t_{FB}	READY to MTREN off	0.3	1.0	5.0	ms	

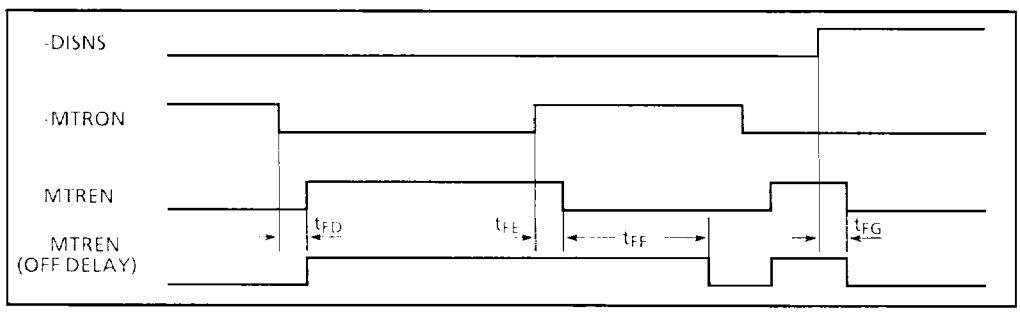


FIG.5.2.6b SPINDLE MOTOR CONTROL TIMING

TABLE 5.2.6b SPINDLE MOTOR CONTROL TIMING

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{FD}	MOTOR on to MTREN on	0.1	0.5	2.8	ms	
t_{FE}	MOTOR off to MTREN off	0.1	0.5	2.8	ms	
t_{FF}	MOTOR off to MTREN off	9.9	10.0	10.1	s	
t_{FG}	DISNS off to MTREN off	0.2	0.5	2.8	ms	

5.2.7 LED CONTROL for SENSOR

The [LEDSCN] output is prepared to reduce the power consumption of LEDs which is used for sensor at standby state. FDMC makes LED lightening only for the time required at the standby state. Controlling the LED for the sensor with [LEDSCN], consideration must be given to the items below. When the automatic chucking is selected, the index sensor always need to keep active while the media is inserted even at the standby state, then index sensor cannot be controlled by [LEDSCN] output.

Unless the track 00 sensor is made high level at the standby state, the internal track counter may cause the erroneous operation. FIG.5.2.7b shows an example of the circuit for the track 00 sensor. In the case the track 00 sensor is fabricated with this circuit, the negative pulse of maximum 20 [μs] is sometimes output to the [-TZSNS] input at the rising edge of the [LEDSCN] output.

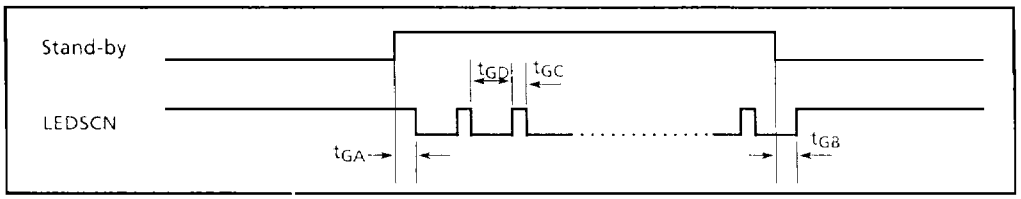


FIG.5.2.7a LED CONTROL for SENSOR

TABLE 5.2.7 LED CONTROL for SENSOR

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{GA}	Stand-by in to LEDSCN off Delay		0.8	3.0	ms	
t_{GB}	Stand-by out to LEDSCN off Delay			200	ns	
t_{GC}	LEDSCN High Level Time	44	48	54	μs	
t_{GD}	LEDSCN Low Level Time	0.5	0.8	2.5	ms	

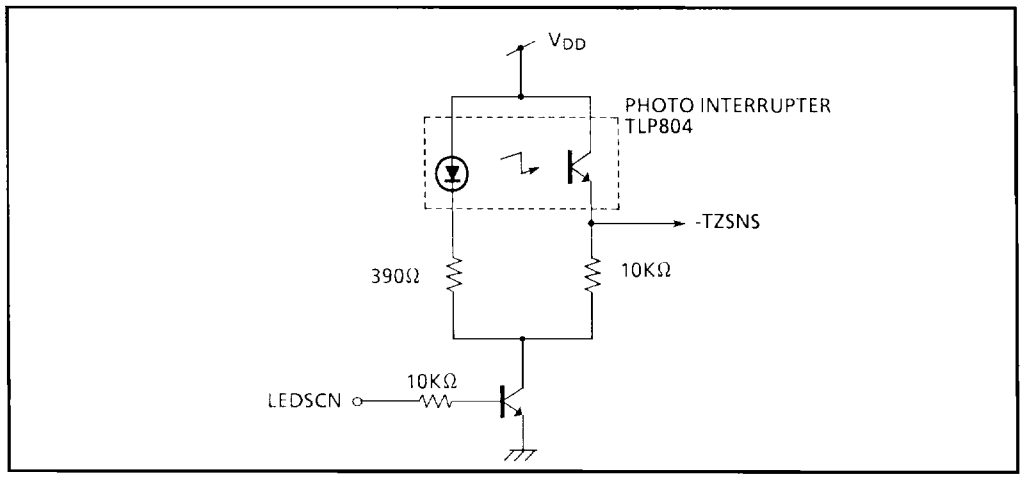


FIG.5.2.7b EXAMPLE CIRCUIT for TRACK 00 SENSOR

5.2.8 SWITCH FILTER CONTROL

The [SWFLT1] output is prepared for adjusting the write current or erase current of R/W analog circuit by the track position. Two types of operation of [SWFTR1] can be selected. One is the mode in which it is activated at the track position inner than 44th track in 135 TPI and at 22nd track in 67.5 TPI, and another is the mode in which it is activated at the track position inner than 60th track in 135 TPI and 30th track in 67.5 TPI.

Considering the whole track positions, the changeover position ideal for reducing the difference between maximum and minimum characteristics of read/write after the correction is 50th to 60th tracks in case of 135 TPI. However, from the view point of the compatibility with the other drives, it is considered better that the correction of the write current is soft.

According to these reasons, TC8605F can select both of them (Refer to TABLE 5.1.3b and TABLE 5.1.4b). In the standby state, the [SWFTR1] output becomes low level to prevent the unnecessary current from flowing to the read/write circuit. When the standby state is released, the level which was obtained before the standby state is restored.

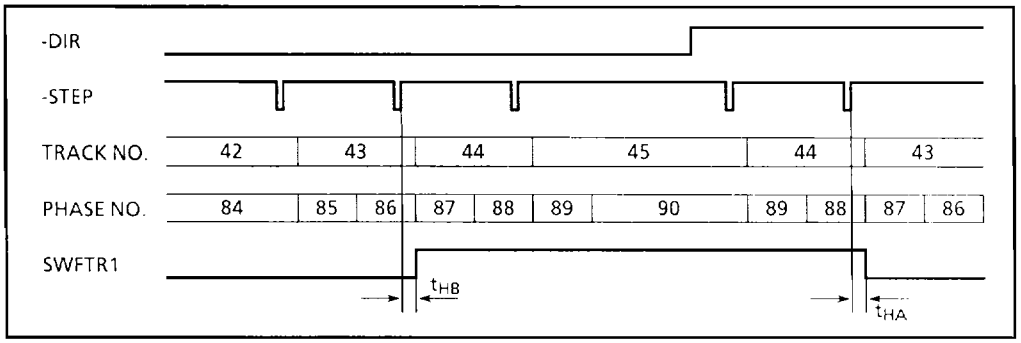


FIG.5.2.8a SWITCH FILTER CONTROL

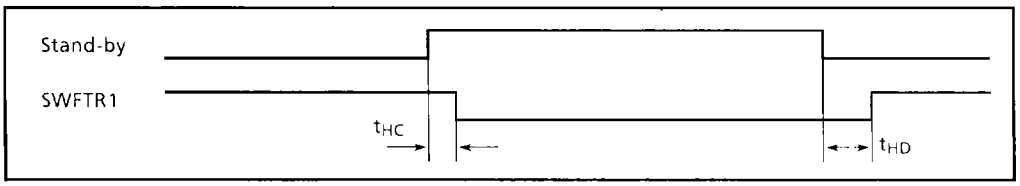


FIG.5.2.8b SWITCH FILTER STANDBY CONTROL

TABLE 5.2.8 SWITCH FILTER CONTROL TIMING

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{HA}	STEP to SWITCH FILTER off		0.8	2.5	ms	
t_{HB}	STEP to SWITCH FILTER on		0.8	2.5	ms	
t_{HC}	Stand-by in to SWFTR1 Delay			200	ns	
t_{HD}	Stand-by out to SWFTR1 Delay			200	ns	

5.2.9 READ/WRITE IC POWER CONTROL

[RWPWR] is prepared for reducing the power to be supplied to the read/write IC. [RWPWR] output is activated to high level when the following condition is satisfied.
([-MTRON] = low level) and (FDMC is not under seeking)

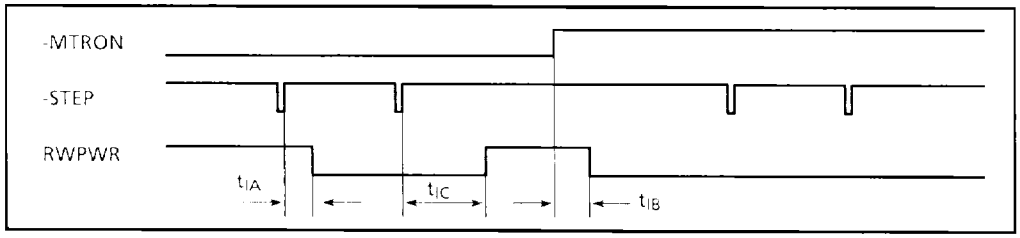


FIG.5.2.9 READ/WRITE IC POWER CONTROL

TABLE 5.2.9 READ/WRITE IC POWER CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{IA}	Step to RWPWR off	100	120	300	μs	
t_{IB}	MTRON off to RWPWR off		0.8	3.0	ms	
t_{IC}	Step to RWPWR on	6.7	7.4	10.0	ms	1Phase/1Step
		8.4	9.0	11.5	ms	Phase Rate = 1.5ms
		9.4	10.0	12.5	ms	Phase Rate = 3.0ms

5.2.10 DISK CHANGE OUTPUT CONTROL

[DSKCHG] output the logical AND of the internal FF output which is monitoring the changing of the disk media and the positive logic signal of [-DS] input. The disk change detecting function of the FDD specification is supported.

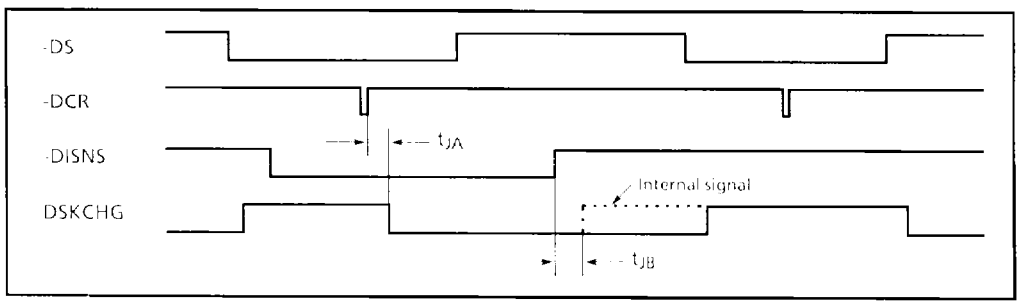


FIG.5.2.10 DISK CHANGE OUTPUT CONTROL

TABLE 5.2.10 DISK CHANGE OUTPUT CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{JA}	DCR to DSKCHG off Delay		0.5	2.5	ms	
t_{JB}	DISNS to DSKCHG on Delay		0.5	2.5	ms	

5.2.11 EJECT TIMER OUTPUT CONTROL

The eject timer output [EJTON] is prepared for controlling the eject mechanism of the disk. The eject timer output can be triggered either by the input [-EJSW] for the mechanical switch which is set at the FDD or by the system interface [-EJECT] input ([-DS] = Low Level). The eject timer output becomes high level for 500ms since FDMC detected the falling edge of [-EJECT] or [-EJSW].

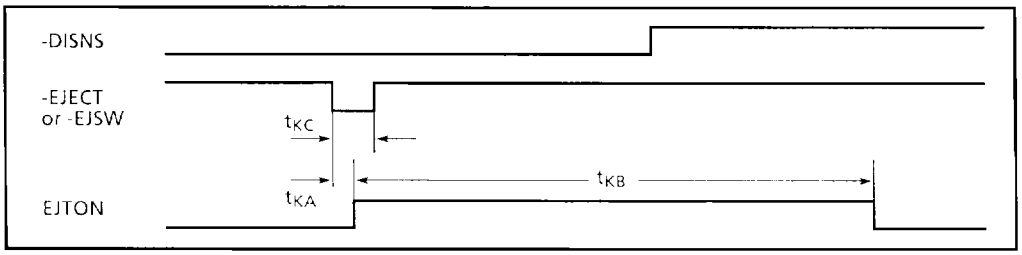


FIG.5.2.11 EJECT TIMER CONTROL

TABLE 5.2.11 EJECT TIMER OUTPUT CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{KA}	EJECT Fall to EJTON on			500	ns	
t_{KB}	EJTON High Level Time	497	500	504	ms	
t_{KC}	EJECT Pulse Width	500			ns	

5.2.12 SPINDLE MOTOR ROTATION MODE CONTROL

[HISP] output is prepared for supporting the 1.6M/1M byte compatible drive which changes rotation speed (300rpm/360rpm) according to the drive mode. The [HISP] output becomes low level when the rotation speed is 300rpm and high level when that is 360rpm corresponding to the rotation speed of the spindle motor which is selected by the combination (TABLE 5.1.1b) of DRT1, DRT2 and HDMODE.

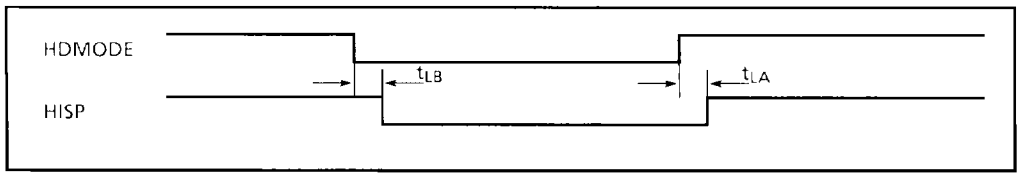


FIG.5.2.12 SPINDLE MOTOR ROTATION MODE CONTROL

TABLE 5.2.12 SPINDLE MOTOR ROTATION MODE CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{LA}	HDMODE Rise to HIPS Delay		0.5	2.5	ms	
t_{LB}	HDMODE Fall to HIPS Delay		0.5	2.5	ms	

5.2.13 FRONT PANEL LED CONTROL

The [LED] output controls turning LED on the front panel on/off. As shown in FIG.5.1.5, the condition can be selected by the [LEDSEL] input.

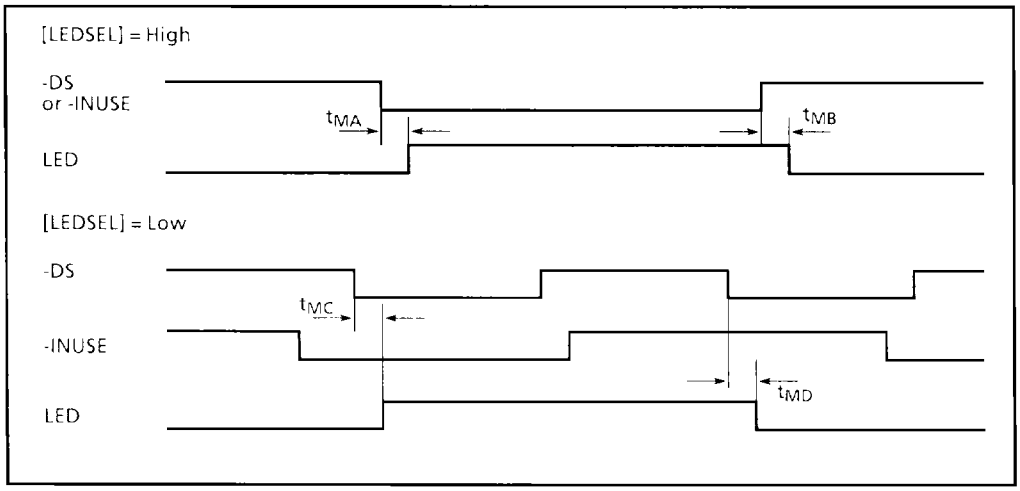


FIG.5.2.13 FRONT PANEL LED CONTROL

TABLE 5.2.13 FRONT PANEL LED CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{MA}	DS Fall to LED on Delay		0.5	2.5	ms	
t_{MB}	DS Rise to LED off Delay		0.5	2.5	ms	
t_{MC}	DS Fall to LED on Delay		0.5	2.5	ms	
t_{MD}	DS Rise to LED off Delay		0.5	2.5	ms	

5.2.14 SYSTEM INTERFACE OUTPUT CONTROL

TC8605F can select the positive logic output mode and the negative logic output mode for the system interface outputs (DSKCHG, TRK00, INDEX, READY, WP, RDDPO, HLDRDY). The positive logic output mode is selected when [-HACTV] input is low level, and the negative logic output mode is selected when [-HACTV] input is high level. In the positive logic output mode, each system interface outputs operate as the totem pole buffers and output each logical state when [-DS] input is low level. Each output needs to be connected to the system interface terminal via open collector inverting buffer. In the negative logic output mode, each system interface outputs operate as the totem pole buffers when [-DS] input is low level and becomes high impedance when [-DS] input is high level then each system interface output can be connected to the system interface terminal directly if the logical level of FDD's system interface is CMOS level. Regardless of the system interface mode, the outputs of the [INDEX] and the [WP] output logical "0" when the disk media is not inserted.

5.3 STANDBY CONTROL

In the TC8605F, various kinds of the power saving functions are available for reducing the power consumption of the FDD system.

5.3.1 STEPPING MOTOR POWER CONTROL

TC8605F begins to control the power saving function when the standby requirements specified in TABLE 5.1.3b and TABLE 5.1.4b are satisfied. [PWRON] output is negated in the standby state so as to cut off the whole current fed into the stepping motor. But if the stepping motor is still seeking, [PWRON] maintains high level to complete the seeking operation until [SMPS] becomes high level.

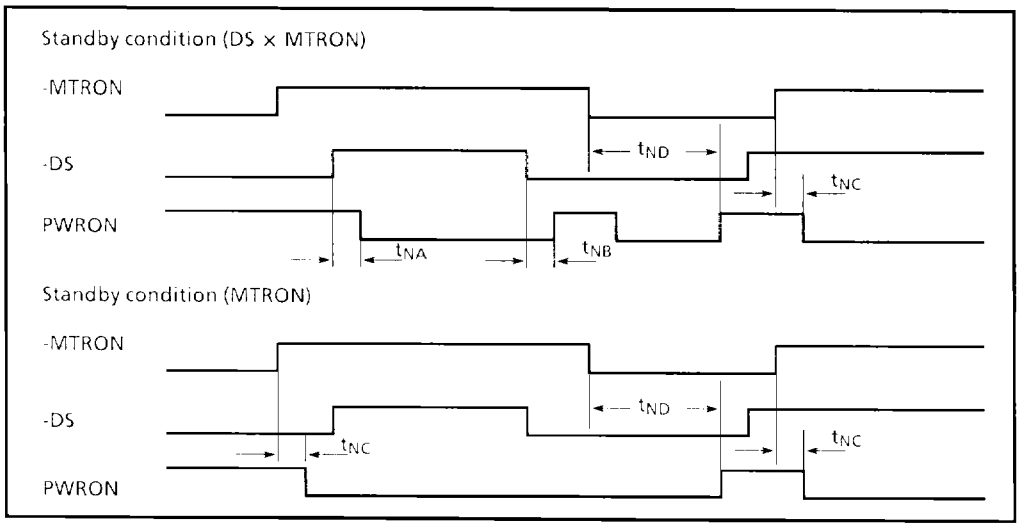


FIG.5.3.1a STEPPING MOTOR POWER CONTROL

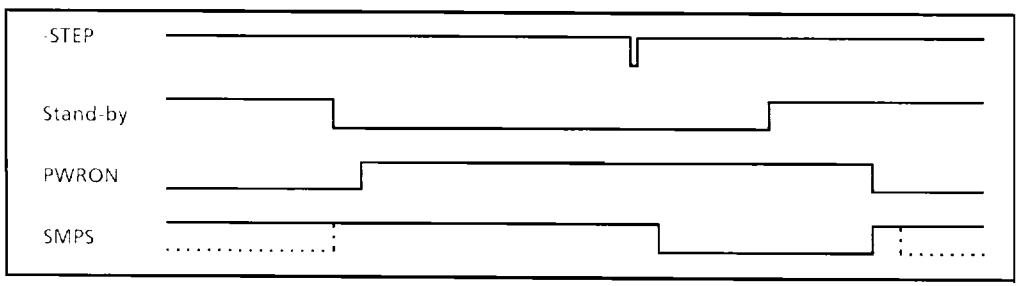


FIG.5.3.1b STEPPING MOTOR POWER CONTROL

TABLE 5.3.1 STEPPING MOTOR POWER CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{NA}	DS off to PWRON off Delay	0.1	0.5	2.5	ms	
t_{NB}	DS on to PWRON on Delay	0.1	0.5	2.5	ms	
t_{NC}	MTRON off to PWRON off Delay		0.5	2.5	ms	

5.3.2 SPINDLE MOTOR POWER-ON CONTROL

For suppressing the peak current consumption at the time when spindle motor starts to rotating, each output of [PWRON] or [RWPWR] is negated for 300ms after the spindle motor starts. When the step pulse is loaded even if [PWRON] is at low level i.e. stepping motor being in power saving state, the seeking operation is instantly started and the power saving state is restored again after 30ms. Some stepping motor loses accuracy of the positioning inside the motor phase after the power saving period. Against this phenomenon, FDMC negates [SMPS] output and activates [PWRON] output whenever the stepper system returns from the power saving state.

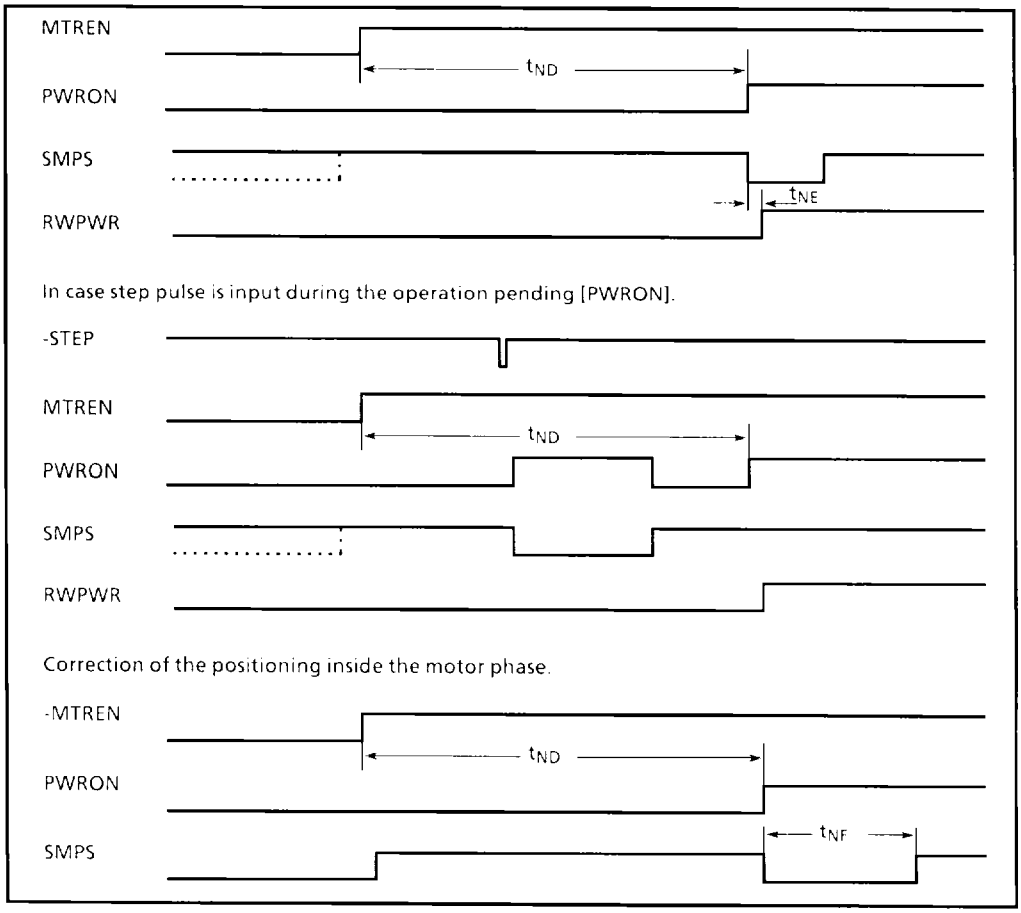


FIG.5.3.2 SPINDLE MOTOR POWER-ON CONTROL

TABLE 5.3.2 SPINDLE MOTOR POWER-ON CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
tND	MTREN on to PWRON on Delay	297	300	302	ms	
tNE	PWRON on to RWPWR on	32	36	240	μs	
tNF	SMPS Low Level Time	29	30	31	ms	
		14	15	16	ms	

5.3.3 STANDBY MODE CONTROL

When the stepping motor comes into the standby state, the standby-mode control function sets each phase output of [PHASE1], [PHASE2], [PHASE3] and [PHASE4] at low level to prevent the idle current from flowing to the stepper drive circuit. As soon as the standby state is released, these outputs recover the level (high or low) before the standby state was obtained.

If the standby state is obtained during the seeking operation ([SMPS] = low level), each phase output is set to low level after the seeking is completed ([SMPS] becomes high level). Regarding the [SMPS], the mode (mode 2) which sets this output to low level at standby time or the mode which keeps it at high level at standby time (mode 1) can be selected. (Refer to TABLE 5.1.3b and TABLE 5.1.4b).

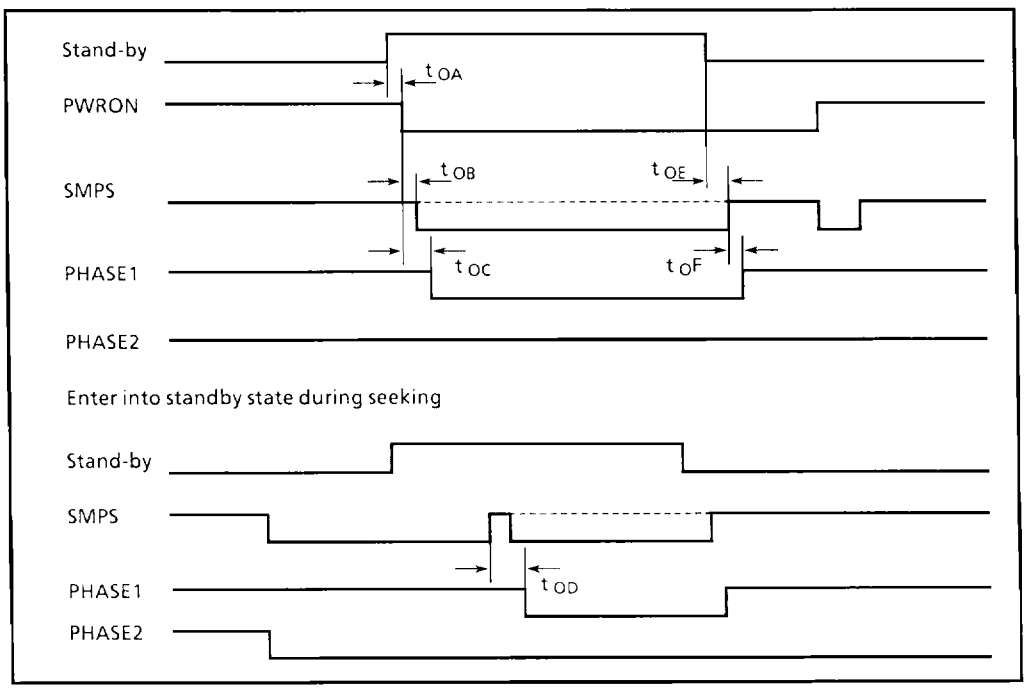


FIG.5.3.3 STANDBY MODE CONTROL

TABLE 5.3.3 STANDBY MODE CONTROL

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	REMARKS
t_{OA}	Stand-by to PWRON off Delay		0.5	2.5	ms	
t_{OB}	PWRON off to SMPS off	44	48	244	μs	MODE 2
t_{OC}	PWRON off to PHASE off	54	60	270	μs	
t_{OD}	SMPS on to SMPS/PHASE off		0.5	2.5	ms	
t_{OE}	Stand-by out to SMPS on		0.8	3.0	ms	MODE 2
t_{OF}	SMPS on to PHASE on	40	60	84	μs	

5.4 EXAMPLE of TC8605F PERIPHERAL CIRCUIT

5.4.1 EXAMPLE of APPLICATION CIRCUIT of [PWRON] and [SMPS]

The control output of the step motor can interface directly with the stepping motor driver TA7774F in case of the double power supply systems of 12V and 5V. As its application to the single power supply system of 5V, the example of the circuit in the case of using the H switch or the low-voltage operation and low-saturation output motor drive IC is shown below.

(1) Case of using TA7774F with double power supply

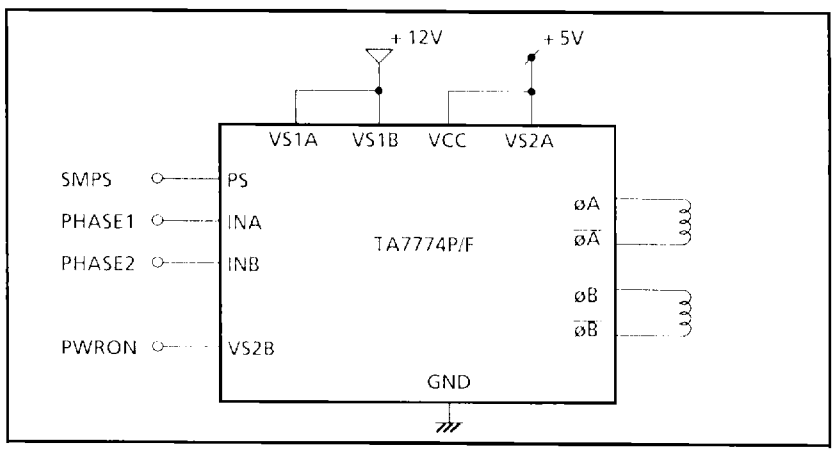


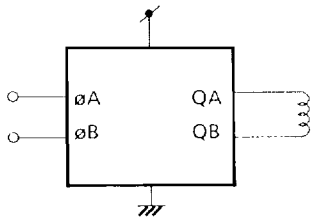
FIG.5 4.1a EXAMPLE OF APPLICATION CIRCUIT USING TA7774P/F

(2) Case of using H switch with 5V single power supply

This is the case in which the H switch of the bipolar driver is used as the stepping motor driver.

INPUT		OUTPUT	
ϕ_A	ϕ_B	Q_A	Q_B
L	L	Z	Z
L	H	L	H
H	L	H	L
H	H	Z	Z

Z : High Impedance



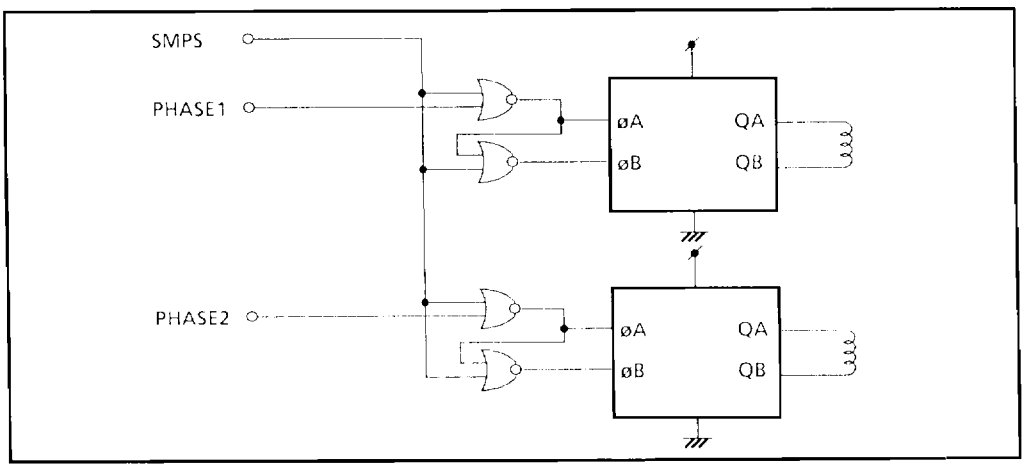


FIG.5.4.1b EXAMPLE of APPLICATION CIRCUIT USING H SWITCH

(3) Case of using motor drive IC with 5V single power supply

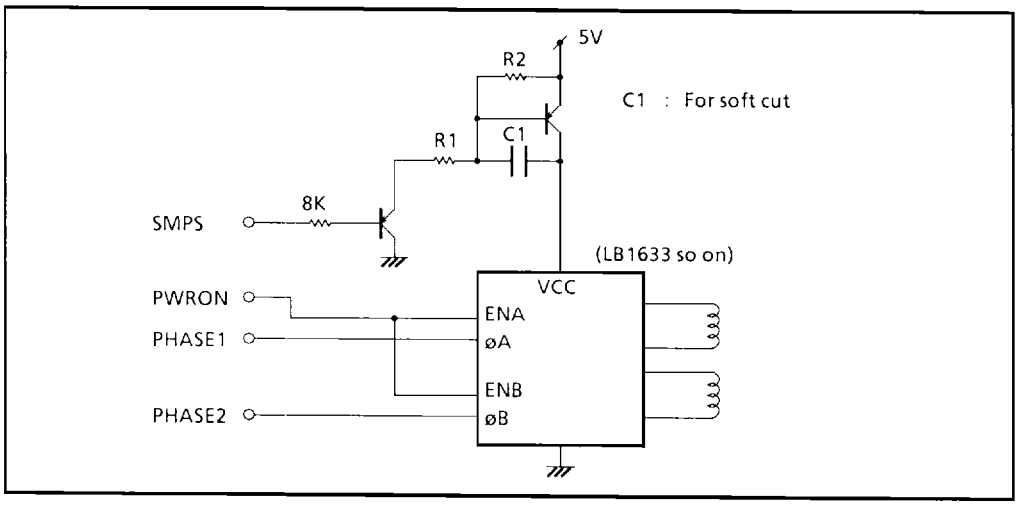


FIG.5.4.1c EXAMPLE of APPLICATION CIRCUIT USING MOTOR DRIVE IC

6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V (GND)

SYMBOL	PARAMETER	RATINGS	UNIT
V_{DD}	Supply Voltage	-0.5 ~ +6.5	V
V_{IN}	Input Voltage	V_{SS}-0.5 ~ V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS}-0.5 ~ V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-55 ~ +125	°C
T_{OPR}	Operating Temperature	-30 ~ +70	°C
I_{OUT1}	Output Current each Terminal	± 3 (Output Group 1) *	mA
I_{OUT2}	Output Current each Terminal	± 8 (Output Group 2) *	mA
P_D	Power Dissipation	300	mW

(note) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended conditions. If these conditions are exceeded, reliability of LSI may be adversely affected.

*Output Group 1 : HD0 , -ERA , -WE , SWFTR1 , XOUT , DSOUT , RWFTR , SMPS , LED , RWPWR , PWRON , LEDSCN , MTREN , PHASE1 , PHASE2 , PHASE3 , PHASE4

*Output Group 2 : DSKCHG , TRK00 , INDEX , READY , WP , RDDPO , HLDRDY

6.1.1 RECOMMENDED OPERATING CONDITIONS

V_{DD} = 5.0V , V_{SS} = 0V (GND)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
T_{OPR}	Operating Temperature		-30	+70	°C
V_{DD}	Supply Voltage		4.5	5.5	V
f_c	Clock Frequency		3.9	4.1	MHz

6.2 DC CHARACTERISTICS

V_{DD} = 5.0V , V_{SS} = 0V (GND) , T_{OPR} = -30~70°C

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HS1}	Hysteresis Width (1)	Input Group 1	0.2	0.4		V
V_{HS2}	Hysteresis Width (2)	Input Group 2	0.4	0.6		V
I_{IH}	Input High Level Current	V_{IH} = 5.0V	-2.0		2.0	μA
I_{IL1}	Input Low Level Current (1)	V_{IL} = 0.0V Input Group A	-30		-5	μA
I_{IL2}	Input Low Level Current (2)	V_{IL} = 0.0V Input Group B	-150		-25	μA
I_{IL3}	Input Low Level Current (3)	V_{IL} = 0.0V Input Group C	-2.0		2.0	μA
V_{IH1}	Input High Level Voltage (1)	Input Group 1	2.1		V_{DD}	V
V_{IL1}	Input Low Level Voltage (1)	Input Group 1	0.0		0.6	V
V_{IH2}	Input High Level Voltage (2)	Input Group 2	2.8		V_{DD}	V
V_{IL2}	Input Low Level Voltage (2)	Input Group 2	0.0		1.0	V
V_{IH3}	Input High Level Voltage (3)	Input Group 3	3.0		V_{DD}	V
V_{IL3}	Input Low Level Voltage (3)	Input Group 3	0.0		2.0	V
V_{IH4}	Input High Level Voltage (4)	Input Group 4	3.5		V_{DD}	V
V_{IL4}	Input Low Level Voltage (4)	Input Group 4	0.0		1.5	V

V_{DD} = 5.0V , V_{SS} = 0V (GND) , T_{OPR} = -30~70°C

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{OH1}	Output High Level Current (1)	V_{OH} = 4.6V Output Group 1			-2.0	mA
I_{OL1}	Output Low Level Current (1)	V_{OL} = 0.4V Output Group 1	2.0			mA
I_{OH2}	Output High Level Current (2)	V_{OH} = 4.6V Output Group 2			-6.0	mA
I_{OL2}	Output Low Level Current (2)	V_{OL} = 0.4V Output Group 2	6.0			mA
I_{OH3}	Output Low Level Current (3)	V_{OH} = 4.6V Output Group 3			-70	μA
I_{OL3}	Output Low Level Current (3)	V_{OL} = 0.4V Output Group 3	70			μA
I_{OL1}	Output Low Level Current (3)	V_{OL} = 0.4V -WE, -ERA output	2.0			mA
I_{OFL1}	Output Off Leak Current (1)	V_0 = 0~5V Output Group 2 and -WE,-ERA output	-2.0		2.0	μA
I_{DD}	Operating Consumption Current	f_c = 4MHz		2	4	mA

*Input Group 1 : -DIR,-SISEL , -DCR , -DS , RDDPI , PHRATE , DRT0 , -INUSE , -WG , HDMODE , -MTRON, -STEP, -EJECT
*Input Group 2 : -CLR , WPSNS , IXSNS , -EJSW , -DISNS
*Input Group 3 : -TZSNS
*Input Group 4 : TEST , XIN , FWSEL0 , FWSEL1 , FWSEL2 , MECNT , DRT1 , TMODE , AUTORZ , AUTOCK , -HACTV
*Input with Pull-up device (RIN = 500KΩ)
Input Group A : WPSNS , IXSNS , -DISNS , -EJSW
*Input with Pull-up device(RIN = 100KΩ)
Input Group B : -DIR , -SISEL , -DCR , -DS , -CLR , -EJCT, PHARATE , DRT0 , AUTORZ , LEDSEL , -HACTV , -INUSE , -WG , HDMODE , -MTRON , -STEP
*Input Group C : RDDPI , TEST , FWSEL0 , FWSEL1 , FWSEL2 , MECNT , DRT1 , TMODE
*Output Group 1 : HD0 , SWFTR1 , DSOUT , RWFTR , SMPS , LED , RWPWR , PWRON , LEDSCN , MTREN , PHASE1 , PHASE2 , PHASE3 , PHASE4
*Output Group 2 : DSKCHG , TRK00 , INDEX , READY , WP , RDDPO , HLDRDY
*Output Group 3 : XOUT

6.3 AC CHARACTERISTICS

6.3.1 PULSE WIDTH

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WSP}	Step Pulse Width	500			ns

6.3.2 TRANSMISSION DELAY CHARACTERISTICS

SYMBOL	PARAMETER			MIN.	TYP.	MAX.	UNIT
t_{WEL}	-WG FALL	→ -WE FALL		–	–	200	ns
t_{WEH}	-WG RISE	→ -WE OFF		–	–	500	ns
t_{IFL}	-DS FALL	→ DSOUT RISE DSKCHG RISE TRK00 RISE INDEX RISE READY RISE WP RISE RDDP0 RISE HLDRDY RISE	*1	–	–	200	ns
t_{IFH}	-DS RISE	→ DSOUT FALL DSKCHG FALL TRK00 FALL INDEX FALL READY FALL WP FALL RDDP0 FALL HLDRDY FALL	*1	–	–	200	ns
t_{IEN}	-DS FALL	→ ENABLE SYSTEM INTERFACE OUTPUT	*2	–	–	200	ns
t_{IDE}	-DS RISE	→ DISABLE SYSTEM INTERFACE OUTPUT	*2	–	–	200	ns
t_{HDH}	-SISEL RISE	→ HD0 RISE		–	–	200	ns
t_{HDL}	-SISEL FALL	→ HD0 FALL		–	–	200	ns
t_{RDH}	RDDPI RISE	→ RDDP0 RISE/FALL	*3	–	–	200	ns
t_{RDL}	RDDPI FALL	→ RDDP0 FALL/RISE	*3	–	–	200	ns
t_{SNH}	IXSNS RISE WPSNS RISE	→ INDEX RISE/FALL → WP RISE/FALL	*3	–	–	200	ns
t_{SNL}	IXSNS FALL WPSNS FALL	→ INDEX FALL/RISE → WP FALL/RISE	*3	–	–	200	ns
t_{DS}	SET UP TIME	-STEP ↓ → DIR		–	–	200	ns
t_{DH}	HOLD TIME	-STEP ↓ → DIR		–	–	200	ns

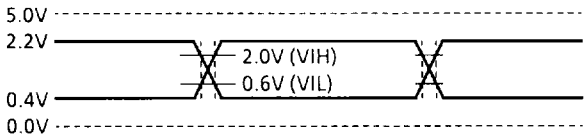
*1 : -HACTV = LOW
*2 : -HACTV = HIGH
*3 : -DS = Low, -HACTV = High

6.3.3 TESTING WAVEFORM

(VDD = + 5V)

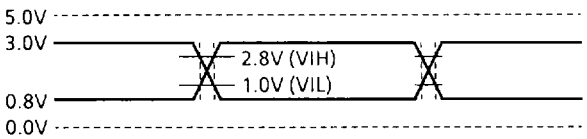
LSTTL Compatible Input Terminals

Input terminal Group 1 : -DIR , -SISEL , -DCR , -DS , RDDPI , PHARATE , DRT0 , -INUSE , -WG , HDMODE , -MTRON , -STEP, -EJECT



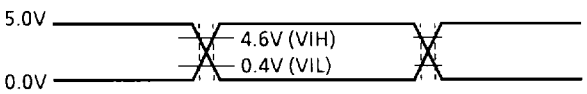
Sensor Input Terminals

Input terminal group 2 : -CLR , WPSNS , IXSNS , -EJSW , -DISNS

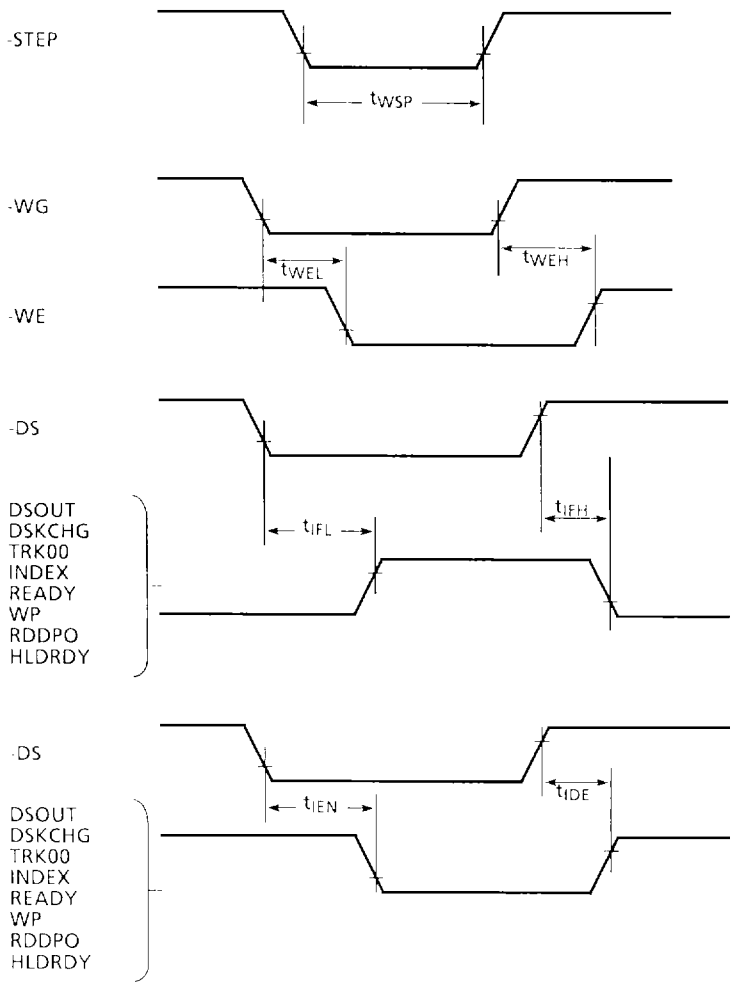


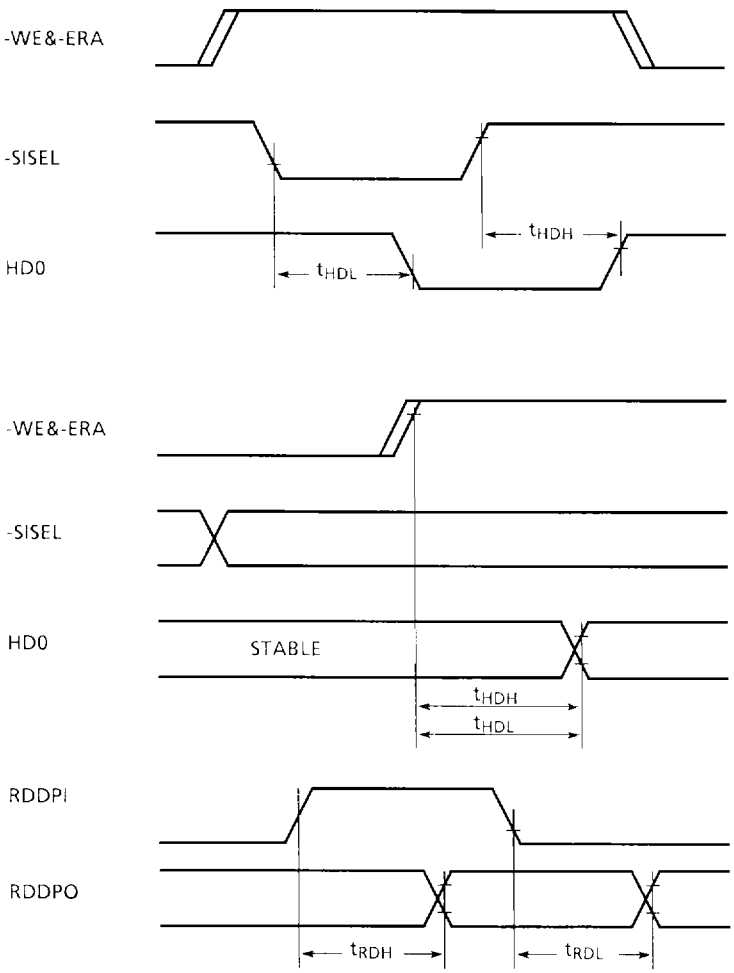
The Other Input Terminals

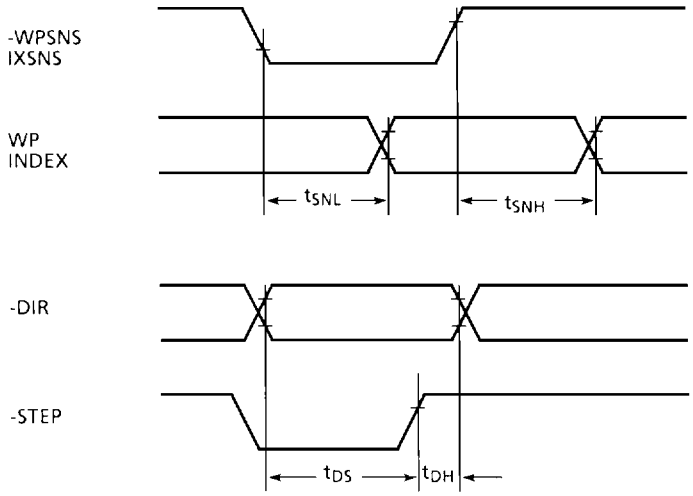
Input terminal group 3 : TEST , XIN , FWSEL0 , FWSEL1 , FWSEL2 , MECNT , PRT1 , TMODE , AUTORZ , LEDSEL , -HACTV, -TZSNS



6.3.4 TIMING WAVEFORM

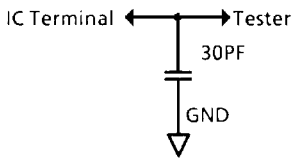



-WE&-ERA
-SISEL
HD0
tHDH
tHDL
-WE&-ERA
-SISEL
HD0
STABLE
tHDH
tHDL
RDDPI
RDDPO
tRDH
tRDL

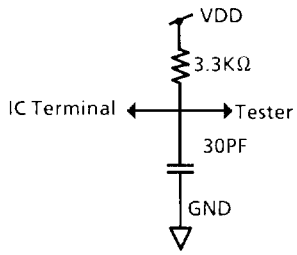


6.3.5 TESTING TERMINAL LOAD

CMOS OUTPUT TERMINAL



OPEN DRAIN OUTPUT



7. PACKAGE DIMENSION

60 PIN mini FP (Flat Package)

Unit : mm