Bulletin CA-107

A Texas Instruments Application Report

SN75 324 monolithic memory driver

SN75 324 MONOLITHIC MEMORY DRIVER

This note* briefly describes the SN75 324 monolithic integrated-circuit memory driver and illustrates how to use it to address and drive a magnetic memory. Detailed specifications of this circuit are found in the appropriate data sheet.

DESCRIPTION OF SN75 324

A functional diagram of the SN75 324 appears in Figure 1. This unit is designed specifically to replace traditional discrete transistor-transformer circuits in magnetic memory systems. However, it can also be used as a lamp driver, relay driver, or high-fan-out logic gate. It consists of four fast, high-current switches controlled by seven logic inputs (denoted A through G) that are compatible with 54/74 TTL and other standard logic systems with precautions mentioned under "Logic Input" below. One pole of each switch leads outside the unit (outputs W,X,Y, and Z). On their opposite poles, two of the switches connect to the memory current source, and the other two connect to ground. Thus two outputs are sources and two are sinks for memory drive current.

The decoding circuitry is arranged so that any or all of the switches in a package may be conducting at any given time. However, the unit will overheat if more than one switch at a time carries memory current. Therefore the system must be designed to prevent this occurrence by such means as the external logic inverters shown in Figure 1.

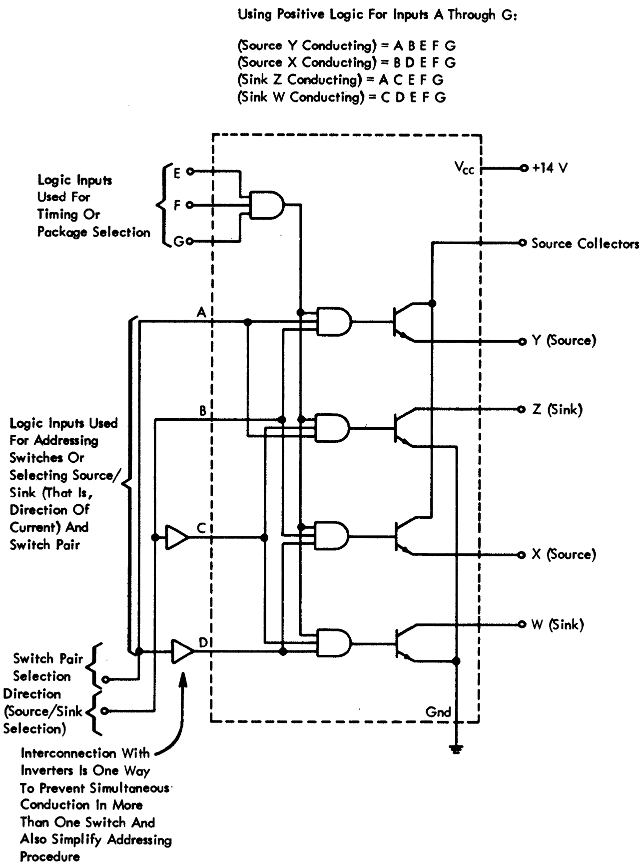

FIGURE 1. Simplified Functional Diagram and Logic Table for SN75 324 with Typical Interconnection of Address Inputs

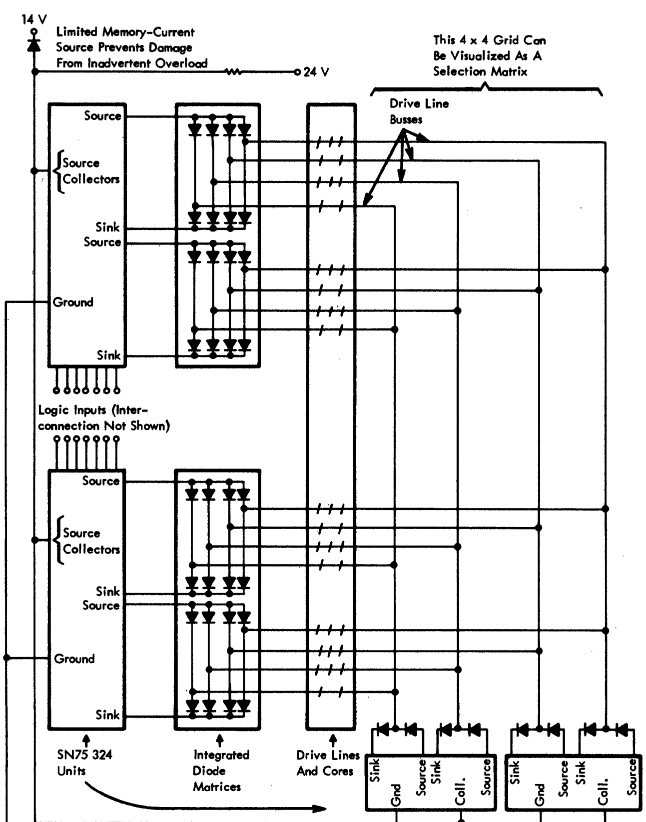

FIGURE 2. Typical Application of SN75 324 in Memory-Drive: A Selection Scheme for 16 Drive Lines

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*Adapted by James Talley and Bill Whittekin by permission from W.F. Jordan, Jr., "A Monolithic Decode-Drive Circuit for Magnetic Memory Systems," Digest, International Solid State Circuits Conference, February, 1968, p. 106; and R.W. Reichard and W.F. Jordan, Jr., "A Compact, Economical Core Memory With All-Monolithic Electronics," AFIPS Conf. Proc. Vol. 32 (Spring Joint Computer Conference) 1968, p. 253. (Jordan and Reichard are employed by Computer Control Division of Honeywell.)

MEMORY-DRIVE APPLICATIONS

In memory-drive applications, the SN75 324 can be connected in any of several fashions. Typically, however, sources and sinks are arranged in pairs from which many drive lines branch off, as shown in Figure 2. Here each drive line is served by a unique combination of two source/sink pairs, so that a selection matrix is formed. The size of such a matrix is limited only by the number of drive lines that a source/sink pair can serve. This number in turn depends on the capacitive and inductive load that each drive line of the particular system imposes on the driver.

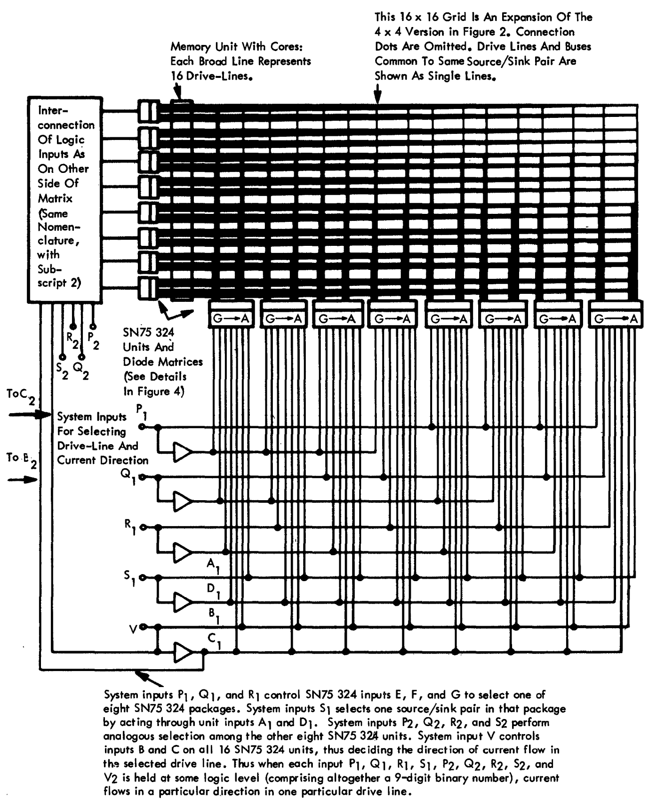


FIGURE 3. SN75 324 Serving 256 Drive Lines in a Magnetic Memory, with Hypothetical Logic Interconnections to Show Input Flexibility

A larger selection matrix is shown in Figures 3 and 4. The hypothetical interconnection of logic inputs demonstrates one way to take advantage of the multiple logic inputs of the SN75 324.

Regardless of the particular line-selection and logic scheme, the SN75 324 can be densely mounted on printed-wiring boards along with monolithic diode arrays and IC logic packages. The result normally is a system that is cheaper, faster, smaller, more reliable, and simpler to connect than a conventional discrete transistor-transformer version.

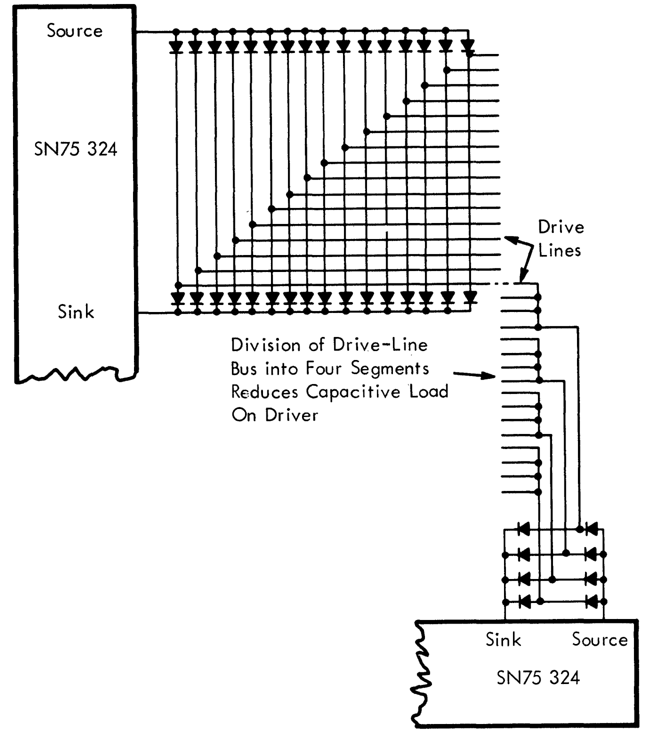


FIGURE 4. Details of Connection of Drive-Lines to Drivers in Figure 3

LOGIC INPUT FROM 54/74 TTL

Because of the high-noise environment in which the SN75 324 is intended to operate, the input logic levels have been purposely designed to be somewhat higher than standard 54/74 TTL logic levels, as compared below:

	54/74 TTL	SN75 324
$V_{out(0)}$	0.4 V max.	---
$V_{out(1)}$	2.4 V min.	---
$V_{in(0)}$	0.8 V max.	1.0 V max.
$V_{in(1)}$	2.0 V min.	3.5 V min.
$V_{threshold}$	1.4 V typ.	2.3 V typ.

The higher logical 0 input level, $V_{in(0)}$ of the SN75 324 guarantees a d-c noise margin of 600 mV when driven from 54/74 TTL. However, the higher $V_{in(1)}$ of the SN75 324 (3.5 V) leads to some minor difficulties when using 54/74 TTL. The minimum guaranteed logical 1 level of 2.4 V at a 54/74 TTL output falls short of the 3.5-V minimum level required at the SN75 324 input. However, this problem can be readily solved by the proper selection of a pull-up resistor at the gate output as shown in Figure 5.

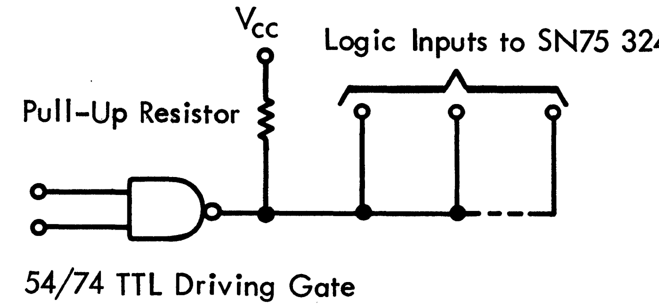
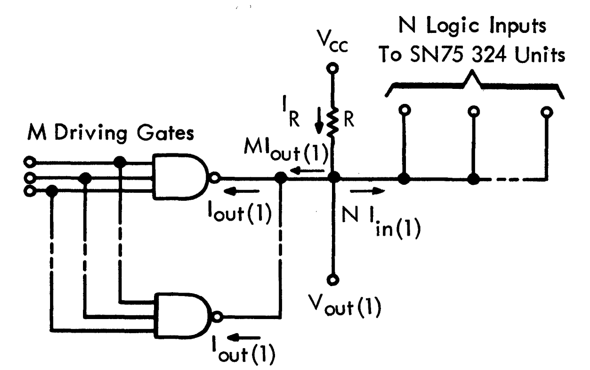


FIGURE 5. Input to SN75 324 from 54/74 TTL Using Pull-Up Resistor

Because of the high logical 0 input current of the SN75 324 (12 mA for the timing inputs, 6 mA for the address inputs), it may be desirable to drive the inputs from 54/74 TTL buffer gates (SN7440 or SN74H40) to assure adequate sink current capability. Each SN7440 buffer gate output is specified at 0.4 V maximum $V_{out(0)}$ at a sink current of 48 mA. The $V_{out(0)}$ for the SN74H40 buffer gate is 0.4 V at a sink current of 60 mA. If additional sink current is required, the inputs and outputs of both gates in the SN7440 or SN74H40 package may be paralleled for 96 and 120 mA capability, respectively. (This parallel connection requires no significant sacrifice, if any, in switching characteristics, but the outputs of these gates should not be paralleled without also paralleling inputs. Otherwise one or both of the gates can be damaged because of the active pull-up or "totem-pole" output configuration.)



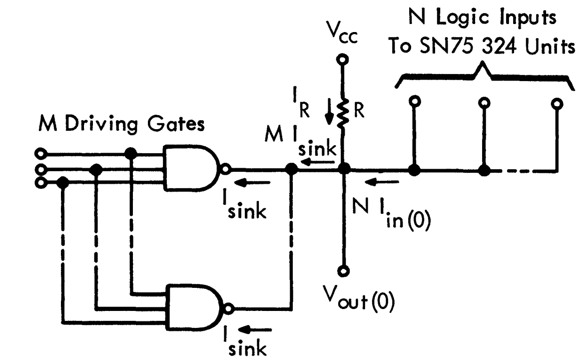
Voltage across R = $V_R = V_{cc}\,(min) - V_{out(1)}$

Current through R = $I_R = M\,I_{out(1)} + N\,I_{in(1)}$

$$\text{Therefore } R_{(max)} = \frac{V_{cc}\,(min) - V_{out(1)}}{M\,I_{out(1)} + N\,I_{in(1)}}$$

where $V_{out(1)}$ = 3.5 V minimum to drive SN75 324 input
$I_{out(1)}$ = 250 μA maximum for 54/74 TTL gate output
$I_{in(1)}$ = 100 μA maximum for SN75 324 timing inputs
= 200 μA maximum for SN75 324 address inputs
M = number of parallel driving gates
N = number of parallel SN75 324 inputs

FIGURE 6: Calculation of Maximum Value of Pull-Up Resistor in Figure 5



Current in resistor = $I_R = M\,I_{sink} - N\,I_{in(0)}$
Voltage across resistor = $V_R = V_{cc} - V_{out(0)}$

$$R_{(min)} = \frac{V_{cc} - V_{out(0)}}{M\,I_{sink} - N\,I_{in(0)}}$$

where $I_{in(0)}$ = 6 mA maximum for address inputs
$I_{in(0)}$ = 12 mA maximum for timing inputs
I_{sink} = maximum specified sink current of driving gate
$V_{out(0)}$ = maximum specified "0" level output voltage of the driving gate (≤1.0 V), which is 0.4 V for 54/74 TTL
M = number of parallel driving gates
N = number of parallel SN75 324 inputs

FIGURE 7. Calculation of Minimum Value of Pull-Up Resistor in Figure 5

A large number of SN75 324 inputs may also be driven from the output of any of several 54/74 TTL decode/drivers. For example, the output of the SN7445 BCD-to-Decimal Decode/Driver can sink 80 mA at $V_{out(0)}$ of 0.9 V or sink 20 mA at $V_{out(0)}$ of 0.4 V. Since the maximum $V_{in(0)}$ of the SN75 324 is 1.0 V, the SN7445 can drive the SN75 324 with a pull-up resistor.

When a pull-up resistor is used at the driving gate output, its value must be determined to ensure proper logic levels. The worst-case resistor values may be readily calculated using available driving-gate data sheet information, as exemplified below.

The maximum resistor value is calculated to ensure that sufficient current is available when the driving gate output is high (off). This current must supply the SN75 324 input as well as the driving gate output. For a logical 1, it is necessary to maintain 3.5 V minimum at the SN75 324 input. A suggested method of calculating the maximum resistor value is shown in Figure 6. The minimum value of the resistor is calculated to ensure that its current plus that from the SN75 324 inputs will not cause the output voltage $V_{out(0)}$ of the driving gate to exceed the maximum of 1.0 V. (See Figure 7).

Assume The Following:

N = 8 Address Inputs

M = 1

$V_{out(1)}$ = 3.5 V Minimum

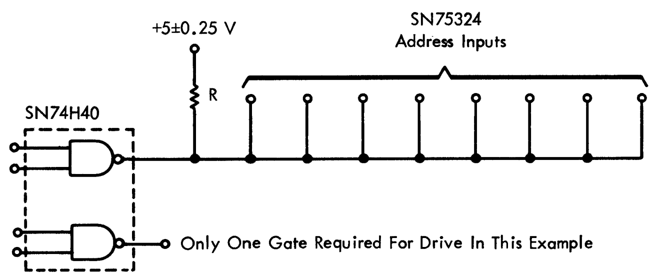
$I_{in(1)}$ = 200μA Per Address Pin

$I_{in(0)}$ = 6 mA Per Address Pin Driving Gate SN74H40:

I_{sink} = 60 mA

$V_{out(0)}$ = 0.4 V Maximum

$I_{out(1)}$ = 250μA (Assumed)



Maximum R

$$= \frac{V_{CC\,(Min)} - V_{out(1)}}{M \cdot I_{out} + N \cdot I_{in(1)}} = \frac{4.75 - 3.5}{(1)(0.25)+(8)(0.2)} = \frac{1.25\text{V}}{1.85\text{mA}} = 675\Omega$$

Minimum R

$$= \frac{V_{CC\,(max)} - V_{out(0)}}{M \cdot I_{sink} - N \cdot I_{in(0)}} = \frac{5.25 - 0.4}{(1)(60) - 8\,(6)} = \frac{4.85\text{V}}{12\text{ mA}} = 333\Omega$$

FIGURE 8. Sample Calculation of Pull-Up Resistor Value for SN74H40

After determining the worst-case minimum and maximum pull-up resistor values, any value between the limits may be selected. (Obviously, the calculated minimum value must be below the calculated maximum value to be practical). Selecting a resistor value near the minimum limit will raise the logical 1 voltage and thereby improve the logical 1 noise margin.

An example of an SN74H40 buffer gate driving eight SN75 324 address inputs is shown along with sample calculations in Figure 8. If, in this example, a value of 400 Ω is selected for the pull-up resistor, the guaranteed logic levels at the SN75 324 inputs are 0.4 V maximum for $V_{in(0)}$ and 4.0 V minimum for $V_{in(1)}$. This resistor results in guaranteed d-c noise margins of 600 mV at the logical 0 level and 500 mV at the logical 1 level at worst-case conditions.

CIRCUIT-BOARD PRECAUTIONS

In any memory-drive application, circuit-board mounting of the SN75 324 should be judiciously considered to satisfy the problems of signal transmission, noise, and thermal management. If flat packs are used, they should be mounted flat on a wide copper lamina using a thermal compound, or "base up" with high-velocity air flowing across them. A row of flat packs should run perpendicular to the cooling air stream rather than along it to avoid accumulated heating of air. If a copper lamina is used, it should be expanded to fill the empty area on the circuit board to enlarge the cooling surface. Futhermore, because memory-drive and logic currents share the same electrical ground in a direct-coupled system exemplified in Figures 2 through 4, it is necessary to take special care to minimize ground noise.

OPERATION OF SN75 324

A schematic representation of the SN75 324 appears in Figure 9. On this single silicon chip lie two 400-mA source-sink pairs and associated logic circuitry with seven inputs. Because ground and sink emitters are common, the circuit exactly fits a standard 14-lead IC package.

Each sink circuit (Figure 10) is an inverting amplifier with a TTL input. Turn-on is enhanced by an overdrive transistor which provides extra base current for charging the transition and Miller capacitances of the sink. A stack discharge resistor is disconnected when the matrix is conducting. During turn-off, the drive current surges through a 14-V internal clamp as line inductance energy is released. This provision limits voltage excursions which could otherwise generate excessive system noise.

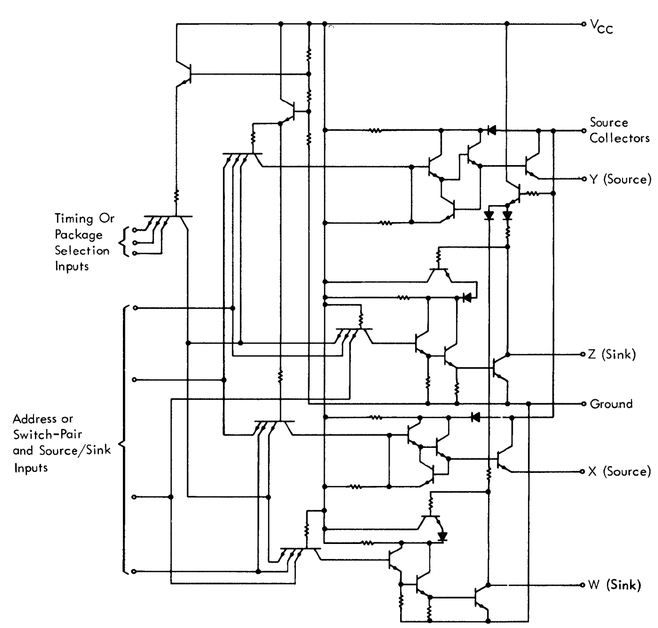


FIGURE 9. Schematic Circuit of SN75 324

The source (Figure 11) is an emitter follower driven from a TTL input stage. Since the base of the input transistor is returned to 3 V, its threshold is effectively 2.3 V. During the turn-on transient, the inductive load is pulled toward 14 V. Transient base drive current for the source is provided from the memory current resistor by the pseudo-Darlington connection. When the load current stabilizes, the load voltage drops to a few volts, the Darlington diode disconnects, and the base drive resistor provides enough drive to saturate the source. While the source is saturated, the diode in the Darlington connection is reverse-biased. During the turn-off transient, the turn-off transistor removes the base charge from the pseudo-Darlington pair and subsequently holds the source base at an OFF potential.

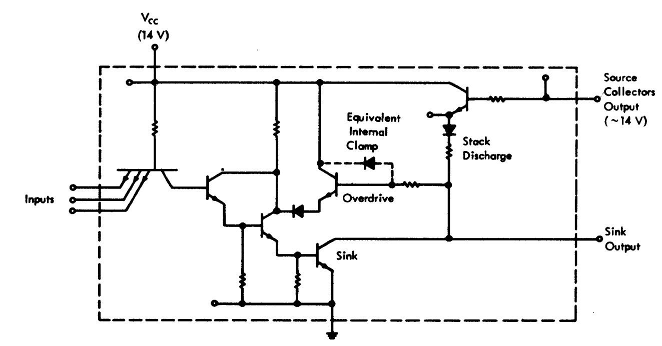


FIGURE 10. An Individual Sink Circuit

The SN75 324 chip is comparable in active area to about 100 components, considering the driver transistors equal to 10 small ones. Since system design can permit only one switch active at a time, the number of switches on a chip is not limited by power dissipation but rather by chip size and complexity. The chip is produced with conventional bipolar integrated circuit processes and techniques. Its size is about 0.060 by 0.120 inch. The epitaxial material is of a resistivity and thickness compatible with linear integrated circuits, permitting higher collector-to-base breakdown voltage than most digital integrated circuits. Gold doping is employed for reduced storage time. A low-resistivity diffusion is employed to enhance vertical conduction to the collector regions. Saturation voltage is less than 850 mV to minimize dissipation and memory drive current variations.

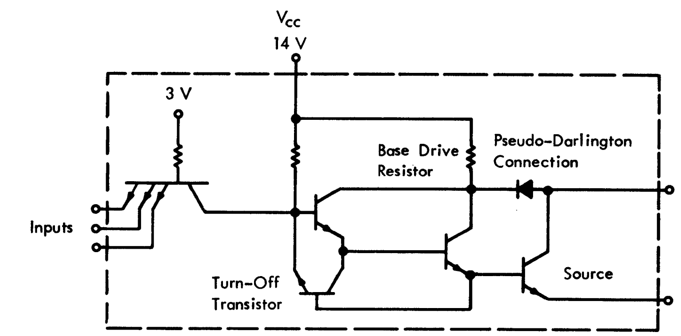


FIGURE 11. An Individual Source Circuit

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