Part I

1. SiS85C496/497 Overview

SiS85C496	*PCI & CPU Memory Controller (PCM)*
SiS85C497	*AT Bus Controller & Megacell (ATM)*

The SiS 486-VIP (VESA/ISA/PCI) chips are two-chip solution ideally for Intel's 80486, SL Enhanced 486, P24D/P24T/DX4 CPU, AMD's 486, Enhanced Am486 and Cyrix's Cx486 (M7)/Cx 5x86 CPU based on green AT system. By supporting the most popular industrial standard system interfaces, it provides flexible configurations for system design and applications.

The SiS85C496 PCI & CPU Memory Controller (PCM) integrates the Host Bridge (Host Interface), the cache and main memory DRAM Controller, the PCI Bridge, the built-in IDE Controller, and the FS-Link Bus (Fast Slow Link Bus). It provides the address paths and bus control for transfers among the Host (CPU/L1 cache), main memory (L2 cache and DRAM), the Peripheral Component Interconnect (PCI) Bus, and the FS-Link Bus. The L2 cache controller supports both write-through and write-back cache policies and cache sizes up to 1 MBytes. The cache memory can be built using standard asynchronous SRAMs. The main memory DRAM controller interfaces DRAM to the Host Bus, PCI Bus, and FS-Link Bus. Up to eight single sided SIMMs or four double sided SIMMs provide a maximum of 255 MBytes of main memory. The installation of DRAM SIMMs is "Table-Free", which allows the SIMMs be installed into any slot location and any combinations. The built-in IDE hard disk controller allows CPU accessing hard disk and also provides higher system integration with lower system cost. The 85C496 is intended to be used with the SiS85C497 which is a AT Bus Controller with built-in 206 controller.

The SiS85C497 AT Bus Controller and Megacells (ATM) provides the interface between PCI/CPU/Memory Bus (fast machine) and the ISA Bus (slow machine). It also integrates many of the common I/O functions in today's ISA based PC systems. The 85C497 comprises the FS-Link interface (Fast-Slow Link interface), ISA bus controller, DMA controller and data buffers to isolate the FS-Link Bus from the ISA Bus and to enhance performance. It also integrates a 14 channel edge/level interrupt controller, refresh controller, a 8-bit BIOS timer, three programmable timer/counters, non-maskable-interrupt (NMI) control logic, Power Management Unit, and RTC. Figure 1.1 shows the system block diagram.
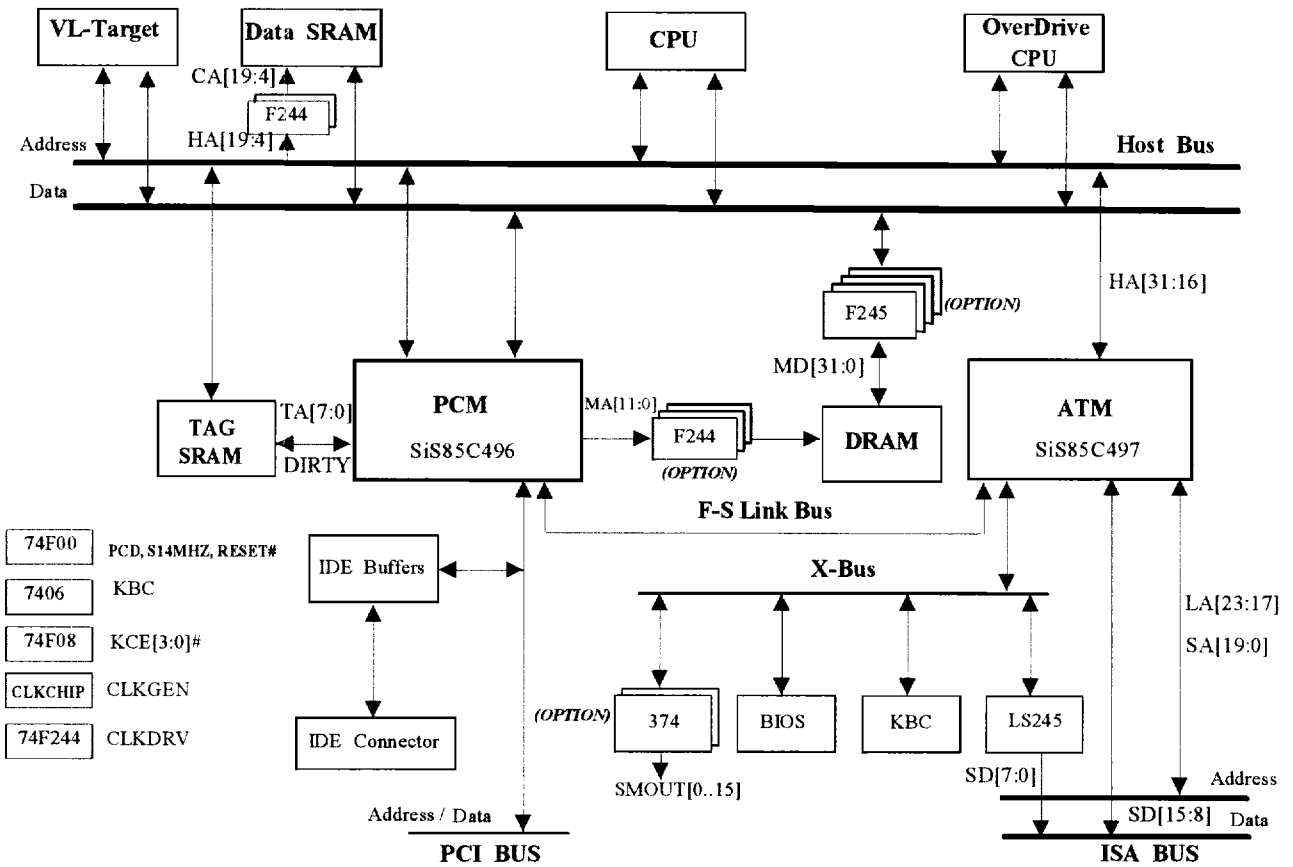
Figure 1.1 SiS85C496/497 System Block Diagram