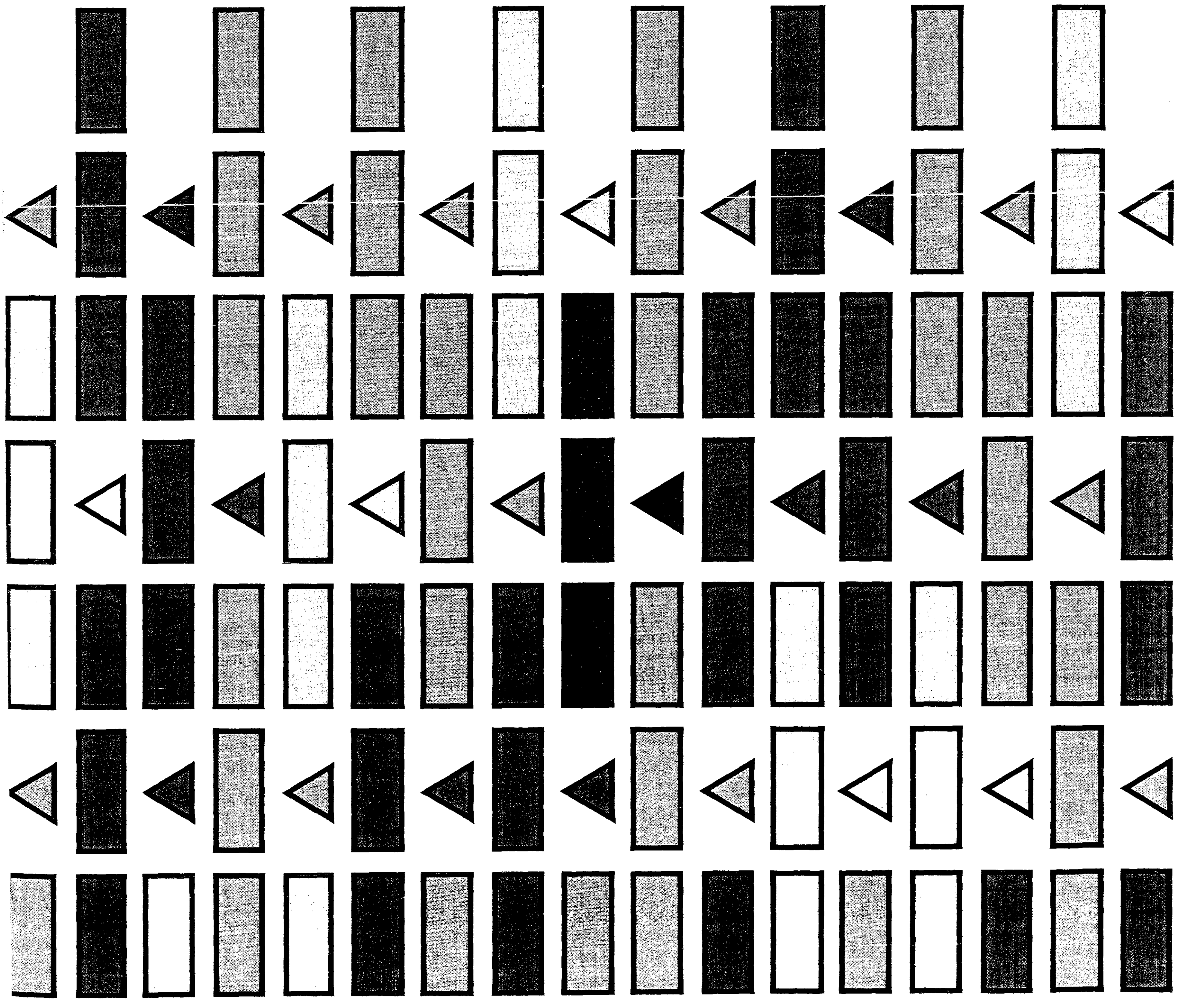
SIGNETICS D-MOS DATA



SIGNETICS D-MOS DATA

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D-MOS FET - SINGLE GATE N-CHANNEL ENHANCEMENT

SD200 SD201 SD202 SD203

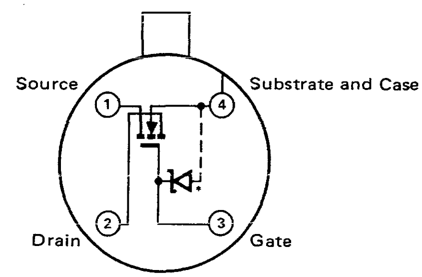
UHF AND GENERAL PURPOSE RF APPLICATIONS

DESCRIPTION

The Signetics D-MOS SD200/201/202/203 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives superior high frequency performance up to 2GHz. A zener diode is connected between the gate and substrate of the SD201 and 203 that bypasses any voltage transient lying outside the range of −0.3V to +25.0V. Thus the gates of the SD201 and 203 are protected against damage in all normal handling and operating situations.

All four devices are general purpose transistors especially suited for amplifier designs in the UHF range (500MHz to 2GHz). They have extremely high transconductance, very low input capacitance and extremely low feedback capacitance. The SD200, 201, 202 and 203 combine high gain with low levels of noise, intermodulation distortion and feedback capacitance. These parameters make them ideally suited for critical amplifier applications. These devices are hermetically sealed in modified 4-lead TO-72 packages.

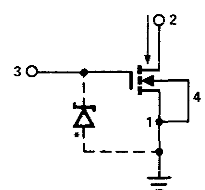
PIN CONFIGURATION (Top View)



Order Part Nos: SD200DC, SD201DC, SD202DC, SD203DC

*Diode Protection On SD201, SD203 Only.

COMMON SOURCE BIAS SCHEME



$+V_{DS} = 0 \to +20$ Volts
$+V_{GS} = 0 \to +4$ Volts
$+I_{DS} = 0 \to +20$mA

*Diode Protection On SD201, SD203 Only.

GENERAL FEATURES

- ION-IMPLANTED FOR GREATER CONTROL AND RELIABILITY
- WIDE DYNAMIC RANGE
- POSITIVE BIAS ONLY

SD200/201 FEATURES

- HIGH GAIN THROUGH UHF RANGE – 10dB AT 1GHz
- LOW NOISE THROUGH UHF RANGE:
  SD200 – 4.5dB
  SD201 – 5.0dB
- LOW INPUT CAPACITANCE – 2.4pF
- LOW FEEDBACK CAPACITANCE – 0.20pF
- HIGH DRAIN-TO-SOURCE VOLTAGE – +30V
- HIGH FORWARD TRANSCONDUCTANCE – 15,000 μmhos

SD202/203 FEATURES

- HIGH GAIN THROUGH UHF RANGE – 10dB AT 1.5GHz
- LOW NOISE THROUGH UHF RANGE – 3.2dB AT 1.0GHz
- LOW INPUT CAPACITANCE – 3.0pF
- LOW FEEDBACK CAPACITANCE – 0.20pF
- HIGH DRAIN-TO-SOURCE VOLTAGE – +25V
- HIGH FORWARD TRANSCONDUCTANCE – 20,000 μmhos

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

Drain-To-Source Voltage (V_{DS})	
SD200/SD201	+25V
SD202/SD203	+20V
Drain-To-Substrate Voltage (V_{DB})	
SD200/SD201	+25V
SD202/SD203	+20V
DC Gate-To-Substrate Voltage (V_{GB})	
SD200	±40V
SD201	−0.3V, +10V
SD202	±40V
SD203	−0.3V, +10V
Drain Current (I_D)	50mA
Ambient Temperature Range	
Storage	−65°C to +175°C
Operating	−65°C to +125°C
Transistor Dissipation (P_T)	
At +25°C Case Temperature	1.2W
(Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	
At +25°C Free-Air Temperature	300mW
(Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	

ELECTRICAL CHARACTERISTICS

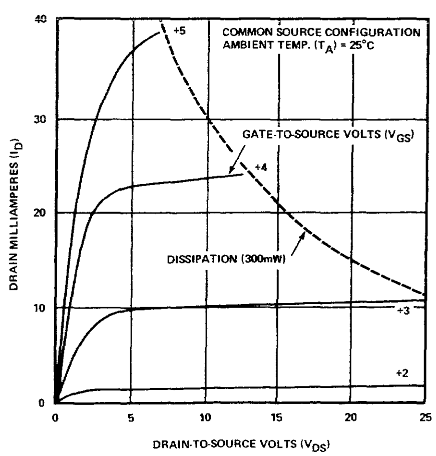
T_A = 25°C (Unless Otherwise Noted)

PARAMETER	
BV_{DS}	Drain-To-Source Breakdown Voltage
I_{GSS}	Gate Leakage Current
I_D (OFF)	Drain-To-Source Current
I_{DSS}	Zero Bias Drain Current
V_T	Threshold Voltage
gfs	Forward Transconductance
Small Signal Short Circuit	
C_{ISS}	Input
C_{OSS}	Output
C_{RSS}	Reverse Transfer
Gps	Power Gain*
NF	Noise Figure*
r_{DS} (ON)	Drain-To-Source On Resistance
P_I	Intercept Point

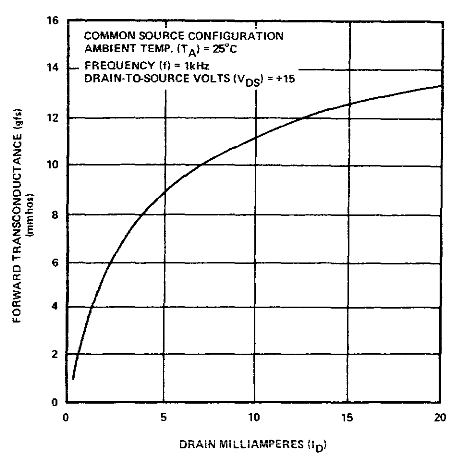
*Measured In Amplifier Test Fixture.

CHARACTERISTIC CURVES – SD200/201

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



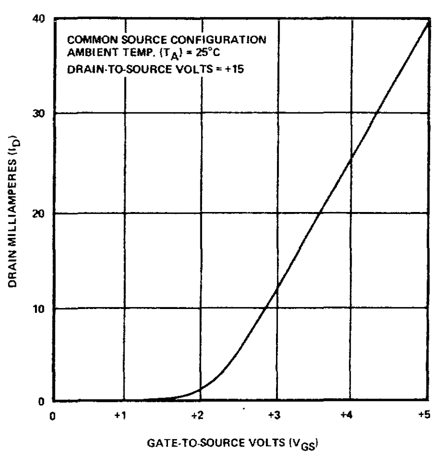
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



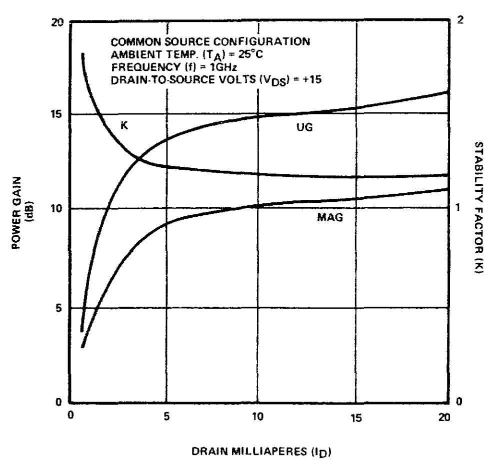
TEST CONDITIONS	SD200			SD201			SD202			SD203			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{GS} = 0V, I_D < 1μA	25	30		25	30		20	25		20	25		V
V_{GS} = ±10V, V_{DS} = 0V			0.1						0.1				nA
V_{GS} = +10V, V_{DS} = 0V					0.001	1.0					0.001	1.0	μA
V_{DS} = +15V, V_{GS} = 0V		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
V_{DS} = +15V, V_{GS} = 0V		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
V_{DS} = V_{GS} = V_T, I_D = 1μA	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
V_{DS} = +15V, I_D = 20mA, f = 1kHz													
V_{GS} ≅ +4V	13.0	15.0		13.0	15.0								mmhos
V_{GS} ≅ +2.5V							17.0	20.0		17.0	20.0		mmhos
V_{DS} = +15V, f = 1MHz													
I_D = 20mA		2.4	3.0		2.4	3.0		3.0	3.6		3.0	3.6	pF
I_D = 0A		1.0	1.2		1.0	1.2		1.0	1.2		1.0	1.2	pF
I_D = 0A		0.20	0.30		0.20	0.30		0.20	0.30		0.20	0.30	pF
V_{DS} = +15V, I_D = 20mA, f = 1GHz													
V_{GS} ≅ +4V	8	10		8	10								dB
V_{GS} ≅ +2.5V							8	10		8	10		dB
V_{GS} ≅ +4V		4.5	6.0		5.0	6.5							dB
V_{GS} ≅ +2.5V								3.5	4.5		4.0	5.0	
V_{GS} = +5V, I_D = 5mA		50	70		50	70		35	50		35	50	Ω
V_{DS} = 15V, I_D = 20mA, f = 1GHz, Δf = 2MHz		29			29			29			29		dBM

CHARACTERISTIC CURVES – SD200/201 (Continued)

DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE

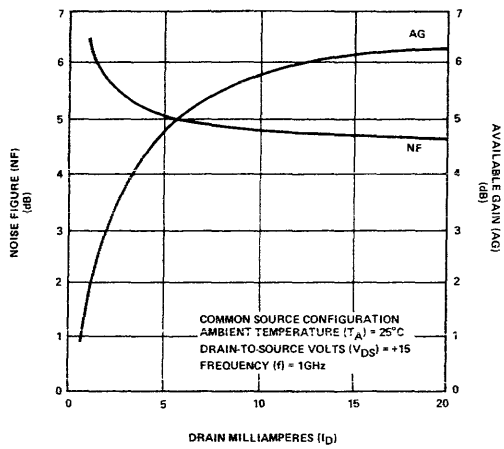


POWER GAIN VS DRAIN CURRENT

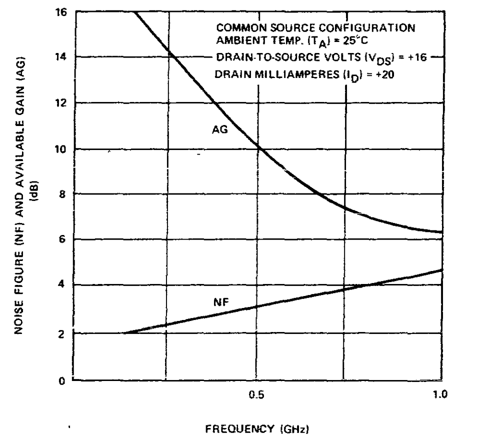


CHARACTERISTIC CURVES – SD200/201 (Continued)

NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



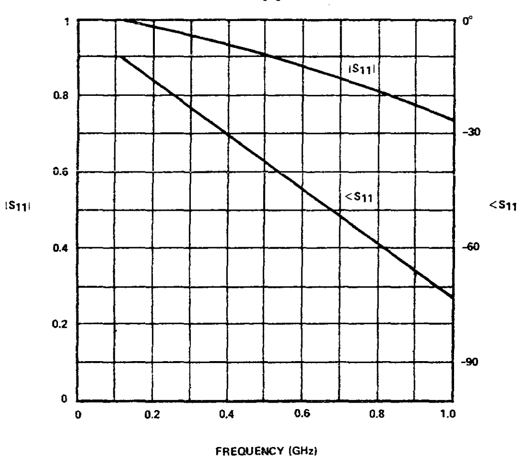
OPTIMUM NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY



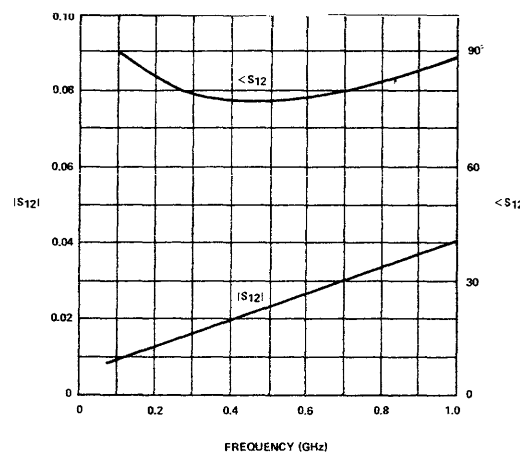
"S" PARAMETERS

COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (T_A) = 25°C
DRAIN MILLIAMPERES (I_D) = 20
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

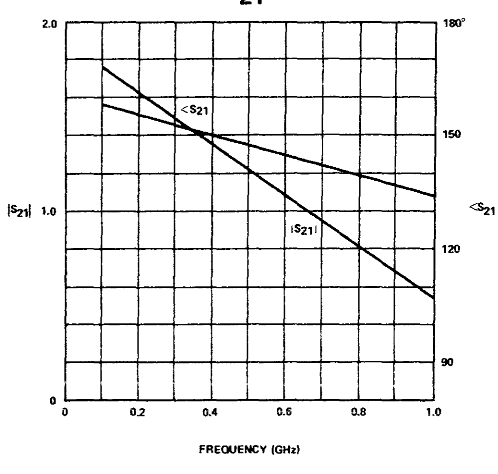
S_{11}



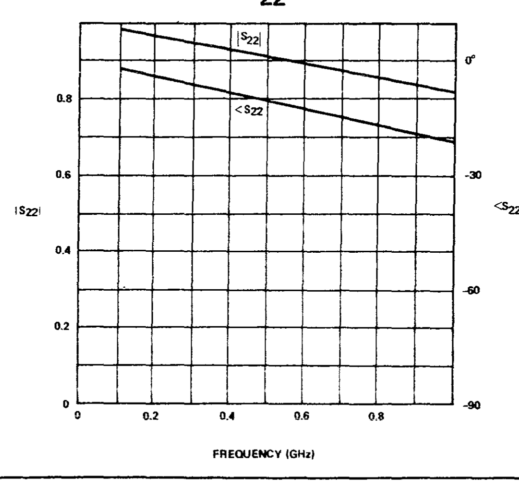
S_{12}



S_{21}

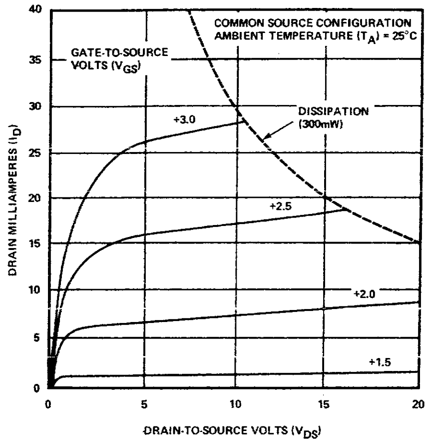


S_{22}

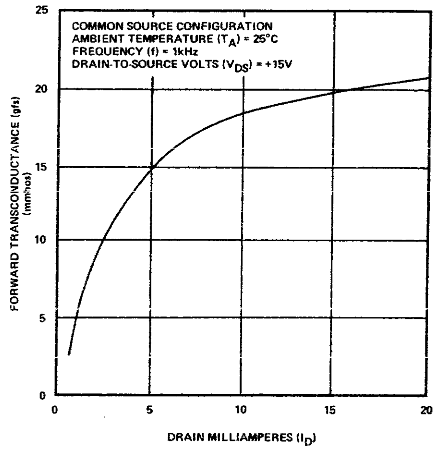


CHARACTERISTIC CURVES – SD202/203

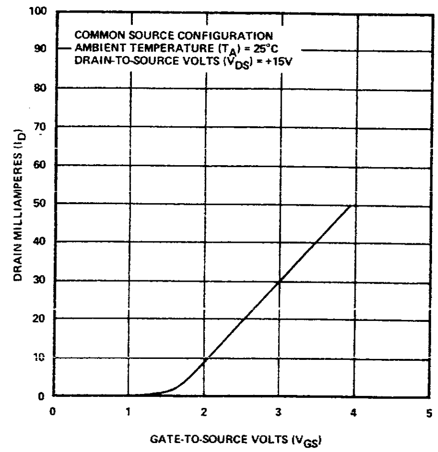
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



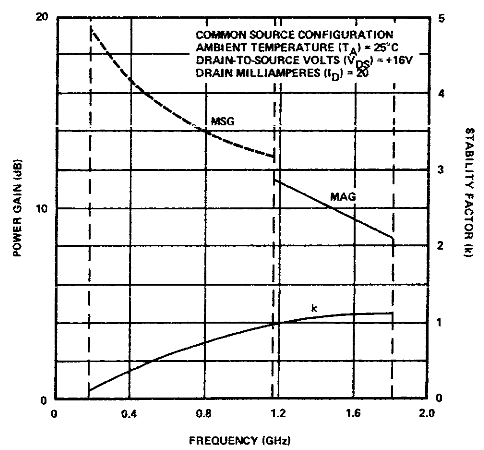
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



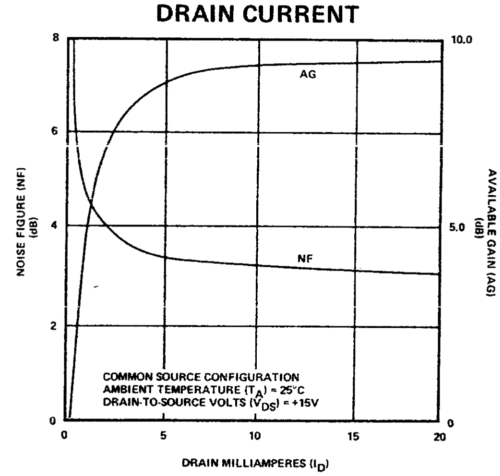
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



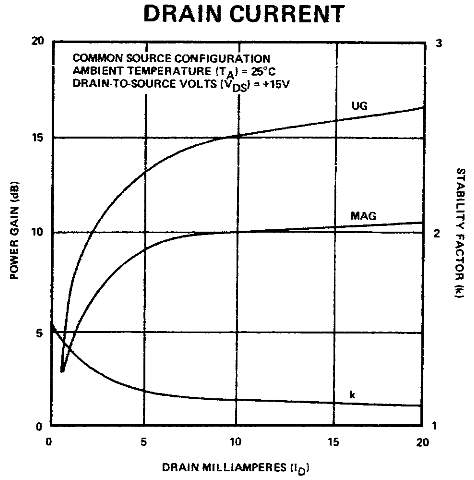
POWER GAIN VS FREQUENCY



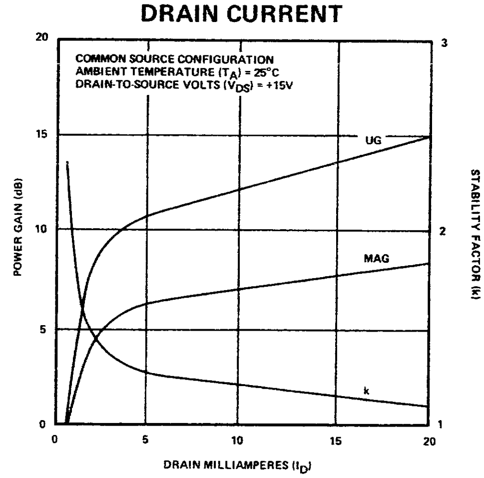
1.0GHz NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



1.5GHz POWER GAIN VS DRAIN CURRENT



1.8GHz POWER GAIN VS DRAIN CURRENT



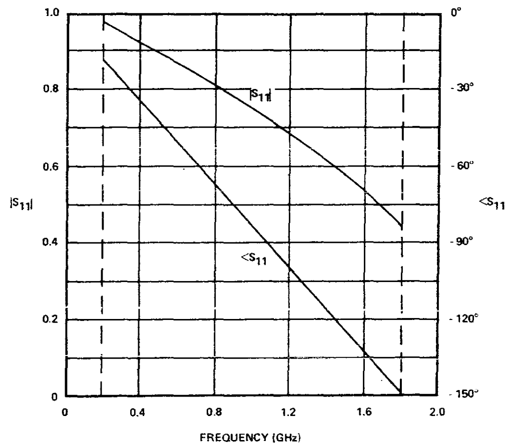
CHARACTERISTIC CURVES – SD202/203 (Continued)

"S" PARAMETERS

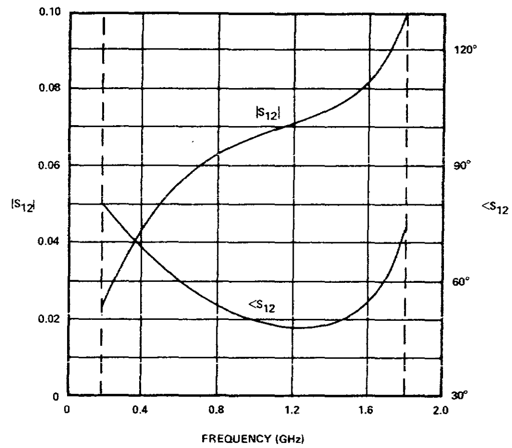
COMMON SOURCE CONFIGURATION
AMBIENT TEMPERATURE (T_A) = 25°C

DRAIN MILLIAMPERES (I_D) = 20
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

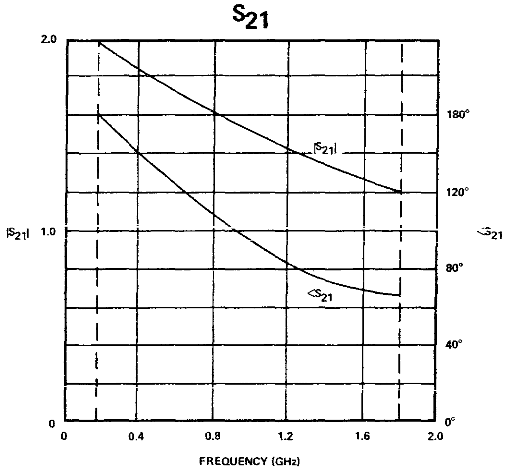
S_{11}



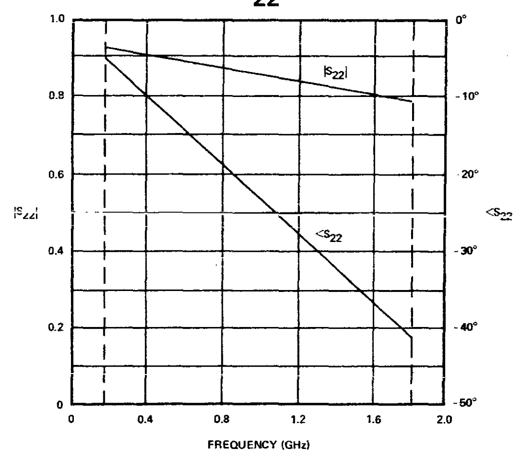
S_{12}



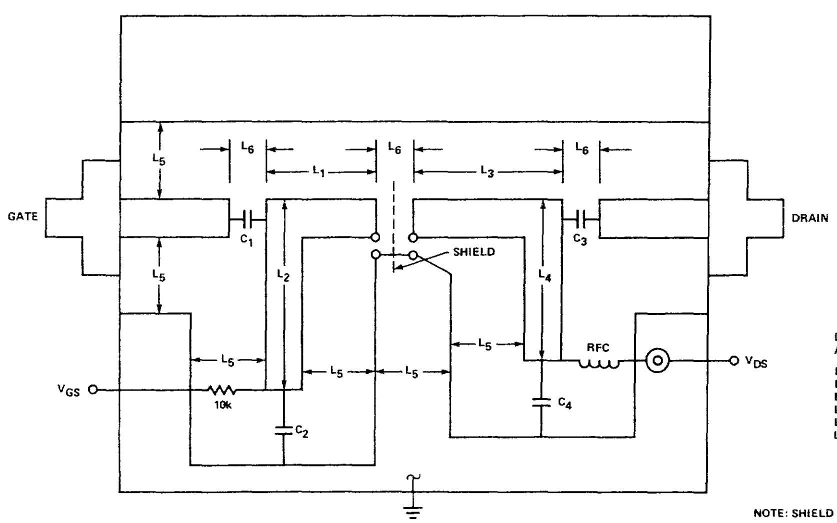
S_{21}



S_{22}



1GHz NOISE FIGURE AND POWER GAIN TEST FIXTURE



DIALECTRIC IS 1/16" TEFLON-FIBERGLASS (3M-K6096-11)
ALL MICROSTRIP WIDTH = 0.175"

L_1 = 0.48"	$C_1 = C_2 = C_3$ = 0.8-10pF Johanson 5201
L_2 = 1.52"	C_4 = 1.20pF Johanson 5501
L_3 = 0.64"	RFC = 10 TURNS 26 AWG 1/4" DIA.
L_4 = 1.36"	1000pF BYPASS CORY FT4-01-2
L_5 = 5/16"	LAUNCHERS – OSM248-2
L_6 = 1/8"	

NOTE: SHIELD AND 4 TUNABLE CAPACITORS ON GROUND PLANE SIDE OF AMPLIFIER.

signetics

D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

ANALOG AND DIGITAL SWITCH AND SWITCH DRIVER APPLICATIONS

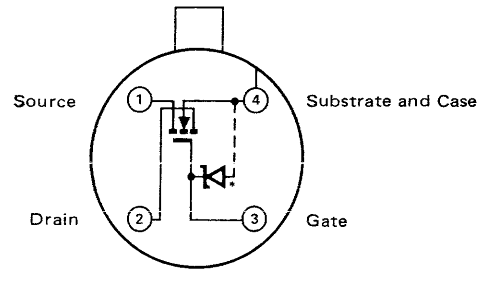
SD210 SD211 SD212 SD213 SD214 SD215

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of −0.3V to +25V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

PIN CONFIGURATION (Top View)



*Diode protection on SD211/213/215 only.

Order Part Nos.
SD210DE, SD211DE, SD212DE,
SD213DE, SD214DE, SD215DE

FEATURES

- LOW FEEDBACK CAPACITANCE – 0.30pF
- LOW DRAIN NODE CAPACITANCE – 1.3pF
- LOW GATE NODE CAPACITANCE – 2.4pF
- LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
- ION-IMPLANTED FOR GREATER RELIABILITY
- EXCELLENT ISOLATION FROM INPUT TO OUTPUT – 120dB
- 35V DRAIN-TO-SOURCE VOLTAGE FOR SD210/211

APPLICATIONS

SWITCH DRIVER
ANALOG SWITCH
MULTIPLEXERS
DIGITAL SWITCH
SAMPLE AND HOLD
CHOPPERS
A-TO-D CONVERTERS
D-TO-A CONVERTERS

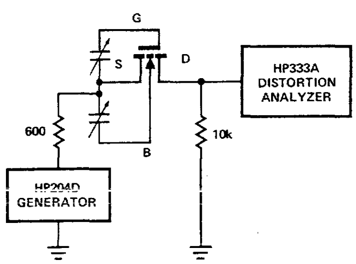
ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ (Unless Otherwise Noted)

	PARAMETER	SD210	SD211	SD212	SD213	SD214	SD215	UNITS
V_{DS}	Drain-to-Source	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	Source-to-Drain	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	Drain-to-Substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{SB}	Source-to-Substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	Gate-to-Source	±40	−15 +25	±40	−15 +25	±40	−25 +30	Vdc
V_{GB}	Gate-to-Substrate	±40	−0.3 +25	±40	−0.3 +25	±40	−0.3 +30	Vdc
V_{GD}	Gate-to-Drain	±40	−15 +25	±40	−15 +25	±40	−25 +30	Vdc

ABSOLUTE MAXIMUM RATINGS (All devices)

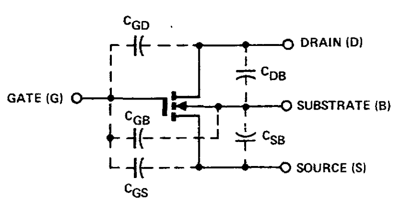
Drain Current (I_D)	50mA
Ambient Temperature Range	
Storage	−65°C to +175°C
Operating	−65°C to +125°C
Transistor Dissipation (P_T)	
At 25°C Case Temperature	1.2W
(Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	
At 25°C Free-Air Temperature	300mW
(Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	

DISTORTION TEST CIRCUIT



NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

CAPACITANCE MODEL



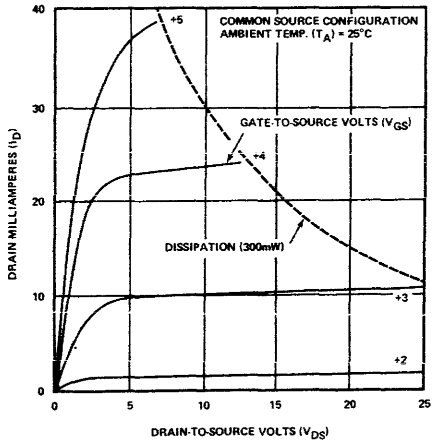
ELECTRICAL CHARACTERISTICS

PARAMETER	
Breakdown Voltage	
BV_{DS}	Drain-To-Source
BV_{SD}	Source-To-Drain
BV_{DB}	Drain-To-Substrate
BV_{SB}	Source-To-Substrate
Leakage Current	
I_{DS} (OFF)	Drain-To-Source
I_{SD} (OFF)	Source-To-Drain
I_{GB}	Gate
V_T	Threshold Voltage
gfs	Forward Transconductance
Small Signal Capacitances (See Capacitance Model)	
$C_{(GS+GD+GB)}$	Gate Node
$C_{(GD+DB)}$	Drain Node
$C_{(GS+SB)}$	Source Node
C_{DG}	Reverse Transfer
r_{DS} (ON)	Drain-To-Source Resistance

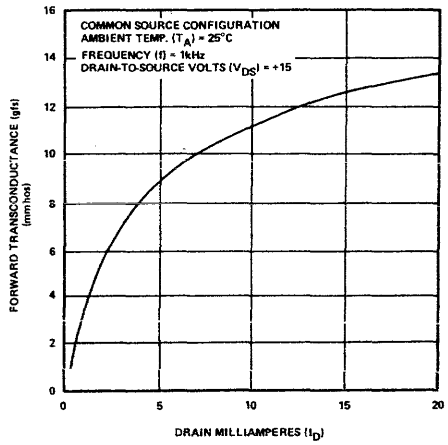
TEST CONDITIONS	SD210			SD211			SD212			SD213			SD214			SD215			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS} = V_{BS} = 0V$, $I_S = 10\mu A$	30	35		30	35														V
$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		10	25		10	25		10	25		20	25		20	25		V
$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	10			10			10			10			20			20			V
$V_{GB} = 0V$, Source OPEN, $I_D = 10nA$	15			15			15			15			25			25			V
$V_{GB} = 0V$, Drain OPEN, $I_S = 10\mu A$	15			15			15			15			25			25			V
$V_{GS} = V_{BS} = -5V$																			
$V_{DS} = +10V$		1	10		1	10		1	10		1	10							nA
$V_{DS} = +20V$														1	10		1	10	nA
$V_{GD} = V_{BD} = -5V$																			
$V_{SD} = +10V$		1	10		1	10		1	10		1	10							nA
$V_{SD} = +20V$														1	10		1	10	nA
$V_{DB} = V_{SB} = 0V$																			
$V_{GB} = \pm 40V$			0.1						0.1						0.1				nA
$V_{GB} = +25V$					10						10								µA
$V_{GB} = +30V$																	10		µA
$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$, $V_{SB} = 0V$	0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
$V_{DS} = 10V$, $V_{SB} = 0V$, $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		10	15		10	15		10	15		mmhos
$V_{DS} = 10V$, $f = 1kHz$, $V_{GS} = V_{BS} = -15V$																			
		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5	pF
		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5	pF
		3.5	4.0		3.5	4.0		3.5	4.0		3.5	4.0		3.5	4.0		3.5	4.0	pF
		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5	pF
$I_D = 0.1mA$, $V_{SB} = 0$																			
$V_{GS} = +5V$		50	70		50	70		50	70		50	70		50	70		50	70	Ω
$V_{GS} = +10V$		30	45		30	45		30	45		30	45		30	45		30	45	Ω
$V_{GS} = +15V$		23			23			23			23			23			23		Ω
$V_{GS} = +20V$		19			19			19			19			19			19		Ω
$V_{GS} = +25V$		17						17						17			17		Ω

CHARACTERISTIC CURVES

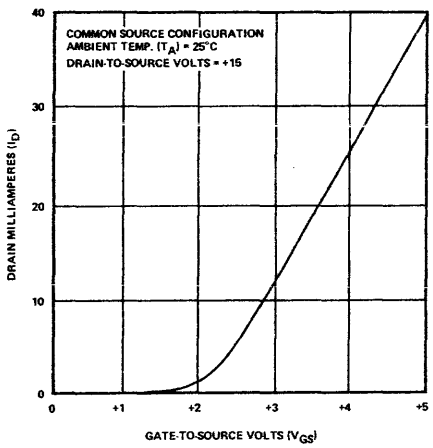
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



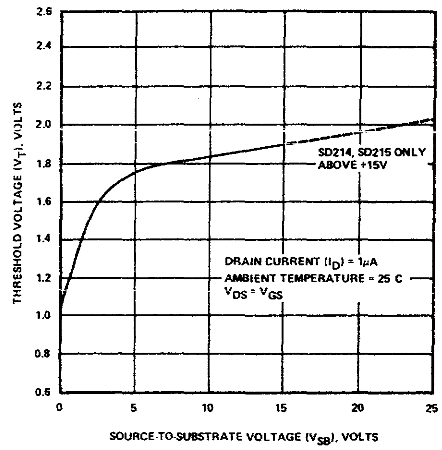
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



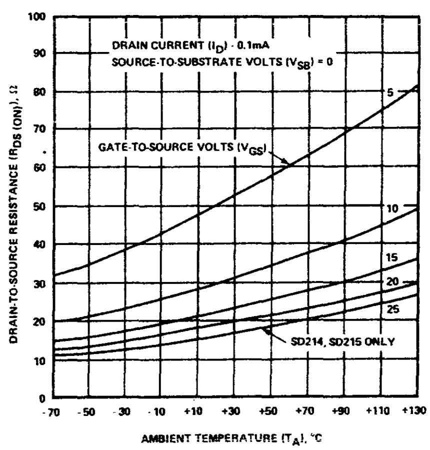
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



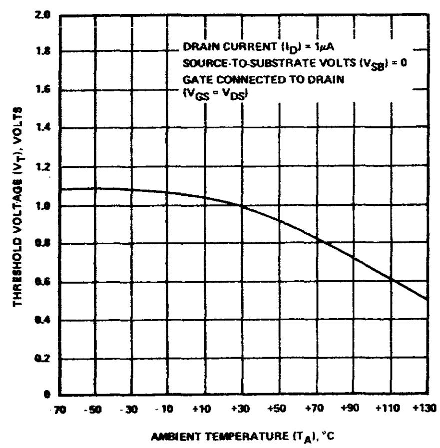
THRESHOLD VOLTAGE VS SOURCE-TO-SUBSTRATE VOLTAGE



DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE

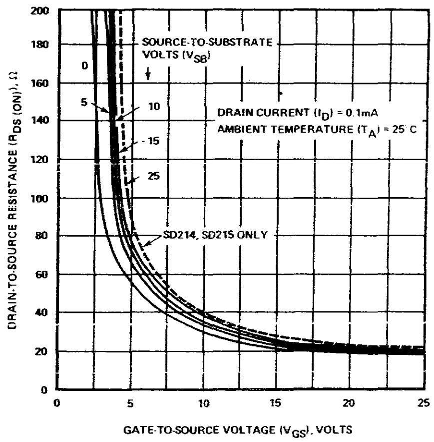


THRESHOLD VOLTAGE VS TEMPERATURE

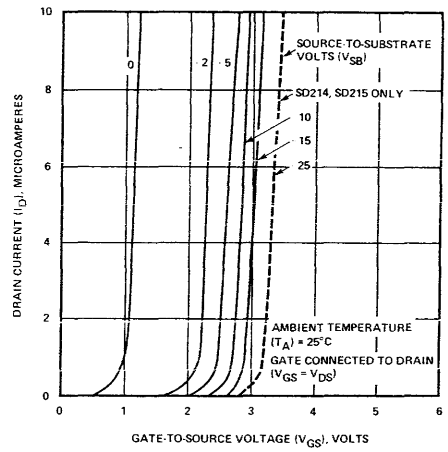


CHARACTERISTIC CURVES (Continued)

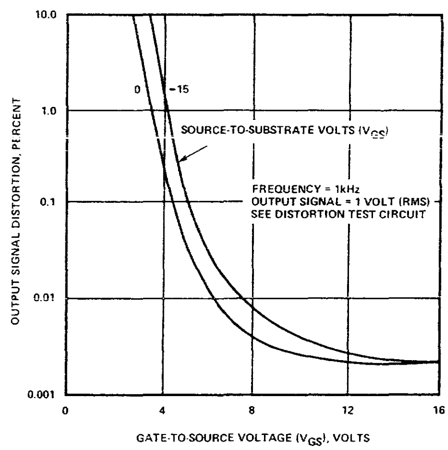
DRAIN-TO-SOURCE RESISTANCE VS GATE-TO-SOURCE VOLTAGE



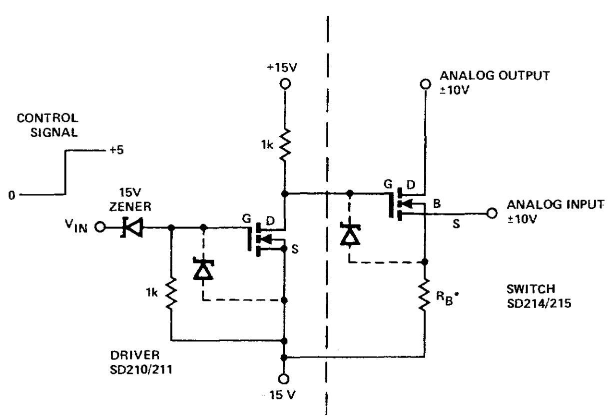
DRAIN CURRENT VS GATE-TO-SOURCE VOLTAGE



DISTORTION VS GATE-TO-SOURCE VOLTAGE



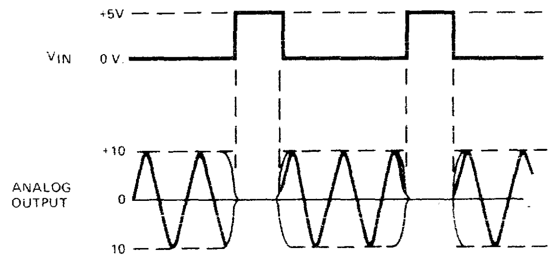
D-MOS DRIVER/SWITCH APPLICATION



R_B* OPTIONAL CURRENT LIMITING RESISTOR

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

TYPICAL WAVEFORMS

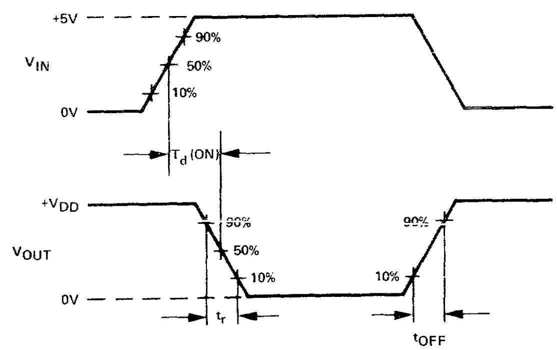


SWITCHING CHARACTERISTICS

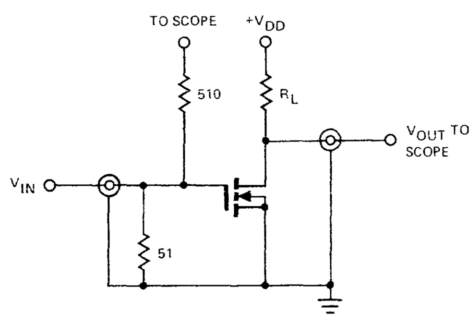
		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SWITCHING WAVEFORMS



TEST CIRCUIT



INPUT PULSE

t_d, t_r < 1ns
PULSE WIDTH = 100ns
REP RATE = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE: ALL RESISTORS STANDARD AND ARE MEASURED IN OHMS.

signetics

D-MOS FET DUAL GATE N-CHANNEL ENHANCEMENT

SD300 SD301 SD303 SD304

VHF, UHF AND GENERAL PURPOSE RF APPLICATIONS

DESCRIPTION

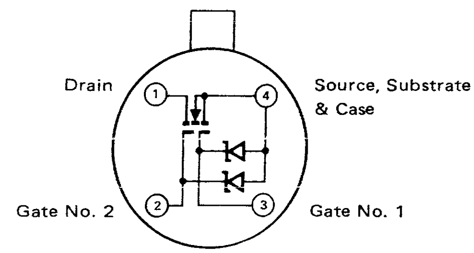
The Signetics D-MOS SD300/301/303/304 are silicon, dual-insulated-gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +25.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The devices' attributes make them ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure, has made the feedback capacity (Crss) less than 0.02pF. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of these devices. The SD300, 301, 303 and 304 are hermetically sealed in modified 4-lead TO-72 packages.

GENERAL FEATURES

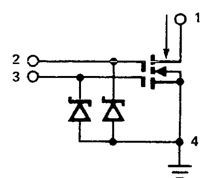
- LOWER CROSS-MODULATION AND WIDER DYNAMIC RANGE THAN BIPOLAR OR SINGLE GATE FETs
- REVERSE AGC CAPABILITY
- LINEAR MIXING CAPABILITY
- DIODE PROTECTED GATES
- HIGH FORWARD TRANSCONDUCTANCE — gfs = 10,000μmhos
- ION-IMPLANTED
- POSITIVE BIAS ONLY

PIN CONFIGURATION (Top View)



Order Part Nos:
SD300DC, SD301DC, SD303DC, SD304DE

DUAL GATE CASCODE BIAS SCHEME



$+V_{DS} = 0 \rightarrow +20$ Volts
$+V_{G1S} = 0 \rightarrow +4$ Volts
$+V_{G2S} = 0 \rightarrow +10$ Volts
$+I_{DS} = 0 \rightarrow +20$mA

FEATURES

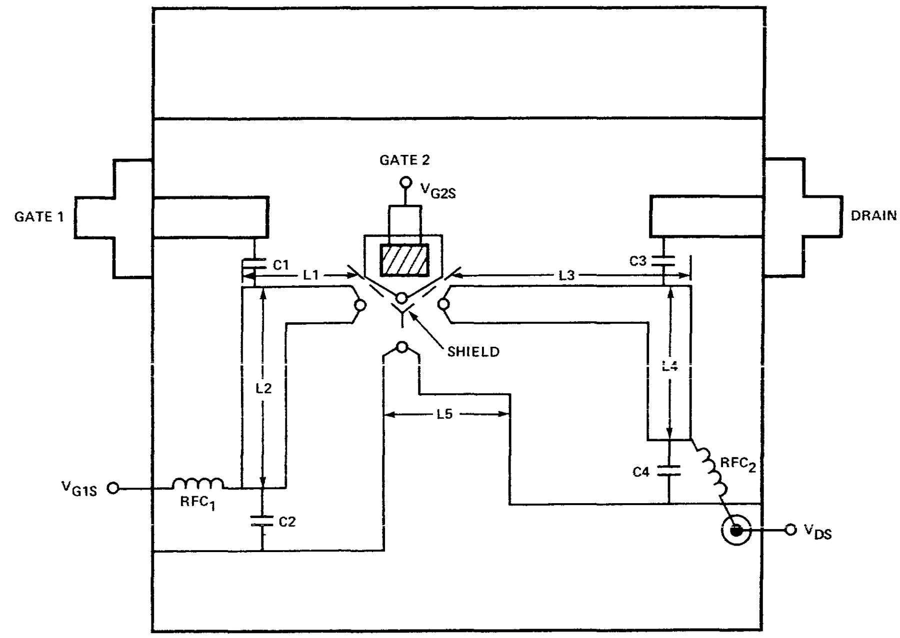
PARAMETER	SD300	SD301	SD303	SD304	UNIT
High Gain Through UHF Range	13	14	14		dB at 1GHz
High Gain Through VHF Range				16	dB at 500MHz
Low Noise Through UHF Range	8	6	5.5		dB at 1GHz
Low Noise Through VHF Range				5	dB at 500MHz
Low Input Capacitance	2.0	2.0	3.0	2.5	pF
Low Feedback Capacitance	0.02	0.02	0.02	0.03	pF
Low Output Capacitance	1.0	0.6	0.6	1.0	pF

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

Drain-To-Source (V_{DS})	
SD300/304	+25V
SD301	+20V
DC Gate No. 1-To-Substrate Voltage (V_{G1B})	-0.3V, +10V
DC Gate No. 2-To-Substrate Voltage (V_{G2B})	-0.3V, +15V
Drain Current (I_D)	50mA
Ambient Temperature Range (T_A)	
Storage	-65°C to +175°C
Operating	-65°C to +125°C
Transistor Dissipation (P_T)	
At +25°C Case Temperature	1.2W
(Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	
At +25°C Free-Air Temperature	300mW
(Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	

TEST FIXTURE (1GHz) (Used With SD300, 301, 303)



DIELECTRIC IS 1/16" TEFLON-FIBERGLASS (3M-K6098-11).
ALL MICROSTRIP WIDTH = 0.175 INCH.

L_1 = 0.42 INCH	C_1 = 0.8-10pF JOHANSON 5201
L_2 = 1.68 INCHES	C_2 = C_4 = 1.20pF JOHANSON 5501
L_3 = 0.64 INCH	C_3 = 0.4-6.0pF JOHANSON 4642
L_4 = 1.52 INCHES	RFC_1 = 0.22μH
L_5 = 0.30 INCH	RFC_2 = 18μH

NOTE: SHIELD AND ALL PASSIVE COMPONENTS ON GROUND PLANE SIDE OF AMPLIFIER.
1000pF BYPASSES ARE:
DRAIN: CORY FT4-01-2
GATE 2: AMERICAN TECHNICAL CERAMICS ATC100B (CHIP CAPACITOR)
LAUNCHERS ARE OSM248-2

ELECTRICAL CHARACTERISTICS T_A = +25°C (Unless Otherwise Noted).

PARAMETER		TEST CONDITIONS	SD300			SD301			SD303			SD304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
BV_{DS}	Drain-To-Source Breakdown Voltage	V_{G1S} = V_{G2S} = 0V, I_D = 5μA	25	30		20	25		20	25		25	30		V
I_{G1SS}	Gate 1 Leakage Current	V_{G1S} = +5V, V_{G2S} = V_{DS} = 0V		0.001	0.1		0.001	0.1		0.001	0.1		0.001	0.1	μA

ELECTRICAL CHARACTERISTICS $T_A = +25°C$ (Unless Otherwise Noted), Continued

PARAMETER		TEST CONDITIONS	SD300			SD301			SD303			SD304			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{G2SS}	Gate 2 Leakage Current	V_{G2S} = +10V, $V_{G1S} = V_{DS}$ = 0V		0.001	0.1		0.001	0.1		0.001	0.1		0.001	0.1	μA
$I_{D\,(OFF)}$	Drain-To-Source Leakage Current	V_{DS} = +15V, $V_{G1S} = V_{G2S}$ = 0V		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero Bias Drain Current	V_{DS} = +15V, $V_{G1S} = V_{G2S}$ = 0V		0.001	1.0		0.001	1.0		0.001	1.0		0.001	1.0	μA
V_{T1}	Gate 1 Threshold Voltage	$V_{DS} = V_{G1S} = V_{T1}$, V_{G2S} = +10V, I_D = 1μA	0.1	1.0	2.0	0.1	1.0	2.0	0.1	0.5	1.5	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold Voltage	$V_{DS} = V_{G2S} = V_{T2}$, V_{G1S} = +4V, I_D = 1μA	0.1	1.0	2.0	0.1	1.0	2.0	0.1	0.5	1.5	0.1	1.0	2.0	V
Small Signal Short Circuit Capacitances		f = 1MHz, Gate 2 AC Grounded													
C_{iss}	Input	V_{DS} = +15V, V_{G1S} ≅ 3.5V, V_{G2S} = +10V, I_D = 18mA		2.0	2.5		2.0	2.5					2.5	3.0	pF
		V_{DS} = +15V, V_{G1S} ≅ +2.5V, V_{G2S} = +10V, I_D = 18mA f = 1MHz								3.0	3.5				pF
C_{oss}	Output	V_{DS} = +15V, V_{G1S} = 0V, V_{G2S} = +10V, f = 1MHz		1.0	1.2		0.6	0.8		0.6			1.0	1.2	pF
C_{rss}	Reverse Transfer	V_{DS} = +15V, V_{G1S} = 0V, V_{G2S} = +10V, f = 1MHz		0.02			0.02			0.02			0.03		pF
gfs	Forward Transconductance	V_{DS} = +15V, V_{G1S} ≅ +3.5V V_{G2S} = +10V, I_D = 18mA, f = 1kHz	8.0	10.0		8.0	10.0					8.0	10.0		mmhos
		V_{DS} = +15V, V_{G1S} ≅ +2.5V, V_{G2S} = +10V, I_D = 18mA							13.0	15.0					mmhos
Gps	Power Gain	V_{DS} = +15V, V_{G1S} ≅ +3.5V, V_{G2S} = +10V, I_D = 18mA													
		f = 1GHz	9.0	13.0*		10.0	14.0*								dB
		f = 500MHz										13.0	16.0		dB
		f = 200MHz	22.0	24.0		22.0	25.0								dB
		V_{DS} = +15V, V_{G1S} ≅ +2.5V, V_{G2S} = +10V, I_D = 18mA, f = 1GHz							10.0	14.0*					dB
NF	Noise Figure	V_{DS} = +15V, V_{G1S} ≅ +3.5V, V_{G2S} = +10V, I_D = 18mA													
		f = 1GHz		8.0*	9.0		6.0*	7.0							dB
		f = 500MHz											5.0	6.0	dB
		f = 200MHz		3.0	4.0		2.0	3.0							dB
		V_{DS} = +15V, V_{G1S} ≅ +2.5V, V_{G2S} = +10V, I_D = 18mA, f = 1GHz								5.5*	7.0				dB
E_{int}	Interfering Signal Level At Gate For 1% Cross-Modulation Distortion. Peak Voltage Referenced To 300Ω System.	V_{DS} = +15V, V_{G2S} = +10V, I_D = 18mA, Desired Signal f = 500MHz, Undesired Signal f = 501MHz		200			200						200		mV
		V_{DS} = +15V, V_{G2S} = +10V, I_D = 18mA, Wanted Signal f = 1GHz, Interfering Signal f = 0.995GHz								150					mV
AGC (V_{G2S})	Range Of Automatic Gain Control	V_{DS} = +15V, V_{G1S} ≅ +3.5V, f = 500MHz		40			40						40		dB
		V_{DS} = +15V, V_{G1S} ≅ +2.5V, f = 500MHz								40					dB
$r_{DS\,(ON)}$	Drain-To-Source On Resistance	V_{G1S} = +5V, V_{G2S} = +10V, I_D = 0.1mA		90	130		90	130		65	80		90	130	Ω

*Measured in amplifier test fixture.

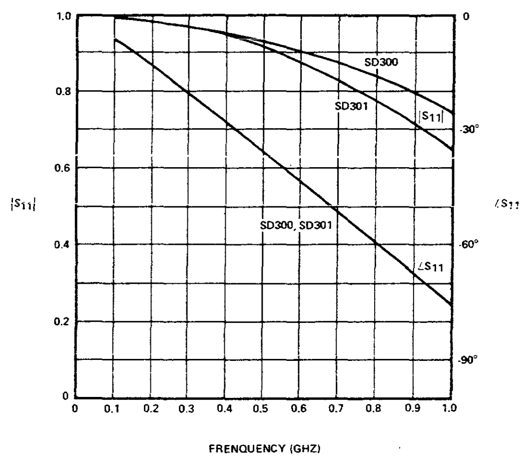
CHARACTERISTIC CURVES

SD300, 301

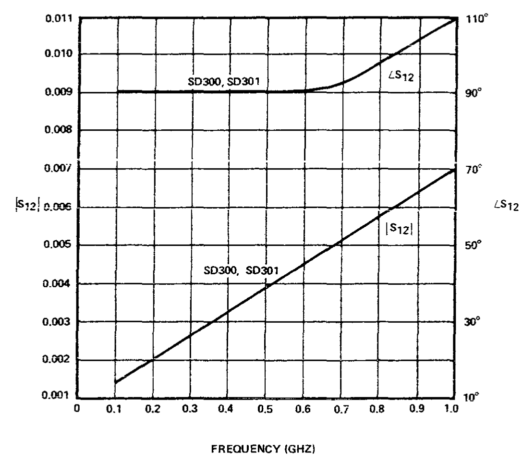
S PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

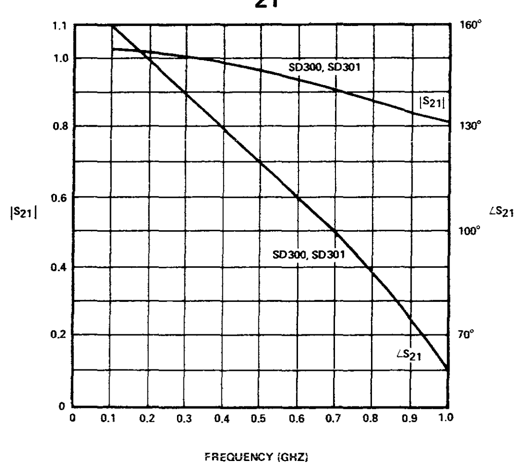
S_{11}



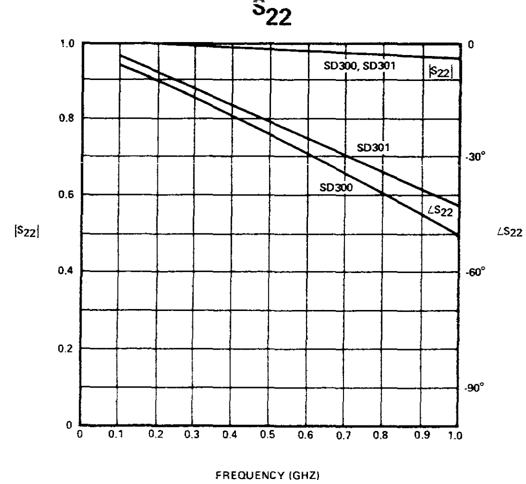
S_{12}



S_{21}



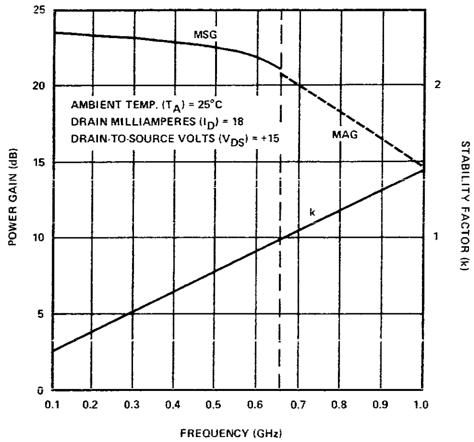
S_{22}



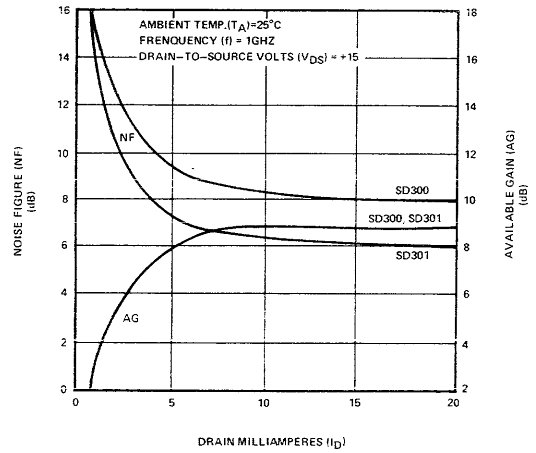
CHARACTERISTIC CURVES (Continued)

SD300, 301

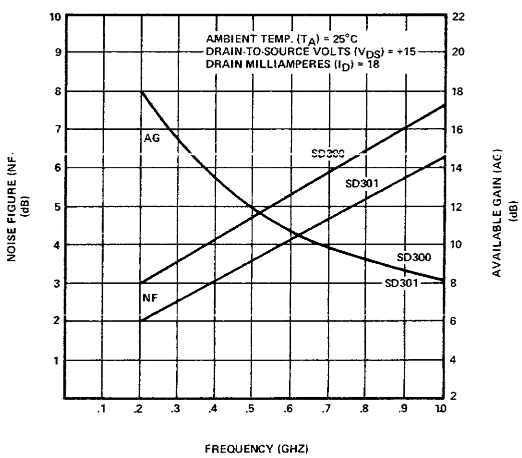
POWER GAIN VS FREQUENCY



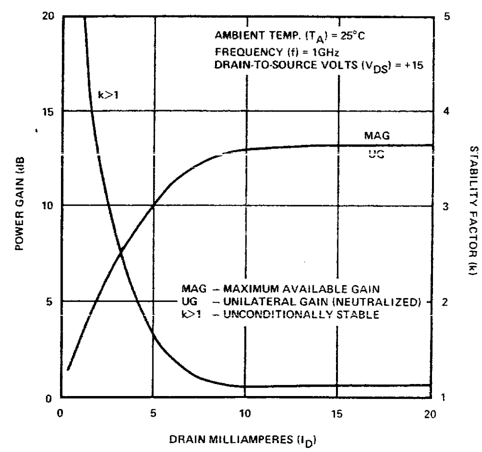
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



NOISE FIGURE AND AVAILABLE GAIN VS FREQUENCY

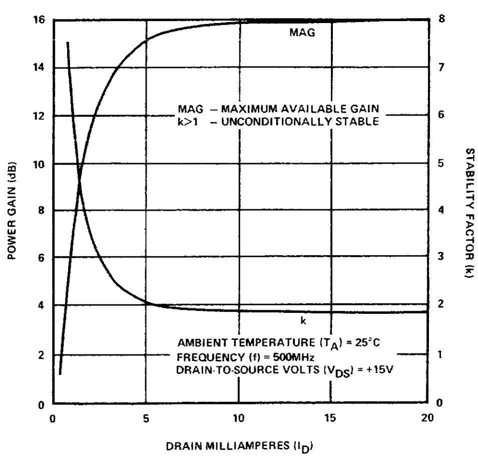


POWER GAIN VS DRAIN CURRENT

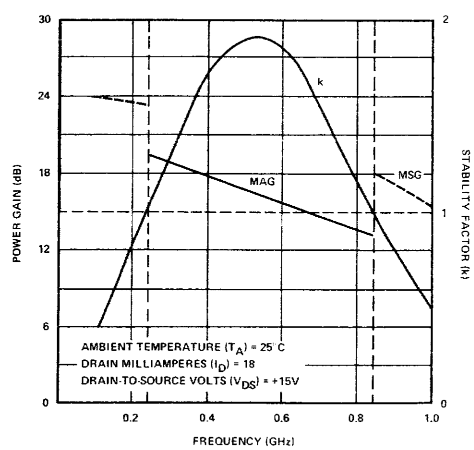


SD304

POWER GAIN VS DRAIN CURRENT



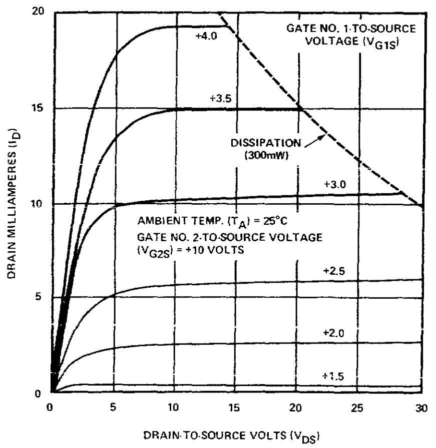
POWER GAIN VS FREQUENCY



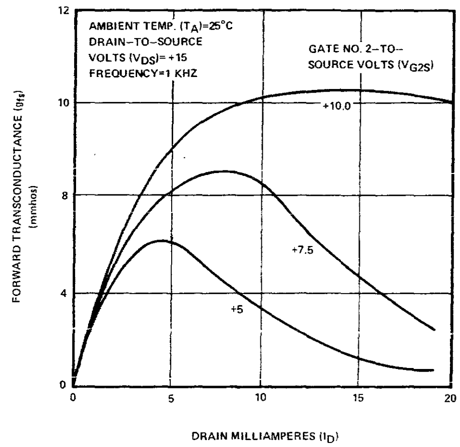
CHARACTERISTIC CURVES (Continued)

SD300, 301, 304

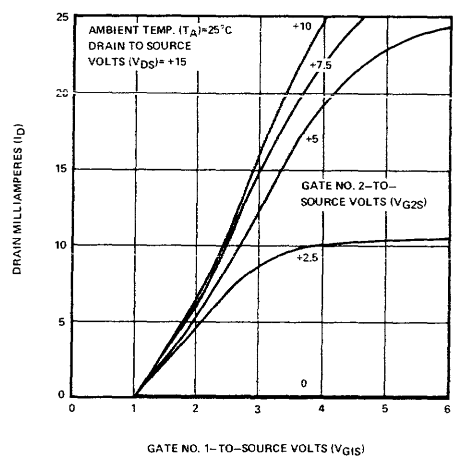
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



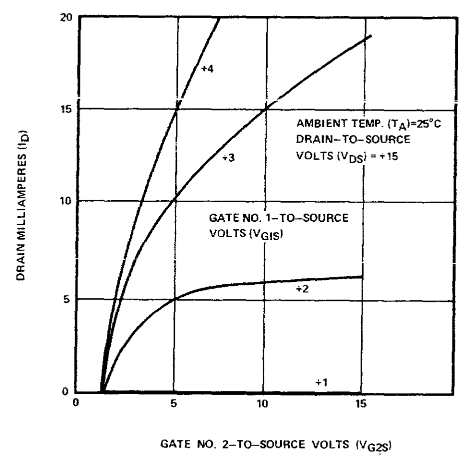
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



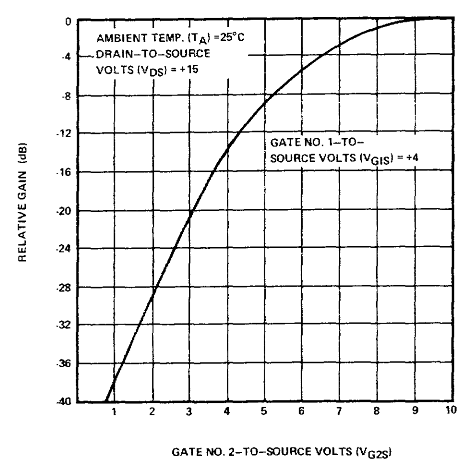
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



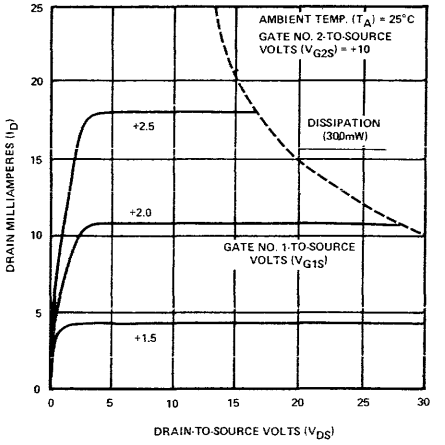
AUTOMATIC GAIN CONTROL RANGE AT 500MHz



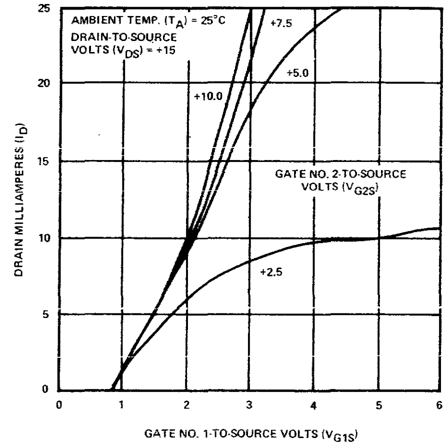
CHARACTERISTIC CURVES (Continued)

SD303

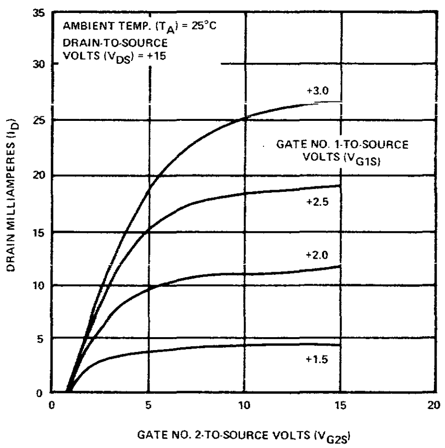
DRAIN CURRENT VERSUS DRAIN-TO-SOURCE VOLTAGE



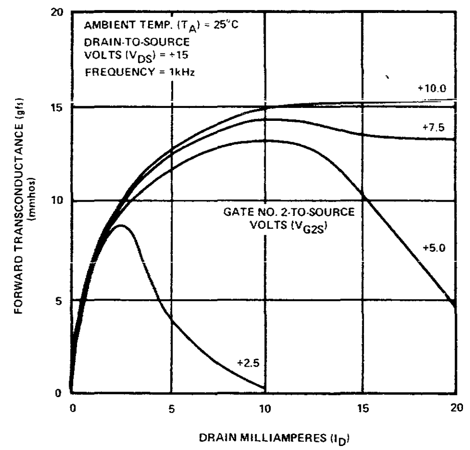
DRAIN CURRENT VERSUS GATE NO. 1-TO-SOURCE VOLTAGE



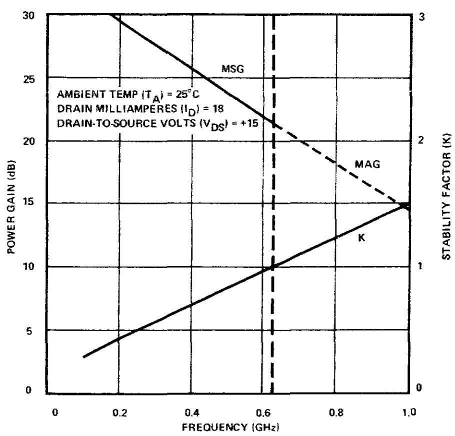
DRAIN CURRENT VERSUS GATE NO. 2-TO-SOURCE VOLTAGE



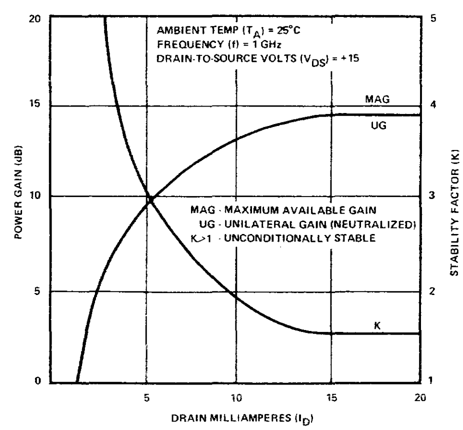
1kHz FORWARD TRANSCONDUCTANCE VERSUS DRAIN CURRENT



POWER GAIN VERSUS FREQUENCY



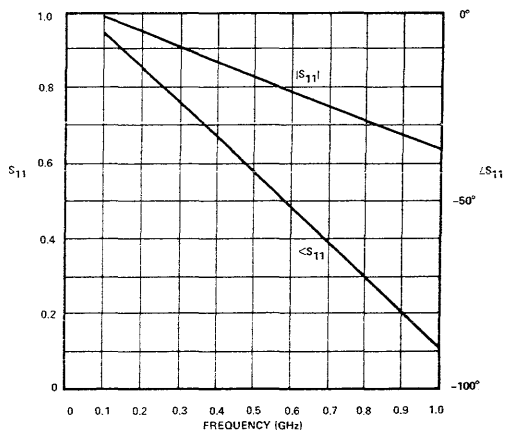
POWER GAIN VERSUS DRAIN CURRENT

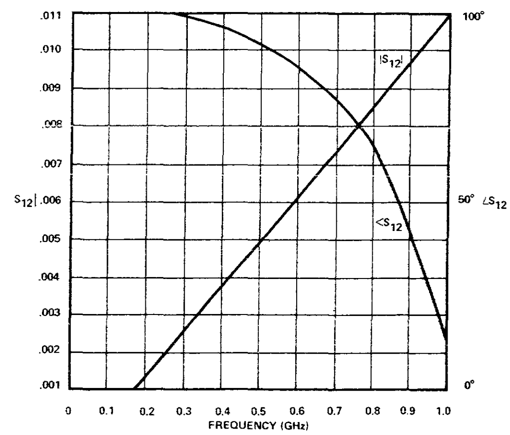


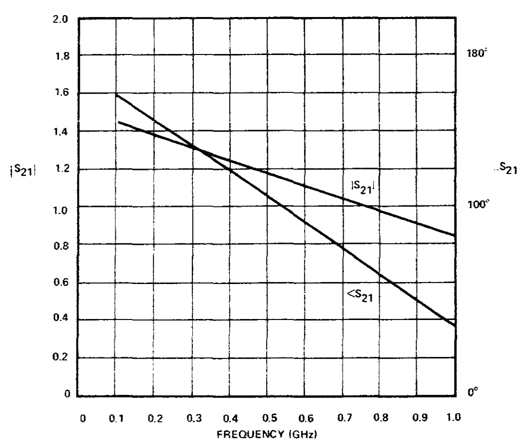
CHARACTERISTIC CURVES (Continued)

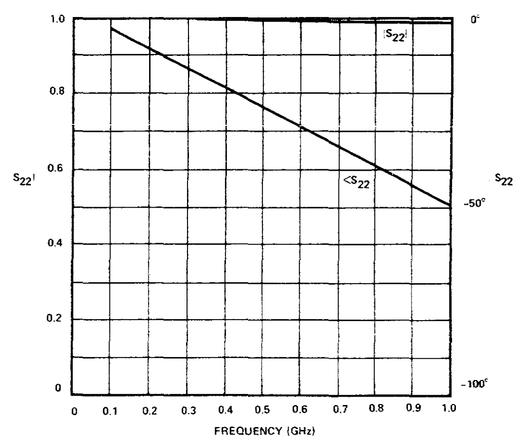
SD303

S PARAMETERS
AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15









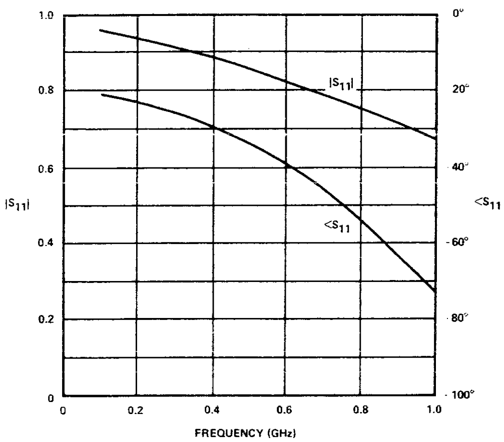
CHARACTERISTIC CURVES (Continued)

SD304

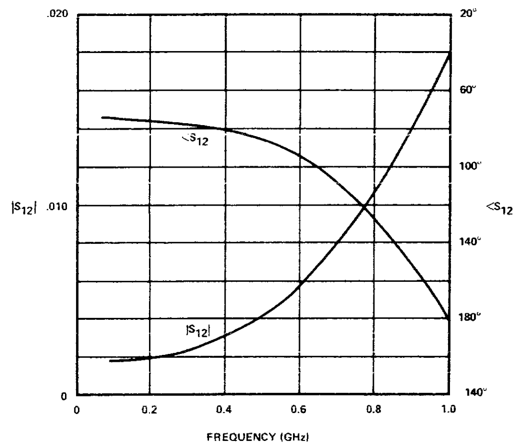
S PARAMETERS

AMBIENT TEMP. (T_A) = 25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

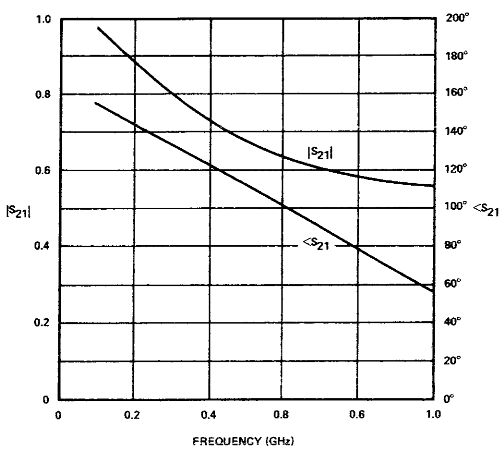
S_{11}



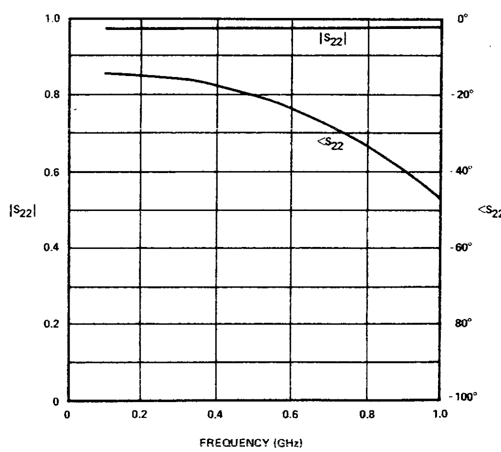
S_{12}



S_{21}



S_{22}



SD305 SD306

DESCRIPTION

The Signetics D-MOS SD305 and 306 are silicon, dual-insulated gate, field-effect transistors of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations.

The devices' attributes make them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (C_{G1D}) typically less than 0.03pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the devices. The SD305 and SD306 are hermetically sealed in a 4-lead TO-72 package.

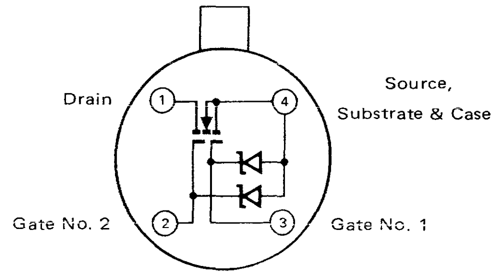
GENERAL FEATURES

- POSITIVE BIAS ONLY
- LOW GATE VOLTAGES
- ENHANCEMENT MODE OPERATION
- WIDE AGC RANGE – 50dB AT 200MHz
- ZENER DIODE GATE PROTECTION
- ION IMPLANTED FOR GREATER RELIABILITY

FEATURES – SD305 (VHF TV and FM Mixer)

- HIGH CONVERSION GAIN – 17dB AT 200MHz WITH $V_{G1S} = V_{G2S}$ FOR BIASING SIMPLICITY

PIN CONFIGURATION (Top View)



ORDER PART NOS. SD305DE and SD306DE

- EXCELLENT ISOLATION FROM GATE NO. 1 (RF) TO GATE NO. 2 (LO) – 20dB AT 200MHz
- LOW INPUT CAPACITANCE – 4.0pF
- LOW FEEDBACK CAPACITANCE – 0.03pF
- EXCELLENT CROSS MODULATION PERFORMANCE AND LOW NOISE OPERATION
- HIGH TRANSCONDUCTANCE – 27mmhos

FEATURES – SD306 (VHF TV and FM RF Amplifier)

- HIGH POWER GAIN WITHOUT NEUTRALIZATION – 20dB AT 200MHz
- LOW NOISE FIGURE – 1.5dB AT 200MHz
- LOW INPUT AND OUTPUT CAPACITANCE – 3.3pF AND 1.0pF CONSTANT WITH AGC
- LOW FEEDBACK CAPACITANCE – 0.03pF
- SUPERIOR CROSS MODULATION PERFORMANCE
- HIGH TRANSCONDUCTANCE – 15mmhos

ABSOLUTE MAXIMUM RATINGS T_A = 25°C (Unless Otherwise Noted)

	PARAMETER	SD305	SD306	UNIT
V_{DS}	Drain-To-Source Voltage	+20		V
V_{G1B}	Gate No. 1-To-Substrate Voltage	−0.3 to +20		Vdc
V_{G2B}	Gate No. 2-To-Substrate Voltage	−0.3 to +20		Vdc
I_D	Drain Current	150	50	mA
T_A	Ambient Temperature Range			
	Storage	−65 to +175		°C
	Operating	−65 to +125		°C
P_T	Transistor Dissipation			
	At 25°C Case Temperature	1.2		W
	(Derate linearly to 125°C case temperature at the rate of 8.0mW/°C)			
	At 25°C Free-Air Temperature	300		mW
	(Derate linearly to 125°C free-air temperature at the rate of 2.0mW/°C)			

ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	SD305			SD306			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFF Characteristics									
BV_{DS}	Drain-To-Source Breakdown Voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		20	25		V
I_D (OFF)	Drain-To-Source Leakage Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{DSS}	Zero Bias Drain Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0		0.001	1.0	μA
I_{G1SS}	Gate No. 1 Leakage Current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
I_{G2SS}	Gate No. 2 Leakage Current	$V_{G2S} = +10V$, $V_{G1S} = V_{DS} = 0V$		0.001	0.1		0.001	0.1	μA
ON Characteristics									
V_{T1}	Gate 1 Threshold Voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
V_{T2}	Gate 2 Threshold Voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	1.0	2.0	0.1	0.5	1.5	V
r_{DS} (ON)	Drain-To-Source On Resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 0.1mA$		30	60		65	100	Ω
Small Signal Characteristics									
gfs	Forward Transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, f = 1kHz							
		$I_D = 50mA$	24	27					mmhos
		$I_D = 18mA$				13	15		mmhos
gfs (CONV)	Conversion Transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, f = 1kHz, E_{LO} (RMS) = 750mV		10					mmhos
Capacitances		f = 1MHz, Gate 2 AC Grounded							
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$							
		$I_D = 50mA$		4.0	5.0				pF
		$I_D = 18mA$					3.3	3.6	pF
		$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	5.0				pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		1.3	1.7		1.0	1.3	pF
C_{G1D}	Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03			0.03		pF
Input Admittance		f = 200MHz, $V_{DS} = +15V$		$V_{G1S} = V_{G2S}$, $I_D = 8mA$			$V_{G2S} = +10V$, $I_D = 18mA$		mmhos
	Re (y_{11})			1.05			1.11		
	Im (y_{11})			6.66			4.76		
Output Admittance									
	Re (y_{22})			0.73			1.05		
	Im (y_{22})			2.09			1.54		

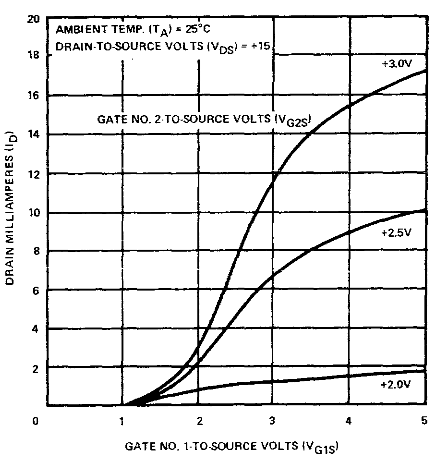
ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$

PARAMETER	TEST CONDITIONS	SD305			SD306			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Forward Transmittance Re (y_{21}) Im (y_{21})			4.69 -3.01			13.23 -5.62		
Reverse Transmittance Re (y_{12}) Im (y_{12})			0.04 -0.03			0.01 -0.04		mmhos
G_{PS} Power Gain[2]	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 200MHz				17	20		dB
$G_{PS\ (CONV)}$ Conversion Power Gain[1]	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{rf} = 200MHz$, $f_{LO} = 245MHz$	14	17					dB
NF Noise Figure	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 200MHz					1.5	2.5	dB
AGC_{VG2S} Range Of Automatic Gain Control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V \rightarrow 0V$, f = 200MHz					50		dB
E_{INT} Interfering Signal Level At Gate 1 For 1% Cross Modulation Distortion, Peak Voltage Referenced To 50Ω System[3]	$V_{DS} = +15V$, $V_{G2S} = +8V$, $I_D = 15mA$, Wanted signal f = 200MHz Interfering signal f = 196MHz					480		mV

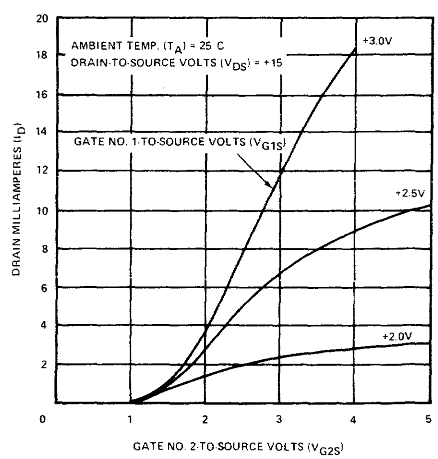
NOTES:
1. Measured in mixer test fixture.
2. Measured in amplifier test fixture.
3. Measured as shown in block diagram.

SD305 CHARACTERISTIC CURVES

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE

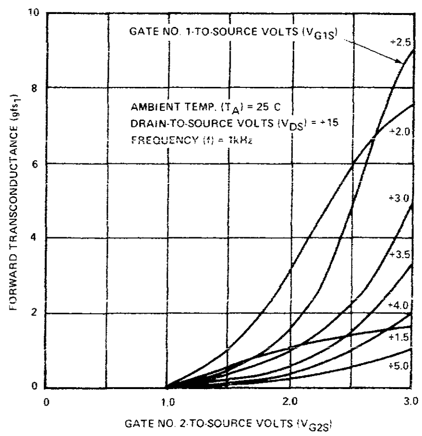


DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE

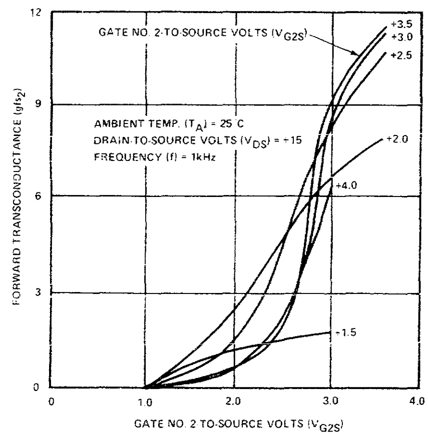


SD305 CHARACTERISTIC CURVES (Continued)

GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE



GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE

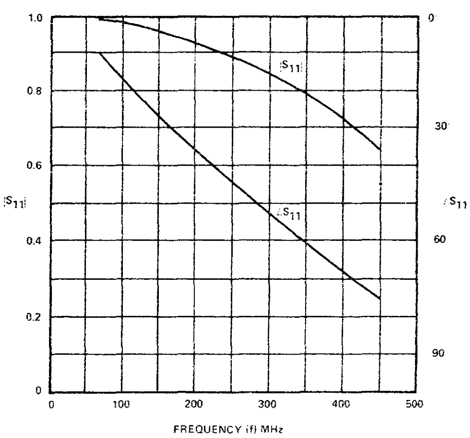


S PARAMETERS

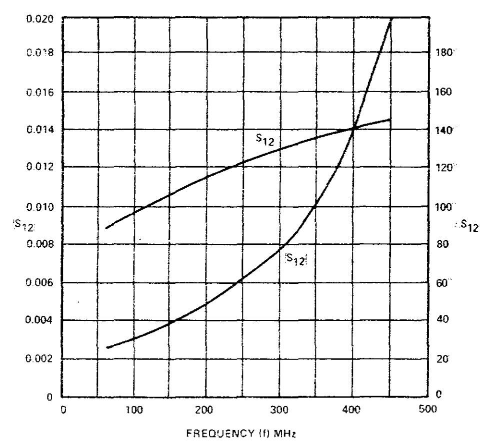
AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

DRAIN MILLIAMPERES (I_D) = 8
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

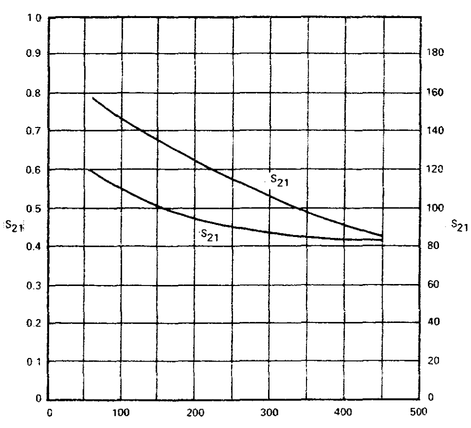
S_{11}



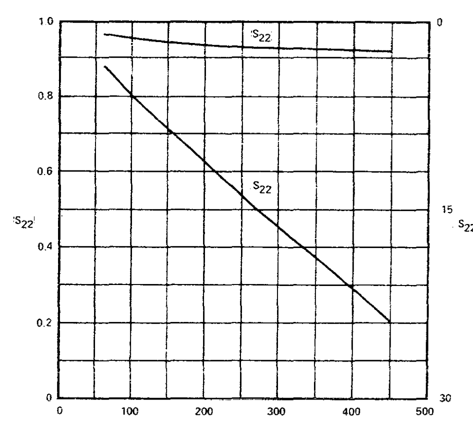
S_{12}



S_{21}

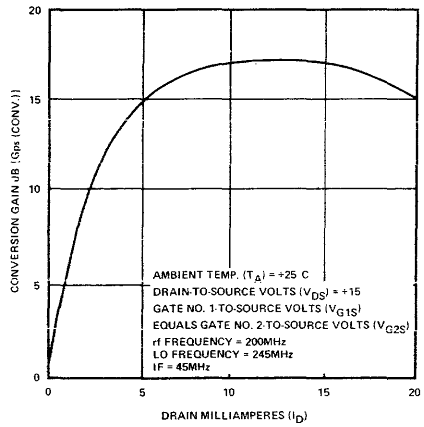


S_{22}

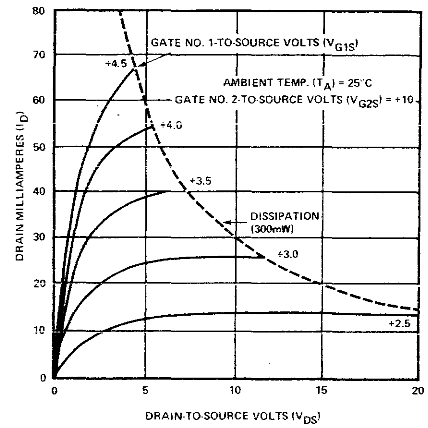


SD305 CHARACTERISTIC CURVES (Continued)

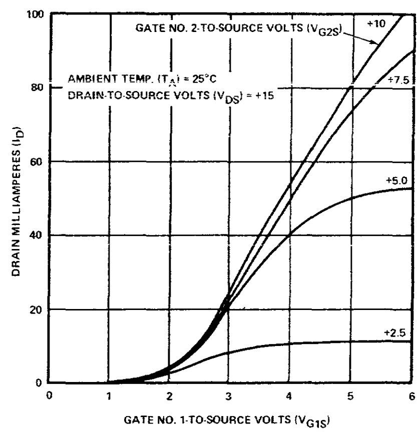
CONVERSION GAIN VS DRAIN CURRENT



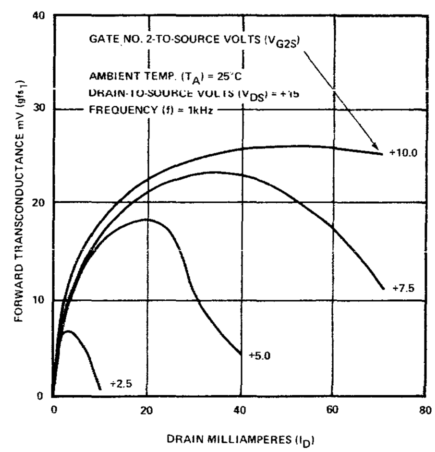
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



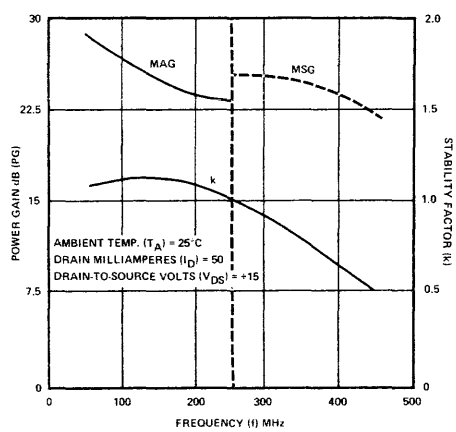
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



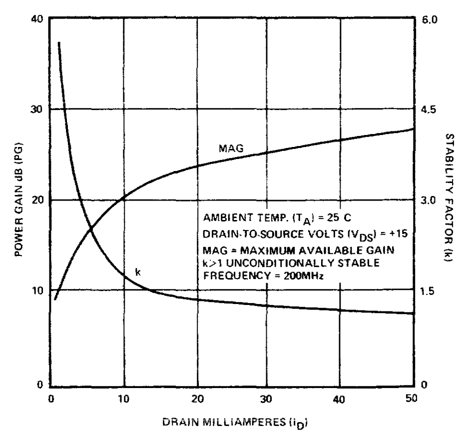
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



POWER GAIN VS FREQUENCY

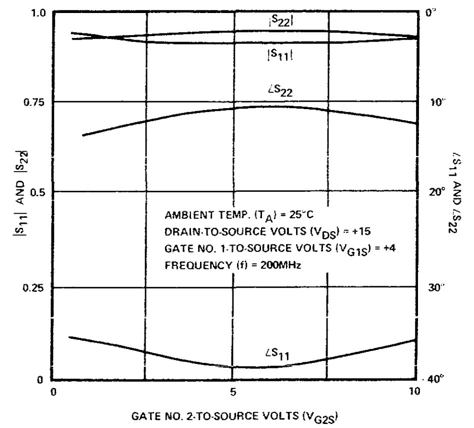


POWER GAIN VS DRAIN CURRENT

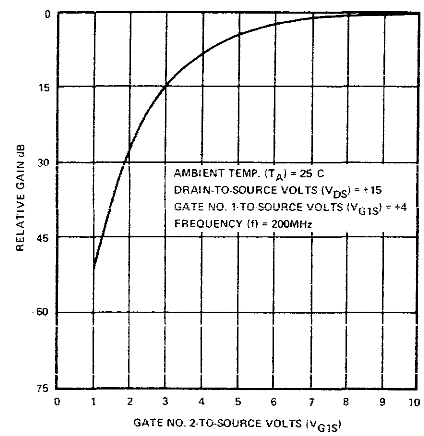


SD305 CHARACTERISTIC CURVES (Continued)

AUTOMATIC GAIN CONTROL VS S_{11} AND S_{22}



AUTOMATIC GAIN CONTROL RANGE

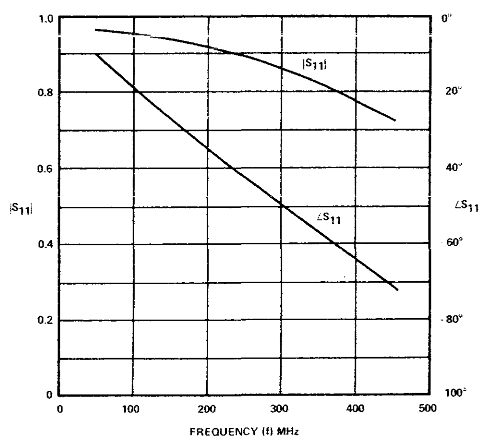


S PARAMETERS

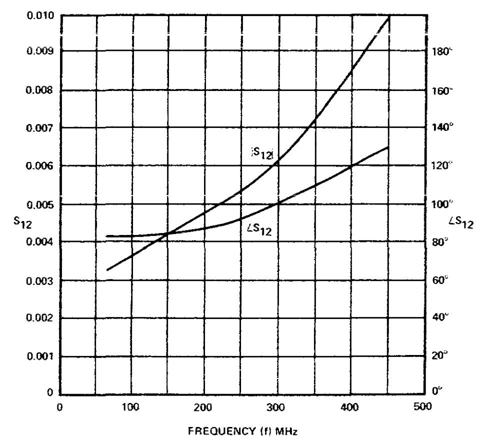
AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15

DRAIN MILLIAMPERES (I_D) = 50
GATE NO. 1-TO-SOURCE VOLTS = GATE NO. 2-TO-SOURCE VOLTS

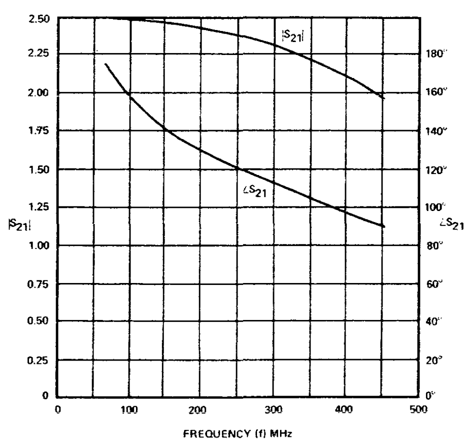
S_{11}



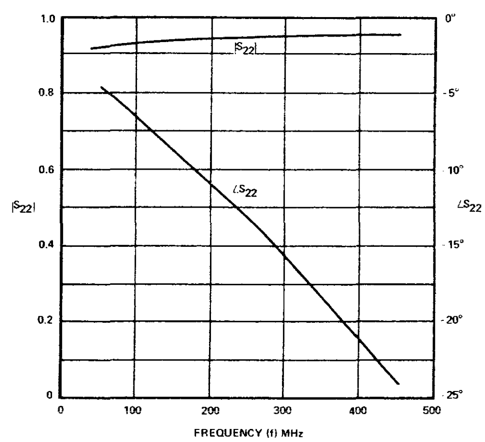
S_{12}



S_{21}

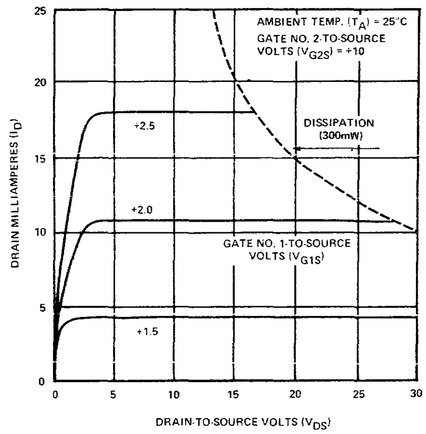


S_{22}

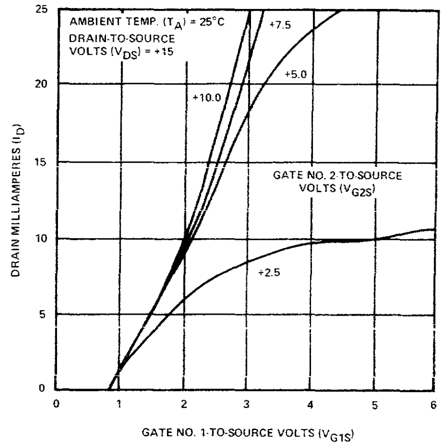


SD306 CHARACTERISTIC CURVES

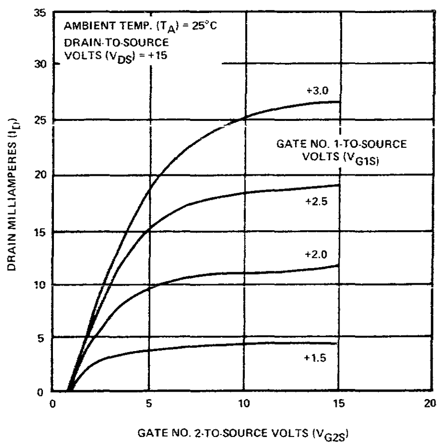
DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



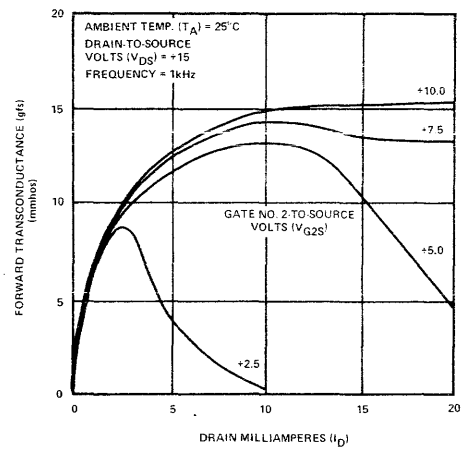
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



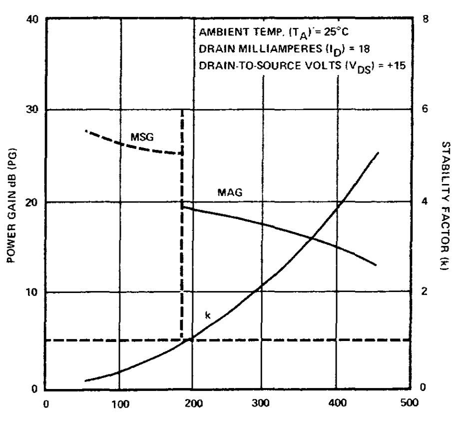
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



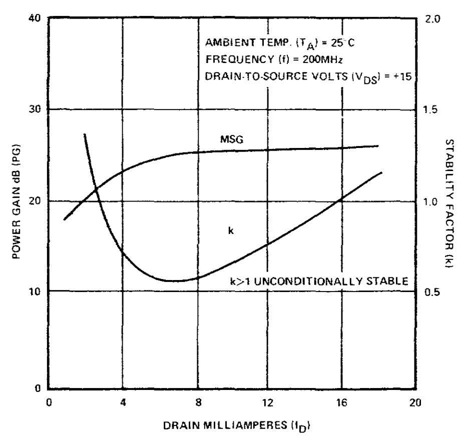
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



POWER GAIN VS FREQUENCY

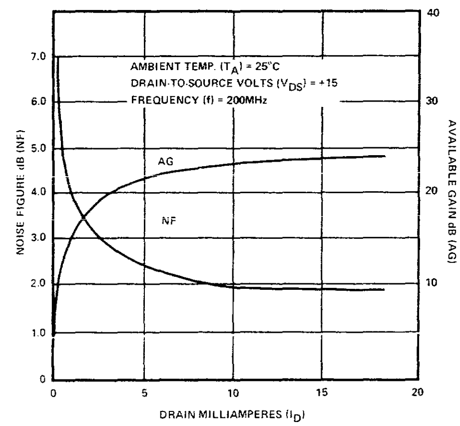


POWER GAIN VS DRAIN MILLIAMPERES

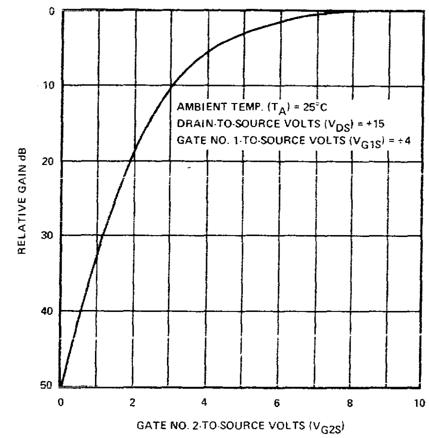


SD306 CHARACTERISTIC CURVES (Continued)

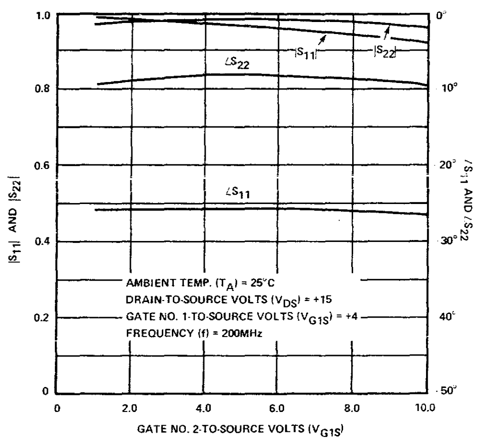
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



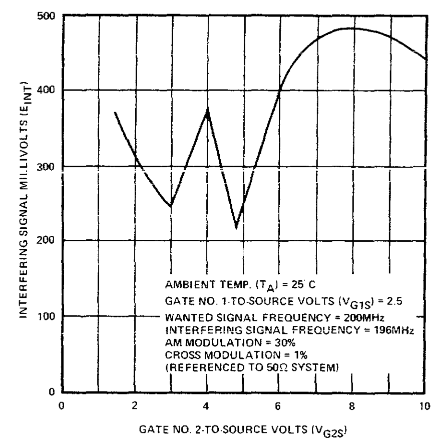
AUTOMATIC GAIN CONTROL RANGE AT 200MHz



S_{11} AND S_{22} VS AUTOMATIC GAIN CONTROL



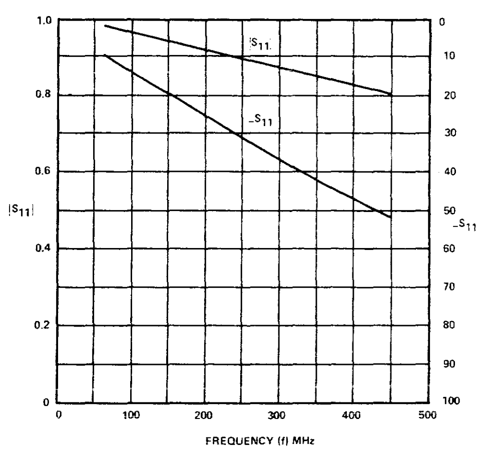
INTERFERING SIGNAL LEVEL VS GATE NO. 2-TO-SOURCE VOLTS



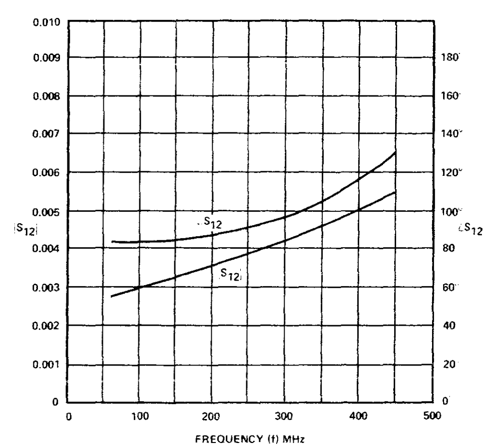
S PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN MILLIAMPERES (I_D) = 18
DRAIN-TO-SOURCE VOLTS (V_{DS}) = 15

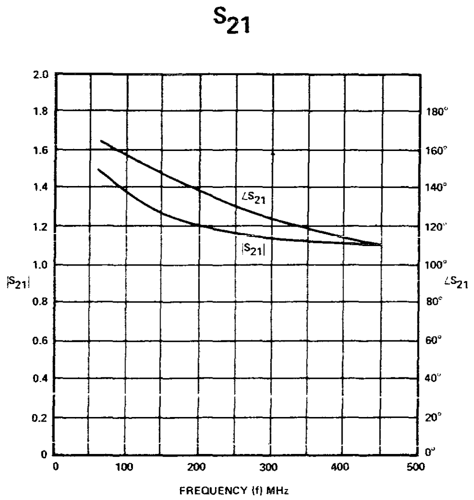
S_{11}

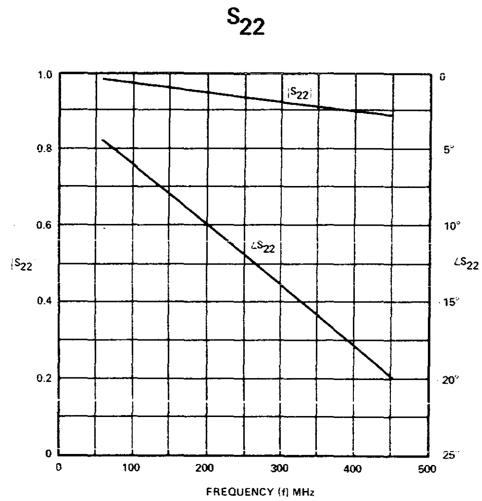


S_{12}

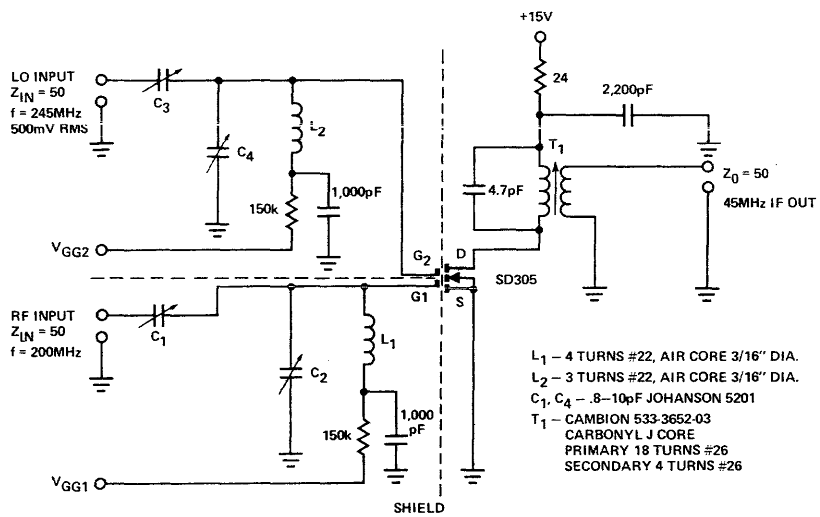


SD306 CHARACTERISTIC CURVES (Continued)

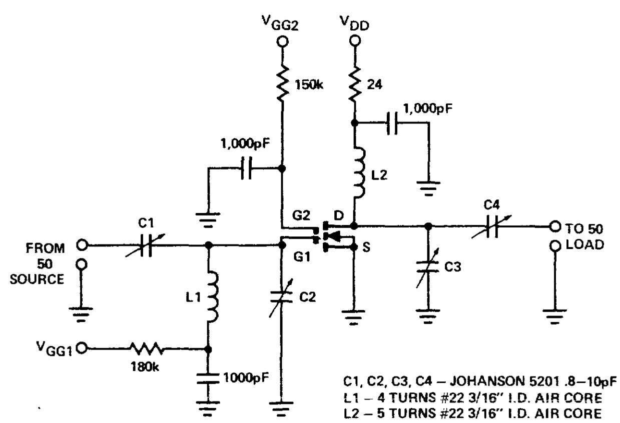




TEST CIRCUITS



SD305 200MHz/45MHz MIXER TEST CIRCUIT

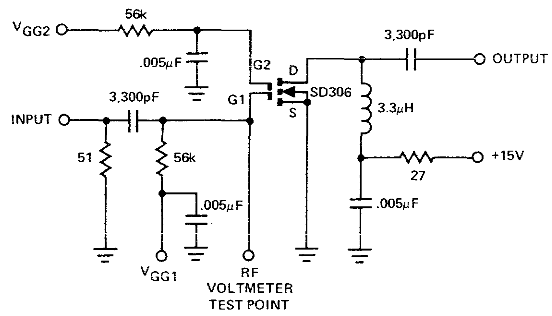


SD306 200MHz TEST AMPLIFIER; POWER GAIN, NOISE FIGURE

SD306
TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

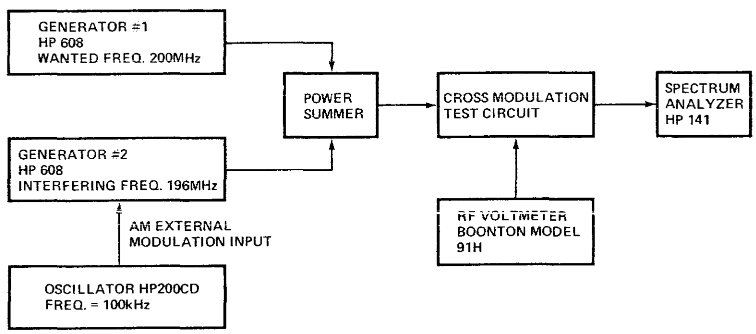
1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately −15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turn off the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

TEST CIRCUIT



SD306 CROSS MODULATION TEST CIRCUIT

BLOCK DIAGRAM OF CROSS MODULATION TEST



NOTES

D-MOS FET QUAD ANALOG SWITCH ARRAYS, MULTIPLEXERS AND DRIVER

ANALOG SWITCHING AND DRIVER APPLICATIONS

SD5000
SD5001
SD5100
SD5101
SD5200

DESCRIPTION

The Signetics D-MOS SD5000, 5100 and 5200 series are monolithic arrays of silicon, insulated-gate, field-effect transistors using the N-channel enhancement mode technology.

This family of devices is designed to handle a wide variety of analog switching and driver applications. They are capable of high speed operation where excellent transient response, and wide voltage range are required. The SD5000 quad switch array and the SD5100 quad multiplexer can handle high voltage analog signals (±10V), whereas the SD5001 and SD5101 are designed for lower voltage applications. The SD5200 is intended for use as a 30V driver to complement the other switch products.

FEATURES

- LOW INPUT CAPACITANCE – 2.4pF
- LOW FEEDBACK CAPACITANCE – 0.3pF
- LOW OUTPUT CAPACITANCE – 1.3pF
- ±10V ANALOG SIGNAL RANGE
- LOW PROPAGATION DELAY TIME – 600ps
- LOW ON RESISTANCE – 30Ω
- LOW FEEDTHROUGH AND FEEDBACK TRANSIENTS
- ION IMPLANTED FOR GREATER RELIABILITY
- HIGH CHANNEL-TO-CHANNEL ISOLATION – 107dB
- TRANSIENT PROTECTION FOR GATES

SD5000 APPLICATIONS

ANALOG SWITCHING (UP TO VERY HIGH FREQUENCIES)

AUDIO ROUTING

CHOPPERS

CROSSPOINT SWITCHES

SAMPLE AND HOLD

SD5100 APPLICATIONS

MULTIPLEXING

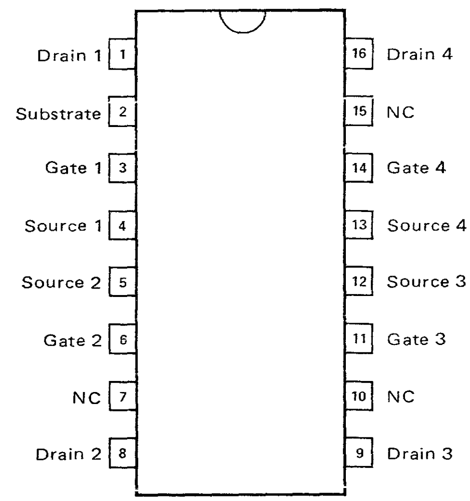
CURRENT SUMMING

SD5200 APPLICATIONS

SWITCH DRIVERS

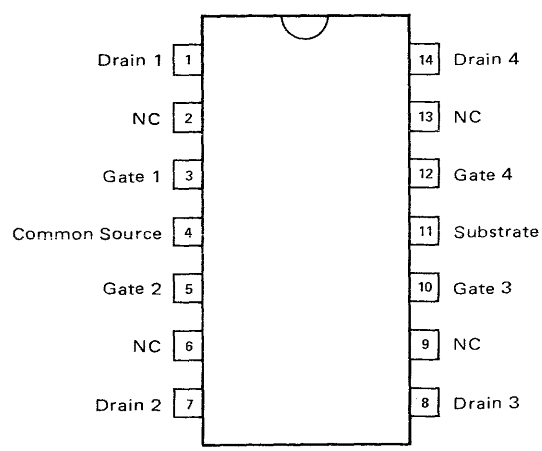
PIN CONFIGURATION (Top View)

B PACKAGE



ORDER PART NOS. SD5000B, SD5001B, SD5200B

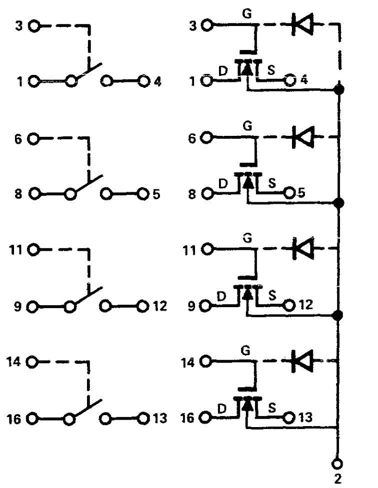
A PACKAGE



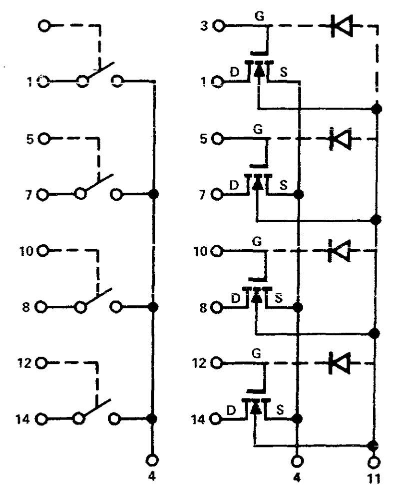
ORDER PART NOS. SD5100A, SD5101A

FUNCTIONAL AND SCHEMATIC DIAGRAMS

SD5000, 5001, 5200



SD5100, 5101



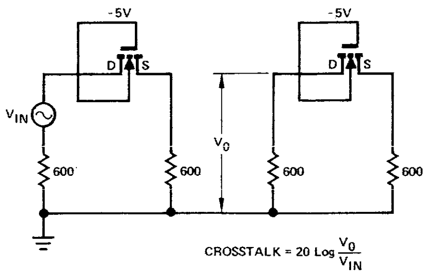
ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ (Unless Otherwise Noted)

PARAMETER		SD5000	SD5001	SD5100	SD5101	SD5200	UNITS
V_{DS}	Drain-To-Source	+20	+10	+30	+15	+30	Vdc
V_{SD}	Source-To-Drain	+20	+10	+.5	+.5	+.5	Vdc
V_{DB}	Drain-To-Substrate	+25	+15	+30	+15	+30	Vdc
V_{SB}	Source-To-Substrate	+25	+15	+.5	+.5	+.5	Vdc
V_{GS}	Gate-To-Source	+25 −25	+20 −15	+20	+20	+20	Vdc
V_{GB}	Gate-To-Substrate	+30 −0.3	+25 −0.3	+20 −0.3	+20 −0.3	+20 −0.3	Vdc
V_{GD}	Gate-To-Drain	+25 −25	+20 −15	+20	+20	+20	Vdc
I_D	Drain Current	50	50	50	50	50	mA
Ambient Temperature Range							
	Storage Operating	−55 to +150 0 to +85					°C °C
Power Dissipation							
	Total Package Dissipation* Individual Transistor Dissipation*	640 300					mW mW

*Derated 5mW per degree centigrade.

CROSSTALK MEASUREMENT

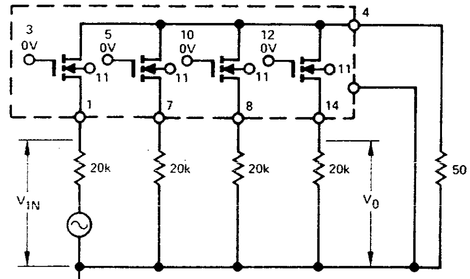
QUAD SWITCH
(SD5000/SD5001)



CROSSTALK = 20 Log $\frac{V_0}{V_{IN}}$
WHERE V_{IN} = 1V RMS AT 3kHz

TEST CIRCUIT NO. 1

MULTIPLEXER
(SD5100/SD5101)



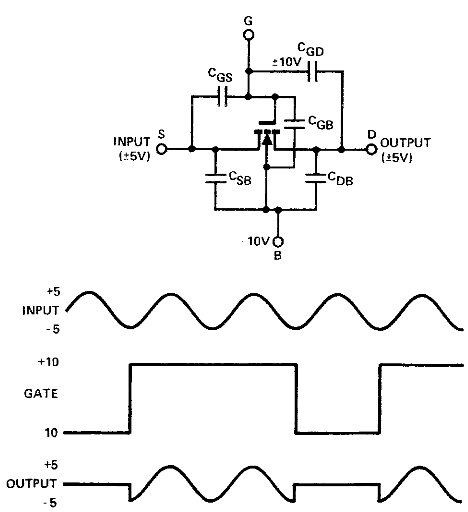
CT = 20 Log $\frac{V_0}{V_{IN}}$
WHERE V_{IN} = 1V RMS AT 3kHz

TEST CIRCUIT NO. 2

THEORY OF OPERATION

The SD5000 series consists of four SPST switches with analog signal capability of up to ±10 volts for the SD5000 and up to ±5 volts for the SD5001. Each switch of the array is a D-MOS N-channel field-effect transistor of the enhancement-mode type; that is, the device is normally off when gate-to-source voltage (V_{GS}) is zero volts. When V_{GS} exceeds the threshold voltage V_T the FET switch starts to turn on. With V_{GS} in excess of +10 volts, a low resistance path (typically 30Ω) exists between input and output of the switch. Figure 1 below shows the normal mode of operation of a single switch of the array for ±5 volt analog signal processing. Note that the source is recommended for the input since feedback or reverse transfer capacitance is lower when drain is used as the output. In this case, the switch is driven by ±10 volts for which the SD5200 could be used as discussed later.

FIGURE 1



When analog signals are routed from one point to another the important factors are **isolation, cross-talk** between switches, **feedthrough** and **feedback transients, insertion loss** and **speed** of operation. The SD5000 series offers superior performance in all these areas.

Isolation. ON resistance is typically 30Ω and OFF resistance is typically 10^{10}Ω, which means the OFF to ON resistance ratio is in excess of 10^9. Isolation from output to input from 3kHz analog signals is −107dB.

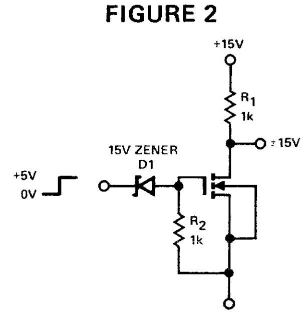
Feedback and feedthrough transients. These are kept to a minimum because of the very low feedback and feedthrough capacitances. This means that "glitchless" or "clean" signals appear at the output.

Insertion loss. This depends upon the source and load impedances involved. As an example for 600Ω source impedance the insertion loss for voice signals (1V RMS at 3kHz) is less than 0.3dB. This indicates that the SD5000 series would make good telephone cross-point switches.

Speed. Because of the low ON resistance and low input capacitance the SD5000 switches turn on at sub-nanosecond speeds. They are also capable of handling very high frequency analog signals and still maintain excellent isolation (20-30dB at 1GHz).

The SD5200 is intended as a driver for the SD5000/5001 but is capable of driving any system which requires ±15 volts. Four drivers are in each package and Figure 2 shows how a single driver is biased for ±15 volts. Two external resistors R_1, R_2 and a zener diode D_1 are required per driver. The input is 5V open collector TTL.

FIGURE 2



The SD5100 series is four channel multiplexers. The SD5100 has 0-30 volts input voltage capability and the SD5101 has 0-15 volts input voltage capability. Each circuit has a common source. The signals at the source are limited to ±200mV and therefore these circuits are used where switching is performed at the virtual ground point of an op amp. In this case, no external driver is required nor are any additional power supplies required. Because the ON resistance of both the SD5000 and SD5001 is very low (30Ω typ) and matched within 5Ω, the need for a compensating FET is minimized and in some cases eliminated. The parts can be driven directly from TTL, either +5 volts or +15 volts open collector.

ANALOG SWITCH/DRIVER APPLICATION

The SD5200 operates as an inverting switch capable of driving 30 volts maximum. This wide range capability with high speed fulfills most analog switching applications. Figure 3 demonstrates how the SD5200 drives the SD5000 in a typical analog switching application.

ANALOG MULTIPLEXER APPLICATION

The SD5100 series is easy to use as shown in Figure 4. Drive circuitry can be TTL or if very low R_{ON} is required (19Ω typ), then TTL open collector logic can drive the SD5100 up to +20 volts. The common source is kept at or near ground and each drain will withstand +30 volts with isolation typically 120dB.

If a compensation transistor is required in series with R_2, then the maximum mismatch error for $R_1 = R_2 = 10k\Omega$ would be:

FIGURE 3

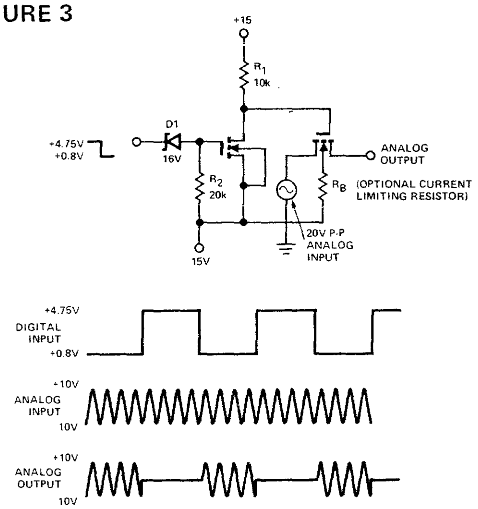
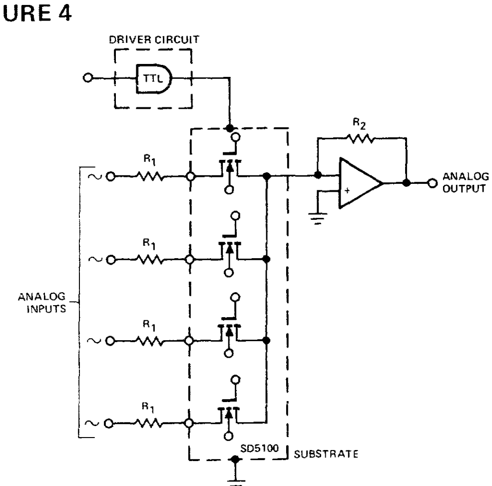


FIGURE 4



ELECTRICAL CHARACTERISTICS $T_A = +25°C$

PARAMETER	
Breakdown Voltage	
BV_{DS}	Drain-To-Source
BV_{SD}	Source-To-Drain
BV_{DB}	Drain-To-Substrate
BV_{SB}	Source-To-Substrate
Leakage Current	
I_{DS} (OFF)	Drain-To-Source
I_{SD} (OFF)	Source-To-Drain
I_{GBS}	Gate
I_{GB}	Gate-To-Substrate
V_T	Threshold Voltage
gfs	Forward Transconductance
Small Signal Capacitances	
$C_{(GS + GD + GB)}$	Gate Node
$C_{(GD + DB)}$	Drain Node
$C_{(GS + SB)}$	Source Node
C_{DG}	Reverse Transfer
C_T	Cross Talk
r_{DS} (ON)	Drain-To-Source Resistance
r_{DSM} (ON)	Resistance Match

TEST CONDITIONS	SD5000			SD5001			SD5100			SD5101			SD5200			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	20	25		10	25											V
$V_{GS} = V_{BS} = 0V$, $I_S = 1\mu A$							30	35		15	30					V
$V_{GS} = V_{BS} = 0V$, $I_S = 10\mu A$													30	35		V
$V_{GD} = V_{BD} = -5V$, $I_D = 10nA$	20			10												V
$V_{GD} = V_{BD} = 0V$, $I_D = 10nA$							.5			.5						V
$V_{GB} = 0V$, Source OPEN																
$I_D = 10nA$	25			15												V
$I_D = 1\mu A$							30			15						V
$V_{GB} = 0V$, Drain OPEN																
$I_S = 10\mu A$	25			15												V
$I_S = 100nA$							.5			.5						V
$V_{GS} = V_{BS} = -5V$																
$V_{DS} = +20V$		1	10													nA
$V_{DS} = +10V$					1	10										nA
$V_{GS} = V_{BS} = 0V$, $V_{DS} = +10V$								1	10		1	10				nA
$V_{GD} = V_{BD} = -5V$																
$V_{SD} = +20V$		1	10													nA
$V_{SD} = +10V$					1	10										nA
$V_{DB} = V_{SB} = 0V$																
$V_{GB} = 25V$			10													μA
$V_{GB} = 20V$						10			10			10			10	μA
Drain and Source OPEN																
$V_{GB} = +30V$			1													μA
$V_{GB} = +25V$						1										μA
$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$, $V_{SB} = 0V$	0.1	1.0	2.0	0.1	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0	0.5	1.0	2.0	V
$V_{DS} = 10V$, $V_{SB} = 0V$, $I_D = 20mA$, $f = 1kHz$	10	15		10	15		10	15		10	15		10	15		mmhos
$V_{DS} = 10V$, $f = 1MHz$, $V_{GS} = V_{BS} = -15V$																
See Capacitance Model in Figure 1		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5		2.4	3.5	pF
		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5		1.3	1.5	pF
		3.5	4.0		3.5	4.0										pF
		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5		0.3	0.5	pF
See Test Circuits No. 1 & 2, $f = 3kHz$								-107								dB
$I_D = 0.1mA$, $V_{SB} = 0$																
$V_{GS} = +5V$								50	70							Ω
$V_{GS} = +10V$								30	45							Ω
$V_{GS} = +15V$								23								Ω
$V_{GS} = +20V$								19								Ω
$i_D = 0.1mA$, $V_{SB} = 0$, $V_{GS} = +5V$								1	5					—		Ω

$$\text{error} = \frac{R_2 + 65\Omega}{R_1 + 70\Omega} = .05\%$$

Without the compensation transistor the error would be:

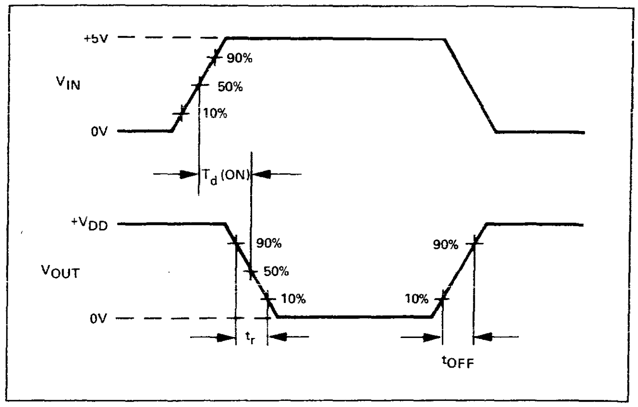
$$\text{error} = \frac{R_2}{R_1 + 70\Omega} = .7\%$$

SWITCHING CHARACTERISTICS

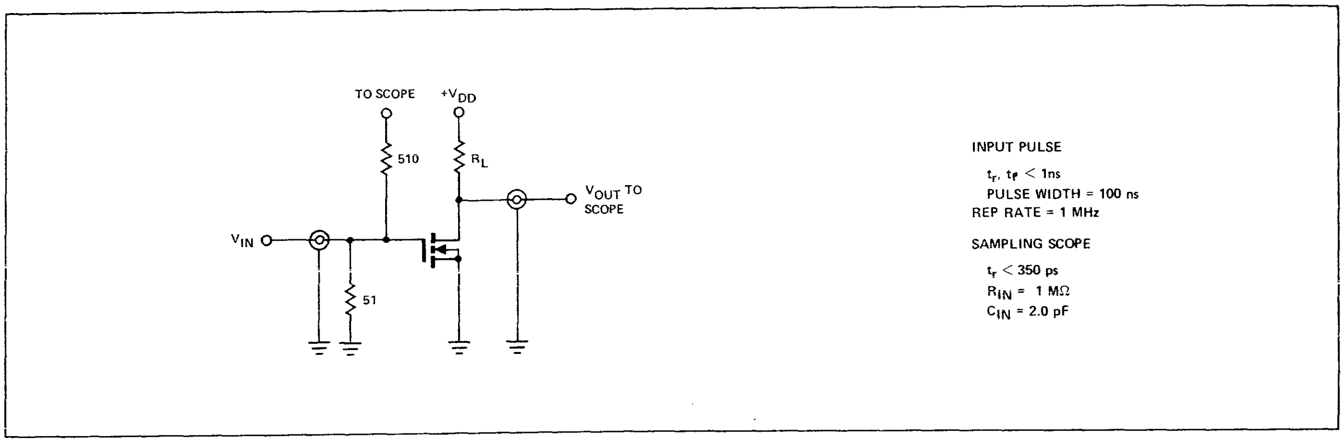
		t_d (ON) (ns)		t_r (ns)		t_{OFF} (ns)	
V_{DD}	R_L	TYP	MAX	TYP	MAX	TYP	MAX
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	
15	1k	0.9		1.0		14.0	

* t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

SWITCHING WAVEFORMS

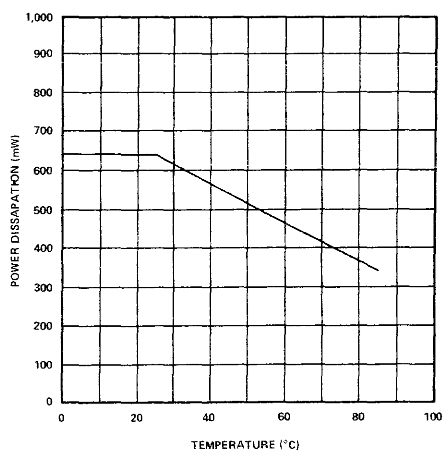


TEST CIRCUIT

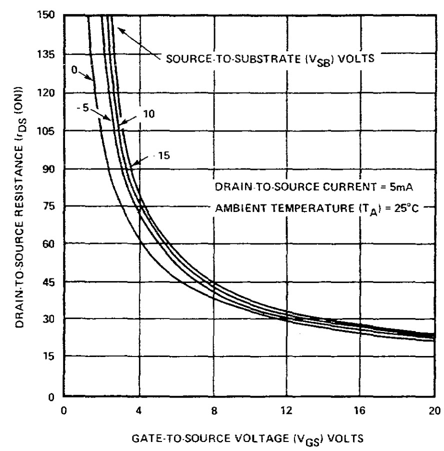


CHARACTERISTIC CURVES

MAXIMUM POWER DISSIPATION VS TEMPERATURE

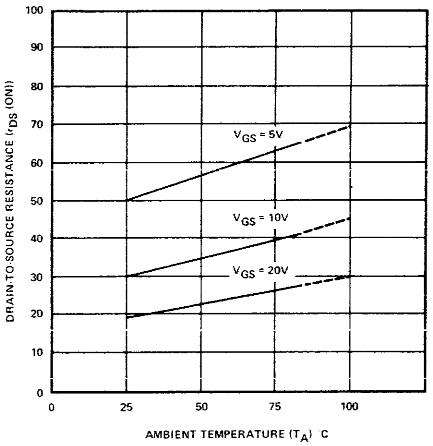


DRAIN-TO-SOURCE RESISTANCE VS SOURCE-TO-SUBSTRATE AND GATE-TO-SOURCE VOLTAGE

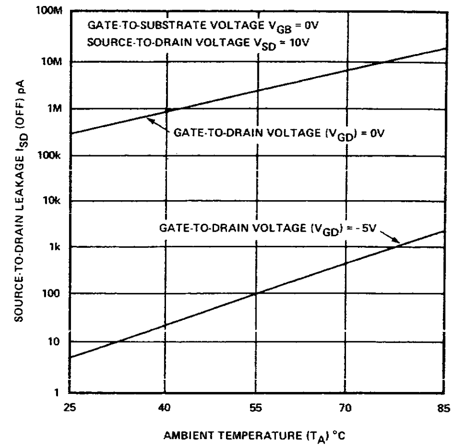


CHARACTERISTIC CURVES (Continued)

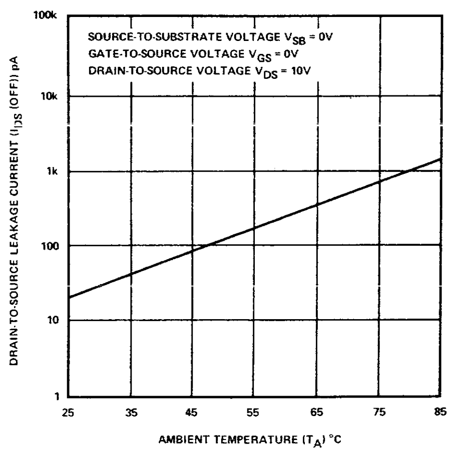
DRAIN-TO-SOURCE RESISTANCE VS TEMPERATURE



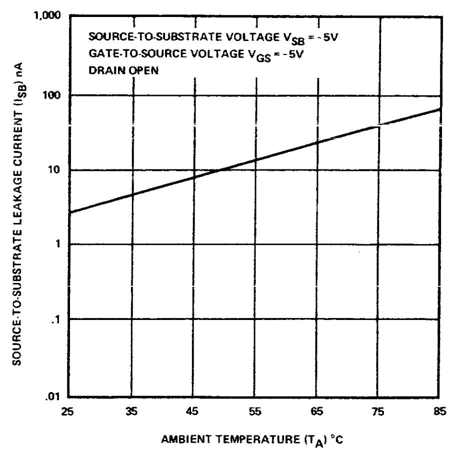
SOURCE-TO-DRAIN LEAKAGE CURRENT VS TEMPERATURE



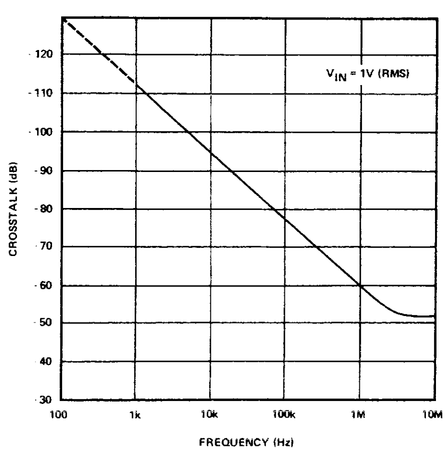
DRAIN-TO-SOURCE LEAKAGE CURRENT VS TEMPERATURE



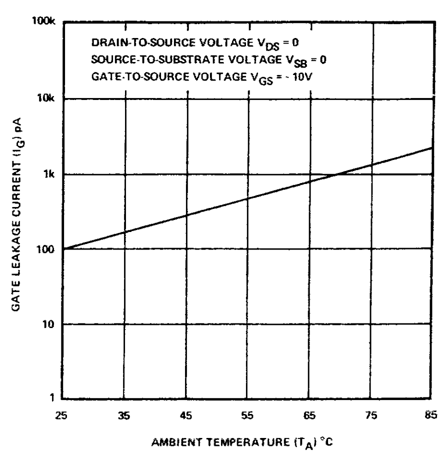
SOURCE-TO-SUBSTRATE LEAKAGE CURRENT VS TEMPERATURE



CROSSTALK VS FREQUENCY



GATE LEAKAGE CURRENT VS TEMPERATURE



signetics

D-MOS DUAL-GATE FETs N-CHANNEL ENHANCEMENT | SD6000

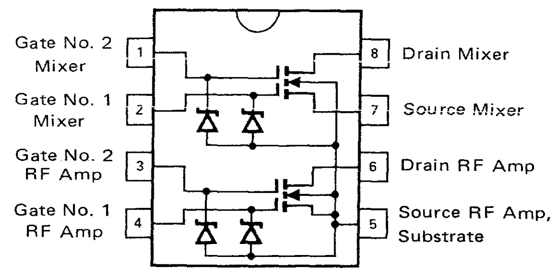
FM AND VHF FRONT-END APPLICATIONS

DESCRIPTION

The Signetics D-MOS SD6000 is an integrated circuit fabricated by the double-diffused process and employing silicon N-channel enhancement mode MOSFETs with dual gates. Zener diodes are connected between all gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3V to +20.0V. Thus, the gates are protected against damage in all normal handling and operating situations. The use of the dual gate structure plus the incorporation of the drift region has made the feedback capacity (C_{G1D}) typically less than 0.03pF. The attributes of the IC make it ideally suited for FM/VHF RF amplifier and mixer applications. The IC is specifically characterized for incorporation into varactor or conventional FM tuners but the performance guaranteed makes it useful in a wide variety of VHF tuner applications. The power gain at 100MHz is 30dB minimum with a guaranteed noise figure of 3.0dB. A wide AGC capability plus significant reduction in cross modulation is now available because of the inherent linearity of the D-MOS FETs. The SD6000 is packaged in the Signetics 8-pin plastic V package.

PIN CONFIGURATION (Top View)

V PACKAGE



ORDER PART NO. SD6000V

GENERAL FEATURES

- POSITIVE BIAS ONLY
- LOW GATE VOLTAGES
- ENHANCEMENT MODE OPERATION
- ZENER DIODE GATE PROTECTION
- ION IMPLANTED FOR GREATER RELIABILITY

FEATURES (RF AMP Section)

- HIGH POWER GAIN WITHOUT NEUTRALIZATION – 25dB AT 100MHz
- LOW NOISE FIGURE – 2.5dB AT 100MHz
- LOW INPUT AND OUTPUT CAPACITANCES CONSTANT WITH AGC – 3.0pF AND 1.0pF
- LOW FEEDBACK CAPACITANCE – 0.025pF
- SUPERIOR CROSS MODULATION PERFORMANCE
- HIGH TRANSCONDUCTANCE – 15mmhos
- WIDE AGC RANGE – 50dB AT 100MHz

FEATURES (Mixer Section)

- HIGH CONVERSION GAIN – 17dB AT 100MHz WITH V_{G1S} = V_{G2S} FOR BIASING SIMPLICITY
- EXCELLENT ISOLATION FROM GATE NO. 1 (RF) TO GATE NO. 2 (LO)
- LOW INPUT CAPACITANCE – 4.0pF
- LOW FEEDBACK CAPACITANCE – 0.03pF
- EXCELLENT CROSS MODULATION PERFORMANCE AND LOW NOISE OPERATION
- HIGH CONVERSION TRANSCONDUCTANCE AT LOW DRAIN CURRENTS – 10mmhos

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C (Unless Otherwise Noted)

V_{DS}	Drain-To-Source Voltage	+20V
V_{G1B}	Gate No. 1-To-Substrate Voltage	−0.3 to +20Vdc
V_{G2B}	Gate No. 2-To-Substrate Voltage	−0.3 to +20Vdc
	Drain Current	50mA
T_A	Ambient Temperature Range	
	Storage	−65°C to +150°C
	Operating	−65°C to +125°C
P_T	Power Dissipation	
	At 25°C Case Temperature	625mW
	Temperature Above 25°C	Derate at 5.0mW/°C

ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
OFF Characteristics — RF Amp and Mixer						
BV_{DS}	Drain-To-Source Breakdown Voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	30		V
$I_{D(OFF)}$	Drain-To-Source Leakage Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
$I_{D\,SS}$	Zero Bias Drain Current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
I_{G1SS}	Gate No. 1 Leakage Current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1	μA
I_{G2SS}	Gate No. 2 Leakage Current	$V_{G2S} = +10V$, $V_{G1S} = V_{DS} = 0V$		0.001	0.1	μA

ON Characteristics			RF AMP			MIXER			
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{T1}	Gate 1 Threshold Voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	0.5	1.5	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold Voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	0.5	1.5	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-To-Source On Resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 0.1mA$		65	100		30	60	Ω

Small Signal Characteristics — RF Amp			MIN	TYP	MAX	
gfs	Forward Transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz	12	15		mmhos
Capacitances		f = 1MHz, Gate No. 2 AC Grounded				
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$		3.0	3.5	pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = 10V$		1.0	1.3	pF
C_{G1D}	Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = 10V$		0.025		pF
Input Admittance		f = 100MHz, $V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$				mmhos
Re (y_{11})				0.21		
Im (y_{11})				2.26		
Output Admittance						
Re (y_{22})				0.20		
Im (y_{22})				0.68		
Forward Transmittance						
Re (y_{21})				12.85		
Im (y_{21})				−1.50		
Reverse Transmittance						
Re (y_{12})				0.01		
Im (y_{12})				−0.03		
Gps	Power Gain*	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 100MHz	20	25		dB
NF	Noise Figure*	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 100MHz		2.5	3.0	dB
AGC(V_{G2S})	Range Of Automatic Gain Control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, f = 100MHz		50		dB

ELECTRICAL CHARACTERISTICS (Continued) $T_A = 25°C$

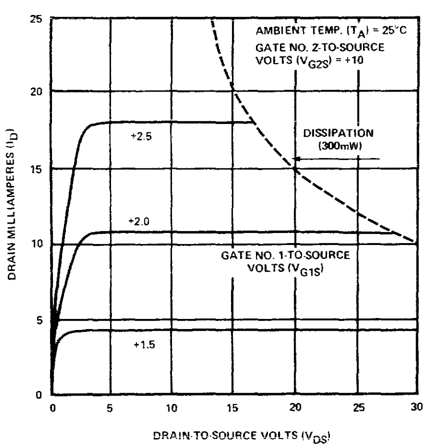
PARAMETER	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Small Signal Characteristics — MIXER					
$gfs_{(CONV)}$ Conversion Transconductance	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$ $I_D = 8mA$, f = 1kHz E_{LO} (RMS) = 750mV		10		mmhos
Capacitances	f = 1MHz, Gate No. 2 AC Grounded				
C_{GIS} Input	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$		4.0	4.75	pF
C_{DS} Output	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		1.1	1.5	pF
C_{G1D} Reverse Transfer	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.030		pF
Input Admittance	f = 100MHz, $V_{DS} = +15V$ $V_{G1S} = V_{G2S}$, $I_D = 8mA$				
Re (y_{11})			0.21		
Im (y_{11})			2.28		
Output Admittance					
Re (y_{22})			0.41		
Im (y_{22})			1.04		
Forward Transmittance					
Re (y_{21})			3.18		
Im (y_{21})			−0.83		
Reverse Transmittance					
Re (y_{12})			0.03		
Im (y_{12})			−0.01		
$Gps_{(CONV)}$ Conversion Power Gain**	$V_{DS} = +15V$, $V_{G1S} = V_{G2S}$, $I_D = 8mA$, $f_{RF} = 100MHz$, $f_{LO} = 89.3MHz$	14	19		dB

*Measured in Amplifier test fixture.
**Measured in MIXER test fixture.

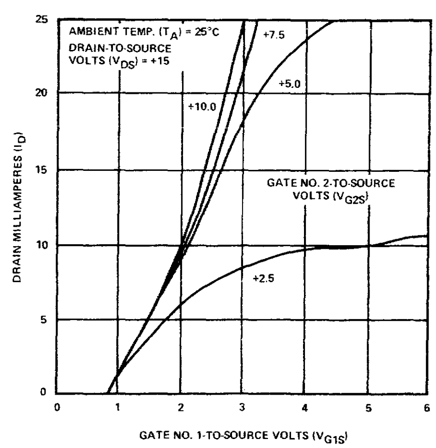
CHARACTERISTIC CURVES

RF AMP SECTION

DRAIN CURRENT VS DRAIN-TO-SOURCE VOLTAGE



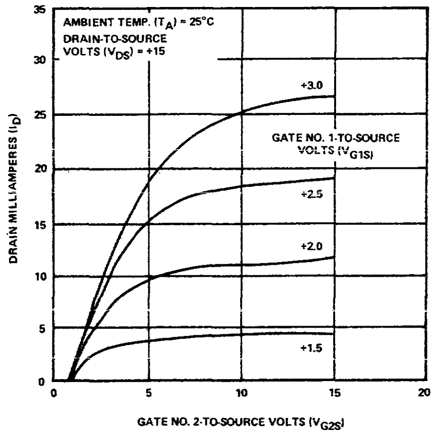
DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



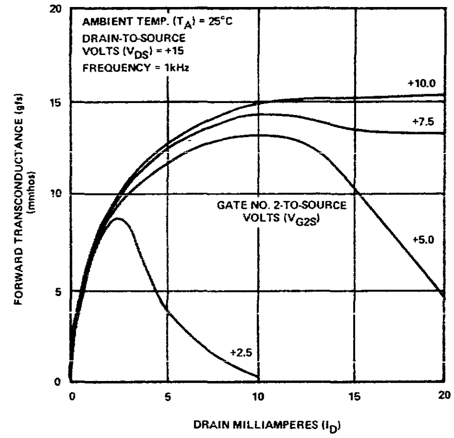
CHARACTERISTIC CURVES (Continued)

RF AMP SECTION

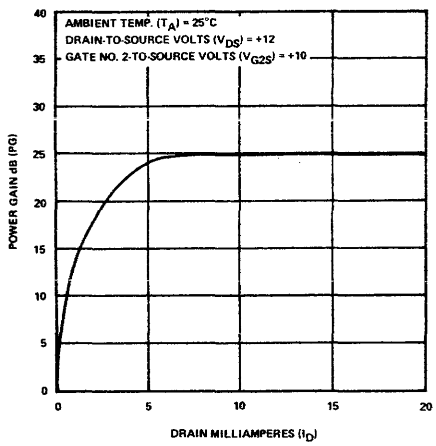
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



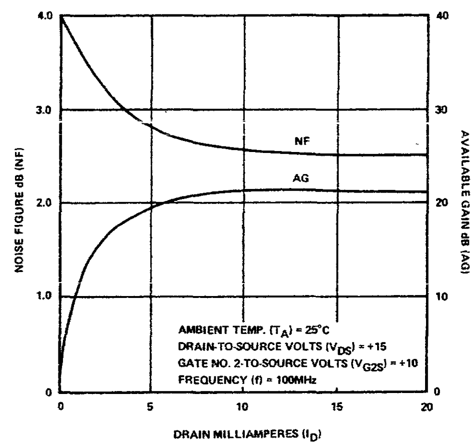
1kHz FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



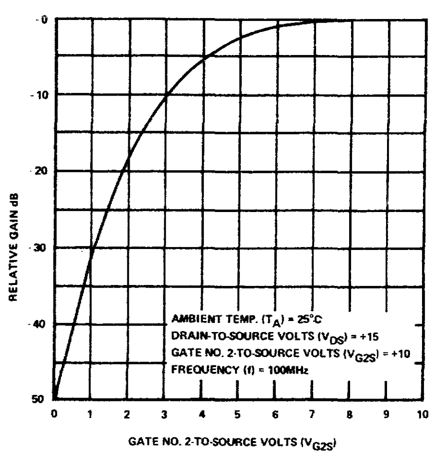
POWER GAIN VS DRAIN CURRENT



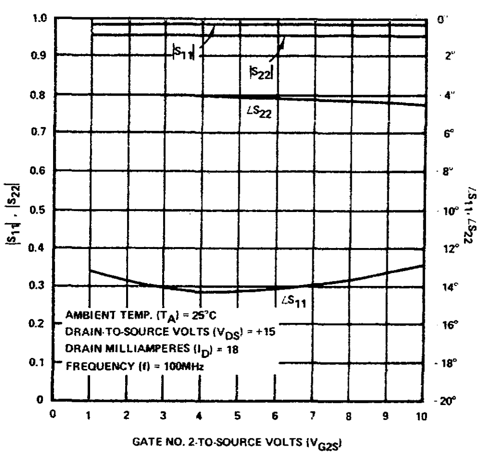
NOISE FIGURE AND AVAILABLE GAIN VS DRAIN CURRENT



AUTOMATIC GAIN CONTROL RANGE



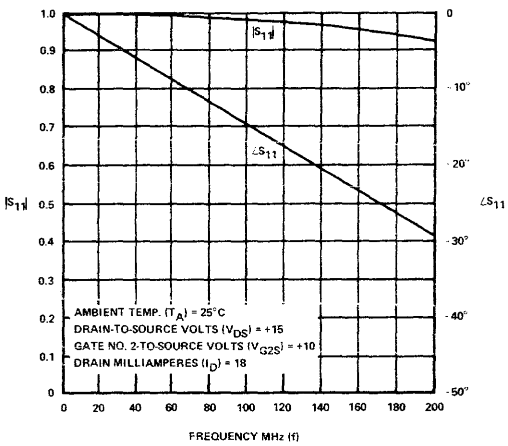
S_{11} AND S_{22} VS GATE NO. 2-TO-SOURCE VOLTAGE



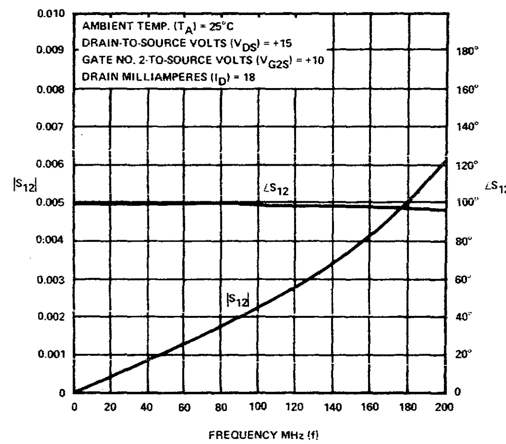
CHARACTERISTIC CURVES (Continued)

RF AMP SECTION

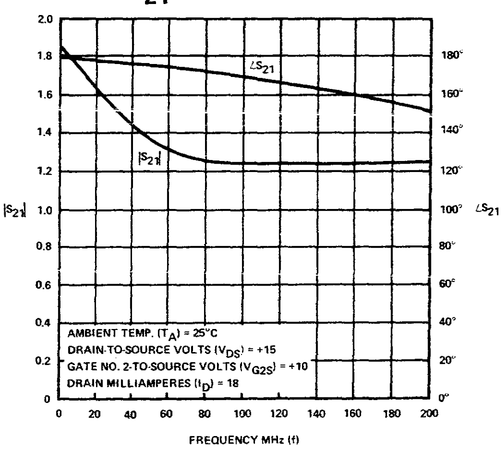
S_{11} VS FREQUENCY



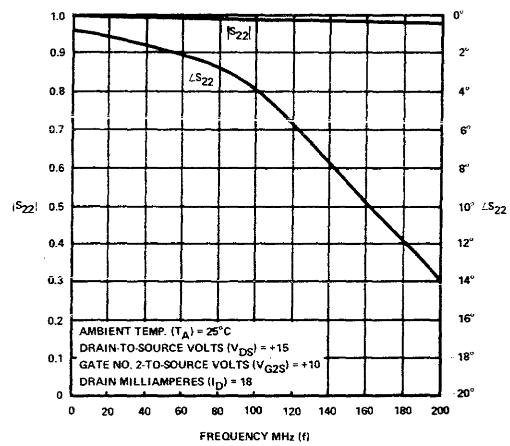
S_{12} VS FREQUENCY



S_{21} VS FREQUENCY

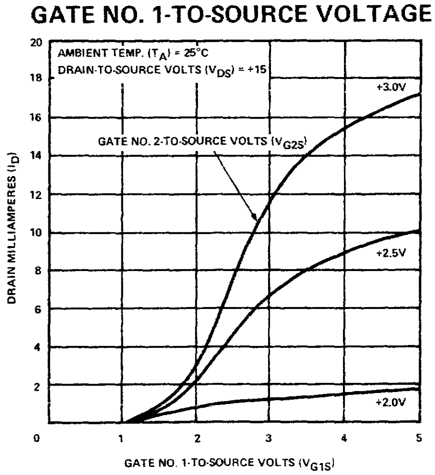


S_{22} VS FREQUENCY

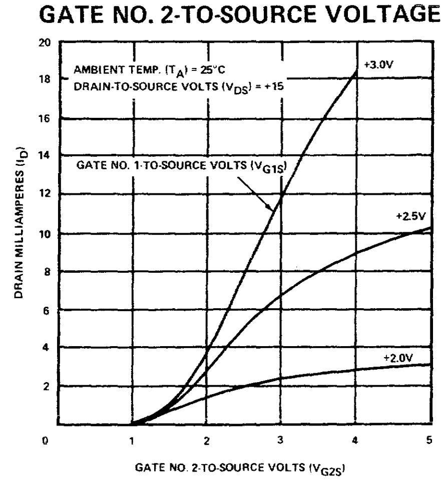


MIXER SECTION

DRAIN CURRENT VS GATE NO. 1-TO-SOURCE VOLTAGE



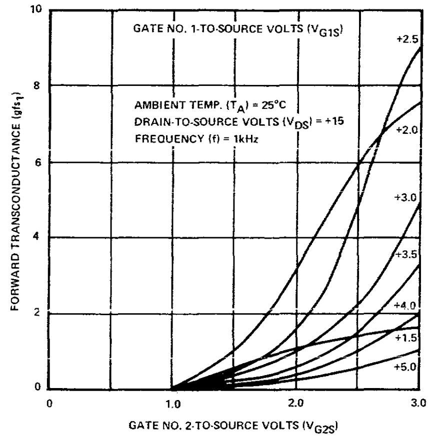
DRAIN CURRENT VS GATE NO. 2-TO-SOURCE VOLTAGE



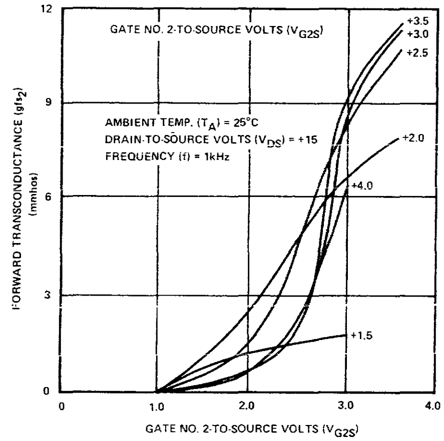
CHARACTERISTIC CURVES (Continued)

MIXER SECTION

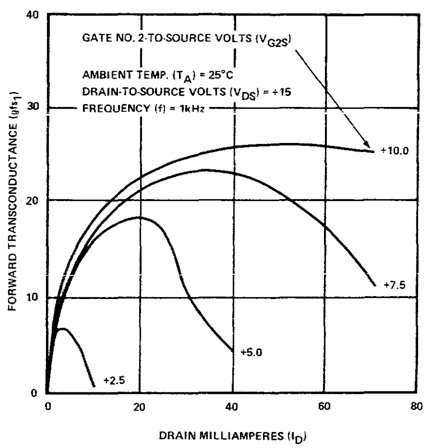
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS GATE NO. 2-TO-SOURCE VOLTAGE



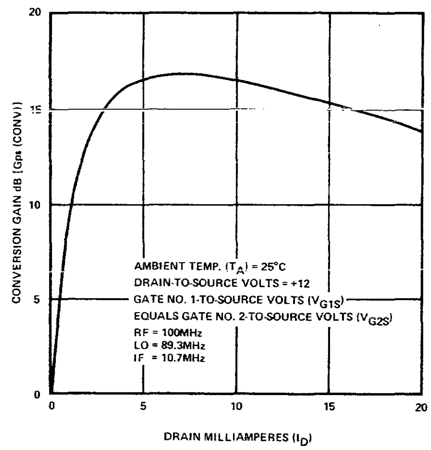
GATE NO. 2 FORWARD TRANSCONDUCTANCE VS GATE NO. 1-TO-SOURCE VOLTAGE



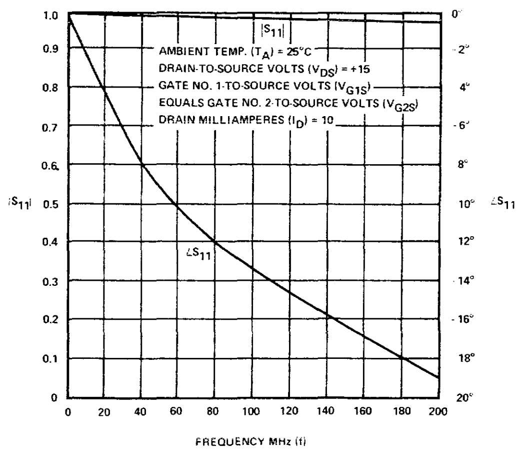
GATE NO. 1 FORWARD TRANSCONDUCTANCE VS DRAIN CURRENT



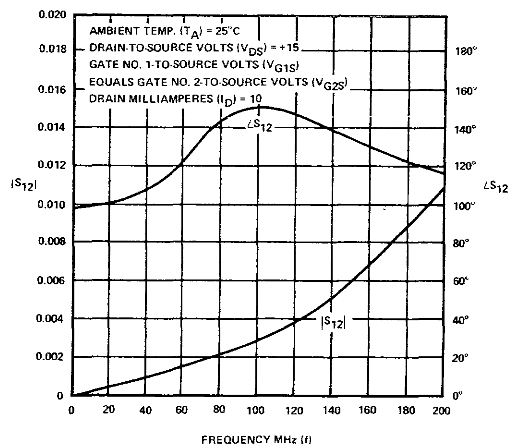
CONVERSION GAIN VS. DRAIN CURRENT



S_{11} VS FREQUENCY



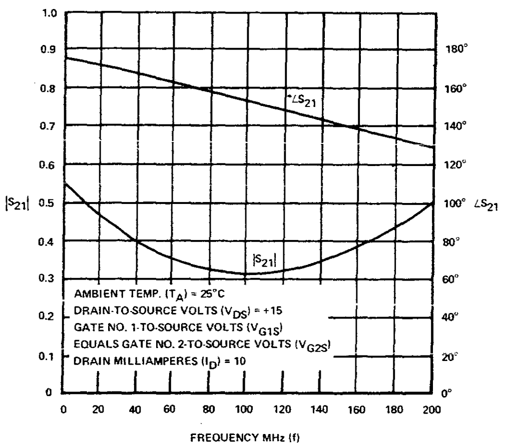
S_{12} VS FREQUENCY



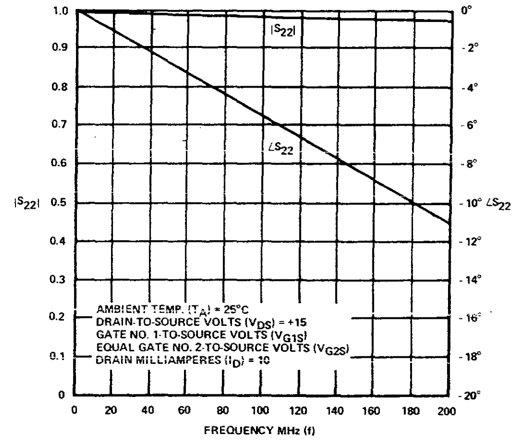
CHARACTERISTIC CURVES (Continued)

MIXER SECTION

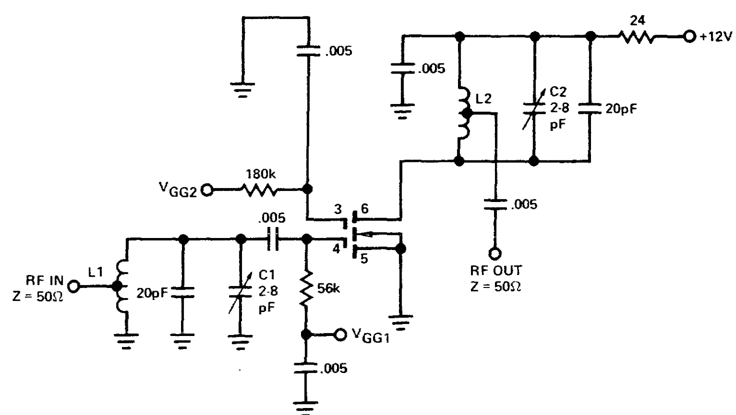
S_{21} VS FREQUENCY



S_{22} VS FREQUENCY

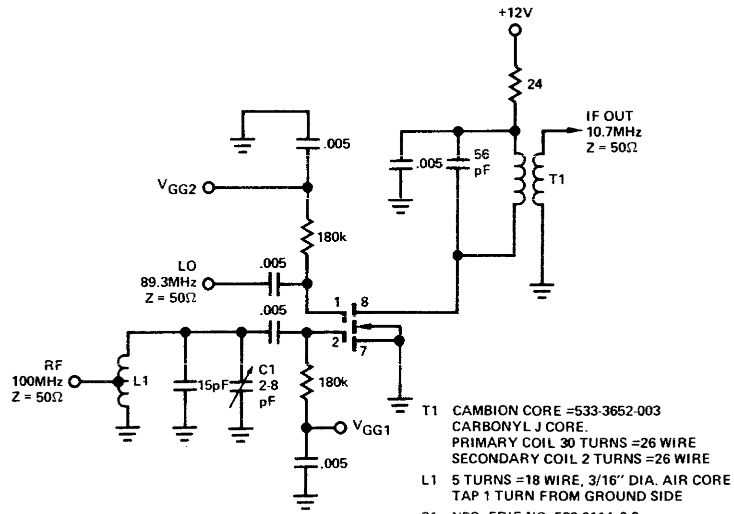


RF AMP SECTION TEST CIRCUIT



L1-L2 5 TURN #18 WIRE 3/16" DIA. AIR CORE
TAPPED AT 1 TURN
C1-C2 NPO, ERIE NO. 538-011A-2-8

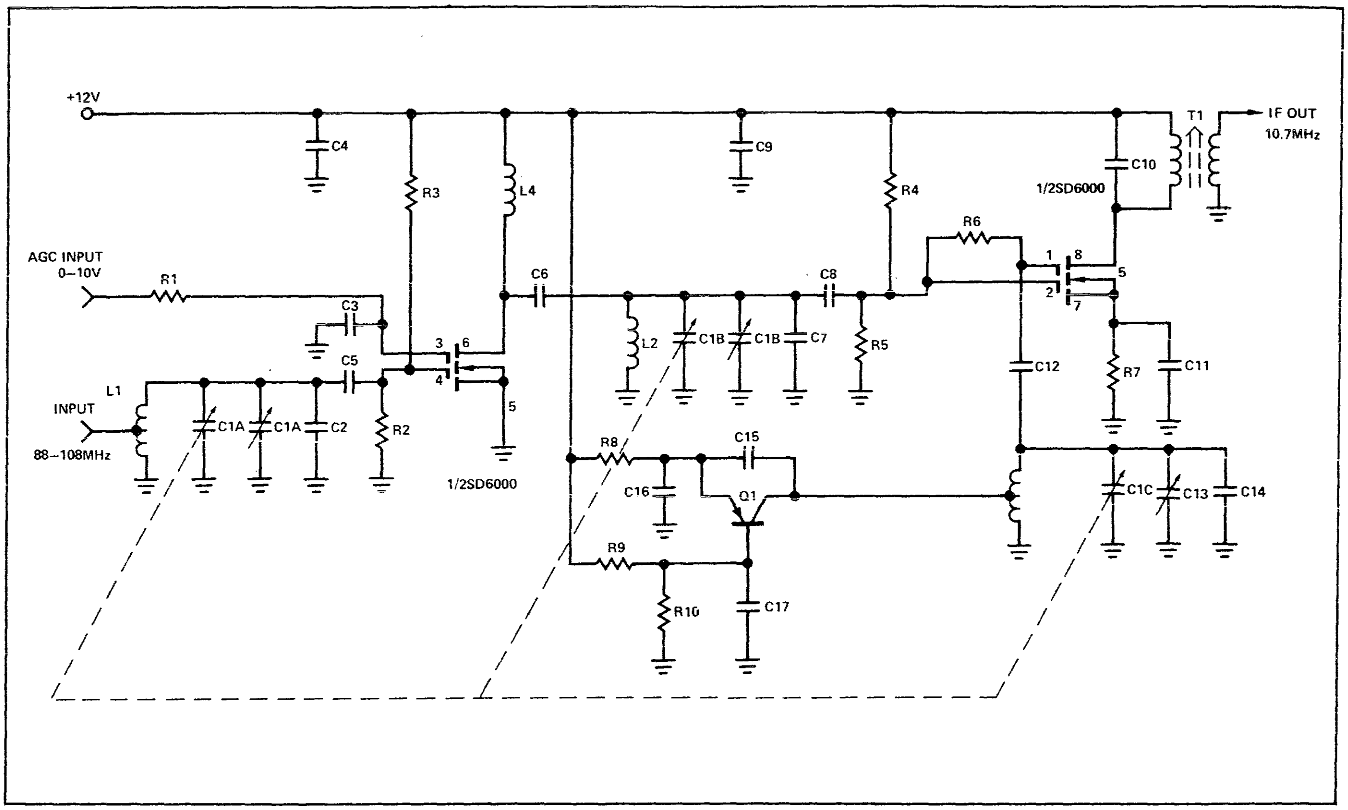
MIXER SECTION TEST CIRCUIT



FM TUNER USING SD6000 ELECTRICAL DATA

PARAMETER	TEST CONDITIONS	TYP
Supply Voltage		+12V
Supply Current	AGC voltage +10V	25mA
Frequency Range		88MHz to 108MHz
Bandwidth	RF Amp (−3dB) Mixer (−3dB)	2.5MHz 300kHz
Input Impedance		75Ω
Output Impedance		50Ω
IF Output Frequency		10.7MHz
Oscillator Stability w/respect to Supply Voltage		40kHz/volt
Oscillator Stability w/respect to Temperature		10kHz/°C
Power Gain	88MHz to 108MHz	30dB Min
Noise Figure	@ 100MHz	3.0dB Max

FM TUNER USING SD6000



PARTS LIST

1. **Transistors**

	Description	Type
Q1	PNP Silicon	2N4126

2. **Integrated Circuits**

U1	Dual D-MOS FET	SD6000V

3. **Resistors** (All carbon resistors in ohms ±10% tolerance.)

	Value
R1	30k
R2	68k
R3	200k
R4	150k
R5	39k
R6	82k
R7	120
R8	6800
R9	13k
R10	3k

4. **Capacitors**

	Value	Type
C1	5-20pF	3 Gang Tuning Capacitor
C2	20pF	±5% NPO
C3, 4, 5, 6, 8, 9, 11, 12, 17	.005	+80% – 20% Ceramic
C7	10pF	±5% NPO
C10	56pF	±5% MICA or Ceramic
C13	2-8pF	Trimmer
C14	12pF	±5% NPO
C15	10pF	±5% NPO
C16	10pF	±5% NPO

5. **Miscellaneous Components**

T1	IF Transformer	Cambion 533-3652-003 Jcore Prim. 30T #26 Sec. 2T #26
L1	RF Input Coil	4 turns #18 on 3/16" dia. Air core – Tap 1 turn from ground side.
L2	RF Output Coil	4 turns #18 on 3/16" dia. air core.
L3	Oscillator Coil	4 turns #18 on 3/16" dia. air core center-tapped.
L4		33µh RF choke

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