signetics

DIGITAL
UTILOGIC II/600
TTL/DTL

TABLE OF CONTENTS

- Dual In-Line Packaging
- Greater than 1-volt DC Noise Margins
- Popular 5V Supply Voltage Characterizations

Section 1 General Information

INTRODUCTION

UTILOGIC II is an improved version of Signetics original UTILOGIC family which was introduced in 1964. New devices and features in UTILOGIC II include dual in-line plug-in package, two J-K binaries, a dual D binary, a complete complement of OR, NOR, AND, and NAND gates, as well as buffer line drivers, a one shot, and a zero crossing detector.

The proven performance of the earlier UTILOGIC family, including greater than 1 volt noise margins and high capacitive drive capability has been retained. The simplicity of the Signetics silicone package provides inherently low cost in both manufacturing and subsequent handling by the user. The reliability of the Signetics silicone package has been proved by over five years of exhaustive testing. A copy of the Signetics package reliability report is available on request.

The SP600A family of compatible DTL elements is a new addition to this handbook. It affords the designer a choice of pull-up resistor values for the NAND gates as well as additional logic functions.

UTILOGIC II and SP600 elements are available in the popular 0°C to 75°C range and are designed to operate on a V_{cc} = 5V ±10% power supply.

The suffix A signifies the 14-pin dual in-line package; the suffix B signifies the 16-pin dual in-line package.

The UTILOGIC II family consists of the following elements:

NOR Gates

314A	Single 7-Input NOR Gate
317A	Dual 4-Input Expandable NOR Gate
370A	Triple 3-Input NOR Gate
380A	Quad 2-Input NOR Gate
381A	Quad 2-Input NOR Gate (Open-Collector)

OR Gates

333A	Dual 3-Input Expandable OR Gate
334A	Dual 4-Input Expandable OR Gate
374A	Triple 3-Input OR Gate
375A	Triple 2-Input Expandable OR Gate
384A	Quad 2-Input OR Gate

AND Gates

302A	Quad 2-Input AND Gate
304A	Dual 4-Input AND Gate (Expandable)
305A	Single 6-Input AND Gate
306A	Dual 3-Input AND Gate

NAND Gates

337A	Dual 4-Input Expandable NAND Gate
377A	Triple 3-Input NAND Gate
387A	Quad 2-Input NAND Gate
391A	Hex Inverter (Open Collector)

Gate Expanders

300A	Dual 3-Input Expander for OR and NOR Gates
301A	Quad 2-Input Diode Expander for NAND Gates

Buffer Drivers

352A	Dual 3-Input Expandable NAND Buffer Driver (Open Collector)
356A	Dual 4-Input Expandable NAND Buffer Driver
357A	Quad 2-Input NAND Power Driver
358A	Quad 2-Input NAND Power Driver (Open-Collector)

Binaries

321A	Dual J-K Binary
322A	Dual J-K Binary
328A	Dual D Binary

Pulse Shapers

362A	Monostable Multivibrator
363A	Dual Zero Crossing Detector

Shift Register

3271B	4-Bit Shift Register

Counters

3280A	BCD Decade Counter
3281A	4-Bit Binary Counter

The SP600 family consists of the following elements:

NAND Gates

616A	Dual 4-Input Expandable NAND Gate
670A	Triple 3-Input NAND Gate
680A	Quad 2-Input NAND Gate

Line Driver

659A	Dual 4-Input Buffer/Driver

J-K Binary

620A	Single J-K Binary

RS/T Binary

629A	Single RS/T Binary

Inverter

690A	Hex Inverter

Expander

631A	Gate Expander

LOADING DEFINITIONS

UTILOGIC II and SP600 loads are classified as "sink loads," or current out of the load inputs, and as "source loads," or current into the load inputs. The standard sink load is the input of a UTILOGIC II AND gate. The standard source load is the input of a UTILOGIC II NOR gate. See the loading chart or specification sheets for specific values.

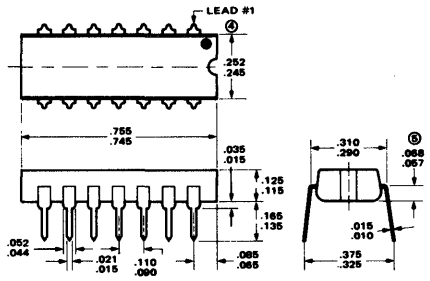
NOISE MARGINS

Signetics specifies noise immunity on UTILOGIC II and SP600 gates in terms of DC margins determined under worst case conditions for both the "0" and "1" levels. The margin for a "1" input applies to negative-going noise on the high level or on the power supply line. The margin for a "0" input applies to positive-going noise on the low logic level or the ground line. The DC margin is defined as the difference between the worst case output level and the worst case input threshold.

For the 305/306 AND gates, maximum offset voltages, which are more appropriate to nonsaturating gates, are specified. These offset voltages ensure maintenance of high DC margins in cascaded logic configurations.

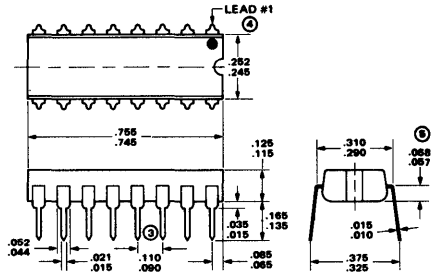
PACKAGE TYPES

A PACKAGE



NOTES:
1. Lead Material: Alloy 42 or equivalent
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash
7. Thermal resistance: $\theta J_A = .16^\circ C/mW$, $\theta J_C = .08^\circ C/mW$

B PACKAGE



NOTES:
1. Lead Material: Alloy 42 or equivalent
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash
7. Thermal resistance: $\theta J_A = .16^\circ C/mw$, $\theta J_C = .08^\circ C/mW$

Section 2
Electrical Characteristics

ELECTRICAL CHARACTERISTICS

This section contains specific test limits and test condition information for use in device evaluation and incoming inspection on D.C. and A.C. parameters.

Also included in this section are pin layouts, package information, circuit diagrams and many typical curves describing the product operating characteristics.

ABSOLUTE MAXIMUM RATINGS (NOTES 1, 2, 3 AND 4)

Voltage Applied (All Terminals)		±5.5V
Current Rating	(All Input Terminals)	±10mA
	(All Other Terminals)	±50mA
Temperature Range		
Operating		0°C to +75°C
Storage		-65°C to +150°C

NOTES:

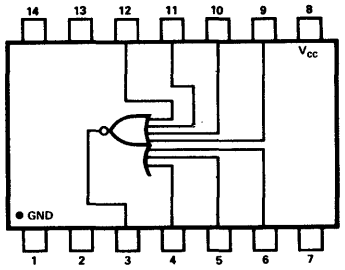
1. Pins not specifically referenced are left electrically open.
2. All voltage measurements are referenced to the ground pin.
3. Positive current flow is defined as current INTO the terminal indicated.
4. Precautionary measures should be taken to ensure current limiting per the maximum ratings, should the isolation diodes become forward biased.
5. Positive logic definition: "UP" level = "1"; "DOWN" level = "0".
6. This characteristic guaranteed by output voltage measurements.
7. Manufacturer reserves the right to make design and process improvements.
8. Capacitance C includes probe and test jig.
9. For this test, the signal input (pin 2 or 13) is tied to -6V through 10kΩ resistor.
10. Pin 14 must be tied to most negative voltage used.
11. Standard Source Load is 180μA and Standard Sink Load is -2.5mA

NOR GATES

SP314A Single 7-Input
SP317A Dual 4-Input Expandable
SP370A Triple 3-Input
SP380A Quad 2-Input

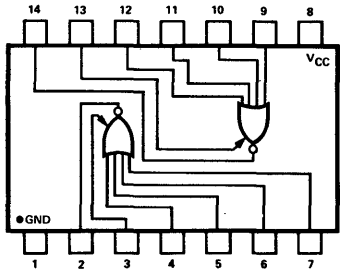
PIN CONFIGURATION

7-INPUT



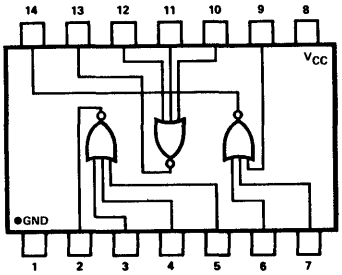
SP314A

DUAL 4-INPUT EXPANDABLE



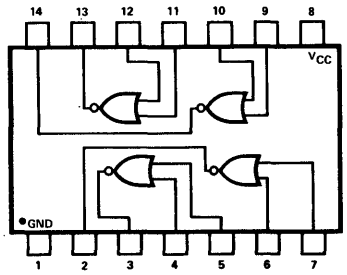
SP317A

TRIPLE 3-INPUT



SP370A

QUAD 2-INPUT



SP380A

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

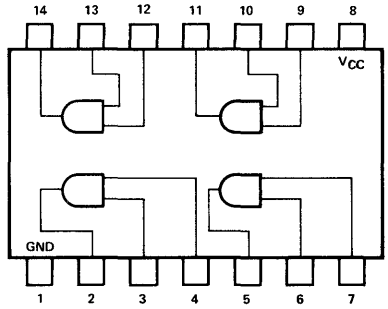
CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP	MAX.	UNITS
Noise Immunity	See Note 6				
for "1"		1100	1700		mV
for "0"		600	1000		mV
Output Voltage					
"1" Level	I_{out} = -2mA, V_{in} = 1.2V	3.8			V
"0" Level	I_{out} = 12.5mA, V_{in} = 2.7V			0.6	V
	I_{out} = 7.5mA, V_{in} = 2.7V			0.4	V
Input Current - input high	V_{in} = 2.7V			180	μA
Power Supply Current					
output high	V_{in} = 0V, T_A = 25°C			0.3	mA/gate
output low	V_{in} = 4.0V, T_A = 25°C		13.4	18.1	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		25	60	ns
Turn off Delay	See Test Figure 1, T_A = 25°C		50	80	ns
Fan-Out					
-To sink loads (2.5mA/load)				5	
-To source loads (180μA/load)				11	
Expander Voltage (317 only)	V_{in} = 2.7V	1.85			V

Typical Values are for T_A = 25°C. See Page 3 for Notes.

signetics

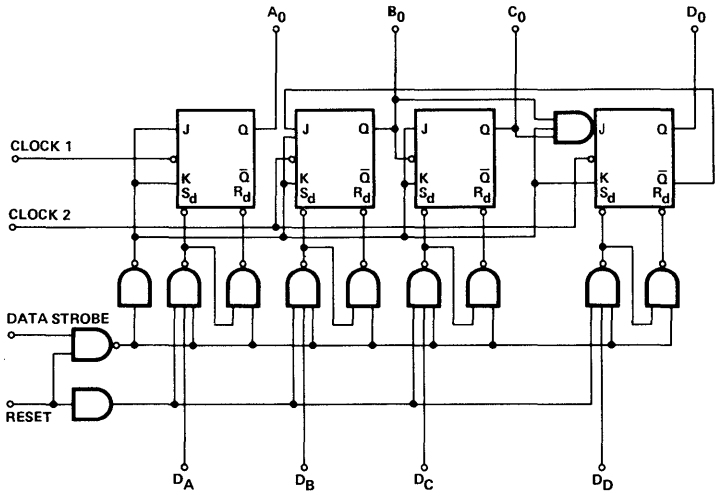
ERRATA - UTILOGIC II HANDBOOK

1. **Page 5 -** Schematic diagram should show output (OUT) at collector of lower transistor rather than upper.
2. **Page 5 -** Switching Time versus Fan-Out curve should read: SWITCHING TIME (RELATIVE VALUE) rather than SWITCHING TIME (nsec.)
3. **Page 11 -** Pin configuration for SP302 should be as shown below.

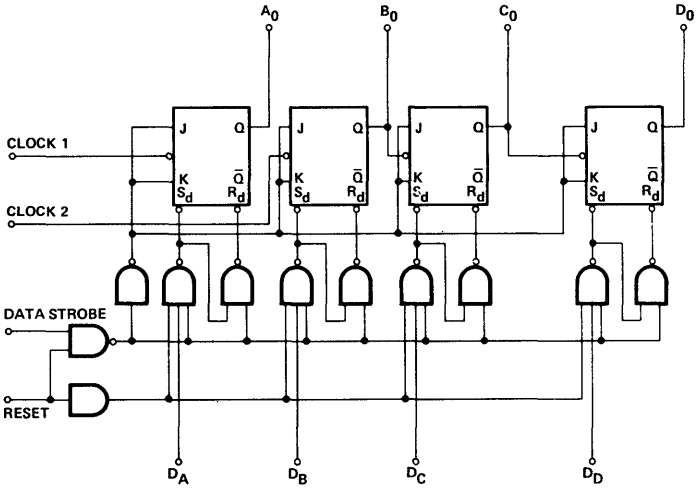


4. **Page 30 -** Typical Turn on and Turn off Delays for the SP321 and SP322 should be 25ns rather than 50ns.
5. **Page 31 -** Both Truth Tables shown are for 321/322.
6. **Page 41 -** Logic Diagrams for SP3280A and SP3281A should be as shown below.

SP3280A



SP3281A

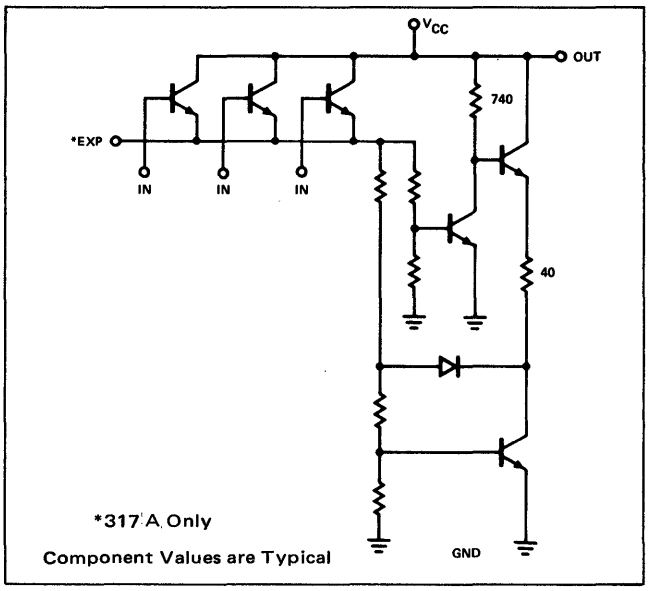


7. **Page 41 -** Add following note to Figure 1.

   Note: T_{on} and T_{off} are measured from the clock input of each binary to the Q output of that binary.

8. **Page 45 -** Circuit schematic for the SP363 should show Zener diode from pin 14 to pin 1. The zener diode lowers -12V to -6V in the event that a -6V supply is not available.

SCHEMATIC DIAGRAM



TEST CIRCUIT AND WAVEFORM

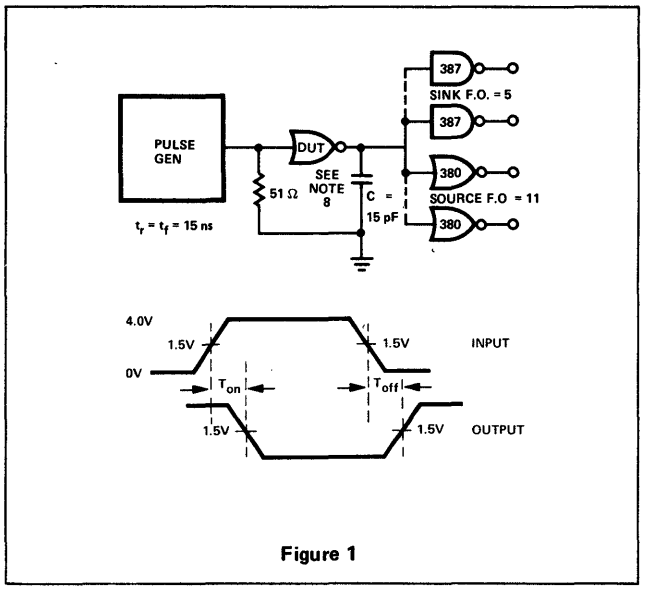
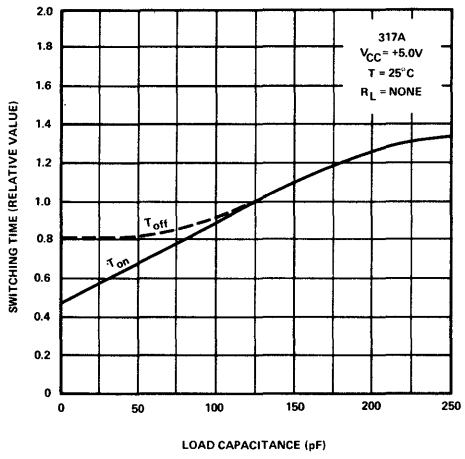
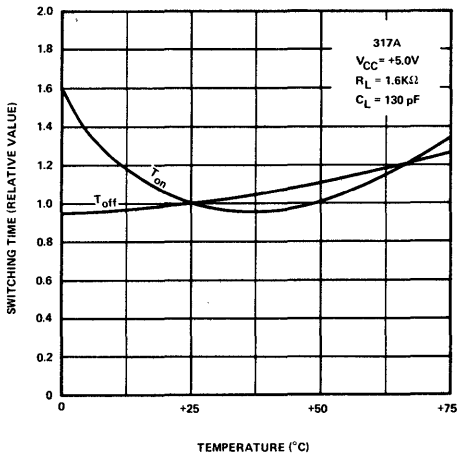
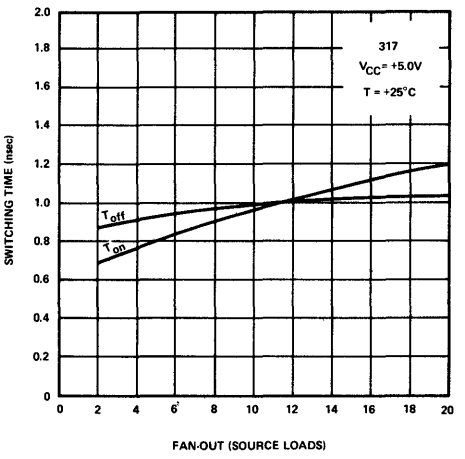


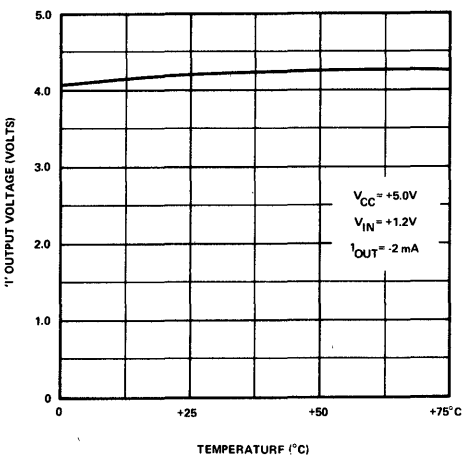
Figure 1

The following curves are normalized, when applicable, to the standard data sheet conditions.

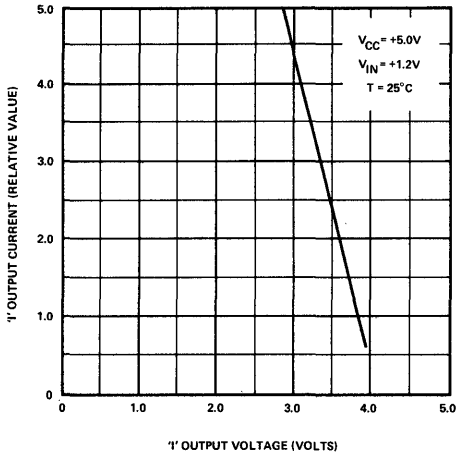


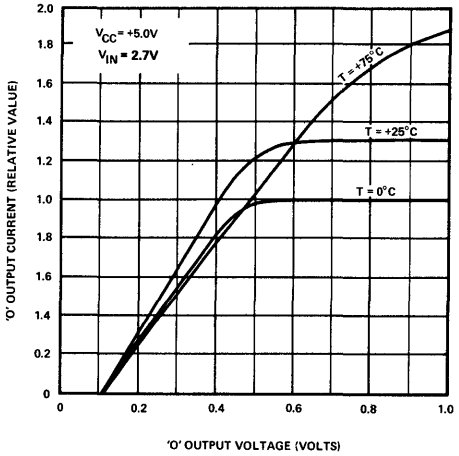


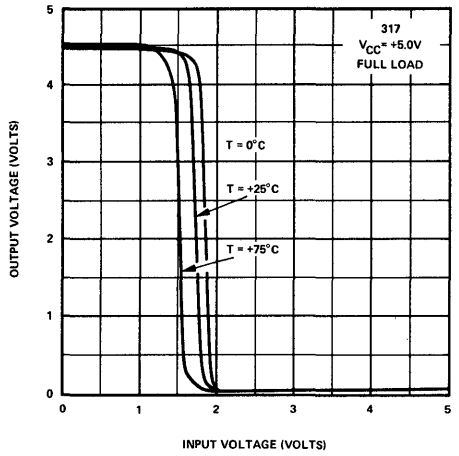


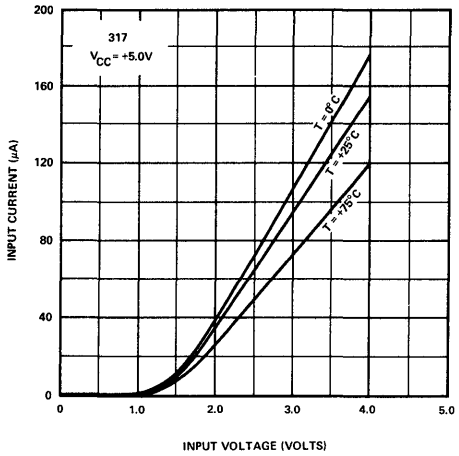


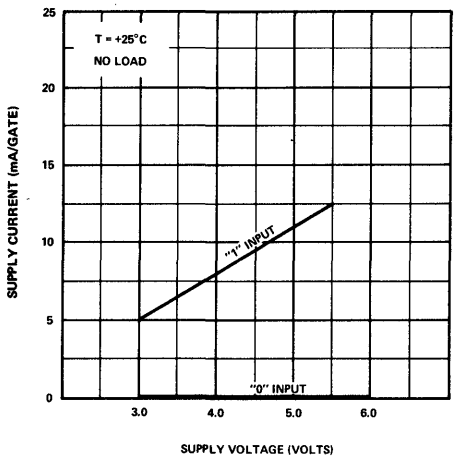
The following curves are normalized, when applicable, to the standard data sheet conditions.



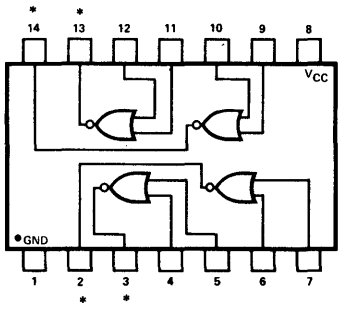








PIN CONFIGURATION



*Open Collector Outputs

SP381A

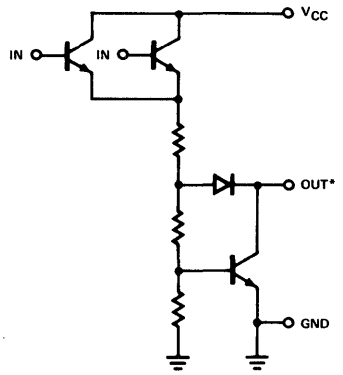
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP	MAX.	UNITS
Output Leakage Current "1" Level	V_{out} = 5.0V, V_{in} = 0.9V			100	μA
Output Voltage "0" Level	I_{out} = 12.5mA, V_{in} = 2.7V			0.6	V
	I_{out} = 7.5mA, V_{in} = 2.7V			0.4	V
Input Current Input high	V_{in} = 2.7V			180	μA
Power Supply Current Output high	V_{in} = 0V, T_A = 25°C			0.3	mA/gate
Output low	V_{in} = 4.0V, T_A = 25°C		13.4	18.1	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		25	60	ns
Fan-Out –To sink loads (2.5mA/load)				5	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



1/4 of circuit is shown

*Outputs are Open-Collector

TEST CIRCUIT AND WAVEFORM

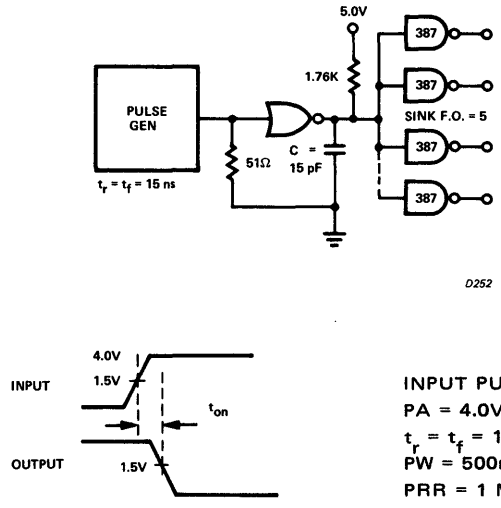


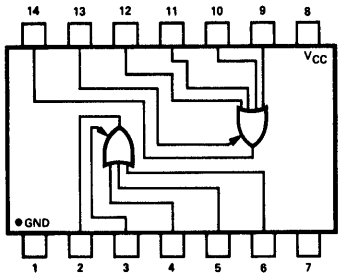
Figure 1

OR GATES

SP333A Dual 3-Input Expandable
SP334A Dual 4-Input Expandable
SP374A Triple 3-Input
SP375A Triple 2-Input
SP384A Quad 2-Input

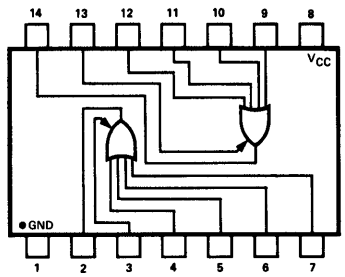
PIN CONFIGURATIONS

DUAL 3-INPUT EXPANDABLE



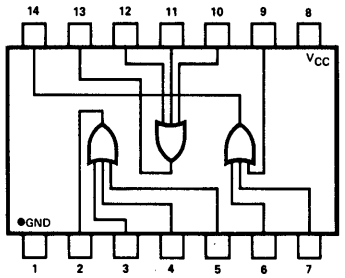
333A

DUAL 4-INPUT EXPANDABLE



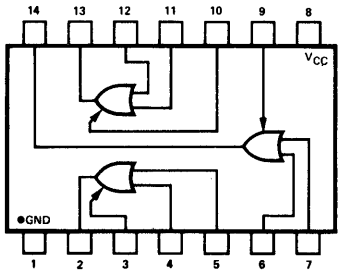
334A

TRIPLE 3-INPUT



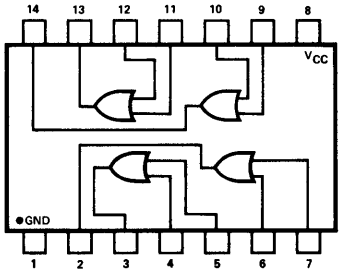
374 A

TRIPLE 2-INPUT EXPANDABLE



375A

QUAD 2-INPUT



384A

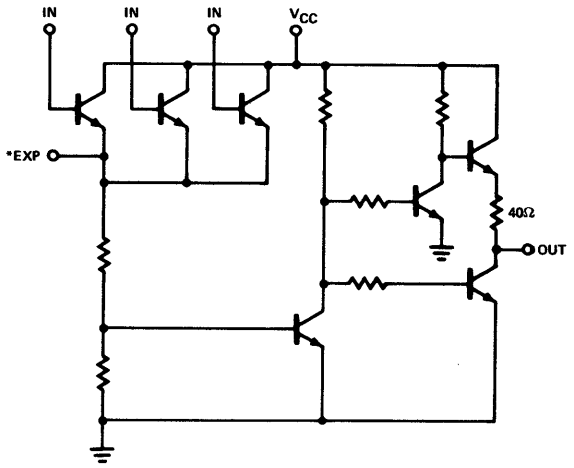
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP	MAX.	UNITS
Noise Immunity					
for "1"	See Note 6	1100	1700		
for "0"	See Note 6	600	1000		
Output Voltage					
"1" Level	I_{out} = –2mA, V_{in} = 2.7V	3.8			V
"0" Level	I_{out} = 12.5mA, V_{in} = 1.2V			0.6	V
	I_{out} = 7.5mA, V_{in} = 1.2V			0.4	V
Input Current -					
input high	V_{in} = 2.7V			180	μA
Power Supply Current					
output high	V_{in} = 4.0V, T_A = 25°C		11.0	14.7	mA/gate
output low	V_{in} = 0V, T_A = 25°C		11.2	15.2	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		50	80	ns
Turn off Delay	See Test Figure 1, T_A = 25°C		40	70	ns
Fan-out					
–To sink loads (2.5mA/load)				5	
–To source loads (180μA/load)				11	
Expander Voltage (333/334/335 only)	V_{in} = 2.7V	1.85			V

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

*333/334/374 Only

TEST CIRCUIT AND WAVEFORM

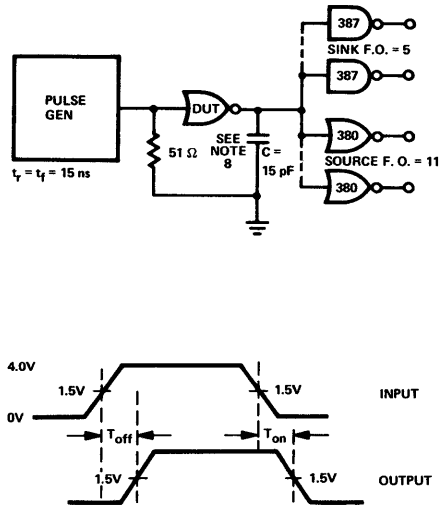
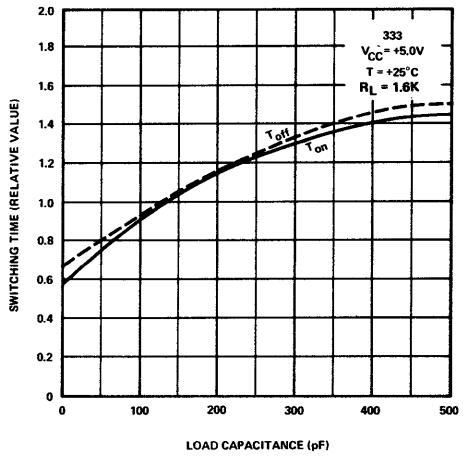
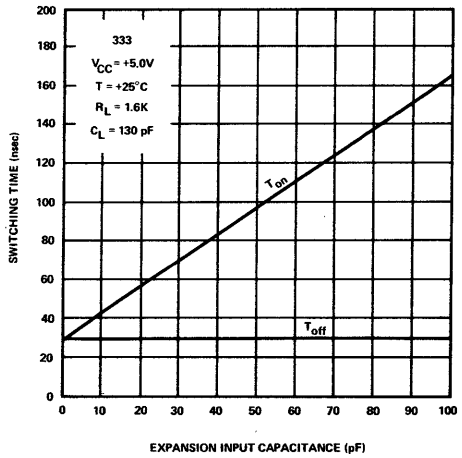
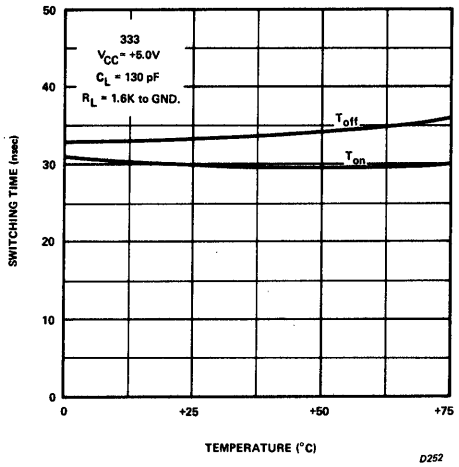


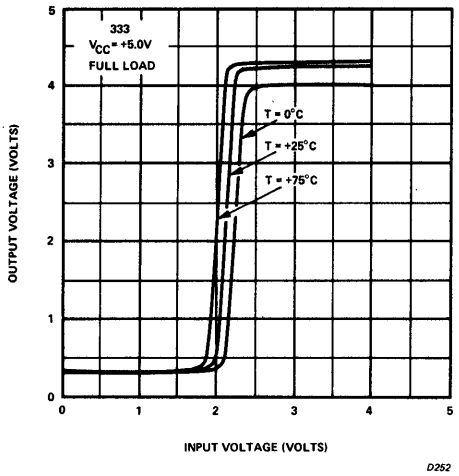
Figure 1

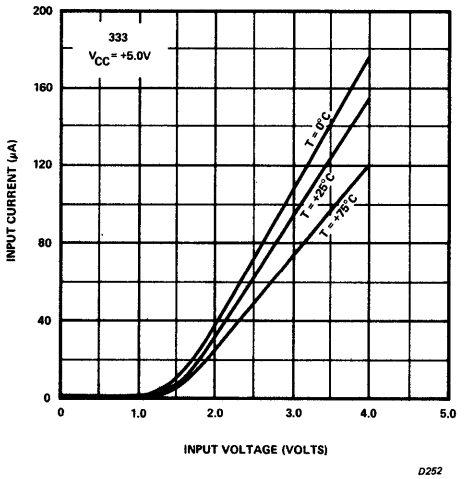
The following curves are normalized, when applicable, to the standard data sheet conditions.

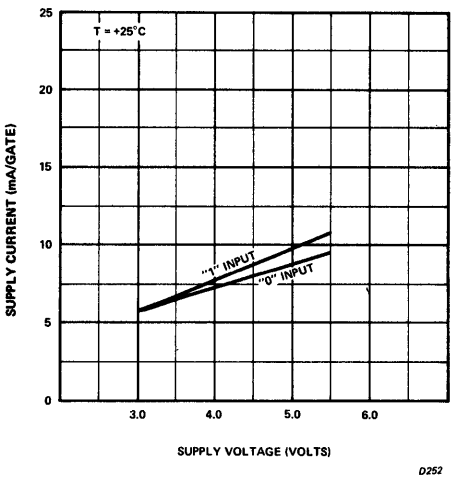





333
V_{CC} = +5.0V
C_L = 130 pF
R_L = 1.6K to GND.
T_{off}
T_{on}
SWITCHING TIME (nsec)
50
40
30
20
10
0
0
+25
+50
+75
TEMPERATURE (°C)
D252

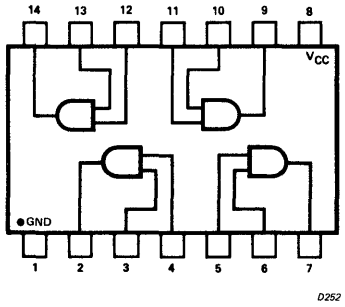

333
V_{CC} = +5.0V
FULL LOAD
T = 0°C
T = +25°C
T = +75°C
OUTPUT VOLTAGE (VOLTS)
5
4
3
2
1
0
0
1
2
3
4
5
INPUT VOLTAGE (VOLTS)
D252


333
V_{CC} = +5.0V
T = 0°C
T = +25°C
T = +75°C
INPUT CURRENT (μA)
200
160
120
80
40
0
0
1.0
2.0
3.0
4.0
5.0
INPUT VOLTAGE (VOLTS)
D252


T = +25°C
"1" INPUT
"0" INPUT
SUPPLY CURRENT (mA/GATE)
25
20
15
10
5
0
3.0
4.0
5.0
6.0
SUPPLY VOLTAGE (VOLTS)
D252

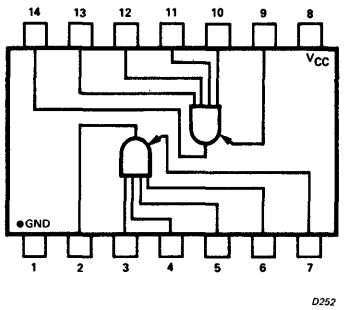
PIN CONFIGURATION

QUAD 2-INPUT



SP302A

DUAL 4-INPUT



SP304A

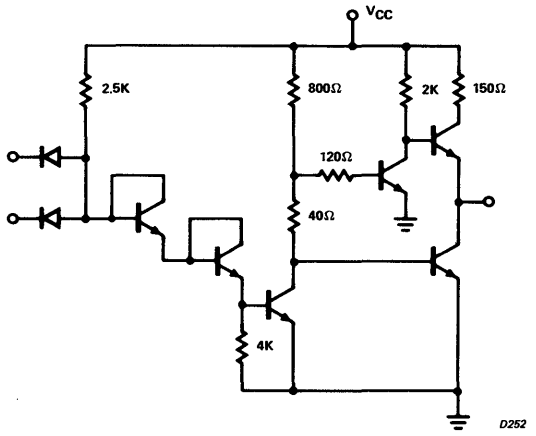
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
"1" Level	See Note 6	1400	1800		mV
"0" Level	See Note 6	300	800		mV
Output Voltage					
"1" Level	I_{out} = −3mA, V_{in} = 2.1V	3.5			V
"0" Level	I_{out} = 30mA, V_{in} = 0.9V			0.6	V
	I_{out} = 17.5mA, V_{in} = 0.9V			0.4	V
Input Current	V_{in} = 5.0V		10	25	μA
"1" Level	V_{in} = 0.6V			−2.5	mA
"0" Level					
Power Supply Current	V_{in} = 4.0V, T_A = 25°C			9.2	mA/gate
Output high	V_{in} = 0V, T_A = 25°C			12.4	mA/gate
Output low	See Test Figure 1, T_A = 25°C		15	50	ns
Turn on Delay	See Test Figure 1, T_A = 25°C		15	50	ns
Turn off Delay					
Fan-Out				12	
−To sink loads (2.5mA/load)				16	
−To source loads (180μA/load)					

Typical Values are for T_A = 25°C. See Page 3 for Notes.

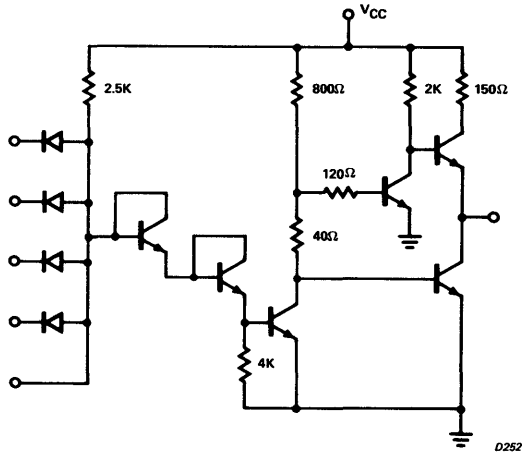
SCHEMATIC DIAGRAM



Component Values are Typical

1/2 of circuit shown **SP304A**

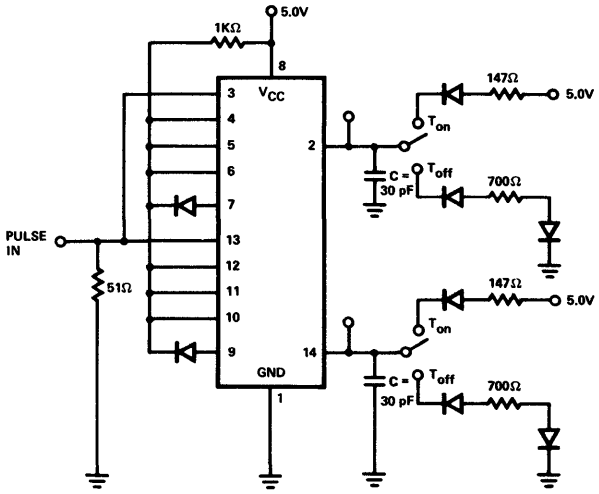
SCHEMATIC DIAGRAM



Component Values are Typical

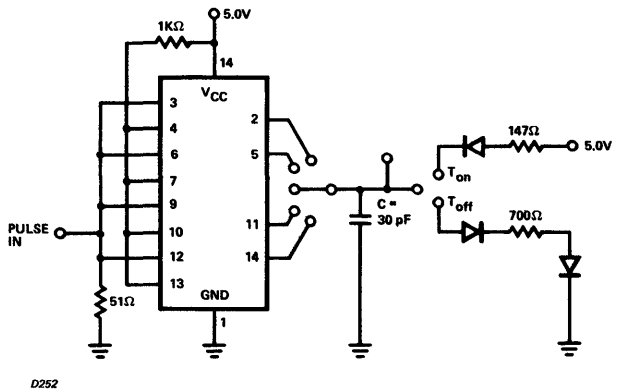
1/4 of circuit is shown **SP302A**

TEST CIRCUIT



All diodes are 1N916's **SP302A**

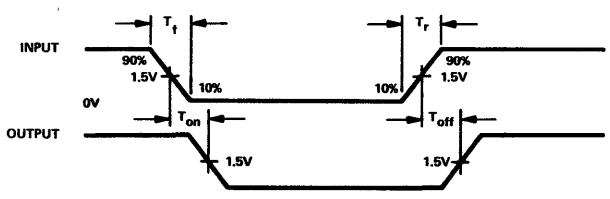
TEST CIRCUIT



All diodes are 1N916's **SP304A**

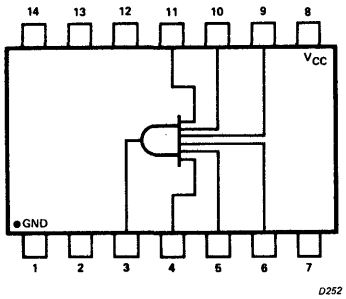
WAVEFORM

INPUT PULSE
PA = 4.0V
t_r = t_f = 10nsec
PW = 500nsec
PRR = 1 MHz



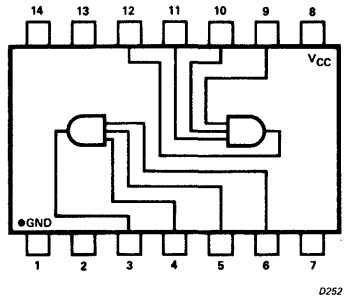
PIN CONFIGURATION

SINGLE 6-INPUT



305A

DUAL 3-INPUT



306A

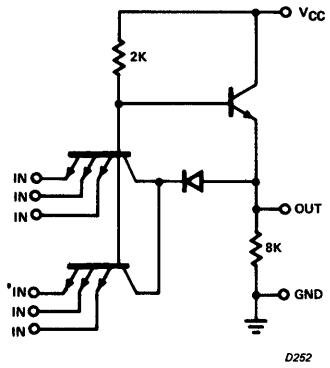
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Offset Voltage					
"1" Level	I_{out} = -1.8mA, V_{in} = 3.8V measure V_{in} - V_{out}			0.15	V
"0" Level	I_{out} = 0, V_{in} = 0.6V measure V_{in} - V_{out}			-0.3	V
Input Current					
input high	V_{in} = 5.0V		10	40.0	μA
input low	V_{in} = 0.6V			-2.5	mA
Power Supply Current					
output high	V_{in} = 4.0V, T_A = 25°C			0.9	mA/gate
output low	V_{in} = 0V, T_A = 25°C			2.9	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		15	50	ns
Turn off Delay	See Test Figure 1, T_A = 25°C		32	60	ns
Fan-out					
-To sink loads (2.5mA/load)				0	
-To source loads (180μA/load)				10	

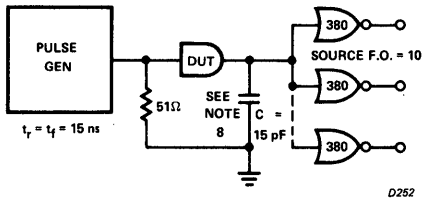
Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

TEST CIRCUIT AND WAVEFORM



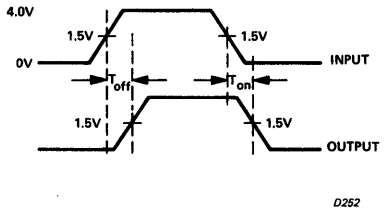
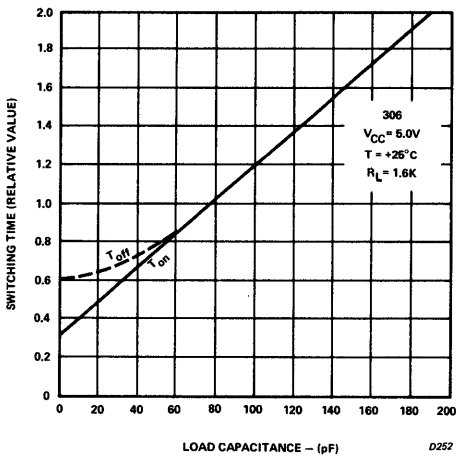
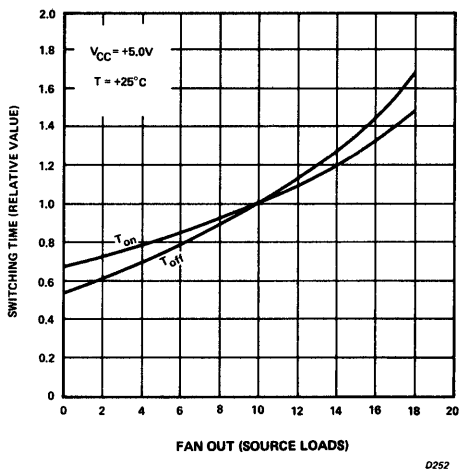
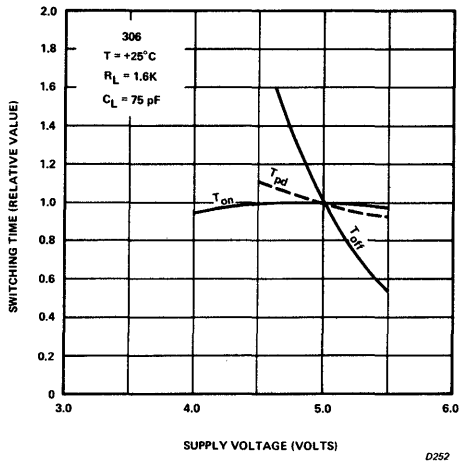


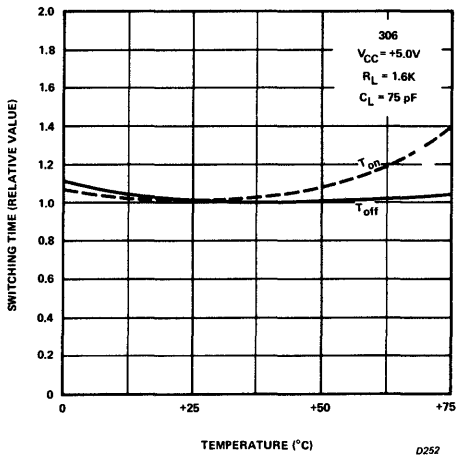
Figure 1

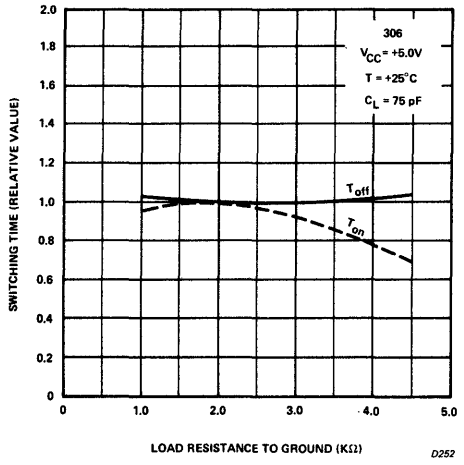
The following curves are normalized, when applicable, to the standard data sheet conditions.

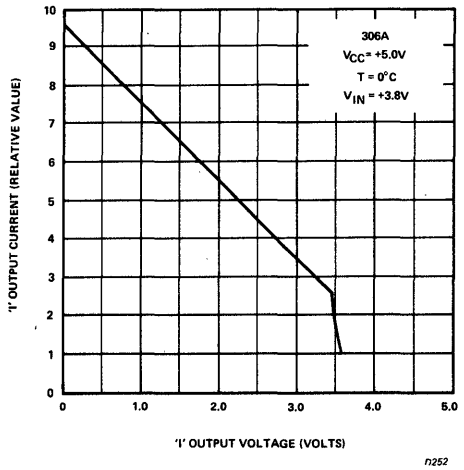


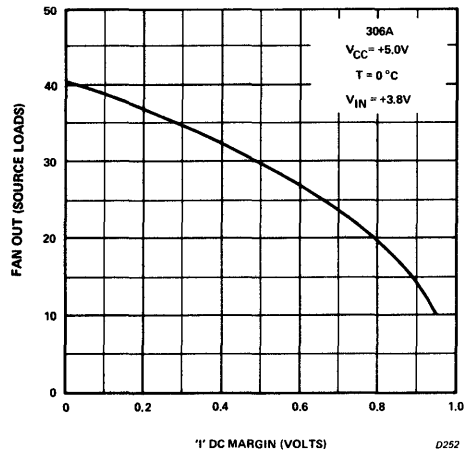


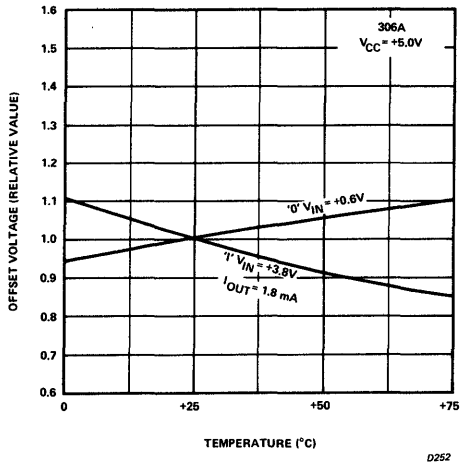

306
T = +25°C
R_L = 1.6K
C_L = 75 pF
T_{pd}
T_{on}
T_{off}
SWITCHING TIME (RELATIVE VALUE)
SUPPLY VOLTAGE (VOLTS)
D252

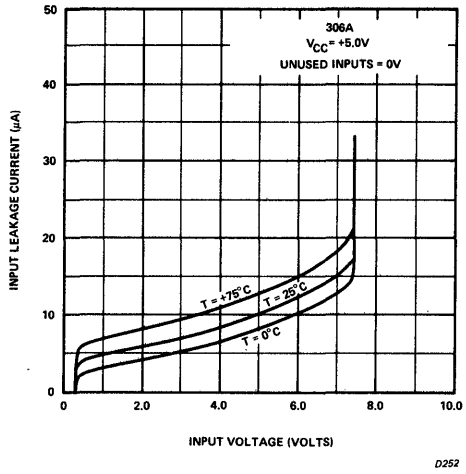

306
V_{CC} = +5.0V
R_L = 1.6K
C_L = 75 pF
T_{on}
T_{off}
SWITCHING TIME (RELATIVE VALUE)
TEMPERATURE (°C)
D252

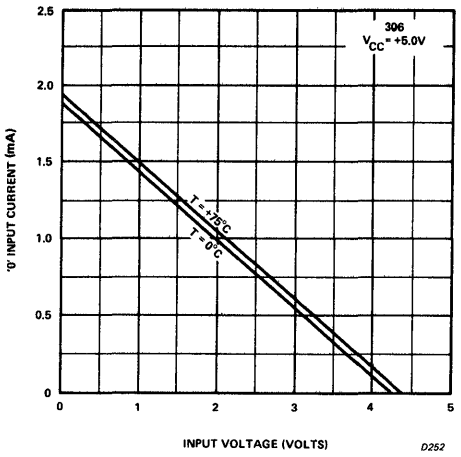

306
V_{CC} = +5.0V
T = +25°C
C_L = 75 pF
T_{off}
T_{on}
SWITCHING TIME (RELATIVE VALUE)
LOAD RESISTANCE TO GROUND (KΩ)
D252

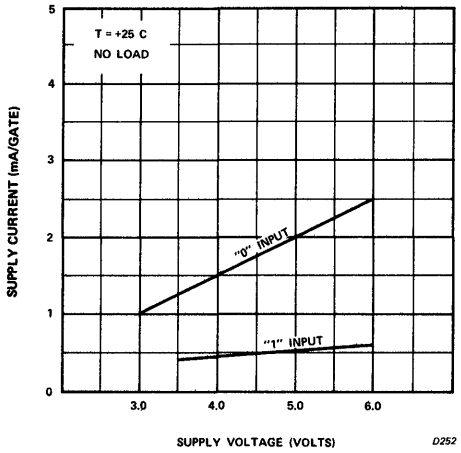

306A
V_{CC} = +5.0V
T = 0°C
V_{IN} = +3.8V
'1' OUTPUT CURRENT (RELATIVE VALUE)
'1' OUTPUT VOLTAGE (VOLTS)
D252


306A
V_{CC} = +5.0V
T = 0°C
V_{IN} = +3.8V
FAN OUT (SOURCE LOADS)
'1' DC MARGIN (VOLTS)
D252


306A
V_{CC} = +5.0V
'0' V_{IN} = +0.6V
'1' V_{IN} = +3.8V
I_{OUT} = 1.8 mA
OFFSET VOLTAGE (RELATIVE VALUE)
TEMPERATURE (°C)
D252

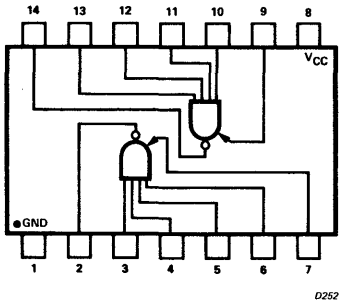

306A
V_{CC} = +5.0V
UNUSED INPUTS = 0V
INPUT LEAKAGE CURRENT (μA)
50
40
30
20
10
0
T = +75°C
T = 25°C
T = 0°C
0
2.0
4.0
6.0
8.0
10.0
INPUT VOLTAGE (VOLTS)
D252


306
V_{CC} = +5.0V
"0" INPUT CURRENT (mA)
2.5
2.0
1.5
1.0
0.5
0
T = +75°C
T = 0°C
0
1
2
3
4
5
INPUT VOLTAGE (VOLTS)
D252


T = +25 C
NO LOAD
SUPPLY CURRENT (mA/GATE)
5
4
3
2
1
0
"0" INPUT
"1" INPUT
3.0
4.0
5.0
6.0
SUPPLY VOLTAGE (VOLTS)
D252

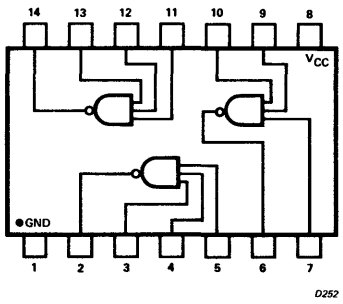
PIN CONFIGURATIONS

DUAL 4-INPUT EXPANDABLE



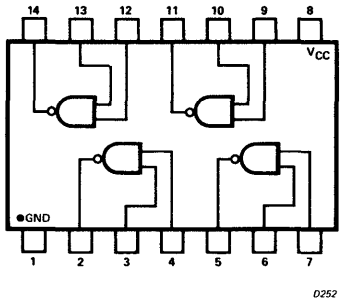
337A

TRIPLE 3-INPUT



377A

QUAD 2-INPUT



387A

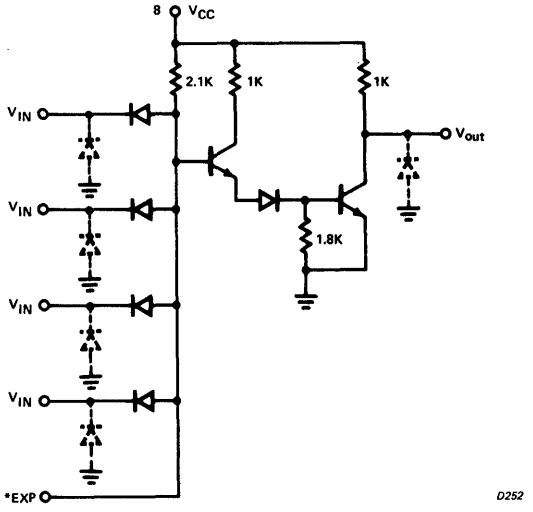
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
for "1"	See Note 6	800	1200		mV
for "0"	See Note 6	300	600		mV
Output Voltage					
"1" Level	I_{out} = –1.08mA, V_{in} = 0.9V	3.5			V
"0" Level	I_{out} = 30mA, V_{in} = 2.7V			0.6	V
	I_{out} = 12.5mA, V_{in} = 2.1V			0.4	V
Input Current					
input high	V_{in} = 5.0V		10	25	μA
input low	V_{in} = 0.6V			–2.5	mA
input low (expander)	V_{in} = 1.1V			–2.5	mA
Power Supply Current					
output high	V_{in} = 0V, T_A = 25°C			2.8	mA/gate
output low	V_{in} = 4.0V, T_A = 25°C			12.8	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		22	50	ns
Turn off Delay	See Test Figure 1, T_A = 25°C		22	50	ns
Fan-out					
–To sink loads (2.5mA/load)				12	
–To source loads (180μA/load)				6	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



*337 only

Component Values are Typical

TEST CIRCUIT AND WAVEFORM

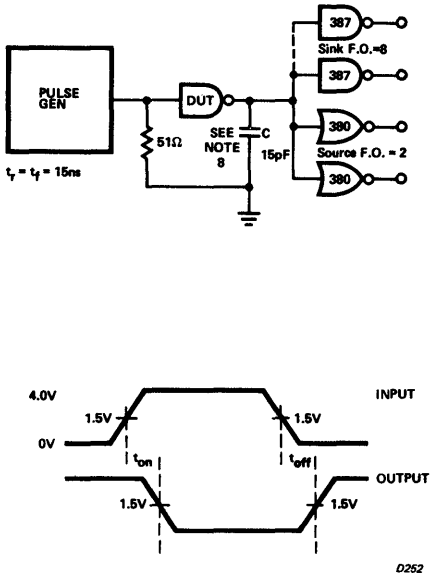
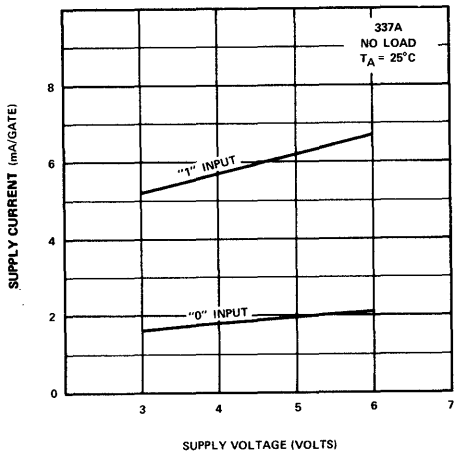
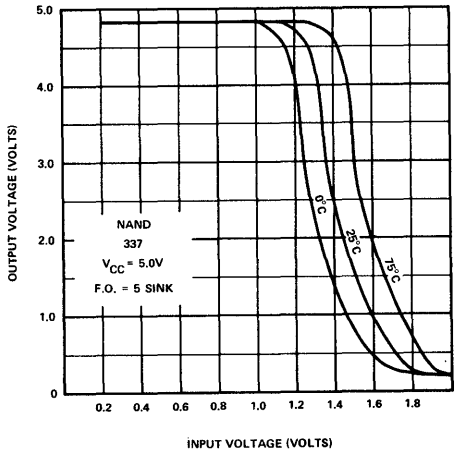
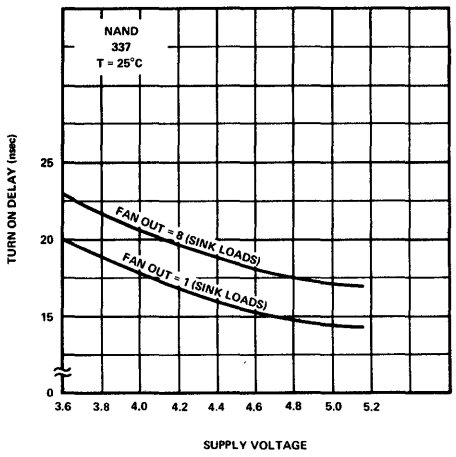


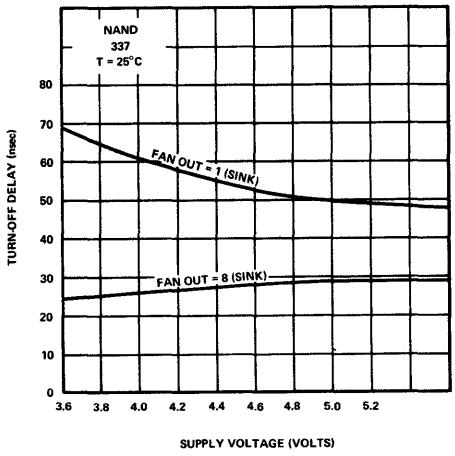
Figure 1

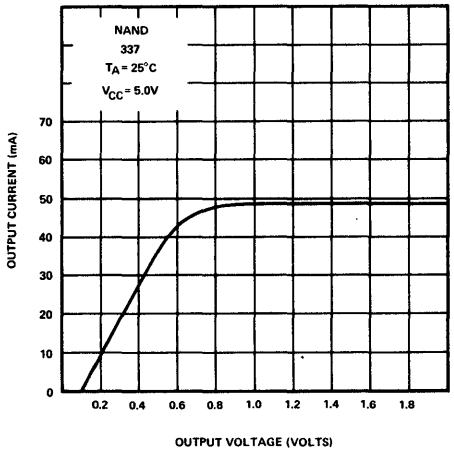
The following curves are normalized, when applicable, to the standard data sheet conditions.





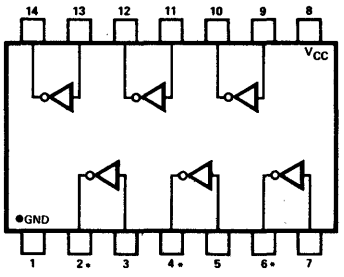

NAND
337
T = 25°C
TURN ON DELAY (nsec)
25
20
15
0
FAN OUT = 8 (SINK LOADS)
FAN OUT = 1 (SINK LOADS)
3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0 5.2
SUPPLY VOLTAGE


NAND
337
T = 25°C
TURN-OFF DELAY (nsec)
80
70
60
50
40
30
20
10
0
FAN OUT = 1 (SINK)
FAN OUT = 8 (SINK)
3.6 3.8 4.0 4.2 4.4 4.6 4.8 5.0 5.2
SUPPLY VOLTAGE (VOLTS)


NAND
337
T_A = 25°C
V_{CC} = 5.0V
OUTPUT CURRENT (mA)
70
60
50
40
30
20
10
0
0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8
OUTPUT VOLTAGE (VOLTS)

HEX INVERTER
SP391A Hex Inverter With Open Collector

PIN CONFIGURATION



*Open-Collector Outputs

SP391A

D252

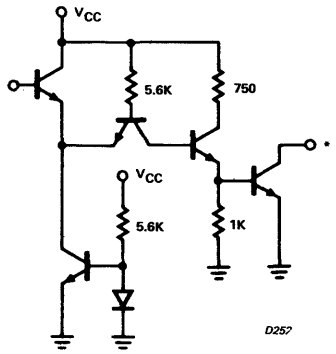
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Leakage Current "1" Level	V_{out} = 5.0V, V_{in} = 1.2V			100	μA
Output Voltage "0" Level	I_{out} = 45mA, V_{in} = 2.7V			0.6	V
	I_{out} = 27mA, V_{in} = 2.7V			0.4	V
Input Current "1" Level	V_{in} = 2.7V			180	μA
Power Supply Current Output high	V_{in} = 0V, T_A = 25°C			2	mA/gate
Output low	V_{in} = 4.0V, T_A = 25°C			10	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		25	50	ns
Fan-Out -To sink loads (2.5mA/load)				18	

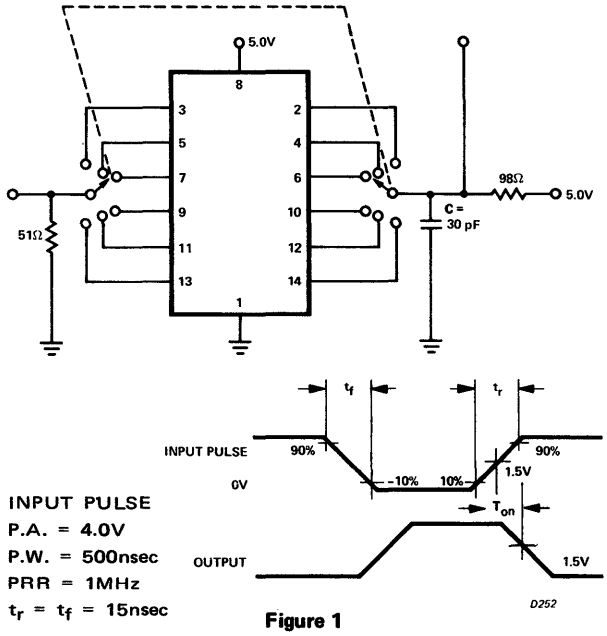
Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



1/6 of circuit is shown
*Outputs are Open-Collector

TEST CIRCUIT AND WAVEFORM

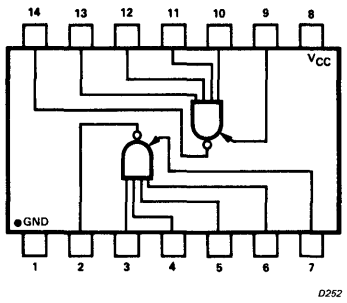


INPUT PULSE
P.A. = 4.0V
P.W. = 500nsec
PRR = 1MHz
t_r = t_f = 15nsec

Figure 1

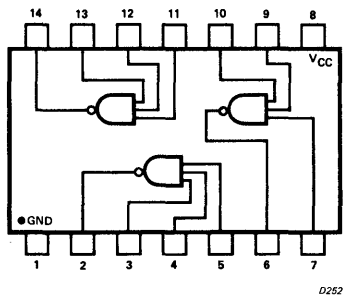
PIN CONFIGURATION

DUAL 3-INPUT EXPANDABLE



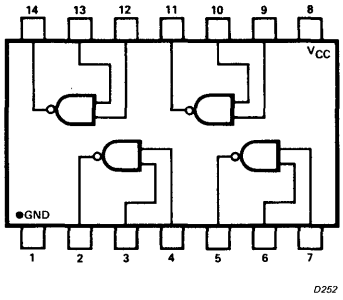
616A

TRIPLE 3-INPUT



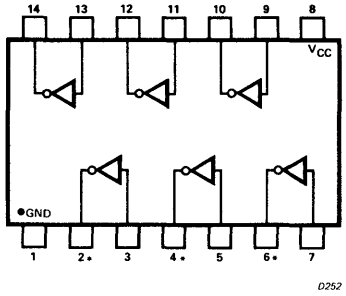
670A

QUAD 2-INPUT



680A

HEX INVERTER



690A

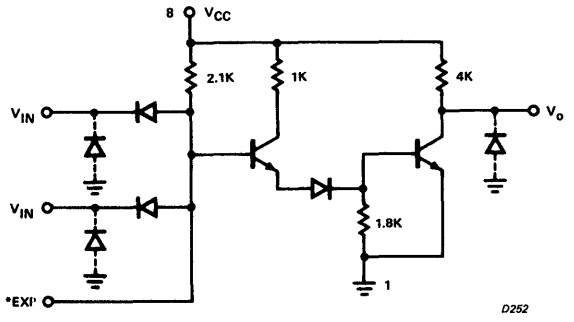
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
for "1"	See Note 6	800	1200		mV
for "0"	See Note 6	300	600		mV
Output Voltage					
"1" Level	V_{in} = 0.9V, I_{out} = 260μA	3.5			V
"0" Level	V_{in} = 2.7V, I_{out} = 20mA			0.6	V
	V_{in} = 2.1V, I_{out} = 12.5mA			0.4	V
Input Current					
input high	V_{in} = 5.0V			25	μA
input low	V_{in} = 0.6V			-2.5	mA
input low (expander)	V_{in} = 1.1V			-2.5	mA
Power Supply Current					
output high	V_{in} = 0V, T_A = 25°C			2.8	mA/gate
output low	V_{in} = 4.0V, T_A = 25°C			9.0	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C		25	65	ns
Turn off Delay	See Test Figure 1, T_A = 25°C		40	70	ns
Fan-out					
-To sink loads (2.5mA/load)				8	
-To source loads (180μA/load)				1	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical
*616 Only

TEST CIRCUIT AND WAVEFORM

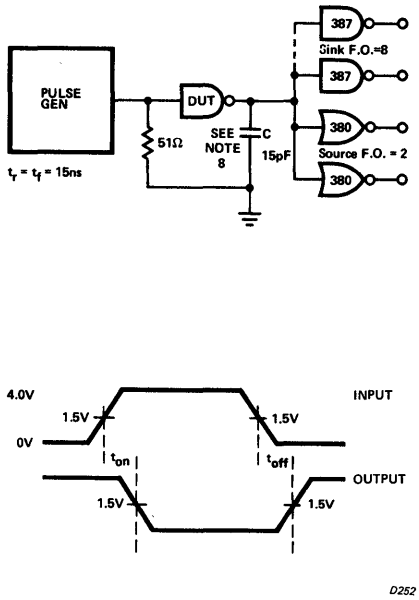
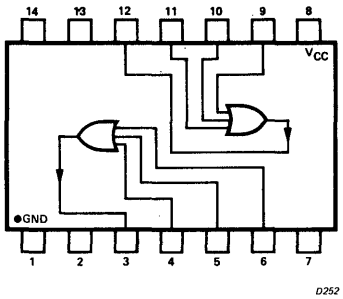


Figure 1

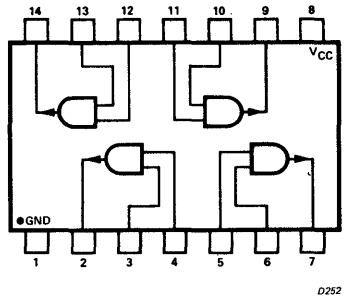
PIN CONFIGURATION

DUAL 3-INPUT



SP300A

QUAD 2-INPUT



SP301A/631A

300 GATE EXPANDER
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Expansion Output Voltage	V_{in} = 2.7V, I_{out} = -3.0mA (620Ω to Gnd.)	1.85			V
Fan-in Expansion of 317	See Text (Page 49) Under NOR Gates			33	

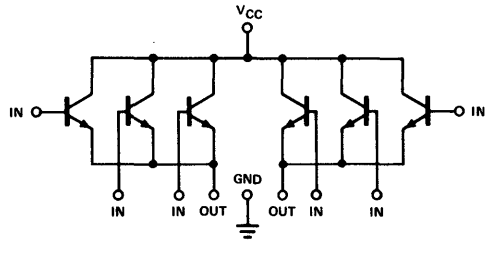
301, 631 GATE EXPANDER
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
"1" Input Current	V_{in} = 5.0V			10	μA
Diode Forward Voltage	I Forward = 2.5mA			0.9	V

Typical Values are for T_A = 25°C. See Page 3 for Notes.

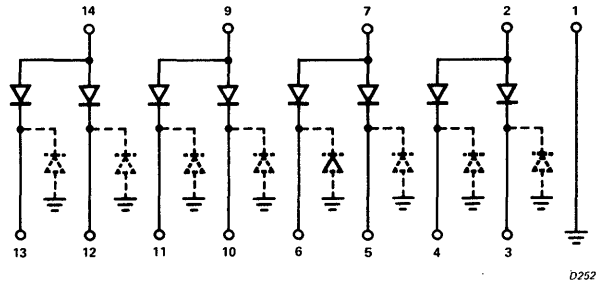
SCHEMATIC DIAGRAM



Component Values are Typical

300A

SCHEMATIC DIAGRAM

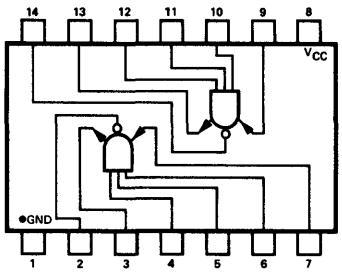


Component Values are Typical

301A/631A

NAND BUFFER DRIVER
SP352 A Dual 3-Input Expandable
(Open Collector)

PIN CONFIGURATION



SP352A

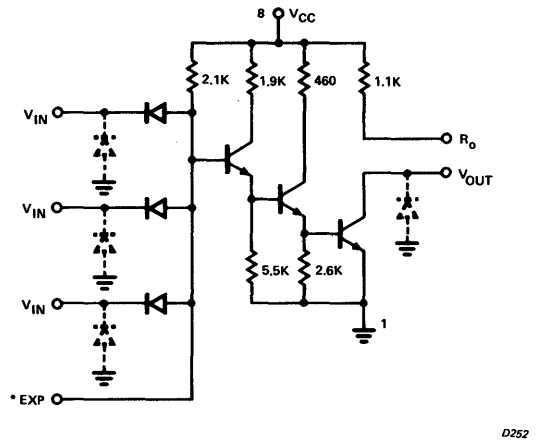
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temp. Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
for "1"	See Note 6	N.A.	N.A.		mV
for "0"	See Note 6	300	600		
Output					
"1" Level Leakage	V_{in} = 0.9V, V_{out} = 5.0V		40	100	μA
"0" Level Voltage	I_{out} = 45mA, V_{in} = 2.7V			0.6	V
	I_{out} = 27mA, V_{in} = 2.1V			0.4	V
Input Current					
input high	V_{in} = 5.0V		5	25	μA
input low	V_{in} = 0.6V			-2.5	mA
input low (expander)	V_{in} = 1.1V			-2.5	mA
Power Supply Current					
output high	V_{in} = 0V, T_A = 25°C			2.8	mA/gate
output low	V_{in} = 4.0V, T_A = 25°C			16.7	mA/gate
Turn on Delay	See Test Figure 1, Output to R_O connected T_A = 25°C			60	ns
Turn off Delay	See Test Figure 1, Output to R_O connected T_A = 25°C			90	ns
Fan-out					
-To sink loads (2.5mA/load)				18	
-To source loads (180μA/load)				N.A.	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component values shown are typical

TEST CIRCUIT AND WAVEFORM

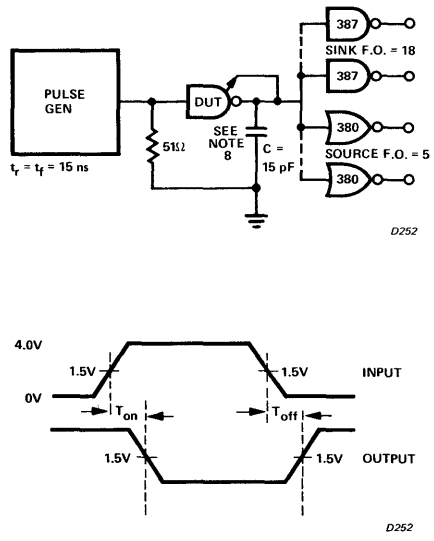
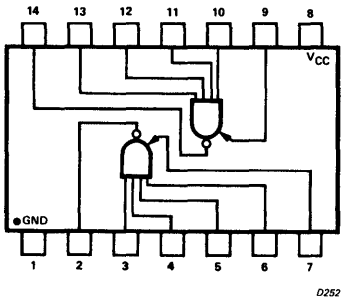


Figure 1

PIN CONFIGURATION



SP356A/659A

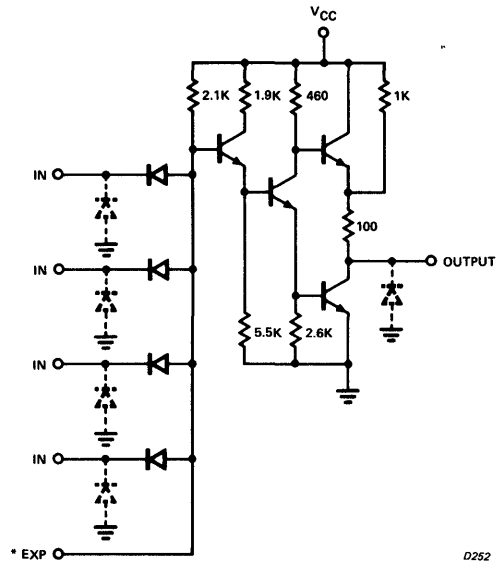
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
for "1"	See Note 6	800	1500		mV
for "0"	See Note 6	300	800		mV
Output Voltage					
"1" Level	I_{out} = –2mA, V_{in} = 0.9V	3.5			V
"0" Level	I_{out} = 45mA, V_{in} = 2.7V			0.6	V
	I_{out} = 27mA, V_{in} = 2.1V			0.4	V
Input Current					
input high	V_{in} = 5.0V		5	25	μA
input low	V_{in} = 0.6V			–2.5	mA
input low (expander)	V_{in} = 1.1V			–2.5	mA
Power Supply Current					
output high	V_{in} = 0V, T_A = 25°C			2.8	mA/gate
output low	V_{in} = 4.0V, T_A = 25°C			22.5	mA/gate
Turn on Delay	See Test Figure 1, T_A = 25°C			60	ns
Turn off Delay	See Test Figure 1, T_A = 25°C			90	ns
Fan-out					
–To sink loads (2.5mA/load)				18	
–To source loads (180μA/load)				11	

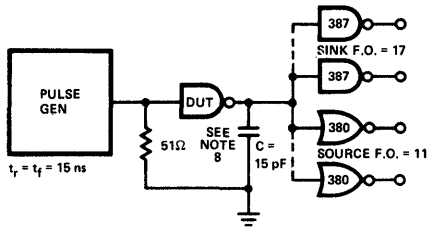
Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

TEST CIRCUIT AND WAVEFORM



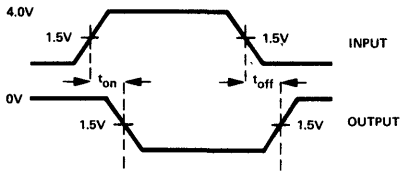
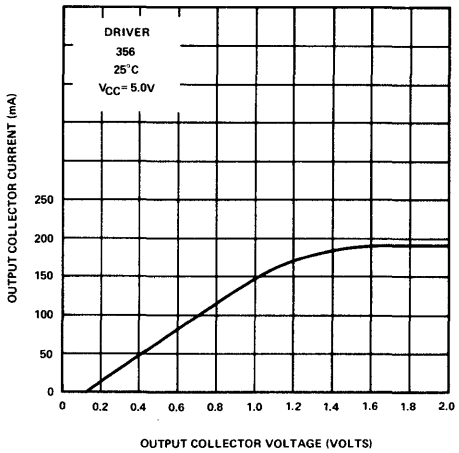
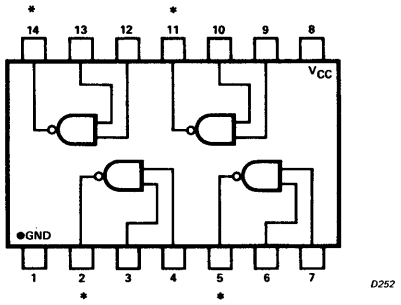


Figure 1

The following curves are normalized, when applicable, to the standard data sheet conditions.



PIN CONFIGURATION



*Open Collector Outputs on SP358A

SP357A/358A

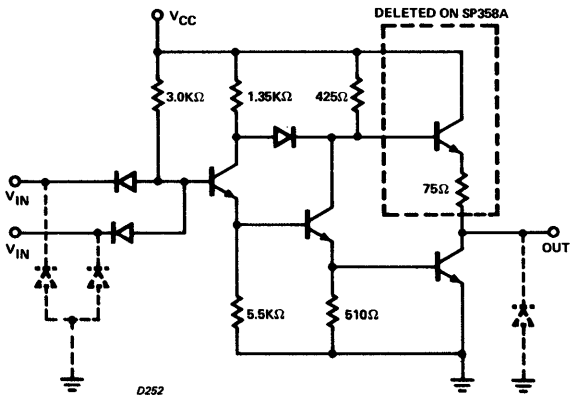
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5, 7 and 9)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
for "1" [357]	See Note 6	800			mV
for "0"	See Note 6	300			mV
Output					
"1" Level Leakage [358]	V_{in} = .9V, V_{out} = 5.0V			100μA	
"1" Level Voltage [357]	V_{in} = .9V, I_{out} = –2.0mA	3.5			V
"0" Level Voltage	V_{in} = 2.1V, I_{out} = 70mA			.4	V
	V_{in} = 2.7V, I_{out} = 100mA			.6	V
Input Current					
Input high	V_{in} = 5.0V			25	μA
Input low	V_{in} = .6V			–2.5	mA
Power Supply Current					
Output High	V_{in} = 0V, T_A = 25°C			3.5	mA/gate
Output Low	V_{in} = 4.0V, T_A = 25°C			18.5	mA/gate
Turn-on Delay	See Test Figure 1, T_A = 25°C			50	ns
Turn-off Delay [357]	See Test Figure 1, T_A = 25°C			50	ns
Fan-out					
–To source load (180μA/load)				11	
–To sink load (2.5mA/Load)				40	

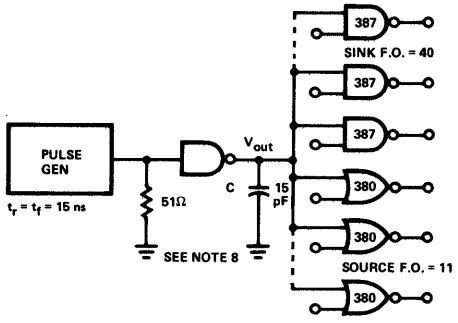
Typical Values are for T_A = 25°C. See Page 3 for Notes.

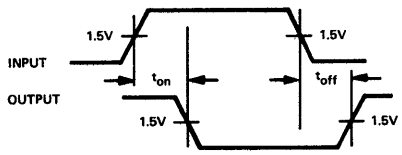
SCHEMATIC DIAGRAM



Component Values are Typical

TEST CIRCUIT AND WAVEFORM



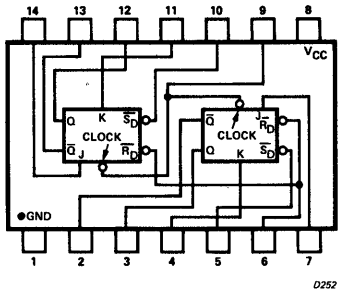


D252

Figure 1

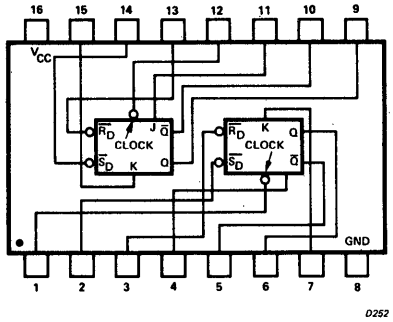
PIN CONFIGURATION

DUAL J-K BINARY



321A

DUAL J-K BINARY



322B

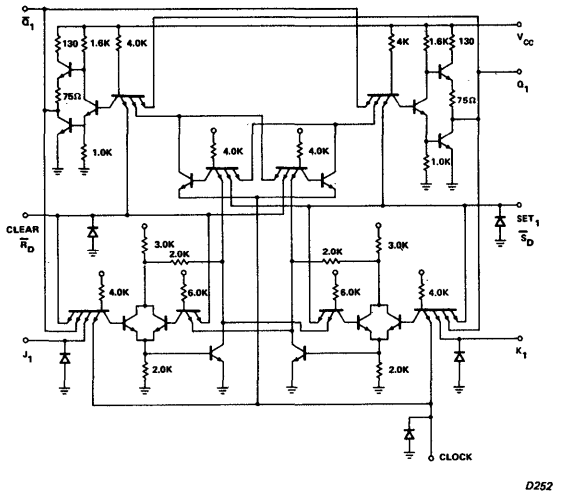
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage					
"1" Level	I_{out} = -1.65mA	3.5			V
"0" Level	I_{out} = 12.5mA			0.6	V
	I_{out} = 7.5mA			0.4	V
Input Current					
input high					
(321) C and $\overline{R_D}$	V_{in} = 5.0		20	100	μA
(321) $\overline{S_D}$	V_{in} = 5.0		10	50	μA
(321) J and K	V_{in} = 5.0		5	25	μA
(322) C, $\overline{R_D}$ and $\overline{S_D}$	V_{in} = 5.0		10	50	μA
(322) J and K	V_{in} = 5.0		5	25	μA
input low					
(321) C and $\overline{R_D}$	V_{in} = 0.6			-6.2	mA
(321) $\overline{S_D}$	V_{in} = 0.6			-3.1	mA
(321) J and K	V_{in} = 0.6			-1.6	mA
(322) C, $\overline{R_D}$ and $\overline{S_D}$	V_{in} = 0.6			-3.1	mA
(322) J and K	V_{in} = 0.6			-1.6	mA
Power Supply Current	V_{in} = 4.0V, T_A = 25°C			28.2	mA/binary
Turn on Delay					
Clocked Mode	See Test Figure 1, T_A = 25°C		50	50	ns
Direct Mode	See Test Figure 2, T_A = 25°C		50	50	ns
Turn off Delay					
Clocked Mode	See Test Figure 1, T_A = 25°C		50	50	ns
Direct Mode	See Test Figure 2, T_A = 25°C		50	50	ns
Fan-out					
-To sink loads (2.5mA/gate)				5	
-To source loads (180μA/gate)				9	

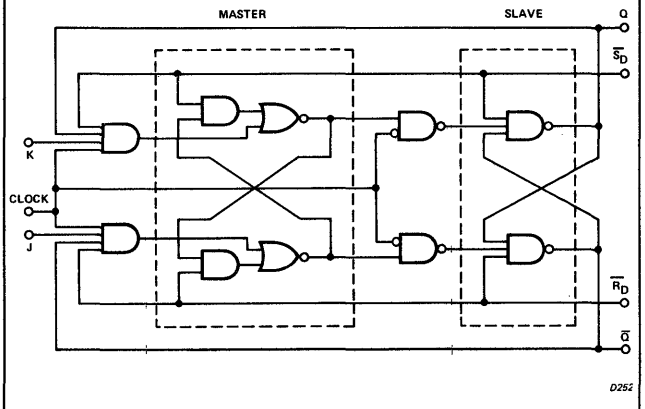
Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

LOGIC DIAGRAM



1/2 of circuit is shown

TRUTH TABLES

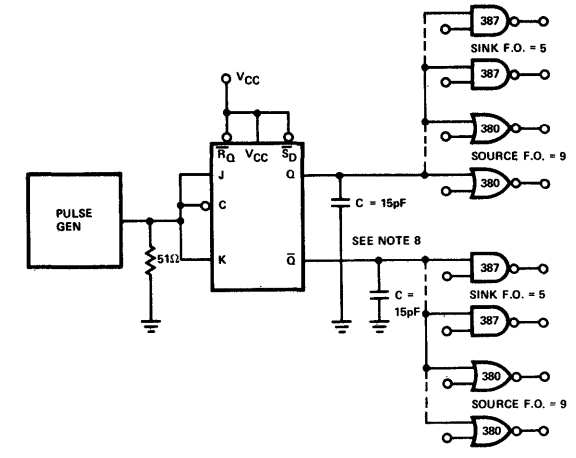
J	K	Q_{n+1}
0	0	Q_n
1	0	1
0	1	0
1	1	$\overline{Q}_n$

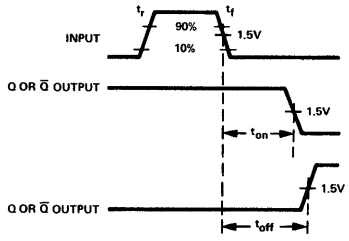
$\overline{S}_D$	$\overline{R}_D$	Q
0	0	*
1	0	0
0	1	1
1	1	No change

*Both Q and $\overline{Q}$ in "1" State.

321 322

TEST CIRCUIT AND WAVEFORMS

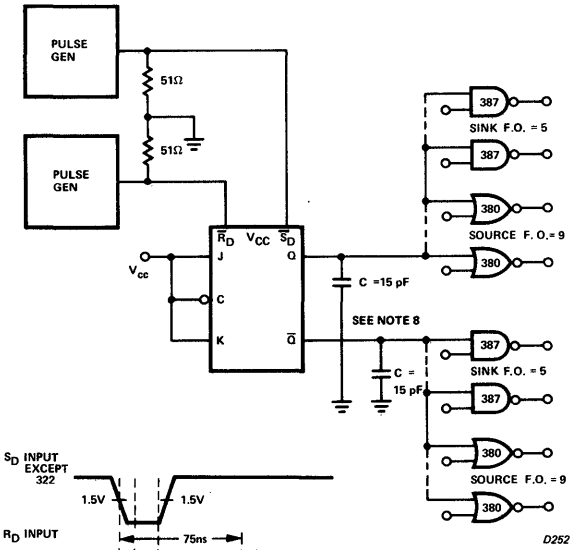




Input Pulse:
Amplitude = 4.0V
Pulse Width = 200ns
$t_r = t_f = 5ns$

Figure 1

TEST CIRCUIT AND WAVEFORMS



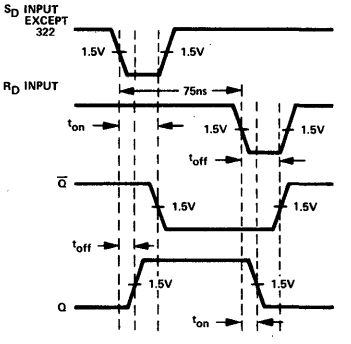
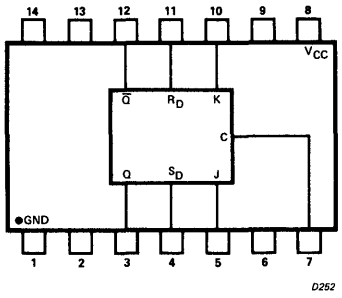


Figure 2

PIN CONFIGURATION



SP620A

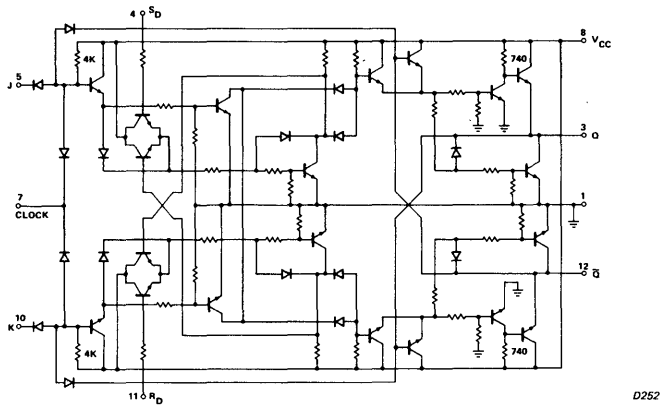
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage					
"1" Level	I_{out} = –2mA	3.8			V
"0" Level	I_{out} = 12mA			0.6	V
	I_{out} = 5mA			0.4	V
Input Current					
input high					
clock	V_{in} = 5.0V			50	μA
J, K	V_{in} = 5.0V			25	μA
R_D, S_D	V_{in} = 2.7V			180	μA
input low					
clock	V_{in} = 0.6V			–1.7	mA
J, K	V_{in} = 0.6V			–1.25	mA
Power Supply Current	V_{in} = 4.0V, T_A = 25°C			38.0	mA
Turn on Delay					
clock	See Test Figure 1, T_A = 25°C		55	100	ns
preset	See Test Figure 2, T_A = 25°C		65	150	ns
Turn off Delay					
clock	See Test Figure 1, T_A = 25°C		90	150	ns
preset	See Test Figure 2, T_A = 25°C		95	175	ns
Fan-out					
–To sink loads (2.5mA/gate)				4	
–To source loads (180μA/gate)				11	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values Shown are Typical

SP620A

TRUTH TABLES

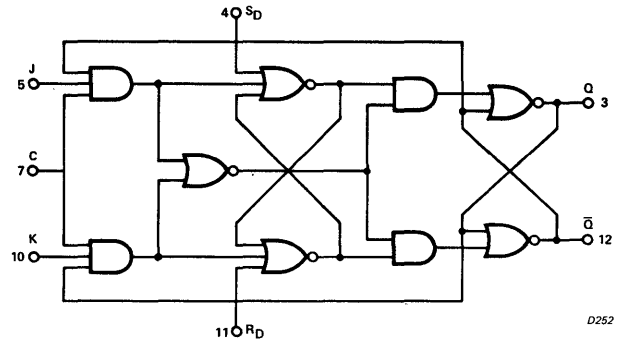
J	K	Q
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

S_D	R_D	Q
0	0	Q
0	1	0
1	0	1
1	1	No Change

Synchronous inputs
at clock time

620A

LOGIC DIAGRAM



TEST CIRCUIT AND WAVEFORM

CLOCK TURN ON/TURN OFF DELAY

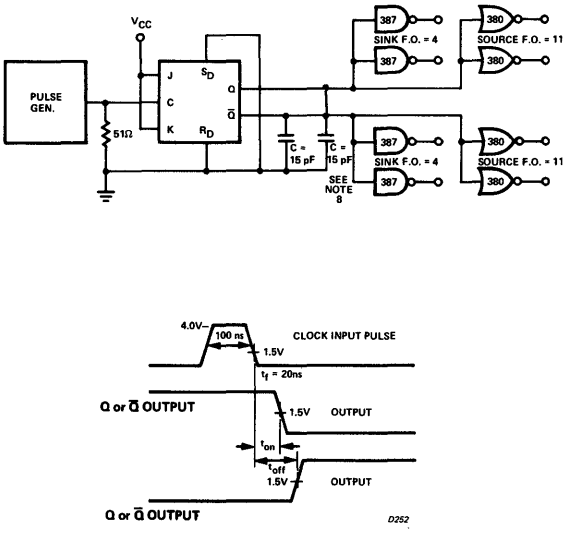


Figure 1

TEST CIRCUIT AND WAVEFORM

PRESET TURN ON/TURN OFF DELAY

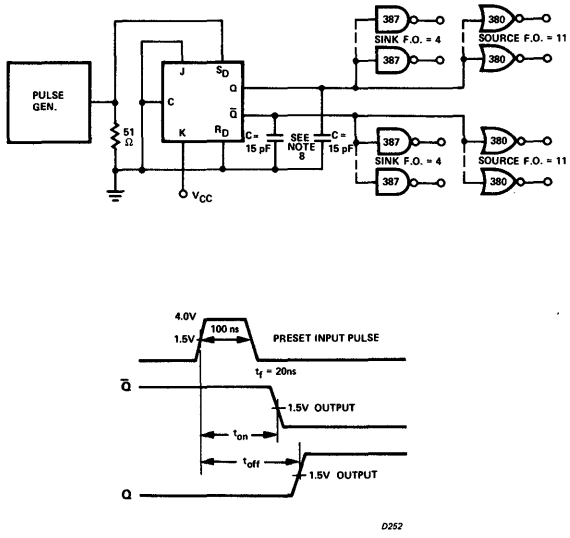
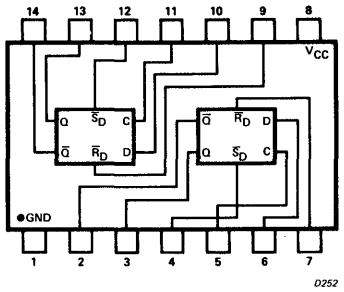


Figure 2

PIN CONFIGURATION



SP328A

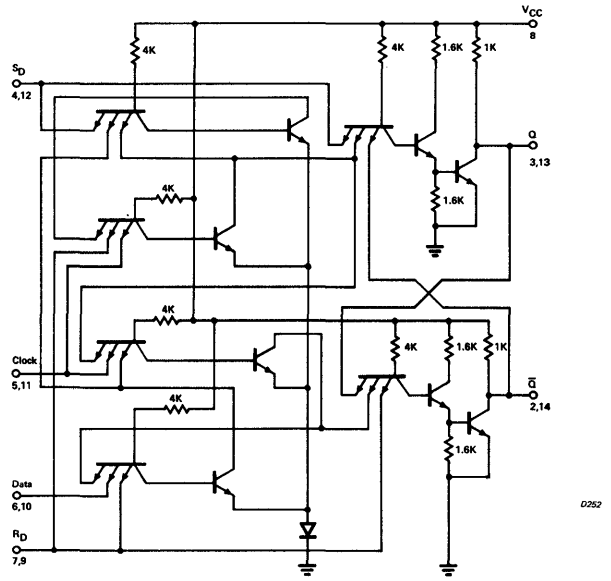
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage					
"1" Level	I_{out} = –1.08mA	3.5			V
"0" Level	I_{out} = 17.5mA			0.6	V
	I_{out} = 7.5mA			0.4	V
Input Current					
input high					
clock	V_{in} = 5.0V		20	50	μA
data	V_{in} = 5.0V		10	25	μA
$\overline{SD}$	V_{in} = 5.0V		20	50	μA
$\overline{RD}$	V_{in} = 5.0V		30	75	μA
input low					
clock	V_{in} = 0.6V			–3.2	mA
data	V_{in} = 0.6V			–1.6	mA
$\overline{SD}$	V_{in} = 0.6V			–3.2	mA
$\overline{RD}$	V_{in} = 0.6V			–4.8	mA
Power Supply Current	V_{in} = 5.0V, T_A = 25°C		14	19	mA/binary
Turn on Delay	See Test Figure 1, T_A = 25°C		25	75	ns
Turn off Delay	See Test Figure 1, T_A = 25°C		30	75	ns
Input Pulse Width for clock, $\overline{SD}$ and data		40			ns
Fan-out					
–To sink loads (2.5mA/load)				7	
–To source loads (180μA/load)				6	

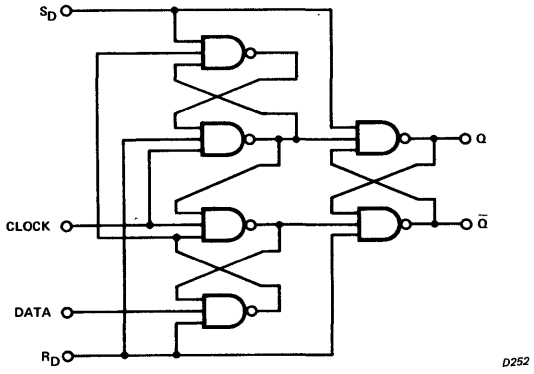
Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

LOGIC DIAGRAM



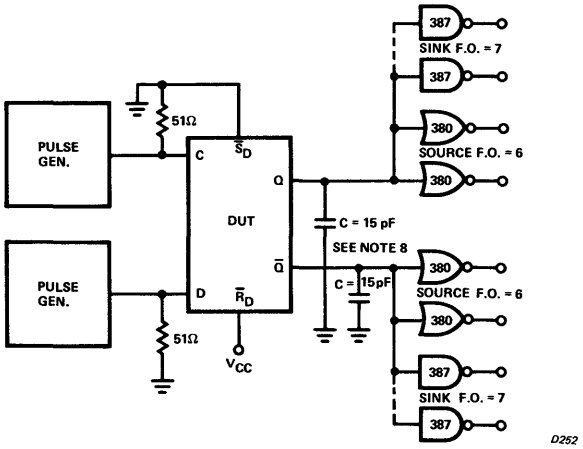
TRUTH TABLES

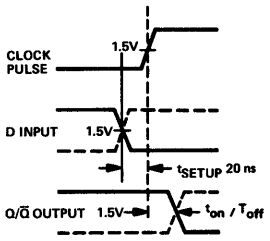
D_n	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1
$\overline{S}_D$	$\overline{R}_D$	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state

n is time prior to clock
n+1 is time following clock

TEST CIRCUIT AND WAVEFORM

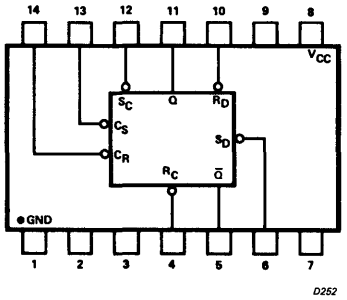




Clock Pulse:
Amplitude = 4.0V, P.W. = 200ns, $t_r = t_f$ = 5ns, f = 2 MHz.
D Input:
Amplitude = 4.0V, P.W. = 500ns, $t_r = t_f$ = 5ns, f = 1 MHz.

Figure 1

PIN CONFIGURATION



SP629A

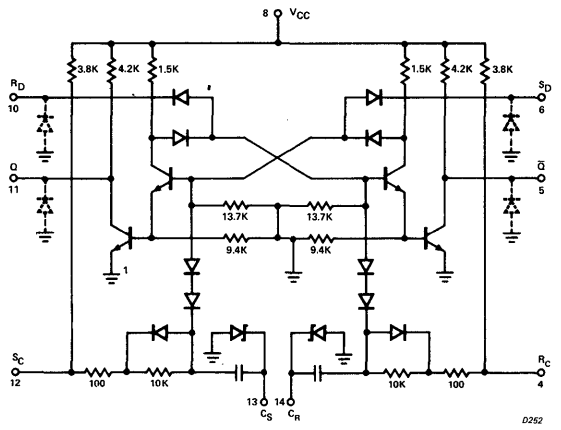
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage					
"1" Level	I_{out} =-200μA, Driven Input	3.8			V
"0" Level	I_{out} = 20mA, Driven Input			0.6	V
	I_{out} = 12.5mA Driven Input			0.4	
Input Current					
input high					
S_D, R_D, clock	V_{in} = 5.0V			25	μA
S_C, R_C	V_{in} = 5.0V			25	μA
input low					
S_D, R_D, S_C, R_C	V_{in} = 0.6V			-2.5	mA
Clock Effective Capacitor			75		pF
Power Supply Current	V_{in} = 5.0V, T_A = 25°C			10	mA
Turn on Delay					
clocked	See Test Figure 1, T_A = 25°C			100	ns
direct	See Test Figure 2, T_A = 25°C			100	ns
Turn off Delay					
clocked	See Test Figure 1, T_A = 25°C			100	ns
direct	See Test Figure 2, T_A = 25°C			100	ns
Fan-out					
–To sink loads (2.5mA/load)				8	
–To source loads (180μA/load)				1	

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



Component Values are Typical

629A

TRUTH TABLES

629A

S_C	R_C	Q
0	0	?
0	1	1
1	0	0
1	1	No Change

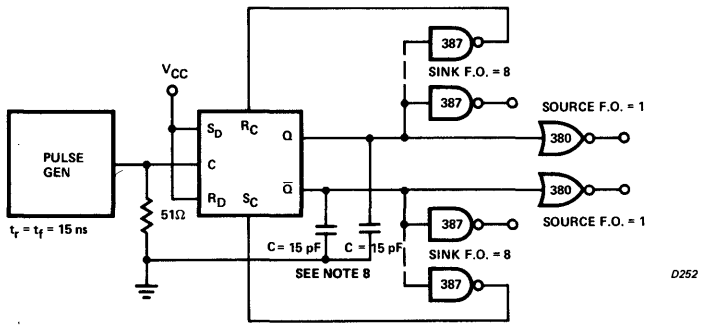
CLOCK SET/RESET

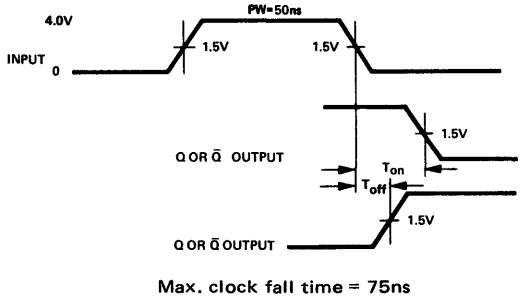
S_D	R_D	Q
0	0	*
0	1	1
1	0	0
1	1	No Change

DIRECT SET/RESET

*Both Q and Q̄ remain in "1" state until S_D or R_D rises.

TEST CIRCUIT AND WAVEFORM

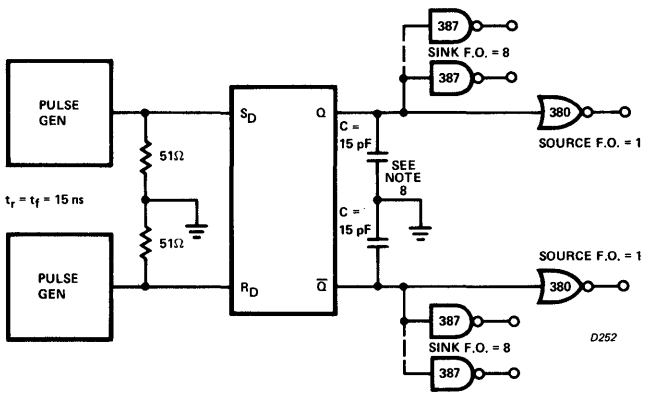


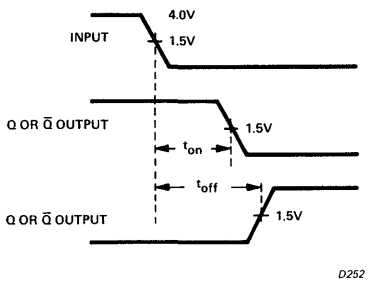


Max. clock fall time = 75ns

Figure 1

TEST CIRCUIT AND WAVEFORM

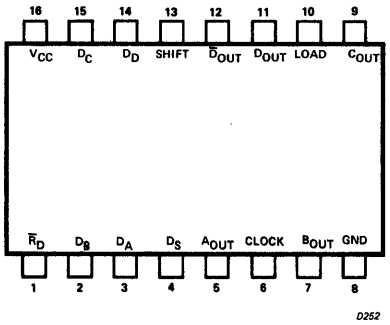




Max. clock fall time = 75ns

Figure 2

PIN CONFIGURATION



SP3271B

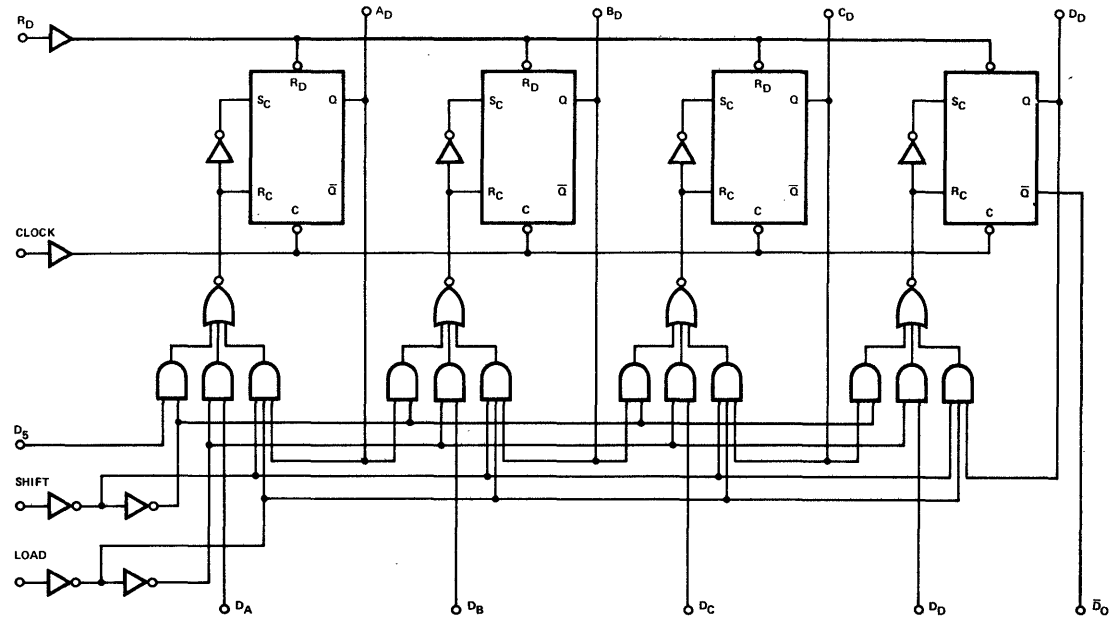
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5, 7 and 9)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTICS	TEST CONDITIONS INPUTS					OUTPUTS	LIMITS			UNITS
	Load	Shift	Data Inputs	Clock	Reset		Min.	Typ.	Max.	
Output Voltage										
"1" Level	2.1V	0.9V	2.1V	Pulse	2.1V	-1.08mA	3.5			V
"0" Level	2.1V	0.9V	0.9V	Pulse	2.1V	15mA			0.4	V
	2.7V	0.9V	0.9V	Pulse	2.7V	25mA			0.6	V
Input Current										
"0" Level										
load	0.6V						-0.1		-1.2	mA
shift		0.6V					-0.1		-1.2	mA
data input			0.6V				-0.1		-1.2	mA
clock				0.6V			-0.1		-1.2	mA
reset					0.6V		-0.1		-1.2	mA
"1" Level										
load	5.0V								25	μA
shift		5.0V							25	μA
data input			5.0V						25	μA
clock				5.0V					25	μA
reset					5.0V				25	μA
Power Supply Current										
All Bits "0"	0V	0V	0V	0V	0V				90	mA
Turn-on Delay										
All Binaries	See Test Figure 1, T_A = 25°C								60	ns
Turn-off Delay										
All Binaries	See Test Figure 1, T_A = 25°C								60	ns
Clock "1" Interval	See Test Figure 1, T_A = 25°C						30			ns
Transfer Rate										
(Shift and Parallel Entry)	See Test Figure 1, T_A = 25°C						10			MHz
Shift or Load Set-up Time								30		ns
Data Set-up Time								30		ns

Typical Values are for T_A = 25°C. See Page 3 for Notes.

SCHEMATIC DIAGRAM



TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
HOLD	0	0
PARALLEL ENTRY	1	0
SHIFT RIGHT	0	1
SHIFT RIGHT	1	1

TEST CIRCUIT AND WAVEFORMS

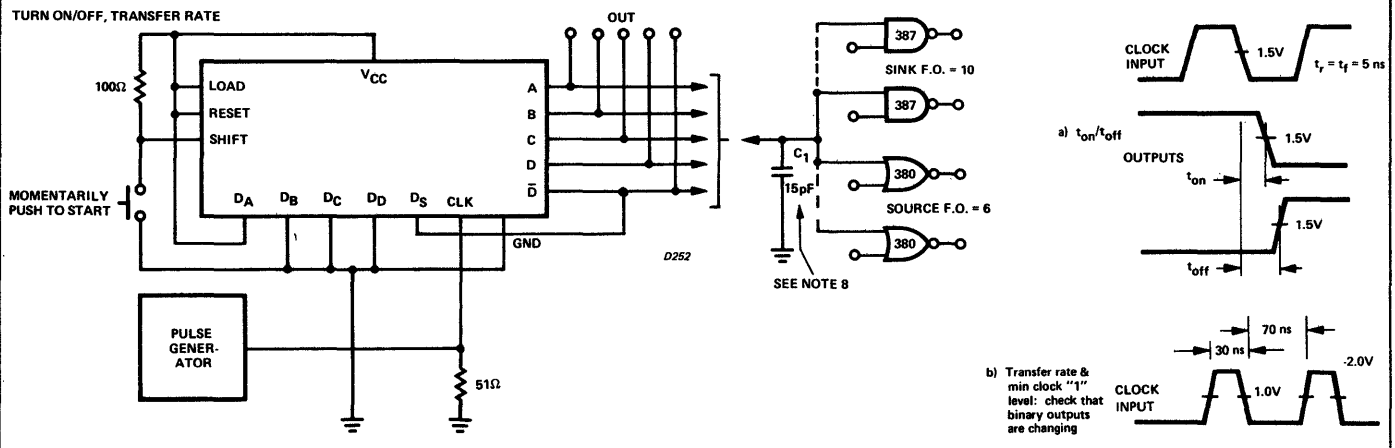
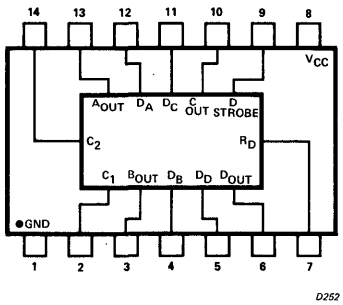


Figure 1

PIN CONFIGURATION



SP3280A/SP3281A

ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

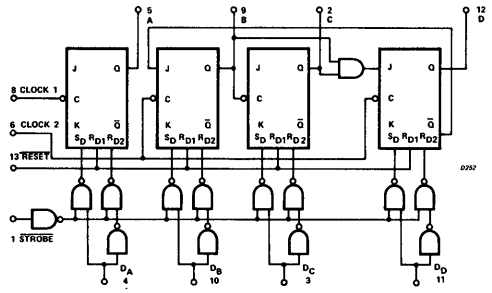
Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS						LIMITS			
	Inputs									
	Data Strobe	Data Inputs	Reset	Clock 1	Clock 2	Outputs	Min	Typ	Max	Units
"1" Output Voltage	0.9V	2.1V	2.1V		Output A	-1.08mA	3.5			V
"0" Output Voltage	0.9V	0.9V	2.1V		Output A	7.5mA			0.4	V
	0.9V	0.9V	2.1V		Output A	12.5mA			0.6	V
"0" Input Current										
Data Inputs		0.6V							-1.2	mA
Clock 1				0.6V					-3.2	mA
Clock 2 (BCD)					0.6V				-3.2	mA
Clock 2 (Binary)					0.6V				-1.6	mA
Reset			0.6V						-3.2	mA
Strobe	0.6V								-3.2	mA
"1" Input Current										
Data Inputs		5.0V							25	μA
Reset			5.0V						50	μA
Clock 1				5.0V					50	μA
Clock 2 (BCD Counter)					5.0V				100	μA
Clock 2 (Binary Counter)					5.0V				50	μA
Strobe	5.0V								25	μA
Power Supply Current	0V	0V	0V	0V	0V				52	mA
Clock Mode T_{on} Delay (any bit)	See Test Figure 1, T_A = 25°C								50	ns
Clock Mode T_{off} Delay (any bit)	See Test Figure 1, T_A = 25°C								50	ns
DATA/STROBE T_{on} Delay (any bit)	See Test Figure 2, T_A = 25°C								50	ns
DATA/STROBE T_{off} Delay (any bit)	See Test Figure 2, T_A = 25°C								50	ns
Toggle Rate	See Test Figure 3, T_A = 25°C						15	25		MHz
STROBE Hold Time		2.7V	2.7V	2.7V	Output A			20	50	ns
RESET Hold Time		2.7V	2.7V	2.7V	Output A			20	50	ns

Typical Values are for T_A = 25°C. See Page 3 for Notes.

LOGIC DIAGRAM

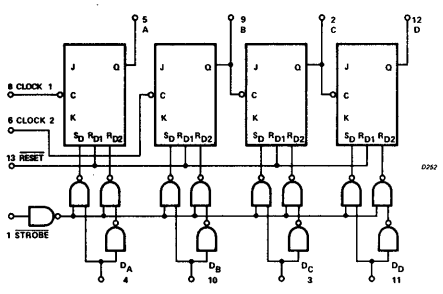
BCD DECADE COUNTER



SP3280A

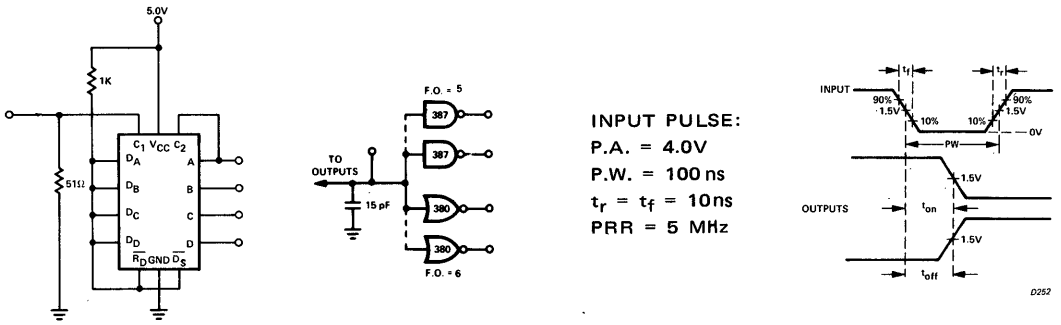
LOGIC DIAGRAM

4-BIT BINARY COUNTER



SP3281A

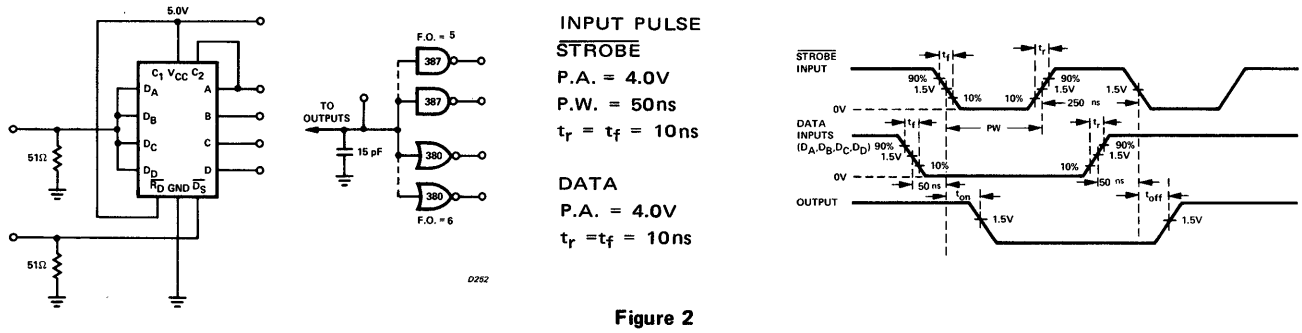
TEST CIRCUIT AND WAVEFORM(Clock Mode T_{on}/T_{off} Delay)



INPUT PULSE:
P.A. = 4.0V
P.W. = 100 ns
$t_r = t_f$ = 10ns
PRR = 5 MHz

Figure 1

TEST CIRCUIT AND WAVEFORM(Data/$\overline{\text{Strobe}}$ T_{on}/T_{off} Delay)

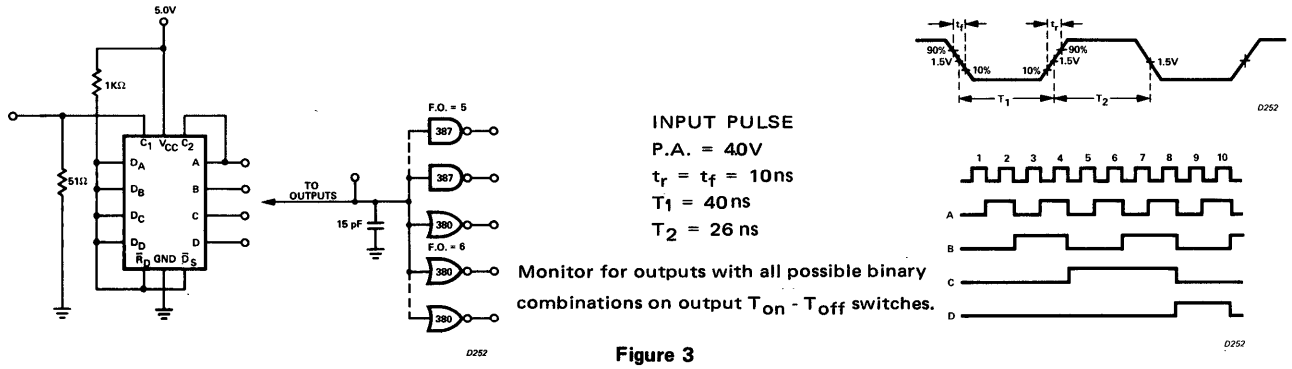


INPUT PULSE
$\overline{\text{STROBE}}$
P.A. = 4.0V
P.W. = 50ns
$t_r = t_f$ = 10ns

DATA
P.A. = 4.0V
$t_r = t_f$ = 10ns

Figure 2

TEST CIRCUIT AND WAVEFORM(Toggle Rate)

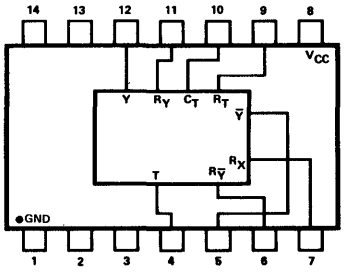


INPUT PULSE
P.A. = 4.0V
$t_r = t_f$ = 10ns
T_1 = 40ns
T_2 = 26 ns

Monitor for outputs with all possible binary combinations on output T_{on} - T_{off} switches.

Figure 3

PIN CONFIGURATION



SP362A D252

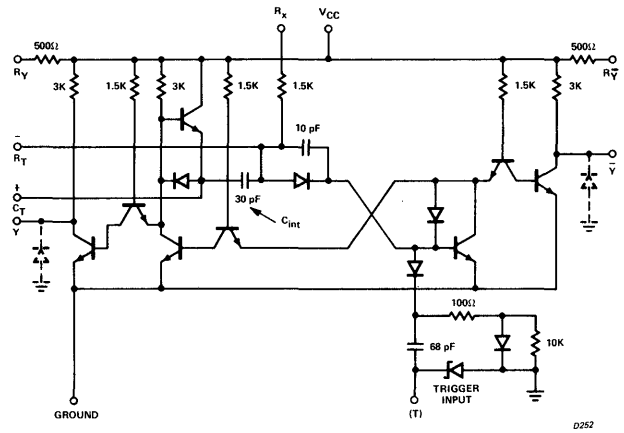
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5 and 7)

Standard Conditions: V_{CC} = 5.0V, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Noise Immunity					
for "0"	See Note 6	800	1000		mV
for "1"	See Note 6	800	1200		mV
Output Voltage					
"1" Level	I_{out} = 360μA (Y and $\overline{Y}$)	3.5			V
"0" Level	I_{out} = 12.5mA (Y and $\overline{Y}$)		0.4	0.6	V
	I_{out} = 7.5mA (Y and $\overline{Y}$)		0.3	0.4	V
Trigger Input Current					
input high	V_{in} = 5.0V			10	μA
input low	V_{in} = 0V		100		μA
Turn off Delay (Y)	See Test Figure 1, I_{out} = 360μA T_A = 25°C		45	75	ns
Turn or Delay ($\overline{Y}$)	See Test Figure 1, I_{out} = 12.5mA T_A = 25°C		35	55	ns
Power Supply Current Y_{out} = 1	R_X to 5.0V, R_T = 0V, T_A = 25°C			19.0	mA
Fan-out					
–To sink loads (2.5mA/load)				5	
–To source loads (180μA/load)				2	

Typical Values are for T_A = 25 C. See Page 3 for Notes.

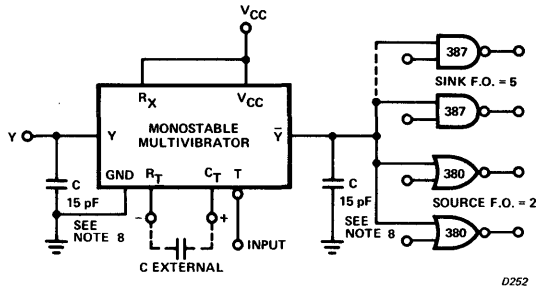
SCHEMATIC DIAGRAM



Component Values are Typical

D252

TEST CIRCUIT AND WAVEFORM



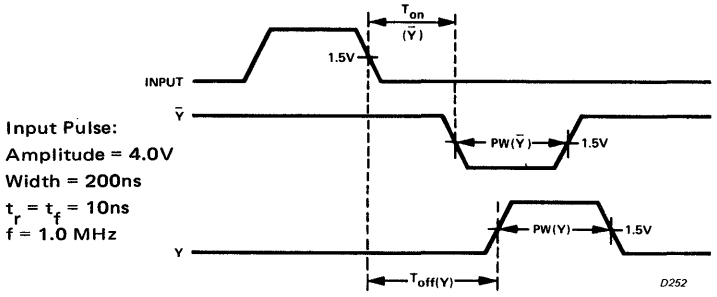


Figure 1

Use the following equations to obtain a desired pulse width:

A. with internal resistor R_x connected to V_{cc}:

$$PW \approx (0.85)\ (C_x + C_{int})\ (10^{-3}\ sec/\mu F)$$

B. with external resistor R_x' ($> 1k\Omega$) paralleled with internal resistor R_x connected to V_{cc}:

$$PW \approx \frac{(0.85)\ (C_x + C_{int})\ (R_x')\ msec/\mu F}{1.5k + R_x'}$$

C. with external resistor R_x' ($0.5k\Omega < R_x' < 4.7k\Omega$) connected between R_T and V_{cc}, internal resistor R_x not connected:

$$PW \approx \frac{(0.85)\ (C_x + C_{int})\ (R_x')\ msec/\mu F}{1.5k}$$

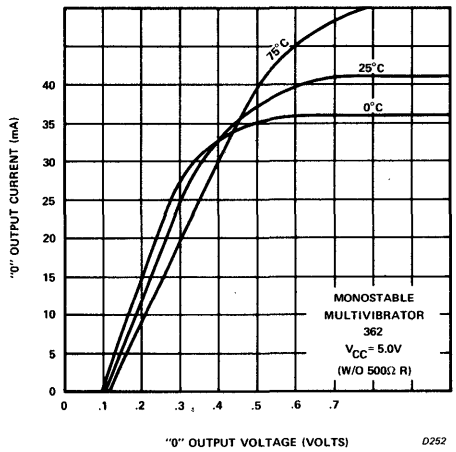
where:

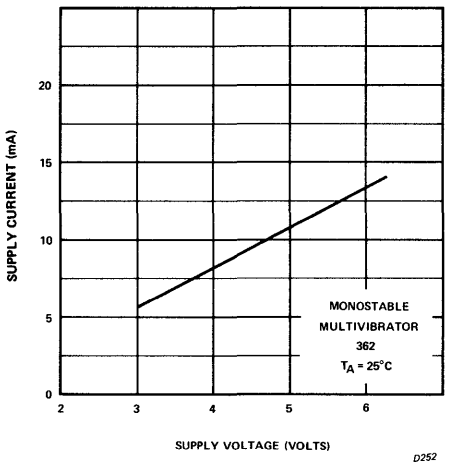
PW = pulse width. Pulse width tolerance using the internal resistor R_x is about ±25% (unit to unit variations). Using external timing resistor R_x', a tolerance of less than ±10% may be obtained.

C_{int} = internal capacitance, typically 30 pF.

C_x = external capacitance in microfarads, connected between C_T and R_T. The positive (+) side of C_x must be tied to C_T.

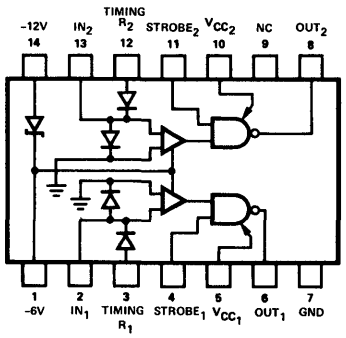
R_x' = external resistor connected between R_T and V_{cc}.





ZERO CROSSING DETECTOR
SP363A Dual

PIN CONFIGURATION



SP363A

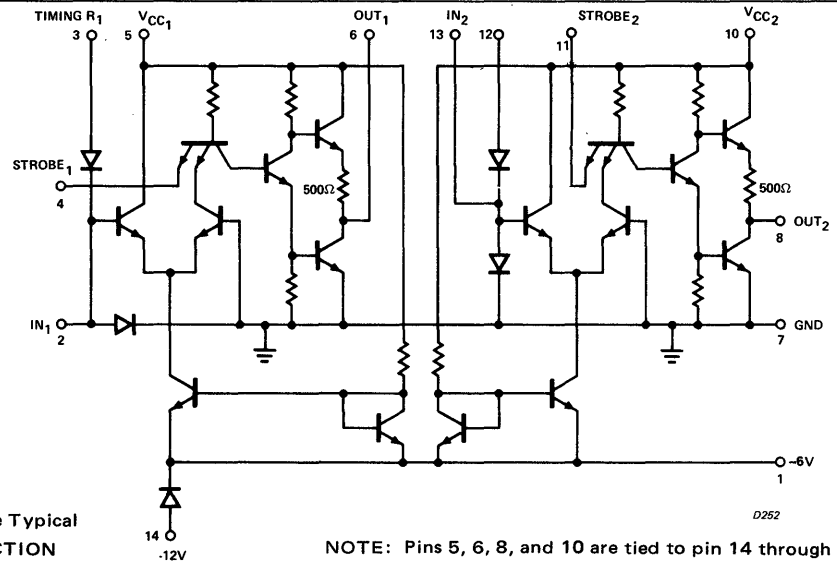
ELECTRICAL CHARACTERISTICS (Notes 1, 2, 3, 5, 7 and 10)

Standard Conditions: $V_{CC_1} = V_{CC_2} = 5.0V$, $V_1 = V_{14} = -6V$, T_A = Operating Temperature Range (Unless Noted)

CHARACTERISTIC	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage					
"1" Level	V signal = –30mV, $I_{out} = -400\mu A$	3.5			V
"0" Level	V signal = +30mV, I_{out} = 12.5mA			.6	V
	V_{signal} = +30mV, I_{out} = 7.5mA			.4	V
Input Current	V signal = Note 9, V strobe = 5.0V,				
Input High — Strobe	$V_7 = V_3 = V_{12}$			25	μA
Signal	V signal = 100mV			100	μA
Input Low — Strobe	V signal = V_{CC} through 10KΩ resistor, V strobe = 0.6V			–1.0	mA
Input Voltage-Timing R	$V_7 = V_2 = V_{13}$, I_3 = 1mA, I_{12} = 1mA,			1	V
Uncertainty Region-Signal				±30	mV
Icc/Detector	$V_7 = V_3 = V_{12}$, Note 9, $T_A = 25°C$			6.5	mA
Turn on Delay					
Detector	See Test Figure 1, $T_A = 25°C$			85	ns
Strobe to Output	See Test Figure 2, V signal = V_{CC} through 10KΩ resistor, $T_A = 25°C$			50	ns
Turn off Delay					
Detector	See Test Figure 1, $T_A = 25°C$			65	ns
Strobe to Output	See Test Figure 2, V signal = V_{CC} through 10KΩ resistor, $T_A = 25°C$			50	ns
Fan-out					
To Sink Loads (2.5mA/load)				5	
To Source Loads (180μA/load)				2	

Typical Values are for $T_A = 25°C$. See Page 3 for Notes.

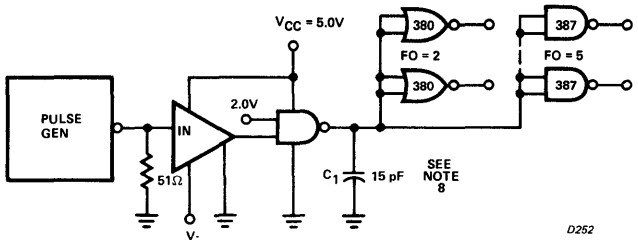
SCHEMATIC DIAGRAM

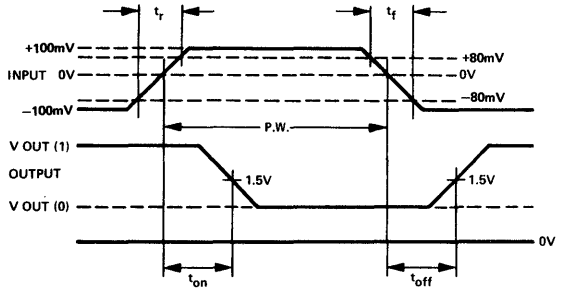


Component Values are Typical
PIN 3 — NO CONNECTION

NOTE: Pins 5, 6, 8, and 10 are tied to pin 14 through isolation diodes.

TEST CIRCUIT AND WAVEFORM





Input Pulse:

V_{IN}

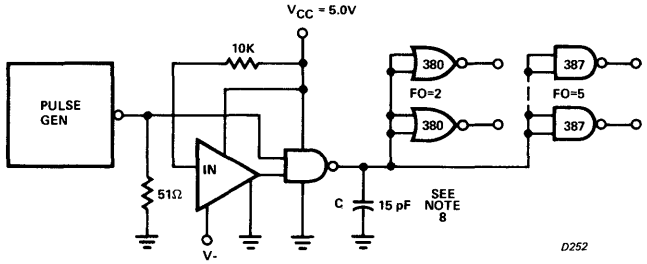
Pulse Width = 350ns at 50% Points

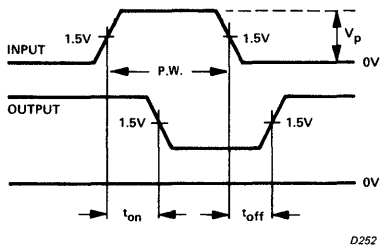
$t_r = t_f = 10ns$

Amplitude = ±100mV

Figure 1

TEST CIRCUIT AND WAVEFORM





Input Pulse:

V_{IN}

Pulse Width = 200ns at 50% Points

$t_r = t_f = 10ns$

Amplitude V_p = 4.0V

Figure 2

Section 3
Applications Information

HOW TO DESIGN WITH UTILOGIC II

Information in this section gives examples of efficient system design with UTILOGIC II integrated circuits. The use of the characterization curves presented earlier for each UTILOGIC II circuit will be demonstrated here.

Interfacing is discussed, including the interconnecting of UTILOGIC II and other circuit types. Typical interfacing techniques are illustrated.

Some of the features of UTILOGIC II that make the family especially interesting to the systems engineer are:

1. High noise immunity, a major design consideration where application may be in high ambient noise environments that are encountered in industrial control equipment, computer peripherals, etc.
2. Low output impedance, essential for good noise immunity, also provides high DC fan-out capabilities. Switching times are relatively unaffected by the increased load capacitance associated with high fan-outs or long inter-connecting lines.
3. Single power supply to provide economy in power supply costs. Tolerance to voltage variations (±10 percent) permit the use of simply regulated supplies for further economy.
4. Availability of OR, AND, NOR and NAND logic functions permits straightforward design approaches which means shorter design times and lower package count.
5. Direct interface of UTILOGIC II to TTL MSI devices ensures that the latest complex functional arrays are available to the designer along with the economy, reliability and simplicity of the UTILOGIC II logic elements.

All members of the UTILOGIC II family have built-in protection against damage produced by momentary short circuit conditions, valuable during debugging or trouble-shooting procedures. Any input or output connection of any UTILOGIC II element may be connected to the input, output, supply voltage, or ground connection of any other UTILOGIC II element momentarily, without producing damage to either circuit. It is not recommended that UTILOGIC II elements be connected so that they produce conditions designated as abnormal for periods of time that can be measured in seconds. If the devices are required to operate for extended periods of time under other than recommended conditions, precautions should be taken to limit the current to safe values within the device's dissipation capabilities.

GENERAL DESIGN CONSIDERATIONS

The normal good design practices that are commonly used in layout of networks of any digital circuit family should also be applied to UTILOGIC II networks. Although all of the UTILOGIC II elements have excellent noise margins, any circuit, discrete or integrated, will produce erroneous results if the noise levels become high enough. As in any system, ground, DC distribution, and noise problems should be considered from the very beginning of the design.

A major consideration with integrated circuits is the higher packaging density, as compared to discrete devices. For example, a printed circuit board that held 3 or 4 discrete flip-flops can now hold 30 to 40 integrated flip-flops; the design of the DC and ground distribution systems must allow for the corresponding current increases. DC and ground lines should be kept as short as possible and of adequate cross-section, and the use of tantalum or other high-frequency type by-pass capacitors is recommended.

The effect of the high circuit density on system cooling requirements and the increased possibility of localized hot spots must also be considered.

Signal leads should be kept as short as possible to minimize cross-talk, noise pick-up, and propagation time down the wire.

Generally, it becomes important to terminate signal lines when the signal propagation time down the wire becomes appreciable as compared to the signal transition times. Since UTILOGIC II rise and fall times are on the order of 10 ns, lead lengths of 2 to 3 feet should not require any special termination. The simple termination network shown in Figure 1 has been found effective at any UTILOGIC II input with lines up to 12 feet in length, and with coaxial cable as well as open wire.

When using a clock distribution system which has several branches, all flip-flops should be driven from the same relative position on the branches. In addition, the clock drivers should be as close as possible to the flip-flops that they will trigger so that the driving lines are short and uniform in length.

TERMINATION NETWORK

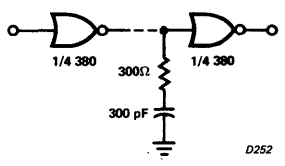


Figure 1

UTILOGIC II CIRCUITS

UTILOGIC II inputs are classified as sink loads and source loads by the direction of current flow required to activate the input. The input of the OR and NOR gates are called source loads because they must be driven by a source of current, e.g., the output of a UTILOGIC II element in the "1" state or a connection to the positive supply. The inputs of the AND gates, NAND gates and the Binary are called sink loads because they must be driven from a current sink: for example, the output of a UTILOGIC II element in the "0" state or a connection to ground.

In this publication, and all other UTILOGIC II literature, the convention of positive logic, i.e., the positive level is "1", has been assumed. If the negative logic notation is assumed (most negative level is "1"), the AND, OR, NAND and NOR gates become OR, AND, NOR and NAND respectively.

The characteristic curves presented in the various sections are designed to allow the system designer to predict system performance characteristics for various operating conditions. In general, characteristics are normalized to the conditions of the specification sheets. The use of the normalized characteristic is a definite design aid in that it is usually the change in the characteristic as a result of a change in the parameter that is of interest.

As long as the effects, e.g.,

$$\frac{\partial V_{sat}}{\partial \text{Temp}'}$$

are small, the total effect may be predicted by taking the product of the individual effects.

Throughout the discussion that follows, V_{cc} is assumed to be 5.0V unless otherwise specified.

UTILOGIC II NOR Gates and Expander

The UTILOGIC II NOR gates (314, 370, and 380), Expandable NOR gate (317) and Expander (300), are all derived from the same basic circuit to ensure full compatibility of the Expandable Gates and Expander, and to give all the circuits identical electrical characteristics. However, the 300 and 317 will have longer turn-off delay times (T_2) because of the additional capacitive loading on the expansion input. Turn-on delays (T_1) are not sensitive to this capacitance because the source impedance is low during turn-on.

The 300 Expander circuit is characterized in terms of its operation in conjunction with the 317 Expandable NOR and 333 Expandable OR. The ways in which 300 and 317 (as well as 300 and 333) compatibility is guaranteed are of interest. The expansion forward voltage for the 300 and the expansion input voltage of the 317 are measured under the same conditions, and the same limits are guaranteed. In addition, the 300 input leakage current and the 317 "0" input current specifications guarantee reverse current compatibility. These specifications assure the user that the 300 and 317 or the 300 and 333 combination will have the same DC characteristics as when the 317 or 333 is used alone. AC characteristics are shown later (with the 317 and 333 curves) as a function of the capacitance on the expansion input.

CIRCUIT DESCRIPTION

The UTILOGIC II NOR gate (page 4) may be considered as a derivation of the DTL NOR gate. The input diodes of the DTL NOR were replaced with transistors to decrease the input current to allow larger source fan-out capabilities from the NOR and other circuits in the family. The NOR employs a totem-pole output to obtain low output impedance in both the "1" and "0" states. The switching thresholds are determined by the ratio of the coupling resistance to the pull-down resistance at the base of each switching transistor. The series resistor at the output provides current-limiting should the output become accidentally shorted to ground. The Expandable NOR is implemented by connecting the common emitters of the input transistors to an expansion input. The Expander (page 23) is a dual array of input transistors; thus, the effect of connecting the Expander output to an expansion input is the same as connecting more input transistors in parallel.

Input Characteristics

The Standard UTILOGIC II Source Load is the NOR input. The Standard Source Load may be simulated by a 15 kΩ resistor and 2 series silicon diodes to ground. An unused NOR input should be tied to ground through a resistance of 60 kΩ (or less) or connected in common with a used input on the same circuit. The capacitance of an open input may become charged during prolonged "1" levels at a driven input. When the driven input goes from "1" to "0", the charged capacitance discharges into the input and gives the effect of a slow circuit. Two or more common inputs represent the same DC load as a single input since the "1" input current is determined by the voltage across the coupling resistors and the gain of the input transistors. Neither of these values changes appreciably when inputs are connected in common. The additional capacitance of a commoned input has no measurable effect on switching times. Input voltages should not exceed the supply voltage unless precautions are taken to limit the resulting current to 30mA in the input transistor collector-base junction.

Output Characteristics

A UTILOGIC II NOR gate has a fan-out of 5 sink loads and 11 source loads. All 16 loads may be connected simultaneously because they do not interact. Because the NOR gates employ transistors for both pull-up and pull-down, their outputs cannot be connected with the output of any other independent circuit (collector-logic). Such operation of an active pull-up device with another device may result in ambiguous output voltages and/or excessively high currents if one device should attempt to reach a "1" level while the other is attempting to reach a level "0". However, two NORs may be connected with common inputs and common outputs. In this case, fan-out is doubled and the input loading is two Standard Source Loads.

UTILOGIC II OR Gates

The UTILOGIC II OR gates are compatible on a pin for pin basis with their UTILOGIC II NOR gate counterparts. This simplifies system design, circuit board layout and checkout.

Comparison of the schematics of the UTILOGIC II OR gate (page 8 through 10) and the UTILOGIC II NOR gate (page 4) shows that both types of gates have essentially identical input and output structures; however, the OR gate uses one more transistor to obtain the additional inversion required to produce an OR gate from the basic UTILOGIC II NOR configuration.

UTILOGIC II AND Gates

The UTILOGIC II AND gates 305 and 306 are fabricated from the same basic chip, and therefore have identical electrical characteristics. The internal connection pattern is varied to produce a single 6-input AND gate in the 305, and the dual 3-input AND gates in the 306.

CIRCUIT DESCRIPTION

Schematic diagrams of the UTILOGIC II AND gates are shown on page 13. The multiple-emitter input structure provides the same function as a Diode AND gate. The output-emitter follower provides the current gain necessary for high fan-out, and also reduces the offset voltage associated with Diode AND gates. The emitter follower provides a low output impedance to effect fast response on "0" to "1" transistions and the current gain necessary for source current fan-out. The input transistor and connecting diode provide a low impedance circuit to maintain good response on "1" to "0" transitions.

Input Characteristics

The input of the AND is defined as a standard UTILOGIC II sink load. The standard sink load may be simulated by 2 kΩ resistor with a series silicon diode to the supply voltage. The input impedance of UTILOGIC II AND gates is low enough so that unused inputs may be left open without degrading circuit performance (open inputs are logical "1") however; it is recommended that unused inputs be connected to the used inputs of the circuit. Connecting the unused inputs to used inputs of the same circuit will not increase the circuit loading. The effect of the added capacitance will be negligible.

Output Characteristics

The fan-out of the UTILOGIC II AND gate is 10 to standard UTILOGIC II source loads. The AND gate does not have output current sinking capability; therefore, it cannot drive sink loads. The AND gate can drive any of the UTILOGIC II source loads. The AND gate outputs should not be paralleled with the outputs of any other circuits as in collector logic configurations. However, outputs of AND gates may be connected to increase fan-out if the inputs of the two circuits are in common.

UTILOGIC II NAND Gates and Expander

The UTILOGIC II NAND gates (337, 377 and 387) and diode expander (301) are DTL gates. This is due to the fact that the basic UTILOGIC input structure does not lend itself to implementing the NAND function. The NAND gates are compatible with all other elements in the UTILOGIC II line. In addition, the NAND gates provide a guaranteed interface with Signetics TTL logic elements.

The 301 expander is specified under the same conditions as the gate inputs, thus ensuring that an expanded 337 will have the same input characteristics as the other NAND gates. The 301 may also be used as an expander for the 356 driver element.

CIRCUIT DESCRIPTION

The UTILOGIC II NAND gates (page 17) are modifications of the proven Signetics 600 series circuits. The major change is that the usual 4 kΩ output resistor has been replaced with a 1 kΩ resistor. The use of a passive pull-up permits outputs to be connected in parallel to perform collector logic. Input and output levels are fully compatible with the other UTILOGIC elements and provide a minimum of 800 mV of noise margin in both the "0" and "1" states.

Input Characteristics

The input structure of the NAND gates makes them sink loads. The NAND inputs, like the UTILOGIC II AND inputs, require that the driving gate to be able to sink 2.5 mA for each such load driven. The UTILOGIC OR and NOR gates can therefore drive up to 5 NAND gate inputs. As with the AND gates, the input load of the NAND gates may be simulated by a 2 kΩ resistor in series with a silicon diode to the supply voltage.

Unused inputs may be left open, however, a more conservative design practice suggests connecting the unused inputs to a driven input. In cases where the source load on the driving gate will not permit connecting the unused inputs to a driven input, the unused inputs may be returned to V_{CC}.

The UTILOGIC II NAND gates have two sets of input and output specifications to enable the NAND gates to be used with both UTILOGIC elements and Signetics TTL logic elements. The "1" level input threshold is specified at 2.7 volts for use with UTILOGIC driving elements and 2.1 volts for use with TTL driving elements. This is accomplished by reducing the fan-out at the lower input voltage. The "0" level input current in both cases is within the 2.5 mA maximum.

Output Characteristics

A UTILOGIC II NAND gate has a fan-out of 12 loads and 6 source loads. All 18 loads may be connected simultaneously. The passive 1 kΩ pull-up resistor used in the NAND output structure permits collector logic to be performed by connecting the outputs of up to 5 NAND gates in parallel. The resulting "wired AND" gate can drive one sink load and 6 source loads.

In cases where additional fan-out may be required, NAND gates may be connected in parallel. The fan-out can be doubled by connecting two gates in parallel; however, the input loading is also doubled.

The UTILOGIC II NAND gates can be used to drive Signetics TTL logic elements and complex arrays. When used in conjunction with TTL circuits, the NAND gate sink fan-out is reduced to 12.5 mA at a "0" output voltage of 0.4 volts. In most cases, this will result in a fan-out of 7 to Signetics DCL sink type loads. Refer to the Signetics DCL Handbook for further information on DCL input requirements.

The 600 Series NAND gates, as stated previously, are the same as the UTILOGIC NANDS except for the pull-up resistor which is 4 kΩ instead of the 1 kΩ used in UTILOGIC. Therefore the comments for UTILOGIC NAND* are applicable to 600 series NANDS with this one difference.

Series 600 Inverter

The 690 Inverter has been designed using the same circuit as the 600 NAND gates and provides six inverters in each package.

The circuit description, input and output characteristics are therefore the same as those for the SP600 NAND gates.

UTILOGIC II Buffer Driver

The UTILOGIC II 356 Buffer Driver is shown on page 26. It is intended for driving the clock and RESET lines of the 321 and 322 J-K binaries. The "1" level output impedance of the driver is approximately 150 ohms for output voltages less than one diode drop below V_{CC}. It should also be noted that the use of active outputs for both the "1" and "0" states means that the output of these drivers cannot be connected in parallel with any other element. However, for those cases where high fan-out is required, but absolutely no clock skew can be allowed, two line drivers may be tied in parallel if the inputs also are made common.

The 352 is an open collector variation of the 356. The open collector allows collector logic to be performed in conjunction with the driving capabilities for clock and reset lines.

UTILOGIC II J-K Binaries.

The UTILOGIC II 321 and 322 are dual J-K general purpose binaries with both synchronous and asynchronous inputs. They employ DC level triggering with clocking effected on the negative-going edge of the clock pulse waveform.

CIRCUIT OPERATION

The 321 and 322 have the following output sequence:

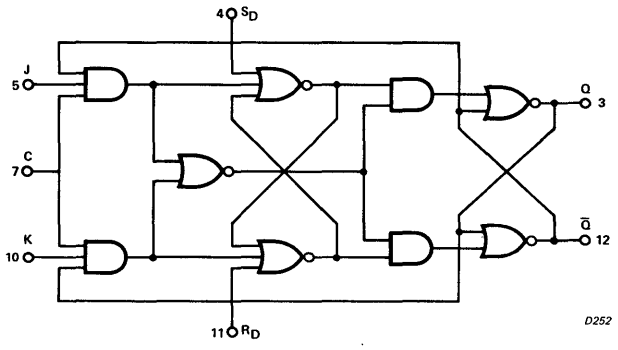
1. With clock pulse low, the logical inputs are disabled and the slave is connected to the master.
2. At the rise of the clock pulse the slave is disconnected from the master and the logical inputs are enabled. Data now enters the master, setting it to the state determined by the logical inputs. The information present at the J and K lines prior to or coincident with the rise of the clock, sets the master FF when the clock reaches a logical "1" level. For reliable operation the original J and K inputs must remain stable during the entire clock "1" interval.

3. At the fall of the clock pulse the logical inputs are disabled to prevent entry of further information and the slave is connected to the master. The slave now takes the state of the master and state of the slave appears at the outputs. The J and K inputs of the 321 and 322 are non-inverting, that is, the flip-flop will be set at "1" when the J input is high and the K input is low. The asynchronous inputs are inverting, that is, actuated by logical "0". The effect of the asynchronous inputs is independent of the state of the clock line.

J-K BINARY ELEMENT – 620A

The 620A is a DC-triggered, master-slave, J-K flip-flop intended for use in systems with a clock rate to 2 MHz. The circuit may be set or reset asynchronously with the S_D and R_D inputs, or switched synchronously by using the J and K inputs together with a clock. When it is switched asynchronously, the 620A behaves as an RS flip-flop. When it is switched synchronously, the circuit acts as a J-K flip-flop. The master and the slave flip-flops are connected by means of two AND gates. When switched synchronously, the rising clock pulse cuts the slave off from the master.

LOGIC DIAGRAM AND TRUTH TABLES



J	K	Q
0	0	$\bar{Q}$
0	1	0
1	0	1
1	1	$\bar{Q}$

S_D	R_D	Q
0	0	$\bar{Q}$
0	1	0
1	0	1
1	1	No change

Synchronous inputs at clock time

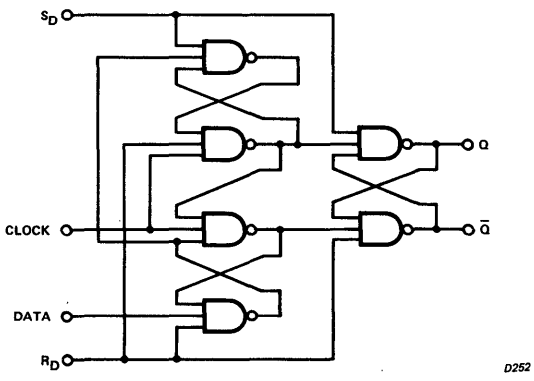
As the clock rises still higher, it allows the logic at the J and K inputs to be set into the master. Then, when the clock returns to its low level, the state of the master is transferred to the slave which, in turn, sets the output levels. The thresholds of the transfer gate and master flip-flop gates are separated by sufficient voltage to guarantee that input and transfer cannot occur simultaneously. This guarantees race-free operation. When the 620A is switched asynchronously, the master and the slave are coupled together and the outputs are set immediately. Setting should be performed with the clock line low. However, in applications such as ripple counting, in which state of the clock line cannot be predicted, setting can be accomplished by lowering the J input while raising S_D or lowering the K input while raising R_D. The J and K inputs should be stable during clock time. If the S_D R_D inputs are not used, they should be tied down. Other unused inputs should be tied to V_{cc}.

The synchronous inputs strictly follow the definition of a J-K flip-flop. The case of S_D R_D both being up will have no immediate effect on the outputs. The input which falls last will control the final state of the flip-flop. Delay through the flip-flop is typically 65 ns. The push-pull output gates minimize switching time degradation under high capacitance loads. The recommended clock pulse width is 200 ns.

D TYPE BINARY 328

The 328 responds to the positive-going edge of the clock pulse. The logic inputs are locked out once the clock is high, thus preventing more than one transition of the binary per clock pulse.

LOGIC DIAGRAM



(2 per package)

TRUTH TABLES

D	Q_{n+1}	$\overline{Q}_{n+1}$
1	1	0
0	0	1

Preset (S_D)	Clear (R_D)	Q
1	1	Q
1	0	0
0	1	1
0	0	+

+Both outputs in 1 state
n is time prior to clock
n+1 is time following clock

RS/T BINARY ELEMENT – 629A

The 629A RS/T Binary element employs capacitively – coupled clock lines for high-speed race free operation. It is intended for use in systems with clock rates to 5 MHz or in counters and shift registers to 10 MHz. Output lines are fully buffered to allow collector logic and for complete assurance that noise on driven lines will not introduce erroneous states in the flip-flop.

TRUTH TABLES

S_C	R_C	Q
0	0	?
0	1	1
1	0	0
1	1	No Change

CLOCKED SET/RESET

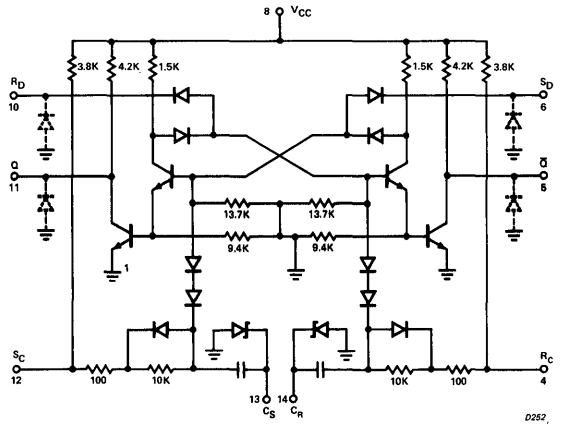
S_D	R_D	Q
0	0	*
0	1	1
1	0	0
1	1	No Change

DIRECT SET/RESET

*Both Q and $\overline{Q}$ remain in "1" state until S_D or R_D rises.

This device has input provision for both clocked (S_C/R_C) and direct (S_D/R_D) operation and features split clock capabilities. Both the clocked and direct inputs are energized by "0" logic levels; that is, they are inverting. The inverting inputs allow implementation of AND or AND-OR control logic with one NAND level (NAND-INVERT = AND). The inverting inputs do not contribute to internal set-up time.

SCHEMATIC DIAGRAM



Component values shown are typical

Logic levels to the S_C/R_C inputs should be stable at the rise of the clock pulse and should remain stable while the clock input is high. Refer to Signetics Application Note AN108 for further usage information.

The fan-out rating for the 600A family elements to the 629A clock line is derived under conditions that assure compliance with the required amplitude and fall time when operated within the power supply, temperature and fan-out ratings for the product line. All unused inputs should be tied to V_{CC}.

362 Multivibrator

The 362 is a one-shot multivibrator with complementary outputs and optional 500-ohm load resistors. The output pulse width can be conveniently adjusted to conform to most one-shot application requirements. The 362 provides high output duty cycle (75%) and complete isolation of the timing stage and the output stage, resulting in good fall time even with wide pulse width. The input pulse width should be at least 50 nanoseconds wide, with a fall time of less than 75 nanoseconds, or 1 volt per 25 ns.

The 362 provides complementary outputs with passive 3k ohm pull-up resistors. An optional 500 ohm pull-up resistor is provided at each output, to be used when driving heavy capacitance loads where rise times must be maintained.

The 362 design employs a 30 pF timing capacitor and an optional 1.5k ohm timing resistor. The output pulse width may be varied by appropriate connection of external R and C at the C_t, R_t, R_y and $R_{\overline{y}}$ terminals.

363 DUAL ZERO CROSSING DETECTOR

The 363 Dual Zero Crossing Detector is a circuit incorporating a differential input and logic gate output. The input amplifier is referenced to zero volts and employs temperature compensation to ensure stable thresholds.

INTERFACING CONSIDERATIONS

GENERAL CONSIDERATIONS

The need to interface UTILOGIC II integrated circuits with discrete component circuitry or with integrated circuits of another family may arise when a UTILOGIC II system or subsystem is added to or must operate with existing hardware. General rules when interfacing are:

1. Inputs to UTILOGIC II source loads must be capable of supplying 180μA input current at the "1" input threshold voltage of at least 2.7 volts.
2. Inputs to sink loads must be capable of sinking 2.5 mA at the "0" voltage (0.6V).
3. A UTILOGIC II output will supply 2 mA at 3.8 volts for NOR and OR gates; it will supply 1.6 mA at 3.8 volts for binaries; and 1.8 mA at 3.8 volts for ANDs.
4. The approximate equivalent circuit for any UTILOGIC II output at "1" is 100 ohms to 4.0 volts. A NOR, OR and binary output will sink 12.5 mA at 0.6 volts or less.
5. The rise and fall times of signals entering a UTILOGIC system should be kept to less than 1μsec to ensure stable operation and avoid oscillation of the gate driving transition of the threshold.

UTILOGIC II AND DTL

A UTILOGIC II-to-Signetics 100 series DTL (DTL in general) interface requires, at most, modification of load definitions. The input resistor of the DTL NAND gate and the UTILOGIC II AND are approximately the same value so that the DTL load is equal to a UTILOGIC II sink load. The "1" and "0" levels at UTILOGIC II outputs are fully compatible with DTL input requirements and vice versa.

SP600 series DTL elements that have passive pull-up outputs generally have fan-outs of 2 to UTILOGIC II source loads. Higher source load fan-out can be obtained by providing 8kΩ of pull-up resistance for each additional source fan-out required. A UTILOGIC II AND gate may be used as buffer for DTL to UTILOGIC II.

Mixed UTILOGIC II – DTL systems should operate with a 5.0 volt power supply; the rules above assume a common power supply.

UTILOGIC II AND RTL

The Resistor-Transistor (grounded-emitter transistor amplifier) logic stage, Figure 2, is often employed as a level translator or general purpose buffer stage since all that is required generally is one transistor and one or two resistors. At these interfaces, the output of a UTILOGIC II element may be treated as a voltage source of 4.0V (less than 100 ohms source impedance). For a typical input current requirement of 0.5 mA, R_{IN} in Figure 21 will be 5 kΩ.

UTILOGIC II AND TTL

The UTILOGIC II NAND gates are designed to interface directly with Signetics TTL integrated circuits. The inputs of the TTL devices in the Signetics DCL family are sink loads of 1.6 mA each. This provides a fan-out of 7 from the NAND gates to DCL sink loads. The output characteristics of the DCL series are a "1" output voltage of 2.8 volts and a "0" output level of 0.4 volts while sinking 16 mA. This gives a fan-out of 6 to NAND inputs.

TTL devices will drive UTILOGIC source load inputs (OR and NOR gates) if a resistor is connected between the TTL output and V_{CC}. The resistor value should be chosen such that it maintains a "1" level output voltage greater than 2.7 volts while supplying sufficient "1" level current to drive the gates. In addition the resistor must be large enough such that it does not require excessive "0" level current sinking capability for the TTL output structure. A reference chart has been included (figure 12 pages 58, 59, 60) for ease of resistor selection.

When intermixing UTILOGIC II and the higher speed TTL circuits in the same system, care should be taken to provide adequate local power supply bypassing. In addition, greater care should be taken in circuit board layout to minimize the unwanted coupling of the rise and fall time pulses associated with the TTL switching speeds. The recommended practice for use of TTL devices is to decouple the power supply with a good R-f capacitor for every 5 gate packages on a board at the rate of .01 μf/package. These capacitors should be located in close proximity to the gates they are to decouple.

MISCELLANEOUS INTERFACES

For applications where input "1" levels are higher than UTILOGIC II "1" levels ("0" voltages about equal), several interfacing possibilities exist. A UTILOGIC II AND gate may be used as a buffer by using a series diode (d) to improve the input breakdown voltage (see Figure 3). The external resistor, (R), may be used to improve the "0" offset voltage, thereby compensating for the voltage rise across the diode (each 20 kΩ load reduces fan-out by 1). High conductance diodes are recommended to keep the input voltage as low as possible.

Interfacing high "1" voltage outputs to UTILOGIC II source load inputs may be accomplished by techniques such as those in the following four examples. In Figure 4, the forward voltage of one or more diodes is the voltage dropping medium. In Figure 5, a zener diode is used when voltage drops of 5 volts or more must be obtained. The resistor, R, may be used to increase the zener current to improve its regulation. Using a zener as shown in Figure 5, may be especially desirable if the "1" level of the driving source has large variations. In Figure 6, a simple resistive voltage divider provides the necessary voltage reduction, and may be used when minor modifications to the logic levels are required and when high speeds are not necessary.

When the "1" level output of another logic circuit will not reach the required UTILOGIC II input level 2.7 volts, the 317 or 333 Expandable gates will often provide an acceptable buffer, shown in Figure 7. Because the voltage required to switch an Expandable Gate is a "diode drop" lower at the Expansion Input than at the regular inputs, "1" levels of 2.0 volts and "0" levels of 0.8 volts are sufficient. Maximum "1" input current is 3 mA. This Expansion Input interface scheme also may be used at interfaces with Diode Logic, shown in Figure 8.

UTILOGIC II TO RTL INTERFACE

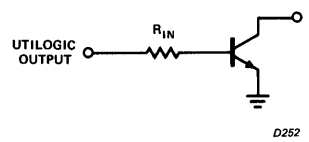


Figure 2

HIGH LEVEL TO AND INTERFACE

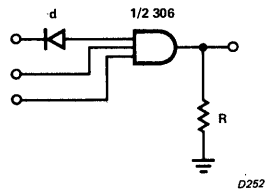


Figure 3

5 VOLT TO SOURCE INPUT INTERFACE

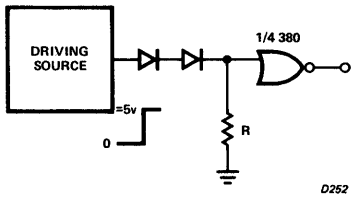


Figure 4

INTERFACING WITH VARIABLE INPUT LEVELS

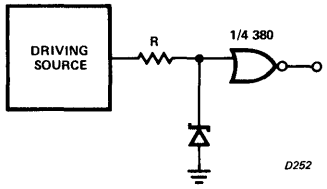


Figure 5

RESISTIVE INTERFACE

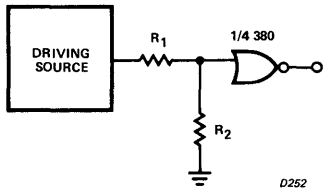


Figure 6

LOW LEVEL TO UTILOGIC II INTERFACE

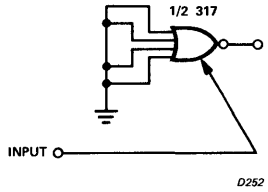


Figure 7

DIODE LOGIC TO UTILOGIC II INTERFACE

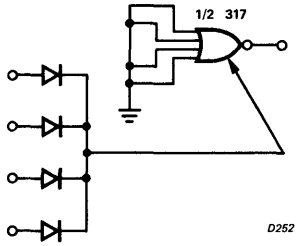


Figure 8

10 VOLT TO SOURCE INPUT INTERFACE

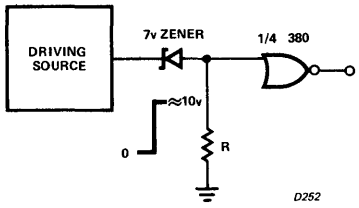
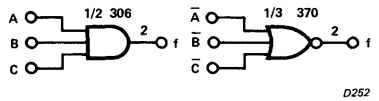


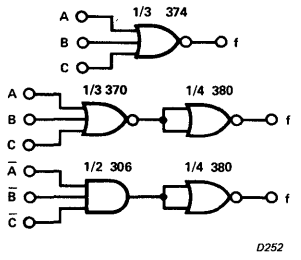
Figure 9

TYPICAL APPLICATIONS OF UTILOGIC II

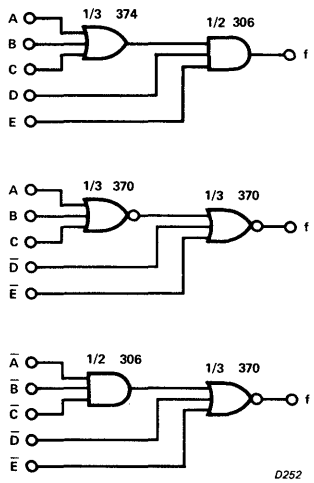
The examples in Figure 13 through 16 illustrate the versatility of the UTILOGIC II AND, OR, NAND and NOR gates and binaries in the implementation of some basic logic configurations.



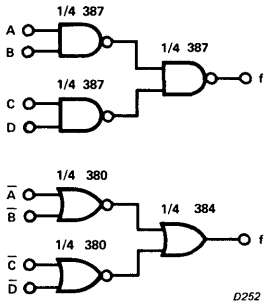
f = ABC **Figure 13**



f = A + B + C **Figure 14**



f = (A + B + C) DE **Figure 15**



f = AB + CD **Figure 16**

Exclusive-OR

The Exclusive-OR (X ⊕ Y) function, shown in Figure 17 is equivalent to the statement, "f equals X or Y, but not both, or X is not equal to Y." The Digital Comparator output, Figure 18, is the complement of the Exclusive-OR output and is used to implement the function, X equals Y.

EXCLUSIVE-OR

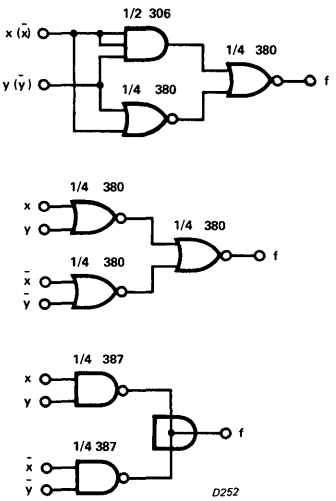
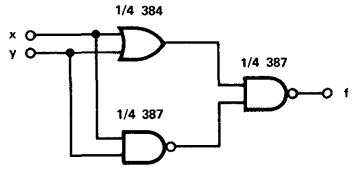


Figure 17

DIGITAL COMPARATOR

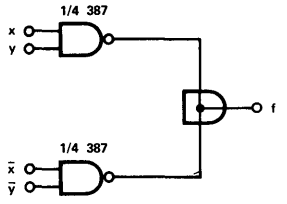


f = xy + $\bar{x}\bar{y}$ **Figure 18**

Collector Logic

Collector logic or "wired AND" is made possible by the use of the UTILOGIC II NAND gates. In this configuration, the outputs of two or more gates are wired together to simulate a new logic function. Thus, as illustrated in Figure 19 the function $f = \overline{AB + CD}$ is generated using only two gates.

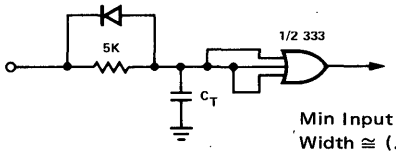
COLLECTOR LOGIC



$f = \overline{AB + CD}$

Figure 19

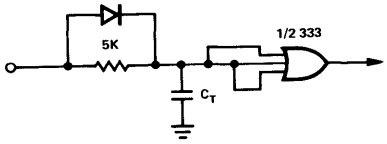
PULSE WIDTH DISCRIMINATOR



Min Input Pulse Width ≅ (.7)(5K)(C_T)

Figure 20

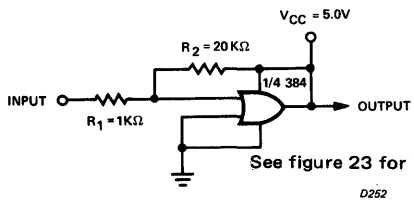
PULSE STRETCHER



Output Pulse Width≅0.5(5K)C_T
(if input pulse>40nsec and C_T<200pF

Figure 21

SCHMITT TRIGGER

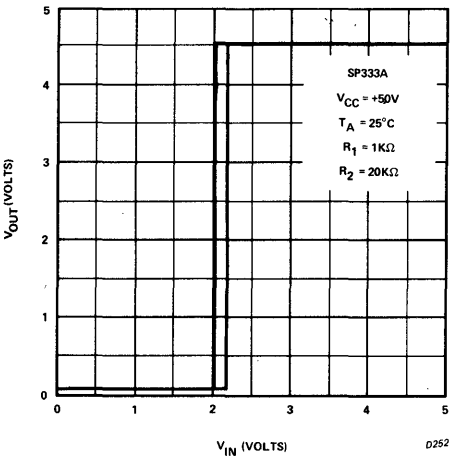


See figure 23 for V_{in} vs V_{out}

D252

Figure 22

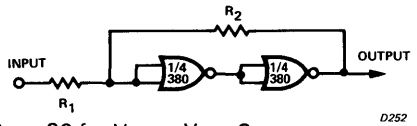
SCHMITT TRIGGER



D252

Figure 23

SCHMITT TRIGGER



D252

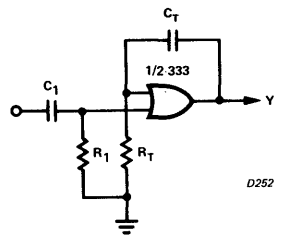
See Figure 23 for V_{in} vs V_{out} Curves.

Figure 24

The Schmitt triggers of figure A and B have a variable hysteresis voltage which is approximately equal to

$$V_{hyst} \cong -3.7 \frac{R_2}{R_1} \text{ Volts, } R_1 \leq R_2$$

ONE-SHOT



D252

$T \cong 1.1\ R_T C_T, R_1 C_1, < R_T C_T$

Figure 25

The one-shot of figure 25 operates in the following manner:

The input pulse is differentiated by the R, C, network for a positive going input transition. This causes the input to the gate to appear as a logical "1" causing the output to rise. This is fed back to the other input thereby locking the output to a "1" until the voltage at the input discharges through R_T C_T to the threshold region. At this point the positive feedback restores the output to a logical "0".

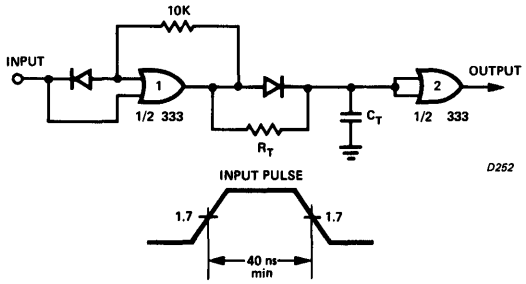
The output pulse will have two modes:

Mode 1 – if: input p.w. < output p.w. then output p.w. = T

Mode 2 – if: input p.w. > output p.w. then output p.w. = input p.w.

This circuit is useful to overcome the contact bounce associated with mechanical to electrical interface and for signal conditioning for short pulse inputs. The same circuit can be built using two NOR gates as shown in figure 26.

ONE SHOT WITH A SCHMITT TRIGGER INPUT, RETRIGGERABLE POSITIVE EDGE TRIGGER



$$T = 0.7\left[\frac{R_T(10K) + R_T(25K) + (25K)(10K)}{R_T(25K)(10K)}\right]$$

Figure 26

Circuit operation: When the input rises to a logical "1" level the output of gate 1 assumes a "1" level. This charges C_T through the diode thereby presenting the input of gate 2 with a "1". The output of gate 2 therefore assumes a "1" level. This condition holds until the input falls to the input threshold level. At this point, and until the input pulse falls to one diode drop below threshold, the 10 kΩ resistor feeds current into the input holding a "1" level output.

When the input falls to a diode drop below threshold the current through the 10 kΩ resistor is "bled" away from the input and the output of gate 1 falls to a logical "0". C_T then discharges through the effective parallel resistance until the voltage at gate 2 input reaches threshold. At this time the output falls to a logical zero. C_T may be recharged at any point in the cycle by another pulse at the input.

RE-TRIGGERABLE ONE-SHOT WITH NEGATIVE EDGE TRIGGERING

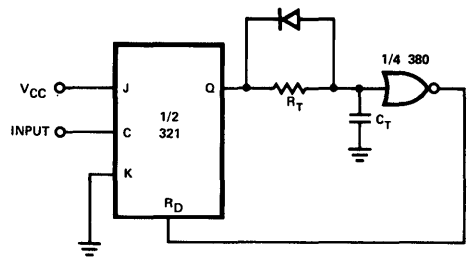
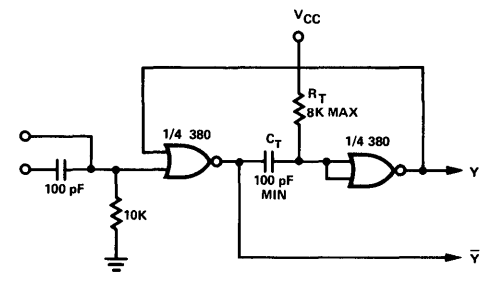


Figure 27

ONE-SHOT WITH COMPLEMENTARY OUTPUTS



$T = 0.7\ R_T C_T$

Figure 28

NOISE DISCRIMINATOR ONE-SHOT

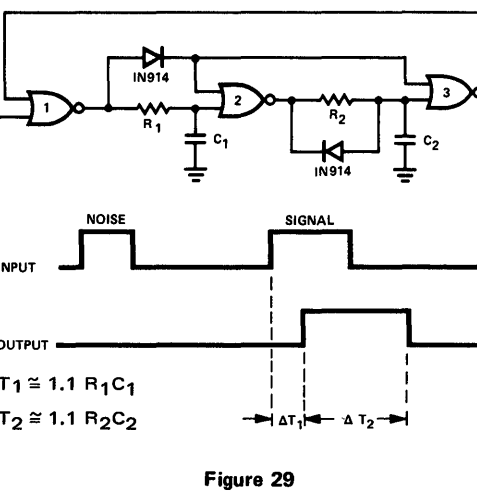
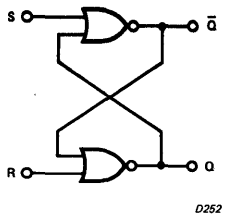


Figure 29

Circuit Operation: This one-shot discriminates between noise lasting less than time ΔT_1 and an input signal having a greater than ΔT_1 duration. An input greater than ΔT_1 produces an output pulse of ΔT_2. The output of gate 3 is fed back into the input of gate 1 which guarantees an output pulse of ΔT_2 if the input goes to "0" during the output "1" cycle. The diodes are used to minimize recovery time.

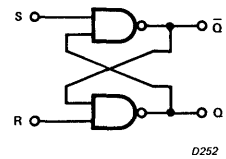
LATCH AND TRUTH TABLE



R	S	Q	$\bar{Q}$
0	0	No	Change
0	1	1	0
1	0	0	1
1	1	0	0

Figure 30

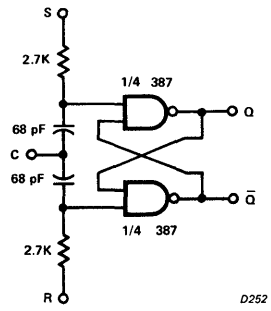
LATCH AND TRUTH TABLE



R	S	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No	Change

Figure 31

SINGLE FLIP-FLOP AND TRUTH TABLE



R	S	Q_{n+1}
0	0	Not Allowed
0	1	0
1	0	1
1	1	Q_n

Figure 32

ARITHMETIC FUNCTIONS

This subsection describes four basic arithmetic functions (Half-Adder, Full-Adder, Parallel Binary Adder and Full Subtractor) and illustrates their implementation with UTILOGIC II circuits.

HALF-ADDER

The Half-Adder (Figure 33) is a functional circuit for obtaining the binary sum of X plus Y. The circuit has two outputs, Sum and Carry (S and C). The Sum output is the same as the output of the Exclusive-OR circuit; the C output indicates a binary carry. A Half-Adder may be used at the lowest order position of a Parallel Adder (all bits added simultaneously) since there is no carry input to this position. Two Half-Adders may be combined to obtain a Full-Adder.

HALF ADDER

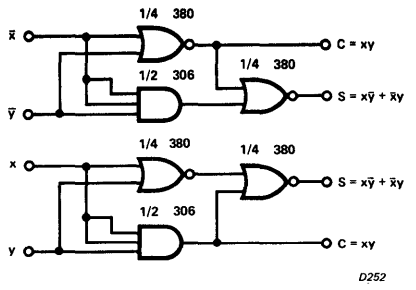
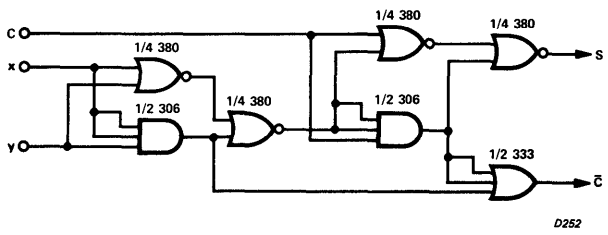


Figure 33

FULL-ADDER

A Full-Adder (Figure 34) is a circuit for obtaining the binary sum of three binary digits, X, Y, and C (carry). The circuit has two outputs: S to indicate the sum of the three inputs and $\bar{C}$ to indicate the value of the resulting carry.

FULL ADDER AND TRUTH TABLE



$S = c(xy + \bar{x}\bar{y}) + \bar{c}(x\bar{y} + \bar{x}y)$

$\bar{C} = xy + c(x\bar{y} + \bar{x}y)$

X	Y	C	S	$\bar{C}$
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

Figure 34

PARALLEL BINARY ADDER

The carry propagation delay is minimized by alternating between Carry and $\overline{\text{Carry}}$ in the carry propagation delay path as shown in Figure 35. It is necessary to alternate the polarity of inputs A and B from stage to stage to do this. Alternating the Q and $\bar{Q}$ of the 328 flip-flop eliminates the need for inverting Sum outputs. The use of collector logic minimizes the number of gates required to perform the function.

PARALLEL BINARY ADDER

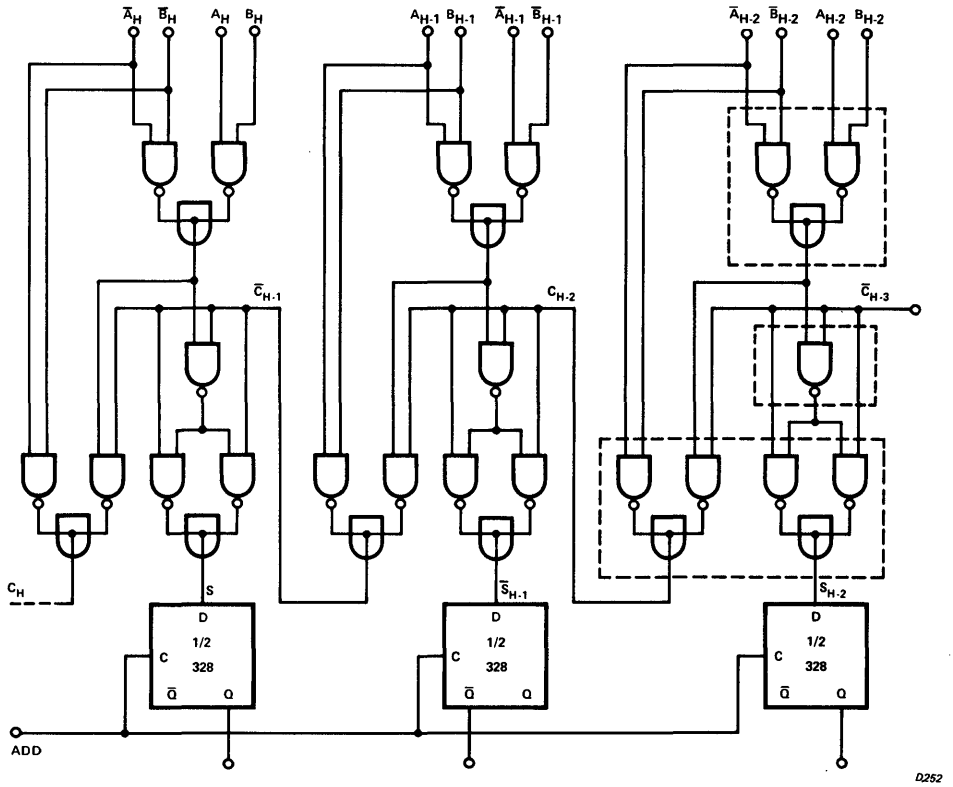


Figure 35

FULL-SUBTRACTOR

The circuitry to obtain the binary Difference, (D equals X minus Y minus Borrow), and B' (new Borrow), is identical to the above Full-Adder, except that a false input and a change of output notation are required. The UTILOGIC II Full-Subtractor implementation is shown in Figure 36.

FULL SUBTRACTOR

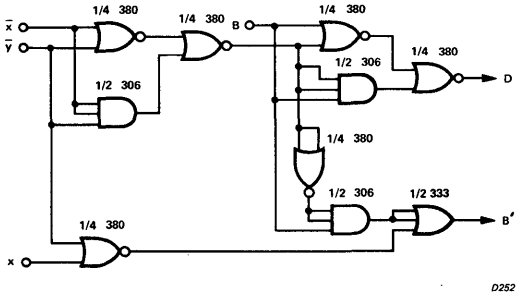


Figure 36

TRUTH TABLE

X	Y	B	D	B'
0	0	0	0	0
1	0	0	1	0
0	1	0	1	1
1	1	0	0	0
0	0	1	1	1
1	0	1	0	0
0	1	1	0	1
1	1	1	1	1

$D = B(XY + \overline{X}\overline{Y}) + \overline{B}(X\overline{Y} + \overline{X}Y)$

$\overline{B} = \overline{X}Y + B(XY + \overline{X}\overline{Y})$

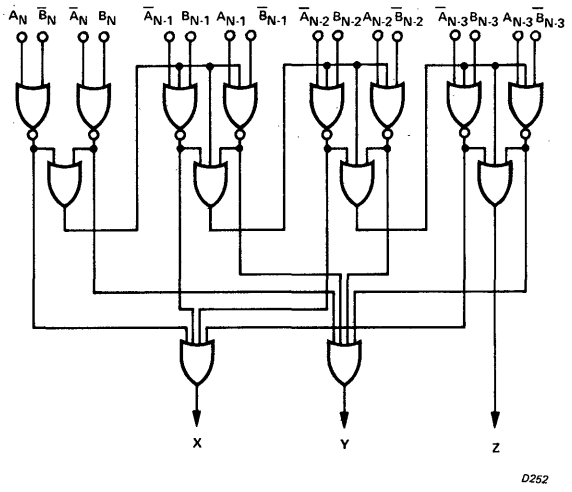
COUNTING FUNCTIONS

Since many computing functions, such as indexing and program control, are essentially counting functions, a large variety of counters is used in computing equipment. Some of the more common counter types discussed in this section showing the flexibility of the UTILOGIC II family are: asynchronous ripple counters, useful for frequency division; simple synchronous counters for high-speed logic operations; reversible counters for specialized control; and feedback shift registers which are especially suited for commutation and very high-speed counting.

EXPANDABLE PARALLEL COMPARATOR

The comparator shown minimizes both package count and ripple through. The appropriate output (<, = , >) will be a logical "1", and the other two outputs will be a logical "0" upon completion of the comparison.

EXPANDABLE PARALLEL COMPARATOR



CONDITION	X	Y	Z
A = B	0	0	1
A < B	0	1	0
A > B	1	0	0

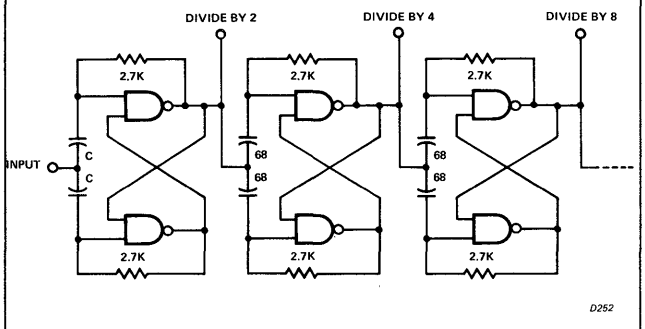
Figure 37

BINARY RIPPLE COUNTERS

In ripple counters, the flip-flop normally operates in the simple toggle mode (change with each clock pulse) with the output of each element driving the clock input of the following stage. Ripple counters operating in this manner are able to operate at higher input frequencies than most other types of counters, require no gating and few interconnections, and present only one clock input to the input line. The asynchronous Set/Reset characteristics of the 321 and 322 binaries allow the binary sequence of the simple ripple counter to be modified to arbitrary sequence lengths, many of which can be obtained without gating. A limitation of all ripple counters is that a change of state may be required to ripple through the entire length of the counter. The propagation time of this change may determine the maximum operating frequency of the modified types and will be determined when any decoding networks may be sampled. A simple Binary Ripple Counter that counts up is shown in Figure 37. Since each stage changes state (complements) on each "1" to "0" transition of the previous stage, the counter is implemented by connecting the clock input of each stage to the "Q" output of the previous stage.

Presetting to "0" is illustrated in the first two stages in Figure 39, presetting to "1" is shown in the third stage. Figure 40 shows a ripple counter implemented with the 321 binary.

BINARY RIPPLE COUNTER

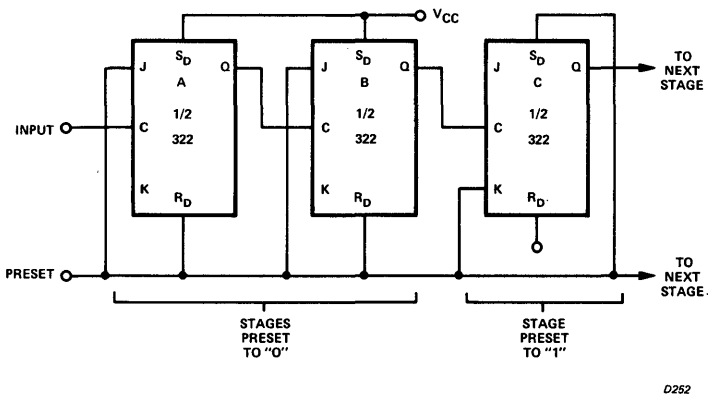


ALL GATES 1/4 387 EACH

Figure 38

BINARY RIPPLE COUNTER – 322 BINARY IMPLEMENTATION

A	B	C
0	0	0
1	0	0
0	1	0
1	1	0
0	0	1
1	0	1
0	1	1
1	1	1
0	0	0



NOTE: Tie all unused J and K inputs to V_{CC}.

Figure 39

BINARY RIPPLE COUNTER – 321 BINARY IMPLEMENTATION

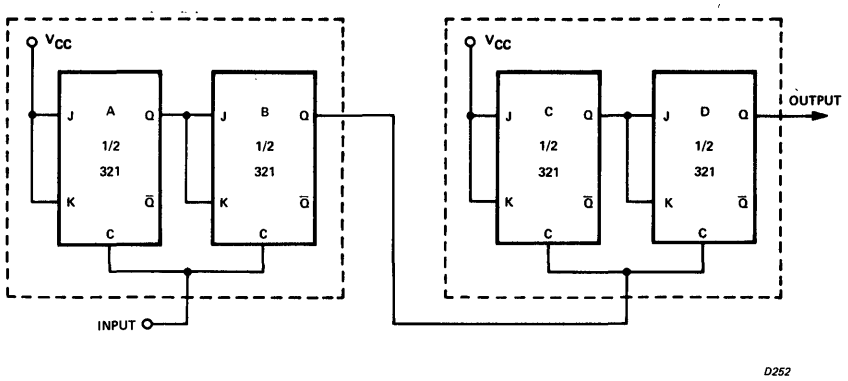


Figure 40

MODIFIED RIPPLE COUNTERS

Many popular counters are modifications of the basic Binary Ripple Counter previously described. The decimal counter modifications, shown in Figure 42 illustrate the versatility obtained by combining the ripple counting technique with logical feedback. In Figure 42 the carry provides resynchronization to the clock pulse. This technique may be applied to other similar ripple counters. It provides most of the speed advantages of ripple propagation while allowing synchronous operation between decades.

SYNCHRONOUS COUNTERS

Synchronous counters are used in applications where all flip-flop outputs must change simultaneously, as in most high-speed logic systems and in counters that must be decoded during counting. Synchronous counters may be used to stop an event on a specific count or may be used for timing events as a function of specific intervals in a clock pulse sequence.

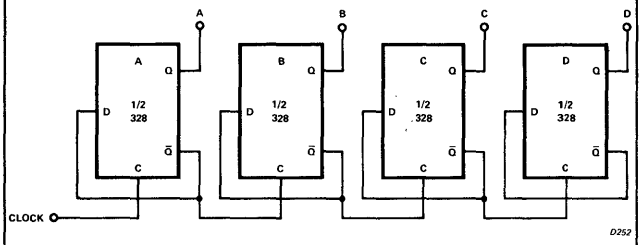
Asynchronous Divide-By-16 Up Counter

This counter (shown in Figure 41) makes use of the 328 Binary which is leading edge triggered. The clock must therefore be driven by the $\overline{Q}$ output of the previous stage to perform the up count. If a down count is required, the clock must be driven by the Q output of the previous stage. This applies to all leading edge triggered systems.

Also, these counters are useful for special computer applications that involve reversing, special codes, and start/stop operations. Some limitations of a synchronous counter as compared to a ripple counter are:

1. Higher flip-flop fan-outs and gate fan-ins are required.
2. The clock line represents a relatively high load.

BINARY COUNTER AND TRUTH TABLES



A	B	C	D
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1
0	0	0	0

Figure 41

BINARY COUNTER

The large fan-in capability of UTILOGIC II NOR gates allows a simple Synchronous Binary Counter to be implemented easily, as shown by the ten sample stages in Figure 43. The large fan-out capability of the 321/322 binaries allows this counter to be extended to 14 stages (16,384 states) without buffering. The alternate implementation shown reduces:

1. The fan-out requirements of the 321/322 binaries.
2. The fan-in requirements of the NOR gates.
3. The number of circuit elements when gate fan-in requirements exceed 7.

However, the operating speed is lowered because of the introduction of additional propagation delays. The counter sequence is the same for both implementations.

MODULAR BINARY COUNTER

This type of counter, as shown in Figure 44, requires lower fan-out and fan-in than required in the previous example but at the expense of propagation delay. The maximum signal delay is through N-2 gates for a counter of N stages. Stages may be added in a modular fashion because the logic is repetitive for each stage.

8-4-2-1 DECADE COUNTER WITH DECIMAL DECODING

Feedback and the J-K characteristics of the UTILOGIC II 321/322 are employed to produce the 8–4–2–1 decade counter shown in Figure 45. UTILOGIC II AND gates may be substituted for the NOR gates illustrated in the decoding matrix when sink fan-out from the decoding gates is not required and decreased propagation delays are desired.

4-2-2-1 DECADE COUNTER

The count sequence of the counter shown in Figure 46 is not as popular as the previously shown 8–4–2–1 sequence but is frequently used since its decimal decoding matrix requires only 3-input gates.

REVERSIBLE BINARY COUNTER

The counter shown in Figure 47 will count every input pulse. The counter will count up when the UP input is low; it will count down when the DOWN input line is low.

REVERSIBLE DECADE COUNTER

The counter shown in Figure 48 uses feedback to produce an 8–4–2–1 decade sequence. The counter will count only when the appropriate command is present.

BCD COUNTER WITH GATED CARRY

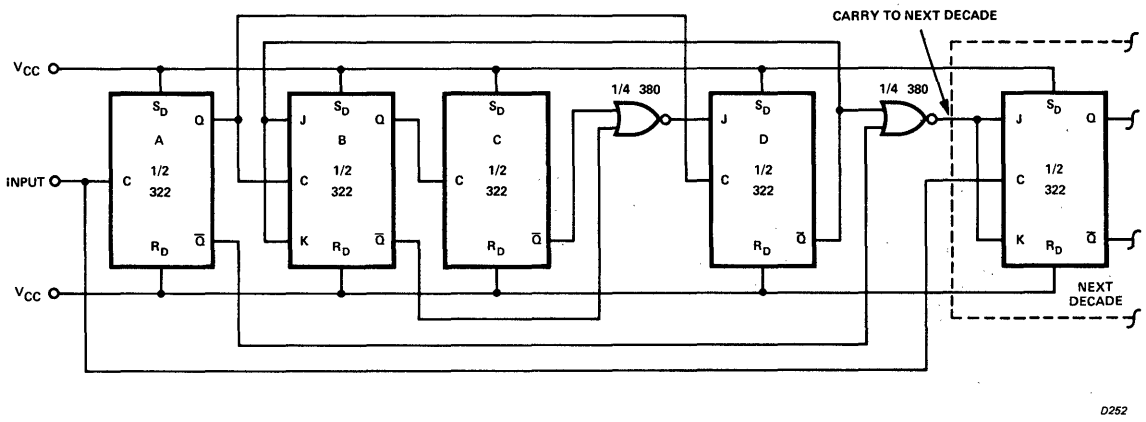


Figure 42

SYNCHRONOUS BINARY COUNTER

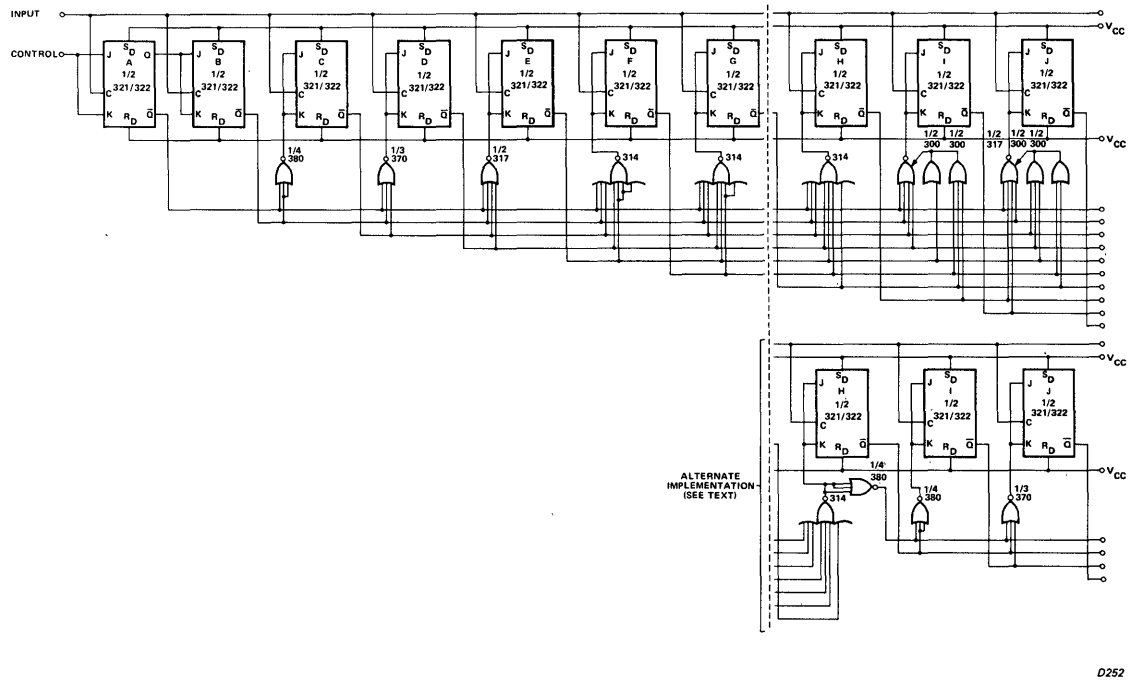


Figure 43

MODULAR BINARY COUNTER

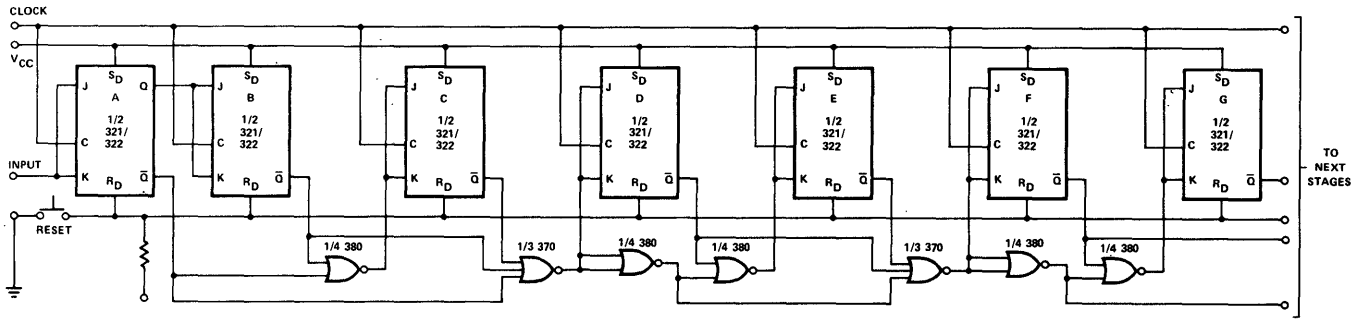
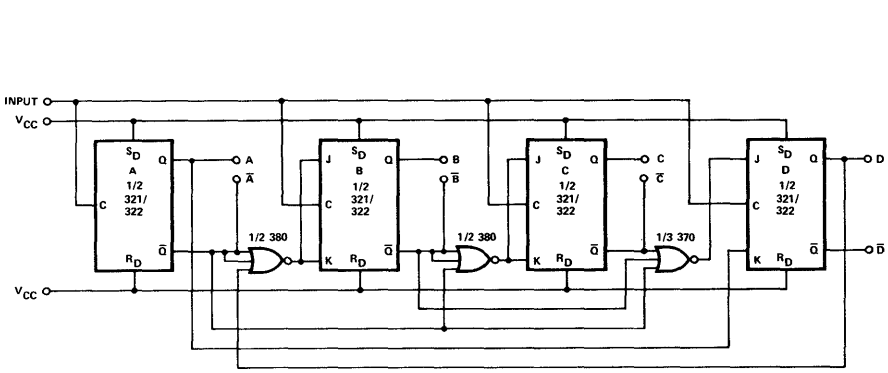


Figure 44

BCD COUNTER WITH DECIMAL DECODING



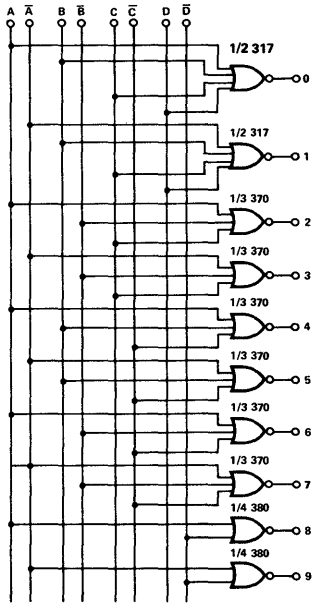
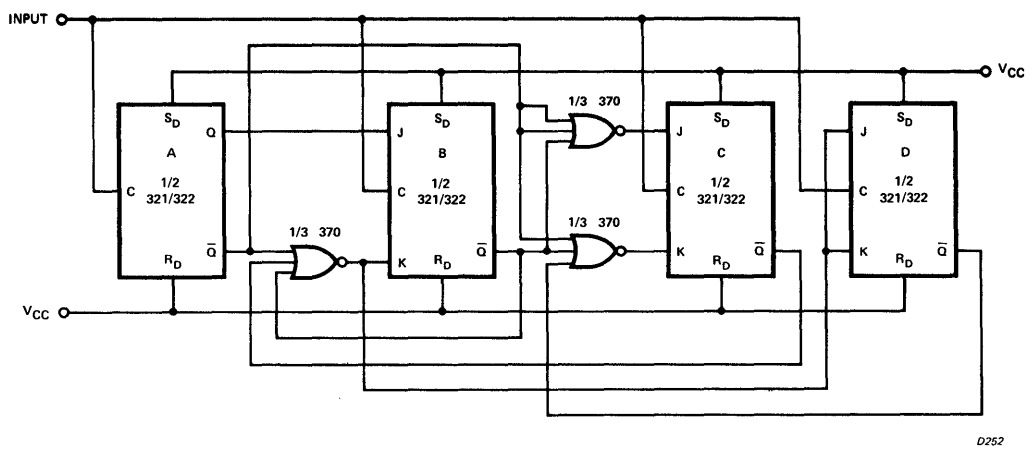


Figure 45

4–2–2–1 DECADE COUNTER



	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	1	1	0
5	1	1	1	0
6	0	0	1	1
7	1	0	1	1
8	0	1	1	1
9	1	1	1	1

Figure 46

REVERSIBLE BINARY COUNTER

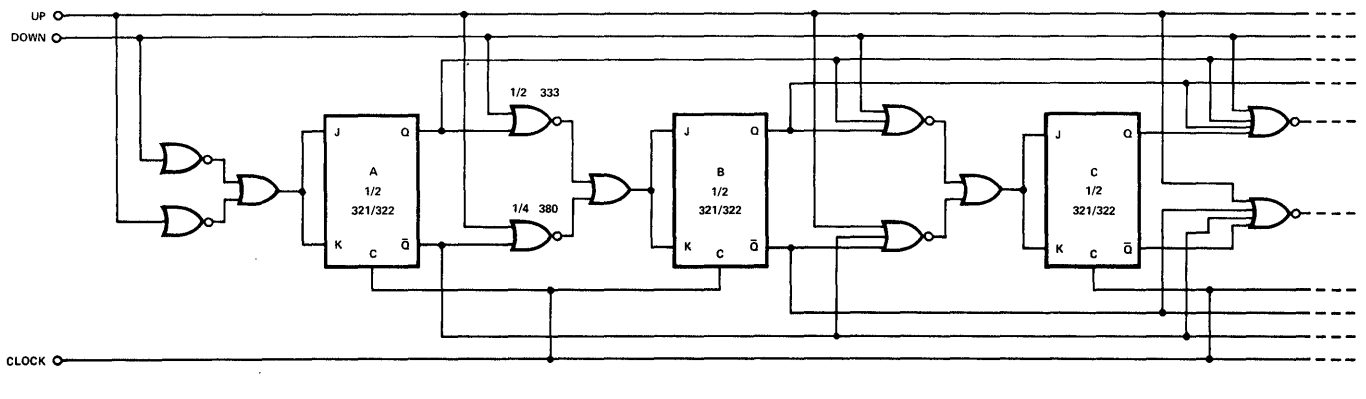


Figure 47

REVERSIBLE DECADE COUNTER

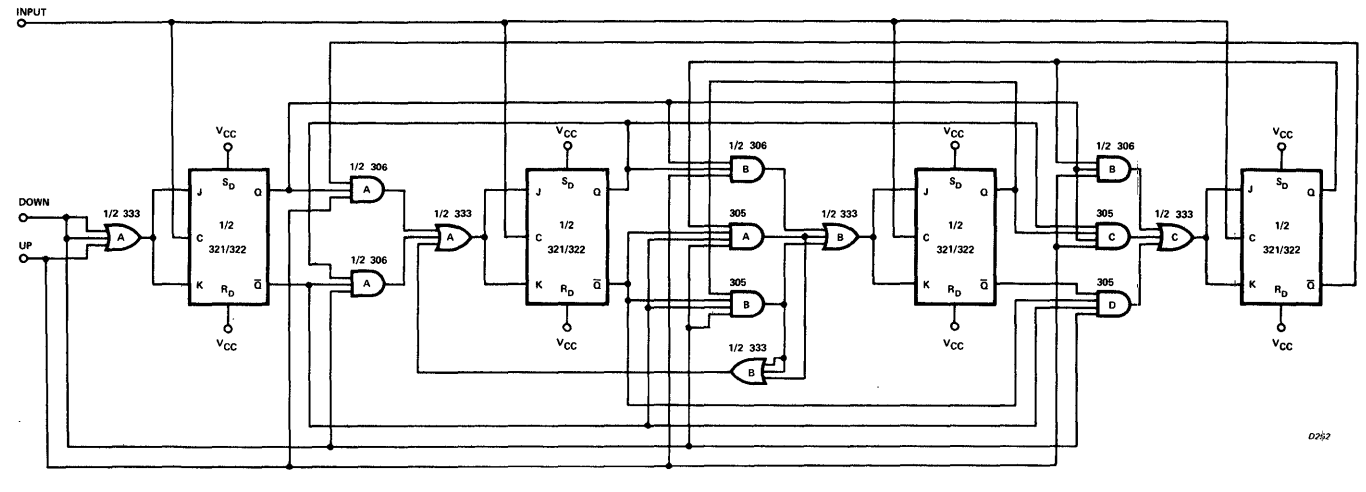
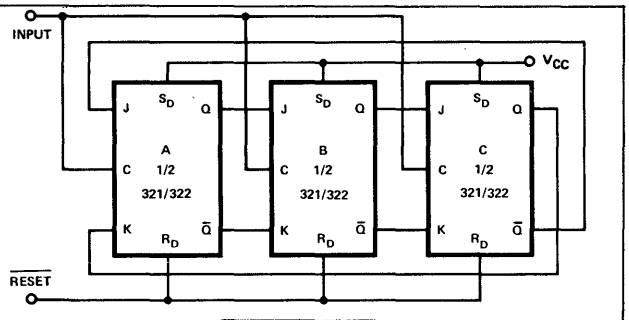


Figure 48

SIMPLE RING COUNTER

A very simple Ring Counter with sequence of 6 (N equals 3) that requires no gating is shown in Figure 49. Presetting is required to ensure that the proper sequence is entered.

SIMPLE RING COUNTER AND TRUTH TABLE



	A	B	C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1

Figure 49

DECIMAL RING COUNTER WITH DECODING AND SELF-SEQUENCING

The counter in Figure 50 is essentially the above counter except that N equals 5, and a gate has been added to provide self-sequencing. Readout gating is shown to illustrate its simplicity. UTILOGIC II AND gates may be substituted for the NOR decoding gates when sink fan-out from the decoding gates is not required, and decreased propagation times are desired.

JOHNSON COUNTER

The Johnson Counter (Feedback Shift Register) has a sequence length, 2^N-1, for most small N (N equals the number of stages). However, for some N, the sequence lengths may be different. For example, when N equals 5, one initial state (00000) gives 21 states; another (11000) gives 7; a third initial state (00100) gives 3 states. The Johnson Counter can be designed to produce sequence lengths not easily obtainable with other high-speed counter designs; however, this type of counter is hard to decode and debug since there is no common pattern to the sequence. The Johnson Counter shown in Figure 51 has a sequence length of 15 (initial state "0000") as shown in the Truth Table.

DECIMAL RING COUNTER

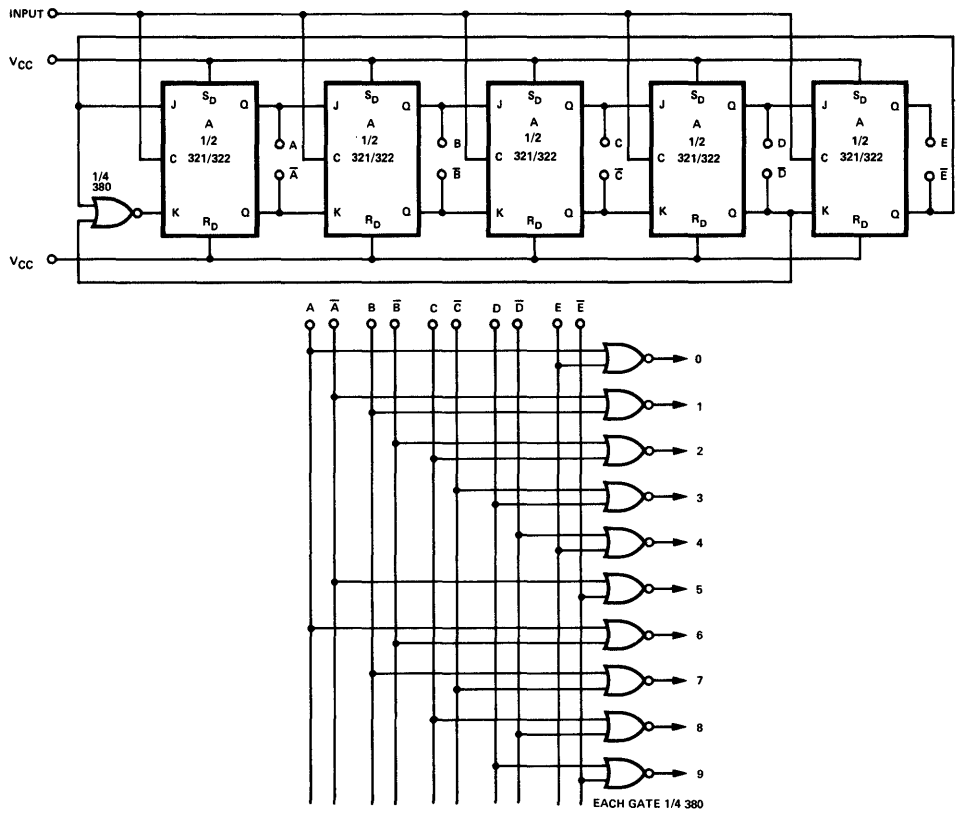
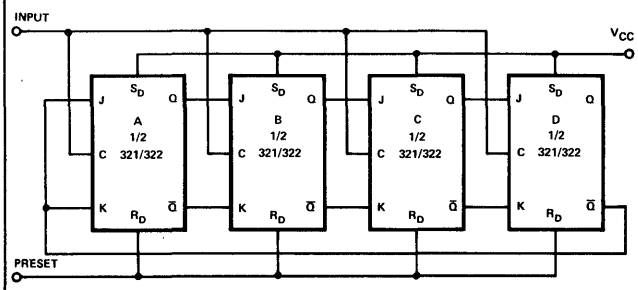


Figure 50

JOHNSON COUNTER AND TRUTH TABLE



	A	B	C	D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	0	1	0
4	0	1	0	1
5	0	0	1	0
6	1	0	0	1
7	1	1	0	0
8	0	1	1	0
9	1	0	1	1
10	1	1	0	1
11	1	1	1	0
12	0	1	1	1
13	0	0	1	1
14	0	0	0	1
0	0	0	0	0

Figure 51

Shift Registers

A Shift Register is a circuit for storing and shifting a number of binary or decimal digits. Shift Registers frequently are used in arithmetic operations to accomplish multiplication or division; they also are used to present information in serial form for use in displays, adders, magnetic tapes, and magnetic drums. The Shift Register, shown in Figure 52, shifts its contents one position to the right upon each occurrence of the clock pulse. The input lines allow entry of new information to the first stage; the clear line will reset all of the stages to "0". A configuration is shown in Figure 53 in which information stored at X_1, $X_2 \ldots X_N$ (another shift register) is entered in parallel to register Y (Y_1, $Y_2 \ldots Y_N$) upon the command ENTER. Upon each command to SHIFT, the information stored in register Y is shifted one stage to the right. Although the parallel entry utilizes the asynchronous inputs, the entire operation is under the direct control of the clock pulse so that the operation is synchronous.

Feedback Shift Registers

Feedback Shift Registers or Ring Counters, like the ripple-carry counters, are capable of operating at the maximum frequency of the flip-flops; they have the additional feature of being able to shift as well as count. This characteristic is very valuable when the information in the counter is to be presented as a serial word to a display or memory device. When connected as a Ring Counter, a Feedback Shift Register will have a sequence length of 2N; other connections may give sequence lengths to the maximum of 2^N-1.

SERIAL ENTRY SHIFT REGISTER

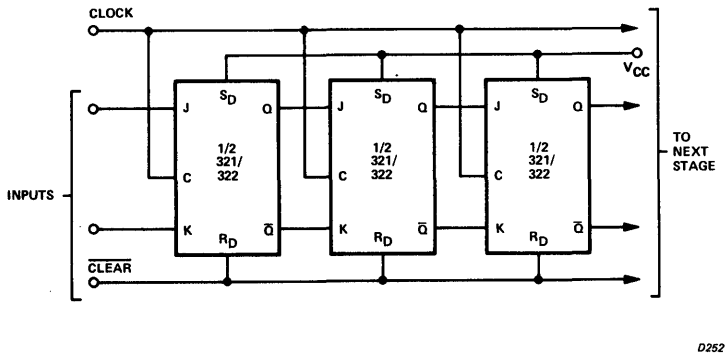


Figure 52

PARALLEL ENTRY SHIFT REGISTER

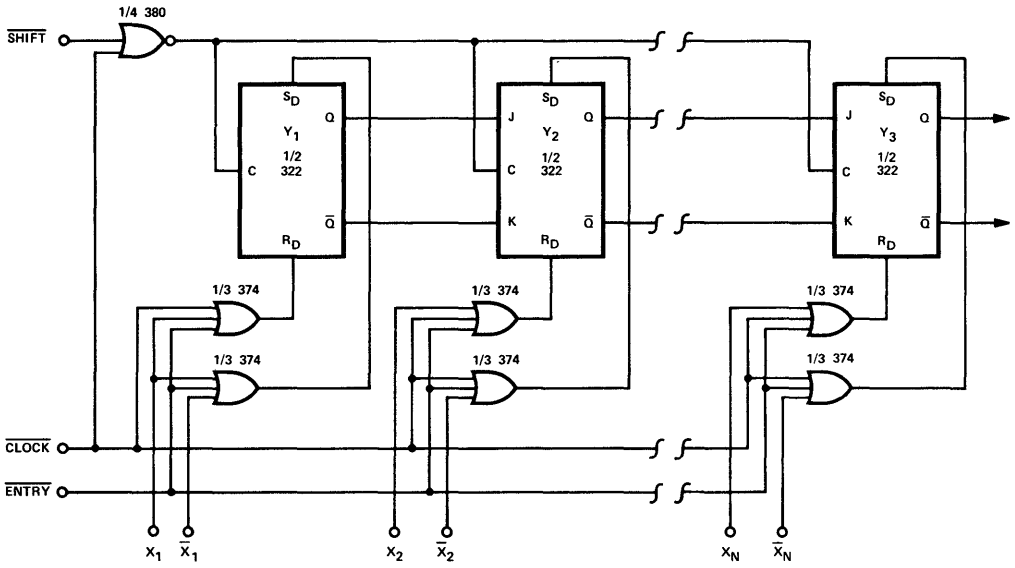


Figure 53

SERIAL-IN, PARALLEL-OUT

In Figure 54, shift registers are implemented with RS/T, J-K, or D binaries

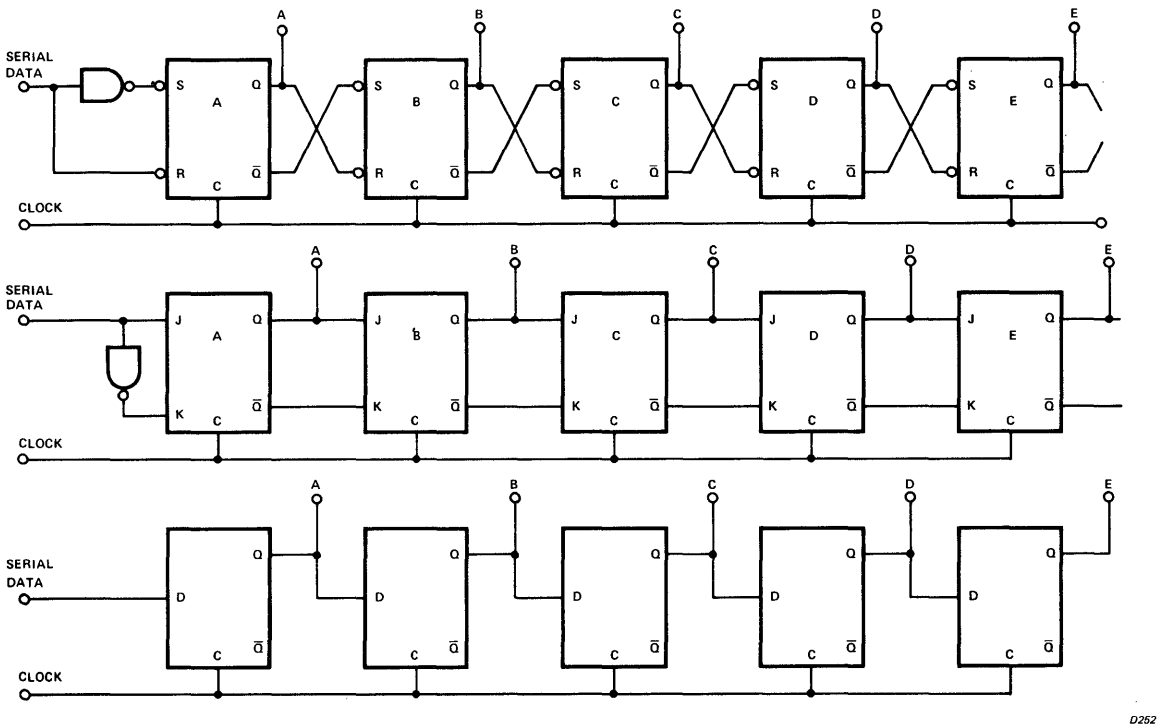


Figure 54

LEFT-RIGHT SHIFT REGISTER

The left-right shift register will shift either one bit to the left, or one bit to the right for each clock pulse. The register will shift to the left if the L-R line is logical "0", and to the right if the L-R line is logical "1". Data will transfer on the leading edge of the clock.

ASYNCHRONOUS CONTROL CONFIGURATIONS

In the following asynchronous examples, the timing of the operations is controlled by internally generated signals instead of by an external clock source as in synchronous operations. The logic required to generate the timing signals may require a great deal of hardware, but the operation may be considerably faster than in an equivalent synchronous operation where the clock period must allow for the maximum circuit delays.

SIMPLE ASYNCHRONOUS ADD SEQUENCE

The simple system shown in Figure 56 illustrates typical asynchronous techniques. In this figure, the Asynchronous Sequencer is cleared and started by the START ADD signal. The Asynchronous Sequencer immediately enables the Transfer operation, which proceeds to completion and signals the Sequencer that it is completed. The Sequencer then enables each succeeding operation in sequence, but only after receiving a completion signal from each signal from each previous operation. After all operations under the control of the Sequencer have been completed, an ADD COMPLETE signal is sent to the master control circuits.

ASYNCHRONOUS SEQUENCER

The circuit shown in Figure 59 will generate the enable signals for "N" asynchronous operations. The Sequencer may be expanded where shown in order to accommodate any number of operations. Typically, the Asynchronous Sequencer will be used in combination with a similar asynchronous circuit, such as the following Shift Register with Asynchronous Transfer.

ASYNCHRONOUS TRANSFER REGISTER

Figure 57 shows a logic configuration to asynchronously transfer information stored at locations X_A, X_B . . X_N (a register) to register Y. Upon receipt of the command TRANSFER, the input NOR gates, which are serving as ANDs, will connect X to Y to allow Y to assume the state of X. The Digital Comparators compare the state of each Y position to the state at each X position. When all of the positions agree, TRANSFER COMPLETE signals completion to a control circuit such as the Asynchronous Sequencer above.

LEFT-RIGHT SHIFT REGISTER

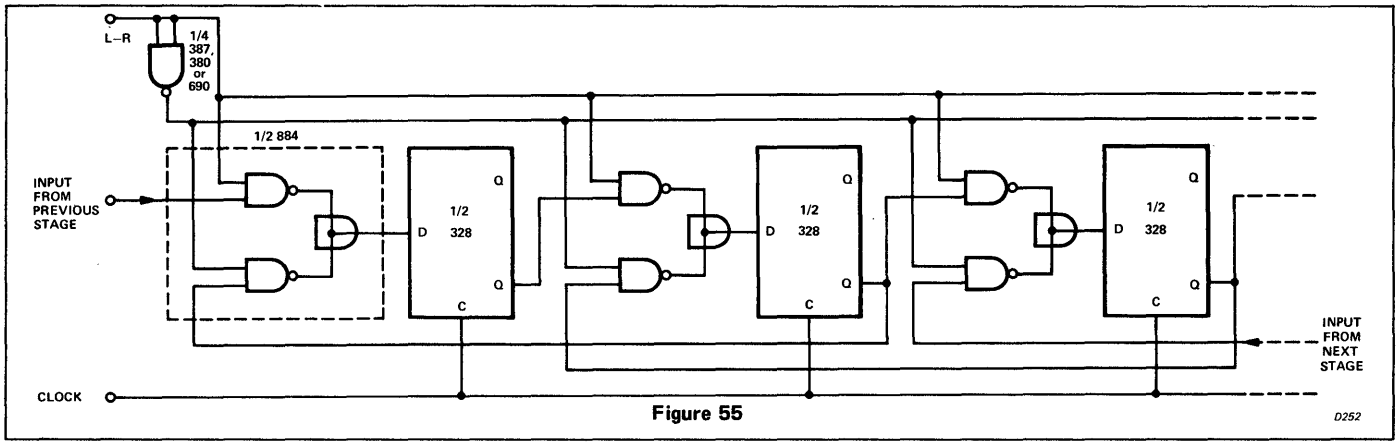


Figure 55

ASYNCHRONOUS SYSTEM

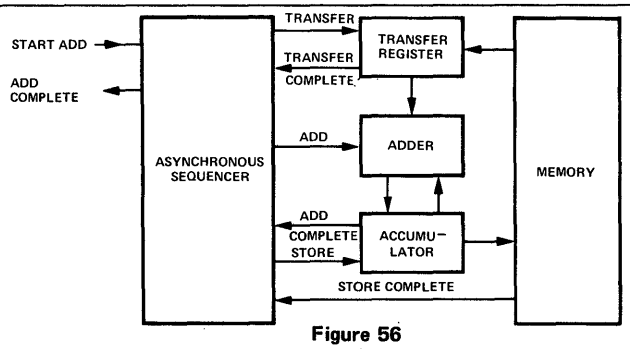


Figure 56

ASYNCHRONOUS TRANSFER

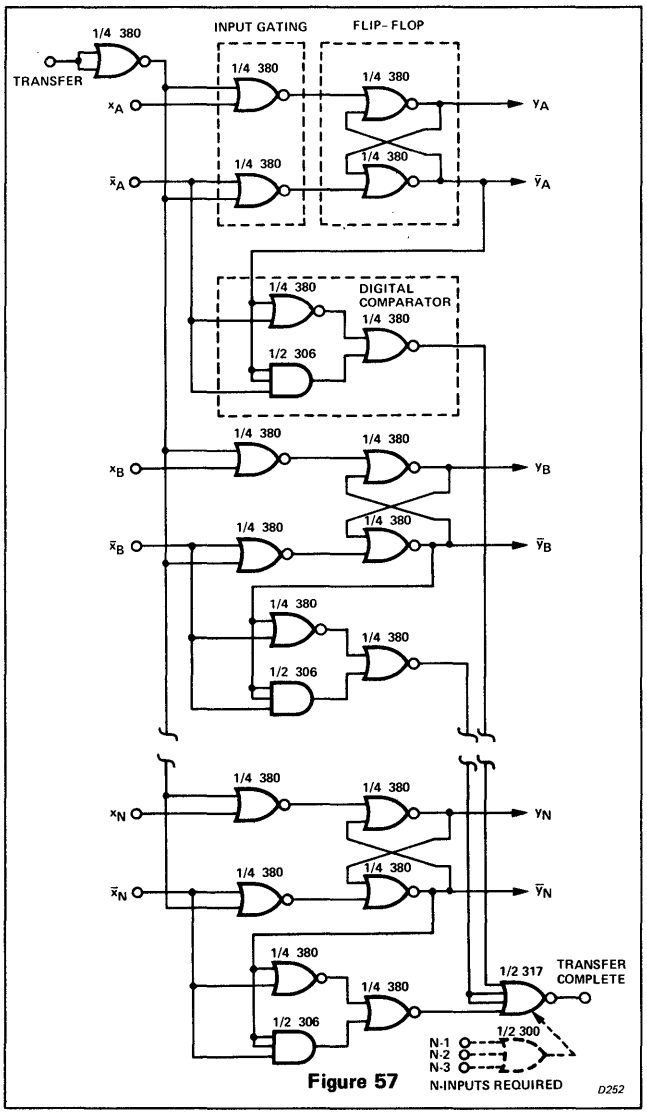


Figure 57

OSCILLATORS AND MULTIVIBRATORS

A simple three stage oscillator using UTILOGIC NOR gates is shown in Figure 58 along with a graph of oscillation frequency versus capacitance.

SIMPLE OSCILLATOR

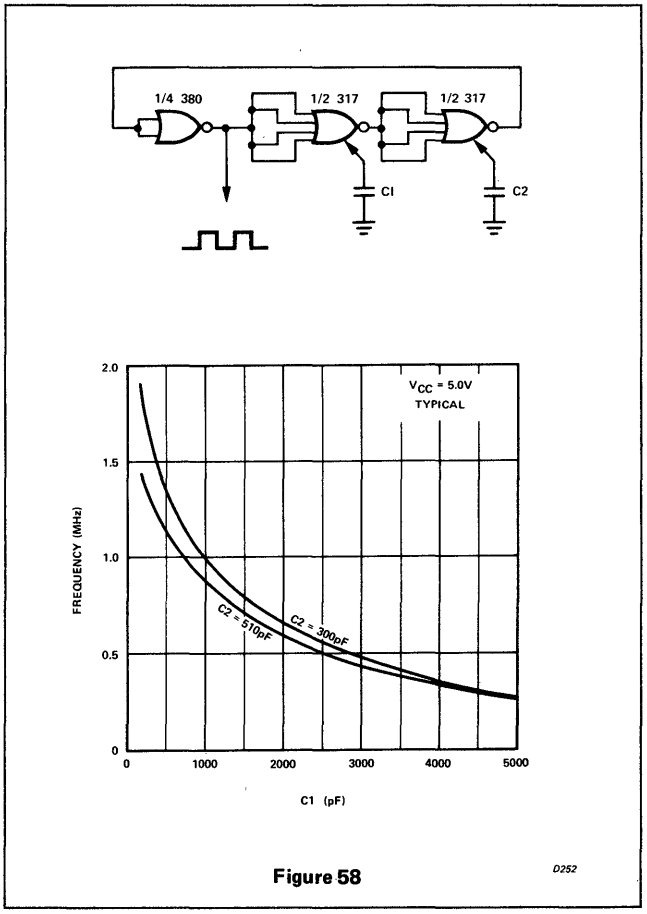


Figure 58

ASYNCHRONOUS SEQUENCER

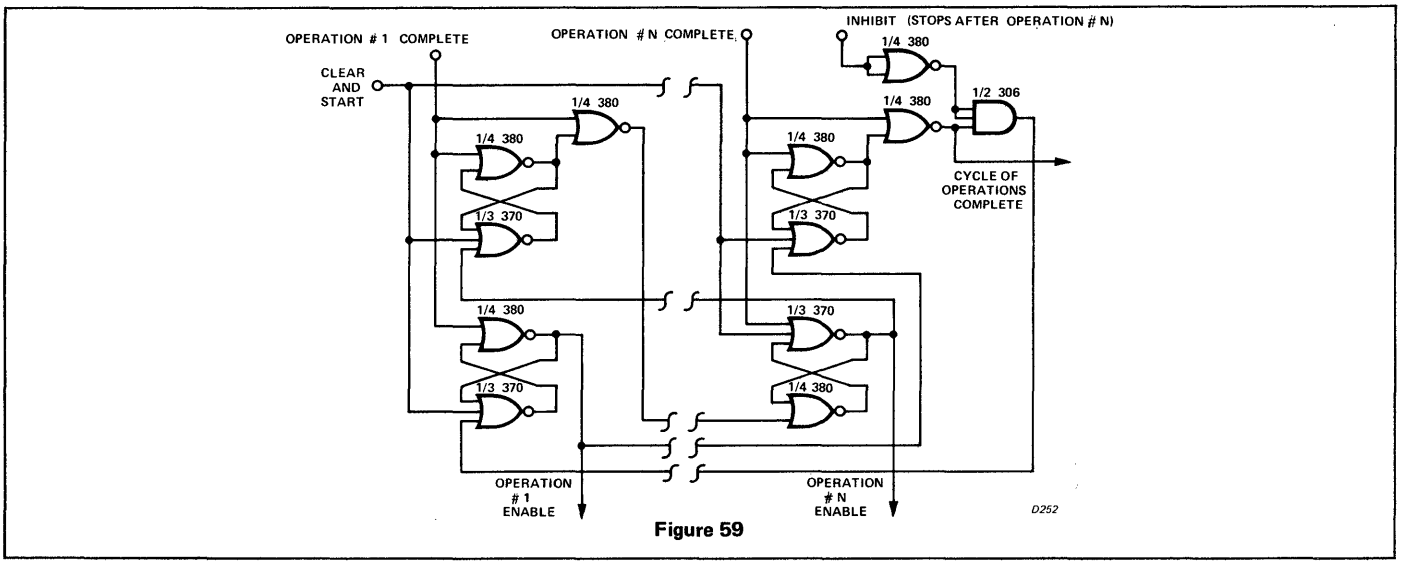


Figure 59

VOLTAGE CONTROLLED OSCILLATORS (Figure 60)

Combining the Schmitt Trigger of Figure 24 with additional NOR logic produces the V.C.O. of Circuit A. There are three modes of operation:

Mode 1 V_{in} open or $R_C = \infty$, fo = 1.2 RC, $R \ll 10k\Omega$
C must be non-polarized

Mode 2 V_{in} connected to a voltage supply and $R_C \ll$ 10 k. As V_{in} decreases from the threshold region of Gate 1 towards a negative voltage f_o increases; a 12:1 range of f_o can be achieved.

Mode 3 V_{in} open or $R_C = \infty$, f_o may be varied over a 1000:1 range by varying R_x. A variable resistor or a voltage controlled resistor (MOS FET) may be used for this application.

This circuit operates best for a $V_{in} < 0V$. The diode across R_x produces a positive going pulse at f_o. This V. C. O. can be made with one 380 package. It is self-starting and has an f_o max $\cong$ 5 MHz.

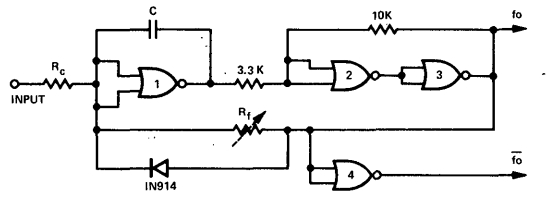
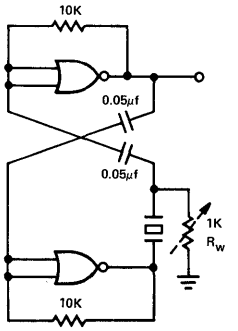


Figure 60

CRYSTAL CONTROLLED OSCILLATOR



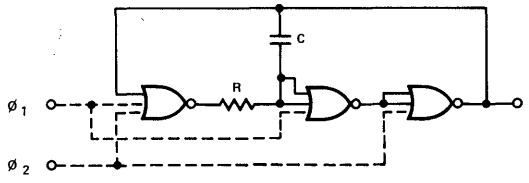
Performance data:

Crystal f_o = 100 kHz to 2 MHz

R_W controls the amount of positive feedback permitting both sinusoidal and square-wave operation.

Figure 61

RC OSCILLATOR – WITH SYNCHRONIZING INPUTS



Performance data:

$f_0 \cong \frac{1}{2\tau}$; τ = RC

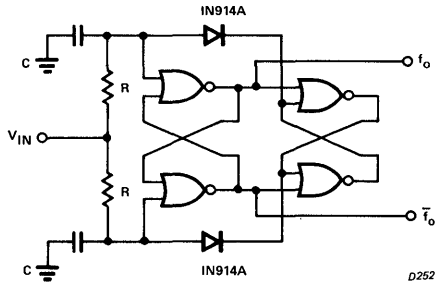
$f_{0\,MAX} \cong$ 5 MHz

Ø 1 and Ø2 must be 180° out-of-phase at a frequency greater than f_0 and have a pulse width of less than 1μ sec.

Figure 62

SELF – STARTING MULTIVIBRATOR

Figure 64 shows a self-starting VCO using a single Utilogic Quad 2-Input NOR package.



Performance data:

$f_0 \cong \frac{1}{\tau}$, τ = RC at V_{IN} = 5V ± 5%

If: V_{IN} = +2.5V to +25V; $R \leq 10K\Omega$

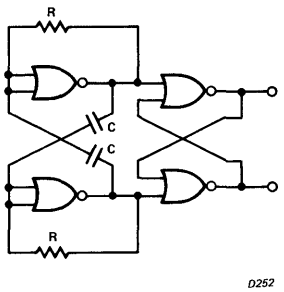
Then: f_0' = 1 f_0 to 100 f_0 or 100:1 range

(f_0' = VCO frequency)

$f_{0\,Max} \cong$ 5 MHz

Figure 63

SELF-STARTING MULTIVIBRATOR



Performance data:

$f_0 \cong \frac{1}{2\tau}$, τ = RC, R $\leq$ 10KΩ

$f_{0\ MAX} \cong$ 5 MHz

C must be non-polarized

Figure 64

LINEAR AMPLIFIER

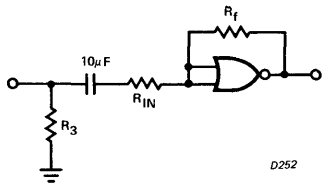
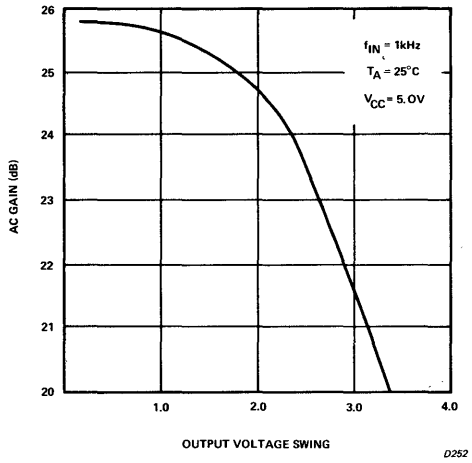


Figure 65

OPEN LOOP GAIN VS OUTPUT VOLTAGE SWING

The gain of the amplifier is $G \cong \frac{A_0 R_f}{(A_0 + 1) R_{IN} + R_f}$

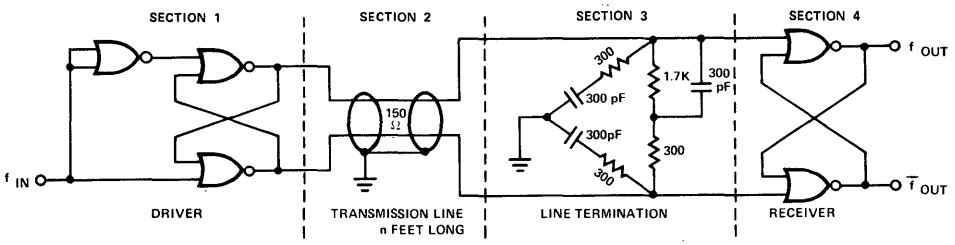
The open-loop gain is shown below as a function of output voltage swing:



The open-loop-3dB cut-off frequency is approximately 5 MHz

Figure 66

TRANSMISSION LINE DRIVER AND RECEIVER



There are four basic sections of this system:

Section 1	The Driver is a D-type latch producing complemented outputs using 380 NOR Gates.
Section 2	A shielded twisted – pair n-feet in length.
Section 3	The 150 ohm Line Termination – Delta configuration. The 1.7K resistor in parallel with 300 pF and in series with 300 ohms between the inputs of the receiver provide an AC line termination as well as a DC load (2K ohms).
Section 4	The receiver is a 380 NOR Gate Latch.

This technique has been used to transmit and receive data up to 1500 feet on multiple conductor telephone cable.

Figure 67

Section 4
Digital Sure Program

The Signetics SURE*/883 Program consists of a combination of 100 percent and statistical sample tests designed to assure specified performance, continuing uniformity, and long term reliability of Signetics products. These tests are made regularly at no extra cost to the user and are performed in addition to the 40 quality assurance inspections and tests to which every circuit is subjected before final seal. The tests, tabulated below for the specifier's convenience, are performed in accordance with the following conditions, sequence, and schedules on equipment calibrated to meet all requirements of MIL-Q-9858A and MIL-C-45662A.

Every circuit of every lot is processed to the environmental screens shown in Table I. These screens are performed in production and include 100% final production electrical tests. Any unit failing either the environmental screens or the final production electrical tests is rejected and removed from the lot.

After completion of Table I tests, each manufacturing lot is sampled and tested by Quality Assurance for conformance to the requirements of Table II. The unsampled portion of the lot is held pending acceptance of the lot sample. Detailed electrical test limits and conditions applicable to each subgroup are shown in the Electrical Characteristics table of the individual part type data sheets.

Tables IIIA, IIIB, and IIIC provide a complete process qualification and verification program in accordance with the conditions of MIL-STD-883, Group A, B and C tests. These tests are performed once in every 90 day manufacturing period, on representative devices from each standard production die process family and on each production package family. The representative circuits and packages selected are changed routinely, and the tests performed monitor and qualify all structurally similar devices produced by the same process and production during that period. A summary of these test results is available on request at the time of order placement.

* Systematic Uniformity and Reliability Evaluation

All of the applicable Electrical Parameters of Table IIIA are performed at pretest on the Table IIIC samples. This provides the MIL-STD-883 electrical parameter and design verification Group A tests. These tests are performed on representative circuit types from every die process family type in manufacturing during this period.

Table IIIB consists of the package oriented qualification environmental stress tests of MIL-STD-883, Groups B and C. Representative samples from each package product family type are monitored and qualified every 90 day period by these tests. A common device is used as the die type for these package and assembly qualification tests.

Table IIIC consists of the die process oriented qualification electrical stress or operational tests at high temperature per MIL-STD-883, Groups B and C. Representative devices from each die process family are monitored and qualified every 90 day period by these tests. The package type is randomly selected as applicable.

An additional screening series is available at extra cost. Details are given in Table V, MIL-STD-883, method 5004, high reliability screening.

Table I — 100% Production Screen Tests

TEST	CONDITIONS
Preseal Visual	High Power — Low Power
Thermal Shock	Liquid to Liquid, 5 Cycles, 60 Seconds at 0°C, 60 Seconds at 100°C, transfer time 5 Seconds. (See Note 1.)
Centrifuge	Y_1 Axis; 30,000 g minimum, 1 minute. (See Note 1.)
Hermeticity	Gross leak test (Bubble Test). (See Note 1.)
Production Electrical Tests	

Table II — Signetics Acceptance Tests (See Notes 2 and 3)

SIGNETICS SUBGROUP	TEST	CONDITIONS	AQL	MIL-STD-105 INSPECTION LEVEL
A-1	Visual and Mechanical Inspection	MIL-STD-883 Method 2009	1.0%	II
A-2	DC Parameters	$T_A = +25°C$	1.0%	II
A-3	DC Parameters	$T_A = +25°C$	1.0%	II
A-4	DC Parameters	$T_A = +125° C$	1.0%	II
A-5	DC Parameters	$T_A = -55°C$	1.0%	II
A-6	AC Parameters	$T_A = +25°C$	1.0%	II

TABLE IIIA. MIL-STD-883 GROUP A ELECTRICAL TESTS

MIL-STD-883 GROUP A SUBGROUP	SIGNETICS SUBGROUP	TEST DESCRIPTION
A1	A-2, A-3	Static tests at 25°C
A2	A-4	Static tests at maximum rated operating temperature.
A3	A-5	Static tests at minimum rated operating temperature.
A4	A-6	Dynamic tests at 25°C,
A5	C-2, when applicable	Dynamic tests at maximum rated operating temperature.
A6	C-2, when applicable	Dynamic tests at minimum rated operating temperature.
A7	*	Functional tests at 25°C.
A8	A-4, A-5	Functibnal tests at maximum and minimum rated operating temperatures.
A9	A-6	Switching tests at 25°C.
A10	C-2, when applicable	Switching tests at maximum rated operating temperature.
A11	C-2, when applicable	Switching tests at minimum rated operating temperature.

TABLE IIIB. MIL-STD-883 GROUPS B AND C ENVIRONMENTAL TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
B_1	Physical Dimensions	2008	Test Condition A	15
B_2	Marking Permanency Visual and Mechanical Bond Strength	2008 2008 2011	Test Condition B, Para. 3,2,1 Test Condition B Test Condition D	4 devices/no failure 1 device/no failure 15
B_3	Solderability	2003	Solder Temperature 260°C ±10°C	15
B_4	Lead Fatigue Hermeticity a. Fine b. Gross	2004 1014	Test Condition B_2 See Note 4 Test Condition A or B Test Condition C	15
C_1	Pre-Test Electrical Parameters Thermal Shock Temperature Cycle Moisture Resistance End Point Electrical Parameters FAILURE CRITERIA	 1011 1010 1004	Signetics Subgroup A-3 15 Cycles. Test Condition C, +150°C to −65°C 10 Cycles. Test Condition C, 150°C to −65°C Omit initial conditioning. Signetics Subgroup A-3 Refer to Table IV.	15
C_2	Pre-Test Electrical Parameters Mechanical Shock Vibration Variable Frequency Constant Acceleration End Point Electrical Parameters FAILURE CRITERIA	 2002 2007 2001	Signetics Subgroup A-3 Test Condition B Test Condition A Test Condition E Signetics Subgroup A-3 Refer to Table IV.	15
C_3	Salt Atmosphere	1009	Test Condition A. Omit initial conditioning.	15
C_4	Pre-Test Electrical Parameters High Temperature Storage End Point Electrical Parameters FAILURE CRITERIA	 1008	Signetics Subgroup A-3 T_A = +150°C, t = 1000 hours Signetics Subgroup A-3 Refer to Table IV.	 λ = 15

TABLE IIIC. MIL-STD-883 GROUPS B AND C HIGH TEMPERATURE OPERATING LIFE TESTS

MIL-STD-883 GROUP B & C SUBGROUP	TEST DESCRIPTION	MIL-STD-883 METHOD	CONDITIONS	LTPD
	Pre-Test and Design Verification Electrical Parameters		Table IIIA as applicable, data sheet groups A & C.	
C_6	High Temperature Steady State Reverse Bias End Point Electrical Parameters FAILURE CRITERIA	1015	Test Condition A. T_A = 150°C t = 72 hours. Signetics Subgroup A-3 Refer to Table IV	λ = 10
B_5 & C_5	High Temperature Operating Life End Point Electrical Parameters FAILURE CRITERIA	1005	Test Condition D or E as applicable. T_A = +125°C or +85°C, per Part Data Sheet. t = 1000 hours. Signetics Subgroup A-3 Refer to Table IV.	λ = 10

*Signetics performs a truth table test.

Table IV — Signetics Failure Criteria

TEST	"1" Input Current	"1" Output Voltage	"0" Input Current	"0" Output Voltage	Expansion Node Current
LIMITS	Data Sheet Limits and: 10X Initial Value for DTL 5X Initial Value for TTL	Data Sheet Limits and: ±20% Initial Value	Data Sheet Limits ±20% Initial Value	Data Sheet Limits and: ±0.1V	Data Sheet Limits and: ±20% Initial Value

Optional High Reliability Screening

To maximize reliability in critical application, the Optional High Reliability Screening of Table V provides for three levels of 100% screening per MIL-STD-883, Method 5004 at extra cost. This series eliminates the necessity for special specification, minimizes cost and provides the shortest possible delivery time. This series is applied after the normal Group A acceptance test. Circuits subjected to this Preconditioning Series are clearly distinguishable from standard products in the following ways:

1. Individual serial number on each circuit (Class A only).
2. The first letters of a part number are either RA, RB, or RC.

   RA = Class A
   RB = Class B
   RC = Class C
   i.e., RA8880J = 100% screening of Table V, Class A.
3. Individual device variables parametric test data is supplied with each shipment (Class A only).

Consult your local representative for price information. Device types should be specified with the appropriate letter prefixes.

Notes:

1. Not applicable to solid molded packaged devices.
2. All test equipment calibrated to meet requirements of MIL-Q-9858A and MIL-C-45662A.
3. Detailed tests, conditions, and limits applicable to each subgroup are given in the Signetics data sheet ELECTRICAL CHARACTERISTICS table. See Table IIIA for the corresponding Group A tests of MIL-STD-883.
4. The Hermeticity tests are not employed for solid molded packages.
5. Class B and Class C may be subjected to thermal shock as an alternate.
6. The test sequence of fine and gross leak may be reversed when fluorocarbons are utilized for gross leak.
7. The individual MIL-STD-883 Test Methods are, in many cases designed to "stand alone" as a sole screen or sole Group B environmental sampling test. But since 5004 specifies a screening series or flow, some of the measurements, etc., specified in an individual Test Method are not intended to be applicable in the screening series.

TABLE V — MIL-STD-883 METHOD 5004, HIGH RELIABILITY SCREENING

TEST	MIL-STD-883 METHOD	CLASS A	CLASS B	CLASS C	CLARIFICATIONS (See Note 7)
Internal Visual (preseal)	2010.1	Cond. A	Cond. B	Cond. B	Test Condition A, Paragraph 3.1.1.7, a, delete the words "and parameter".
Stabilization Bake	1008 (24 hours)	Cond. C	Cond. C	Cond. C	Condition C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements at this point.
Thermal Shock	1011	Cond C	Not required. NOTE 5	Not required. NOTE 5	Cond. C (150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection at this point.
Temperature Cycling	1010	Cond. C	Cond. C NOTE 5	Cond. C NOTE 5	(150°C) max. for au/al metallization system. Cond. D (200°C) max. for al/al metallization system. No electrical measurements, no external visual inspection, no hermeticity tests at this point.
Mechanical Shock	2002, Y1 plane only	Cond. B	Not Required	Not Required	No electrical measurements at this point.
Centrifuge	2001	Cond. E Y2 then Y1 plane	Cond. E Y1 plane	Cond. E Y1 plane	
Hermeticity A. Fine Leak B. Gross Leak	1014, Note 6 (Hermetic devices only)	 Cond. A or B Cond. C	 Cond. A or B Cond. C	 Cond. A or B Cond. C	
Critical Electrical Parameters	Signetics Subgroup A-3	Read and Record	Not Required	Not Required	
Burn-In Test	1015, T_A = +125°C	240 hours Cond. D or E (as applicable)	168 hours Cond. D or E (as applicable)	Not Required	
Critical Electrical Parameters	Signetics Subgroup A-3	Read and Record	Not Required	Not Required	
Signetics FAILURE CRITERIA		Table IV	Not Required	Not Required	
Reverse Bias Burn-In	1015, T_A = +150°C t = 72 hours	Cond. A or C	Not Required	Not Required	Required only when specified in the applicable procurement document. Signetics standard burn-in (above) includes reverse bias of unused junctions.
Final Electrical Test	Perform go-no-go measurements of Signetics Subgroup A Parameters	Signetics Subgroups A-2, A-4, A-5, A-6, Functional tests, truth table when applicable	Signetics Subgroups A-2, A-3, A-6, Functional tests, truth table when applicable	Signetics Subgroups A-2, A-3 Functional tests, truth table when applicable	
Radiographic Inspection	2012	Yes	Not Required	Not Required	
External Visual	2009	Yes	Yes	Yes	

signetics

811 EAST ARQUES AVENUE • SUNNYVALE, CALIFORNIA
94086 • TEL: (408) 739-7700 • TWX: (910) 339-9283

PRINTED IN U.S.A.

D252 DIG-001-11-35M