Ordering number : EN3155

CMOS LSI

SANYO No.3155

LC8945

SCSI (Small Computer System Interface) Protocol Controller

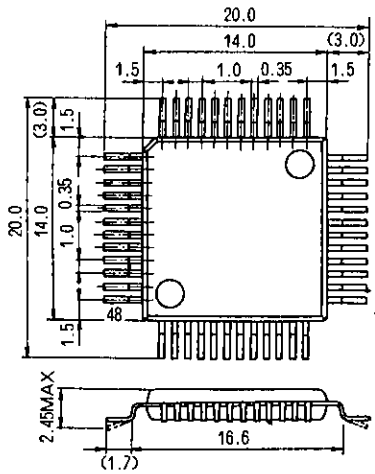
Overview

The LC8945 SCSI controller provides complete support and arbitration for asynchronous data transfer between an MPU bus and a single-ended SCSI bus. It is capable of operating as either initiator or target roles, and incorporates automatic arbitration, selection and reselection functions, parity generation and checking circuits, and 48mA open-drain line drivers. It does not support synchronous data transfer.
The LC8945 uses a high-speed low-power 1.5µm CMOS process. It operates with a 20MHz clock and a single 5V power supply. The LC8945 is available in either a 48-pin QIP package or a 68-pin PLCC package.

Features

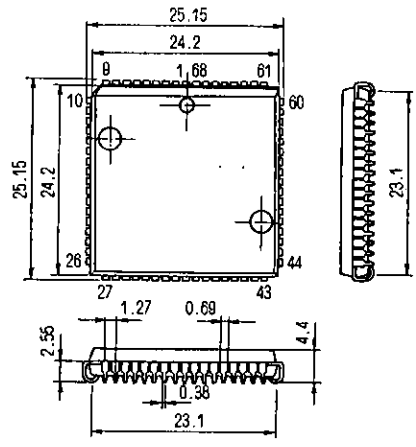
- SCSI protocol controller
- Data transfer under program or DMA control
- Maximum asynchronous transfer rate of more than 5MB/s
- Capable of operating as either initiator or target
- Automatic arbitration, selection and reselection functions
- Parity generation and checking circuits
- 48mA currents sink open-drain SCSI bus drivers
- 24-bit transfer counter, 24-bit timeout counter

Package Dimensions 3052A-Q48AIC
(unit: mm)



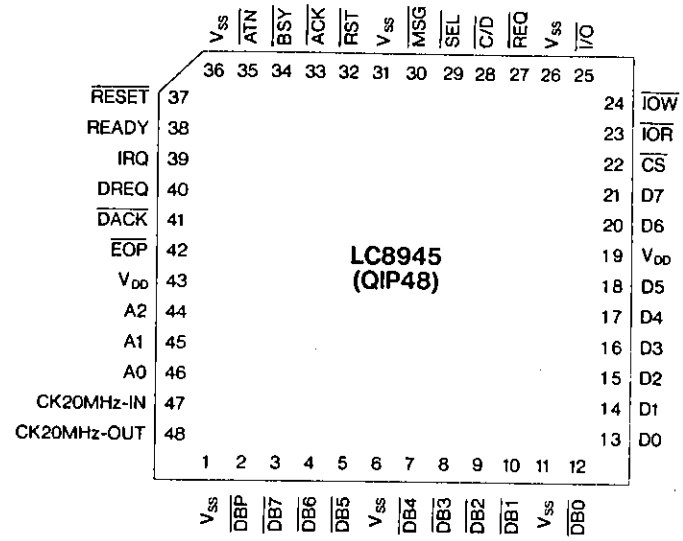
48PIN
QIP-48A

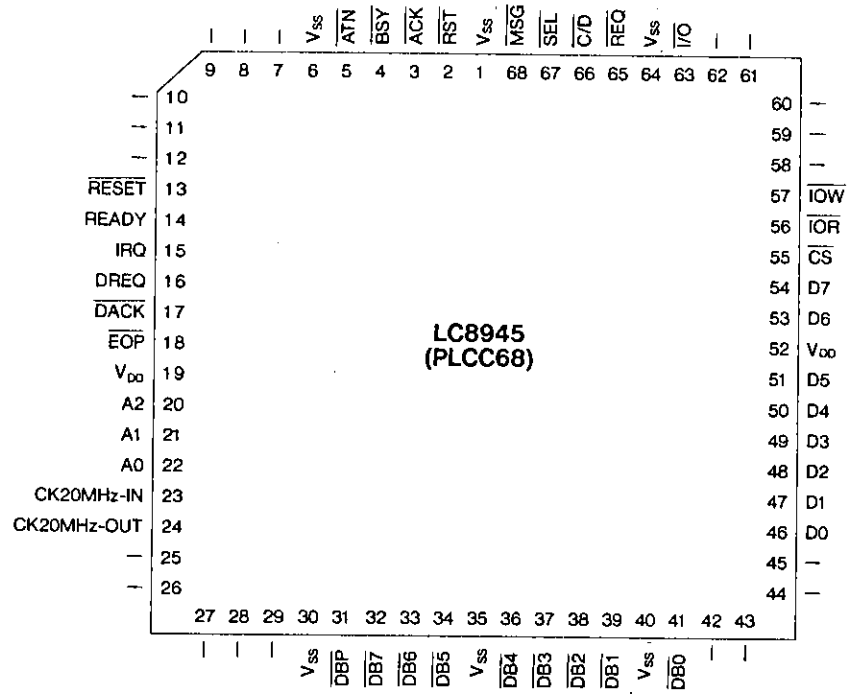
Package Dimensions 3132-PLCC68VL
(unit: mm)



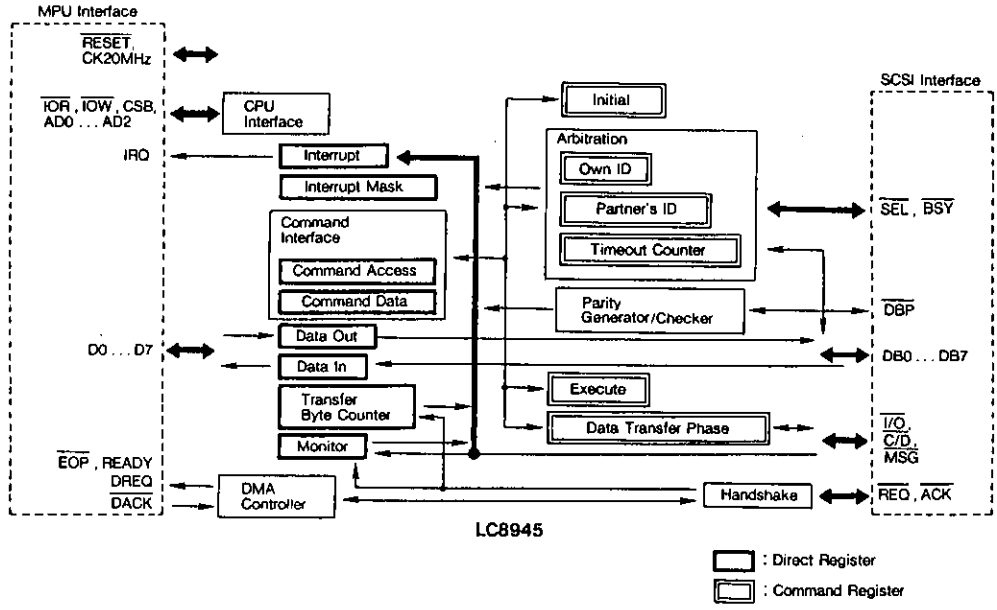
68PIN
PLCC-68

Pin Assignment





Equivalent Circuit Block Diagram



Pin Description

<MPU Interface>

A0 to A2	Input	Internal register address select : The addressed register is selected when $\overline{CS}$ = "0"
$\overline{CS}$	Input	Chip select : Enables write to and read from internal registers.
$\overline{DACK}$	Input	DMA acknowledge : $\overline{DACK}$ resets DREQ and connects the Data-In and Data-Out data transfer registers to D0 to D7.
DREQ	Output	DMA request : DREQ requests read from and write to the data transfer registers in DMA transfer mode
D0 to D7	Input/Output	MPU data bus : D0 to D7 are connected to the internal registers.
$\overline{EOP}$	Output	End of process : Command completion with byte being currently transferred or already transferred in DMA transfer mode
READY	Output	Accepts DMA acknowledge in DMA transfer mode
$\overline{IOR}$	Input	I/O read : Data in the register specified by A0 to A2 is placed on the MPU data bus.
$\overline{IOW}$	Input	I/O write : Data on the MPU data bus is written into the register specified by A0 to A2.
IRQ	Output	MPU interrupt request line : Active HIGH on command completion or abortion, or on error condition.
$\overline{RESET}$	Input/Output	Initializes the LC8945
CK20MHz-IN	Input	Internal oscillator amplifier input
CK20MHz-OUT	Output	Internal oscillator amplifier output A 20MHz crystal may be connected between CK20MHz-IN and CK20MHz-OUT, or an external 20MHz clock may be applied to CK20MHz-IN.

<SCSI Interface>

The SCSI interface consists of the signals listed below. These signals conform fully to the SCSI specification. Refer to the SCSI standard documentation for the functions of these signals.

$\overline{ACK}$	$\overline{REQ}$
$\overline{ATN}$	$\overline{RST}$
$\overline{BSY}$	$\overline{SEL}$
$\overline{C/D}$	$\overline{DB0}$ to $\overline{DB7}$
$\overline{I/O}$	$\overline{DBP}$
$\overline{MSG}$	

Direct Registers

A2	A1	A0	R/W	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	W	Interrupt Mask	MSK	"0"	"0"	"0"	"0"	"0"	"0"	"0"
0	0	0	R	Interrupt	END	ERR	ABRT	PMM	TO	PE	RST	ATN
0	0	1		·····RESERVED····								
0	1	0	W	Command No	CN7	CN6	CN5	CN4	CN3	CN2	CN1	CN0
0	1	0	R	Monitor	PM1	PM2	I/O	C/D	MSG	ATN	RST	DATA
0	1	1	R/W	Command Data	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
1	0	0	R/W	Transfer 1	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
1	0	1	R/W	Byte 2	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
1	1	0	R/W	Counter 3	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
1	1	1	W	Data-out	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0
1	1	1	R	Data-in	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

<Interrupt Mask> Address 0, Write Register

When all bits of the interrupt register are not 0, the interrupt mask determines whether the IRQ signal should be output or not.

All bits "1" : IRQ signal is output.

All bits "0" : IRQ signal is not output.

<Interrupt> Address 0, Read Register

When the LC8945 requests interrupt service from the CPU, the appropriate bits of the interrupt register are set HIGH, and IRQ is set HIGH.

Bit 7 : END Command execution complete.
- (1) Selection
- (2) Reselection
- (3) Data transfer

Bit 6 : ERR Abnormal condition occurred during command execution.
- (1) ID number incorrect
- (2) A Start Reselection command is ineffective, when arbitration is disabled by the Initialize command.

Bit 5 : ABRT Command execution aborted.
- (1) Defeated by arbitration.

Bit 4 : PMM Phase mismatch.

The set values of I/O, C/D and MSG conflicted with the SCSI bus I/O, C/D and MSG values during the data transfer phase.

Bit 3 : TO Timeout executed during selection/reselection phase.

Bit 2 : PE Parity error.

Only occurs if parity check has been set by the Initialize command : parity check error in selection/reselection phase or data transfer phase.

Bit 1 : RST SCSI bus $\overline{RST}$ signal active

Bit 0 : ATN Initiator requires attention.

<Command Access, Command Data> Address 2,3, Write Register
The Command Access and Command Data registers are used to write commands to the LC8945, or to read the partner's ID. Refer to Commands.

<Monitor> Address 3, Read Register
Bit 7,6 : Phase Monitor

PM1	PM0	Description
0	0	Another
0	1	Arbitration-Phase
1	0	Selection · Reselection-Phase
1	1	Data Transfer Phase

Bit 5 : I/O SCSI bus I/O signal value
Bit 4 : C/D SCSI bus C/D signal value
Bit 3 : MSG SCSI bus MSG signal value
Bit 2 : ATN SCSI bus ATN signal value
Bit 1 : RST SCSI bus RST signal value
Bit 0 : DATA True if data is present in the data transfer registers during a data transfer phase.

<Transfer Byte Counter> Address 4,5,6, Read/Write Register
The data transfer counter is 24 bits wide. Transfer Byte Counter register 1 is the least significant 8 bits, and counter 3 is the most significant 8 bits. Since data transfer starts when Transfer Byte Counter 1 is set, Transfer Byte Counter 2 and 3, and any other registers that need to be set must be written to beforehand.

<Data Out Register> Address 7, Write Register
Data is transferred from the MPU bus to the SCSI bus during the Data Transfer Phase via the Data-Out Register.

<Data In Register> Address 7, Read Register
Data is transferred from the SCSI bus to the MPU bus during the Data Transfer Phase via the Data-In Register.

Commands

The command data CD0 to CD7 is first written to the Command Data Register, then the command code CA0 to CA2 is written to the Command Access Register.
The command code is first written into the Command Data Register, then the Command Access Register is read to access the specified data.

CA2	CA1	CA0	R/W	Command Name	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
0	0	0	W	Initial	I/T	ARB	MONO	PC	"0"	"0"	"0"	"0"
0	0	1	W	Set Own ID	"0"	"0"	"0"	"0"	"0"	OI2	OI1	OI0
0	1	0	W	Set Partner's ID	"0"	"0"	"0"	"0"	"0"	PI2	PI1	PI0
0	1	0	R	Get Partner's ID	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
0	1	1	W	Set Timeout Counter	TC24	TC23	TC22	TC21	TC20	TC19	TC18	TC17
1	0	0		·····RESERVED·····								
1	0	1	W	Set Data Transfer Phase	I/O	C/D	MSG	DMA	BLK	"0"	"0"	"0"
1	1	0		·····RESERVED·····								
1	1	1	R/W	Execute	SEL	RSL	ATN	RST	DTP	CLR	"0"	RRR

<Initialize> Command 000

SCSI operational mode is set according to bits 4 to 7 written into the Command Data Register.

Bit 7 : Initiator/Target
Bit 6 : Arbitration Select/Deselect
Bit 5 : Initiator Single/Multiple
Bit 4 : Parity Check Select/Deselect
Bit 3 : "0"
Bit 2 : "0"
Bit 1 : "0"
Bit 0 : "0"

<Set Own ID> Command 001

The binary value written into the Command Data Register bits 2 to 0 is set as the Own ID.

<Partner's ID> Command 010

The binary value written into the Command Data Register bits 2 to 0 is set as the Partner's ID.

<Get Partner's ID> Command 010

The value read from the Command Access Register is the partner's ID, where the position of the set bit indicates the ID, as follows :

Bit 7 : Partner's ID = 7
Bit 6 : Partner's ID = 6
Bit 5 : Partner's ID = 5
Bit 4 : Partner's ID = 4
Bit 3 : Partner's ID = 3
Bit 2 : Partner's ID = 2
Bit 1 : Partner's ID = 1
Bit 0 : Partner's ID = 0

<Set Timeout Counter> Command 011

The value written into the Command Data Register is loaded into the timeout counter. Value between 13.1ms and 6.7s may be set.

<Set Data Transfer Phase> Command 101

Transfer mode is set according to bits 4 to 7 written into the Command Data Register.

Bit 7 : I/O
Bit 6 : C/D
Bit 5 : MSG
Bit 4 : DMA/Program
Bit 3 : Block/Single
Bit 2 : "0"
Bit 1 : "0"
Bit 0 : "0"

<Execute> Command 111

The phase specified by the value written into the Command Data Register is started.

Bit 7 : Selection
Bit 6 : Reselection
Bit 5 : Attention
Bit 4 : SCSI reset
Bit 3 : Data Transfer Phase
Bit 2 : Clear
Bit 1 : "0"
Bit 0 : RRR (Chip Reset)

Absolute Maximum Ratings at $V_{SS}=0V$

				unit
Maximum Supply Voltage	V_{DD} max	Ta=25°C	−0.3 to +7.0	V
Input/Output Voltage	V_I, V_O	Ta=25°C	−0.3 to V_{DD}+0.3	V
Operating Temperature	Topr		−30 to +70	°C
Storage Temperature	Tstg		−55 to +125	°C
Soldering Temperature		10s . (at pin)	260	°C

Allowable Operating Conditions at Ta=−30 to +70°C, $V_{SS}=0V$

		min	typ	max	unit
Supply Voltage	V_{DD}	4.5		5.5	V
Input Voltage	V_{IN}	0		V_{DD}	V

DC Characteristics at $V_{SS}=0V$, $V_{DD}=4.5$ to 5.5V, Ta=−30 to +70°C

(1) SCSI Interface

			min	typ	max	unit
Input 'H'-Level Voltage	V_{IH1}		2.0			V
Input 'L'-Level Voltage	V_{IL1}				0.8	V
Output 'L'-Level Voltage	V_{OL1}	$I_{OL}=48mA$			0.5	V

(2) MPU Interface (Except CK20MHz-IN, CK20MHz-OUT)

			min	typ	max	unit
Input 'H'-Level Voltage	V_{IH2}		2.2			V
Input 'L'-Level Voltage	V_{IL2}				0.8	V
Output 'H'-Level Voltage	V_{OH2}	$I_{OL}=3mA$			2.4	V
Output 'L'-Level Voltage	V_{OL2}	$I_{OL}=3mA$			0.4	V