KMM332V803AS-L Fast Page Mode

8Mx32 Based on 8Mx8, 4K Refresh, 3.3V, Low power/Self-Refresh

GENERAL DESCRIPTION

The Samsung KMM332V803A is a 8M bit x 32 Dynamic RAM high density memory module. The Samsung KMM332V803A consists of four CMOS 8Mx8bit DRAMs in 32-pin TSOPII packages mounted on a 72-pin four layer zigzag glass-epoxy substrate. 0.1uF or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM332V803A is a Dual In-line Memory Module with edge connections and is intended for mounting into 72 pin dual readout zigzag edge connector sockets.

FEATURES

- Part Identification
  - KMM332V803AS-L6/L7
    (4096 cycles/128ms Ref, TSOP, Low Power, 60/70ns)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- **JEDEC standard PDPin & pinout (72 pin)**
- **PCB : Height(1000mil), double sided component**

PERFOMANCE RANGE

Speed	tRAC	tCAC	tRC
- L6	60ns	15ns	110ns
- L7	70ns	20ns	130ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	DQ18
2	DQ0	38	DQ19
3	DQ1	39	Vss
4	DQ2	40	$\overline{CAS0}$
5	DQ3	41	$\overline{CAS2}$
6	DQ4	42	$\overline{CAS3}$
7	DQ5	43	$\overline{CAS1}$
8	DQ6	44	$\overline{RAS0}$
9	DQ7	45	NC
10	Vdd	46	NC
11	PD1	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ20
14	A2	50	DQ21
15	A3	51	DQ22
16	A4	52	DQ23
17	A5	53	DQ24
18	A6	54	DQ25
19	A10	55	NC
20	NC	56	DQ27
21	DQ9	57	DQ28
22	DQ10	58	DQ29
23	DQ11	59	DQ31
24	DQ12	60	DQ30
25	DQ13	61	Vdd
26	DQ14	62	DQ32
27	DQ15	63	DQ33
28	A7	64	DQ34
29	A11	65	NC
30	Vdd	66	PD2
31	A8	67	PD3
32	A9	68	PD4
33	NC	69	PD5
34	$\overline{RAS2}$	70	PD6
35	DQ16	71	PD7
36	NC	72	Vss

PIN NAMES

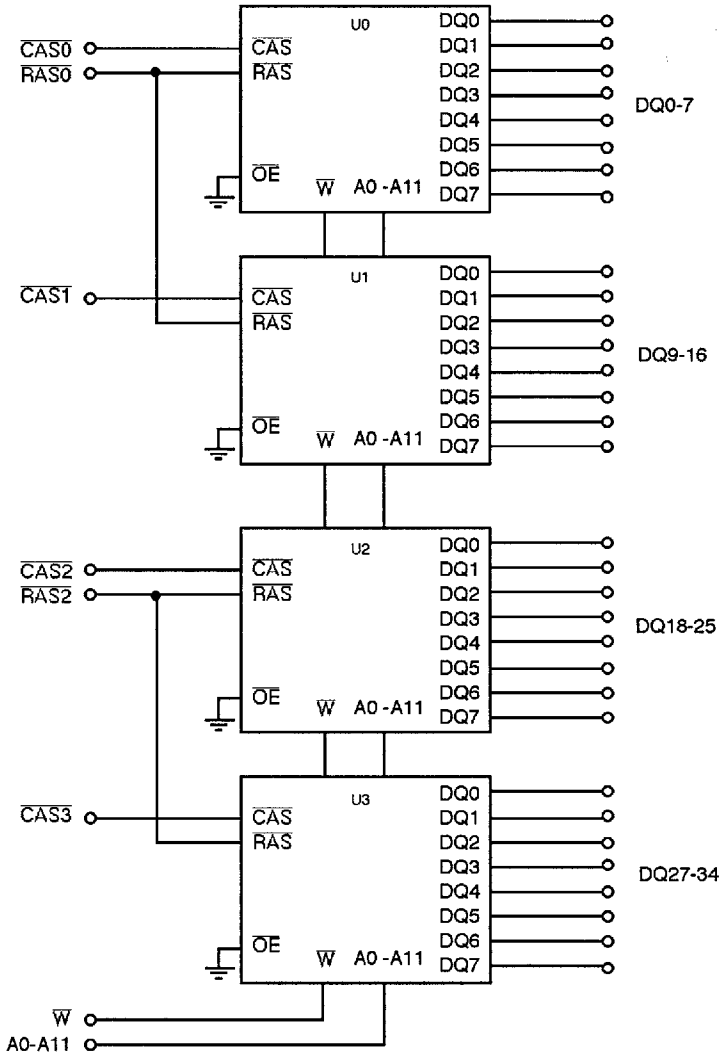
A0 - A11	Address Inputs
DQ(0-7,9-16, 18-25,27-34)	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 - PD7	Presence Detect
Vdd	Power(+3.3V)
Vss	Ground
NC	No Connection

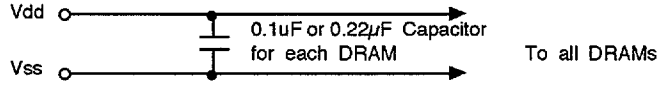
PRESENCE DETECT PINS (Optional)

Pin	60NS	70NS
PD1	Vss	Vss
PD2	Vss	Vss
PD3	NC	NC
PD4	NC	NC
PD5	NC	Vss
PD6	NC	NC
PD7	Vss	Vss

*Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-0.5 to +4.6	V
Voltage on Vdd supply relative to Vss	Vdd	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	4	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vdd	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.0	-	Vdd+0.3 *1	V
Input Low Voltage	VIL	-0.3 *2	-	0.8	V

*1: Vdd+1.3V/15ns(3.3V), Pulse width is measured at Vdd.
*2: -1.3V/15ns(3.3V), Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	KMM332V803AS		Unit
		Min	Max	
ICC1	- L6	-	560	mA
	- L7	-	520	mA
ICC2		-	4	mA
ICC3	- L6	-	560	mA
	- L7	-	520	mA
ICC4	- L6	-	280	mA
	- L7	-	260	mA
ICC5		-	1200	μA
ICC6	- L6	-	560	mA
	- L7	-	520	mA
ICC7		-	2200	μA
ICCS		-	1800	μA
II(L)		-20	20	μA
IO(L)		-5	5	μA
VOH		2.4	-	V
VOL		-	0.4	V

ICC1 : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @tRC=min.)
ICC2 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=VIH)
ICC3 : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$= VIH, $\overline{RAS}$ cycling @tRC =min.)
ICC4 : Fast Page Mode Current * ($\overline{RAS}$=VIL, $\overline{CAS}$ cycling : tPC=min.)
ICC5 : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=Vdd-0.2V)
ICC6 : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC =min.)
ICC7: Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(VIH)=Vcc-0.2V, Input low voltage(VIL)=0.2V, $\overline{CAS}$=0.2V)
DQ0-31=Don't care, tRC=31.25μS, tRAS=tRASmin~ 300ns
ICCS: Self Refresh Current ($\overline{RAS}$=$\overline{CAS}$=VIL, W=OE=A0-A11=Vcc-0.2V or 0.2V, DQ0-DQ31=Vcc-0.2V, 0.2V or OPEN
II(L) : Input Leakage Current (Any input 0 ≤ VIN ≤ Vdd+0.3V, all other pins not under test = 0 V.)
IO(L) : Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vdd)
VOH : Output High Voltage Level (IOH = -2mA)
VOL : Output Low Voltage Level (IOL = 2mA)

* NOTE : ICC1,ICC3,ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one page mode cycle .

CAPACITANCE (Ta = 25 °C, f=1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A11]	CIN1	-	30	pF
Input capacitance [$\overline{W}$]	CIN2	-	38	pF
Input capacitance [$\overline{RAS0}$, $\overline{RAS2}$]	CIN3	-	24	pF
Input capacitance [$\overline{CAS0}$ - $\overline{CAS3}$]	CIN4	-	17	pF
Input/Output capacitance [DQ0-7,9-16,18-25,27-34]	CDQ1	-	17	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vdd=3.3 V±0.3V. See notes 1,2.)

Test condition : Vih /Vil = 2.0V / 0.8 V , Voh / Vil = 2.0V / 0.8 V , Output Loading CL=100pF

STANDARD OPERATIO	Symbo	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		ns	
Access time from $\overline{RAS}$	tRAC		60		70	ns	3,4
Access time from $\overline{CAS}$	tCAC		15		20	ns	3,4,5
Access time from column address	tAA		30		35	ns	3,11
$\overline{CAS}$ to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	tRP	40		50		ns	
$\overline{RAS}$ pulse width	tRAS	60	10K	70	10K	ns	
$\overline{RAS}$ hold time	tRSH	15		20		ns	
$\overline{CAS}$ hold time	tCSH	60		70		ns	
$\overline{CAS}$ pulse width	tCAS	15	10K	20	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	tRCD	20	45	20	50	ns	4
$\overline{RAS}$ to column address delay time	tRAD	15	30	15	35	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		15		ns	
Column address hold referenced to $\overline{RAS}$	tAR	45		55		ns	6
Column Address to $\overline{RAS}$ lead time	tRAL	30		35		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to $\overline{CAS}$	tRCH	0		0		ns	9
Read command hold referenced to $\overline{RAS}$	tRRH	0		0		ns	9
Write command hold time	tWCH	10		15		ns	
Write command hold referenced to $\overline{RAS}$	tWCR	45		55		ns	6
Write command pulse width	tWP	10		15		ns	
Write command to $\overline{RAS}$ lead time	tRWL	15		20		ns	
Write command to $\overline{CAS}$ lead time	tCWL	15		20		ns	
Data-in set-up time	tDS	0		0		ns	10
Data-in hold time	tDH	10		15		ns	10
Data-in hold referenced to $\overline{RAS}$	tDHR	45		55		ns	6
Refresh period	tREF		128		128	ms	
Write command set-up time	tWCS	0		0		ns	8
$\overline{CAS}$ setup time (C-B-R refresh)	tCSR	5		5		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	tCHR	10		15		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	tRPC	5		5		ns	

STANDARD OPERATIO	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Access time from $\overline{CAS}$ precharge	tCPA		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		ns	
$\overline{CAS}$ precharge time (Fast page)	tCP	10		10		ns	
$\overline{RAS}$ pulse width (Fast page)	tRASP	60	100K	70	100K	ns	
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	tWRP	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	tWRH	10		10		ns	
$\overline{CAS}$ precharge(C-B-R counter test)	tCPT	20		30		ns	
$\overline{RAS}$ pulse width(C-B-R self refresh)	tRASS	100		100		us	12
$\overline{RAS}$ precharge time(C-B-R self refresh)	tRPS	110		150		ns	12
$\overline{CAS}$ hold time(C-B-R self refresh)	tCHS	- 50		- 50		ns	12

NOTES

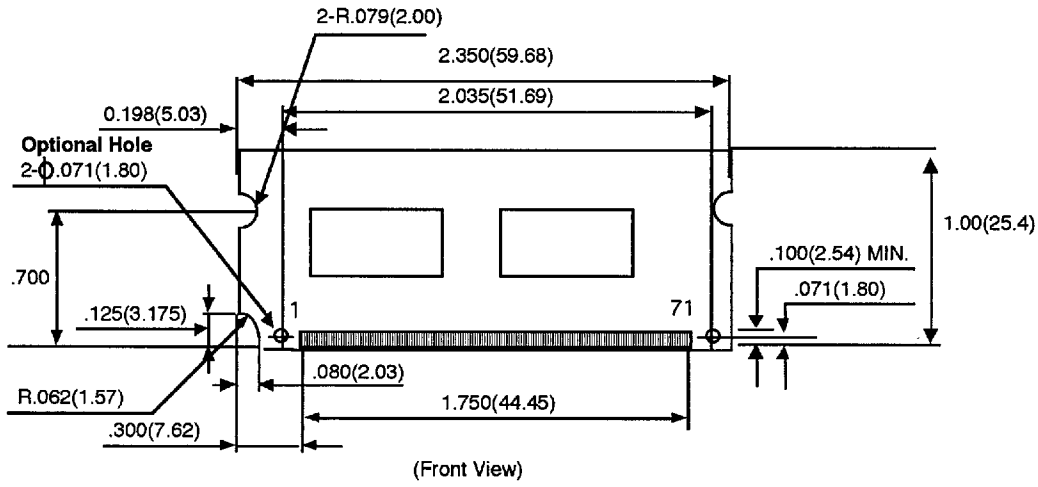
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF, Voh=2.0V and Vol=0.8V.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD(max).
6. tAR, tWCR, tDHR are referenced to tRAD(MAX)
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenc -ed to VOH or VOL.
8. tWCS is non restrictive operating parameter. It included in the data sheet as electrical characteristic only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
9. Either tRCH or tRRH must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
11. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.
12. 4096 cycle of Burst Refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

TIMING DIAGRAM

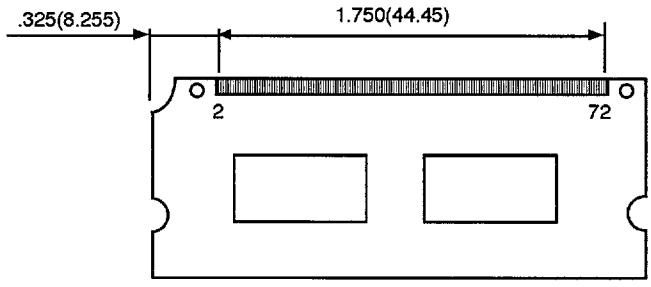
Please refer to attached timing chart (III) !!!

PACKAGE DIMENSIONS

Units : Inches (millimeters)

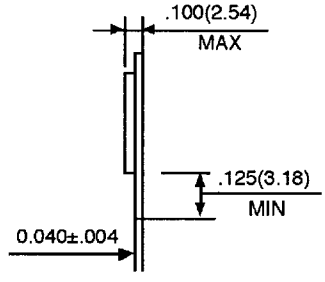


(Front View)

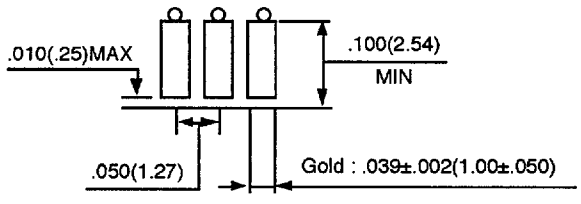


(Back View)

KMM332V803AS-L



Gold Plating Lead

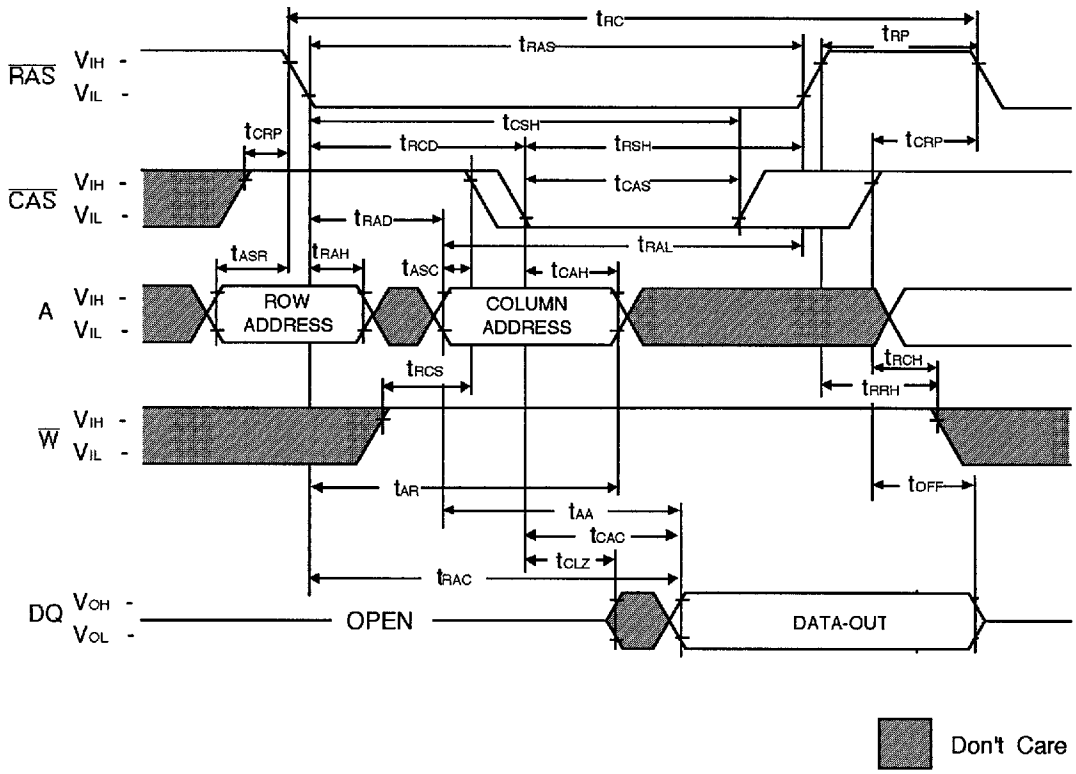


Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 8Mx8 DRAM. , TSOP Ⅱ
DRAM Part No. : KM48V8100AS-L (400 mil) with Self Refresh

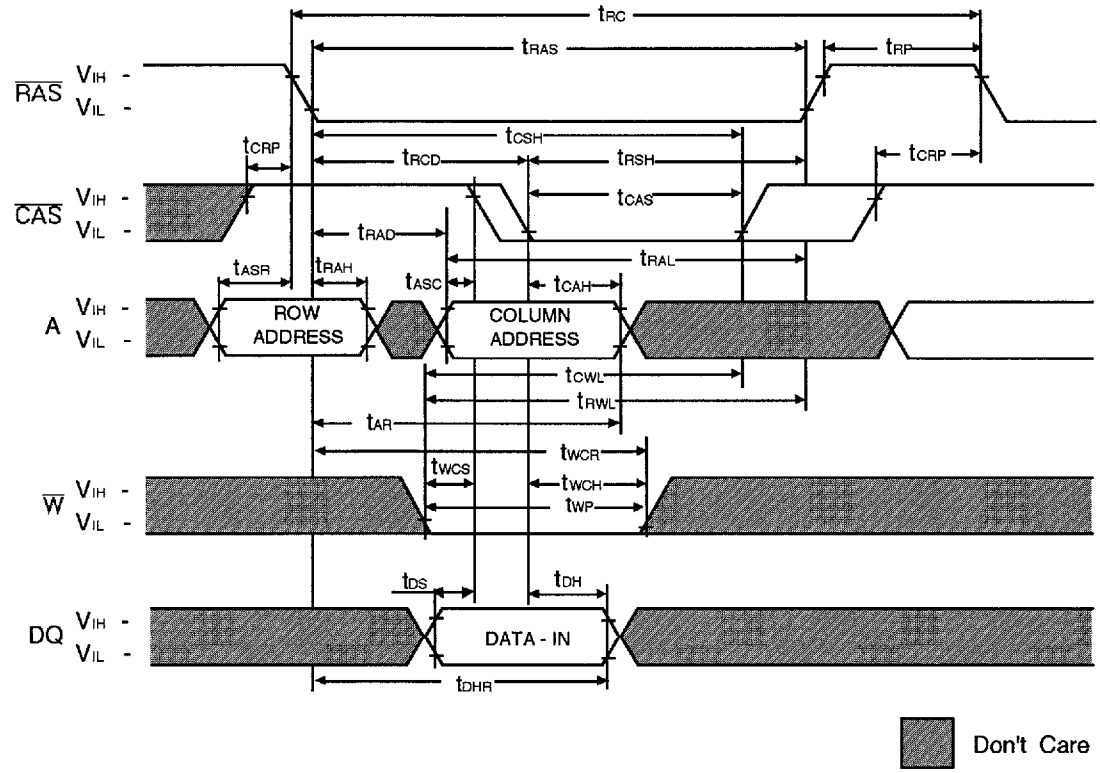
TIMING DIAGRAM

READ CYCLE



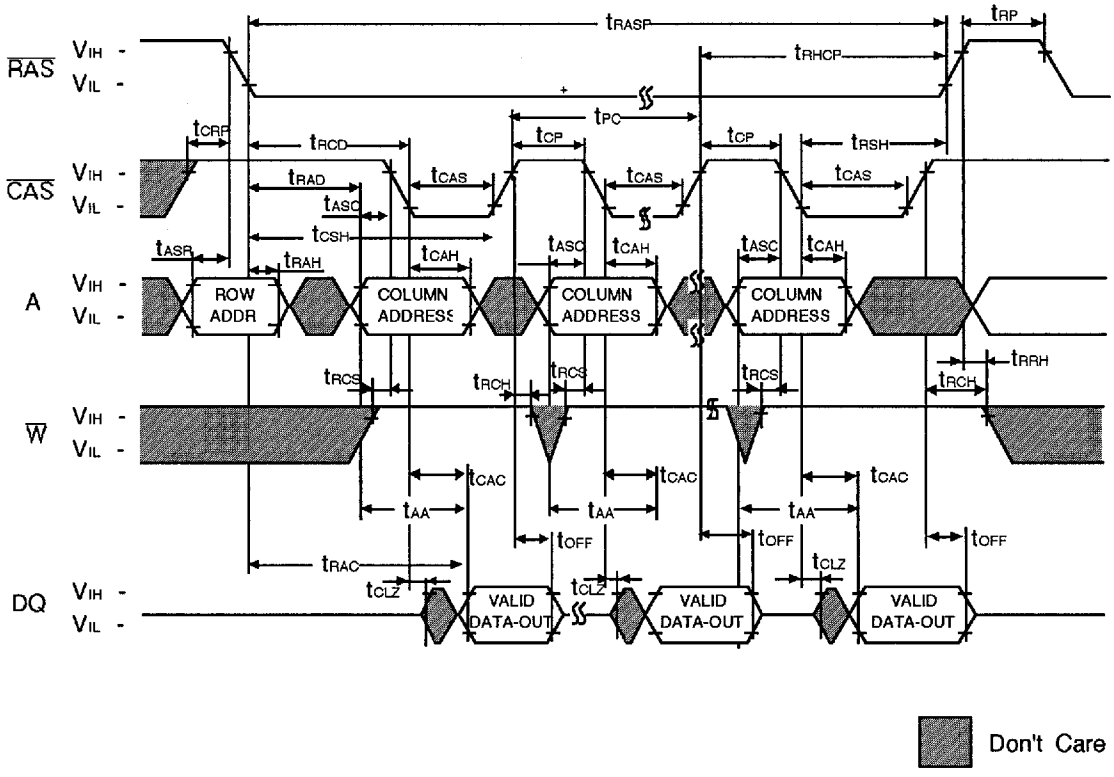
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



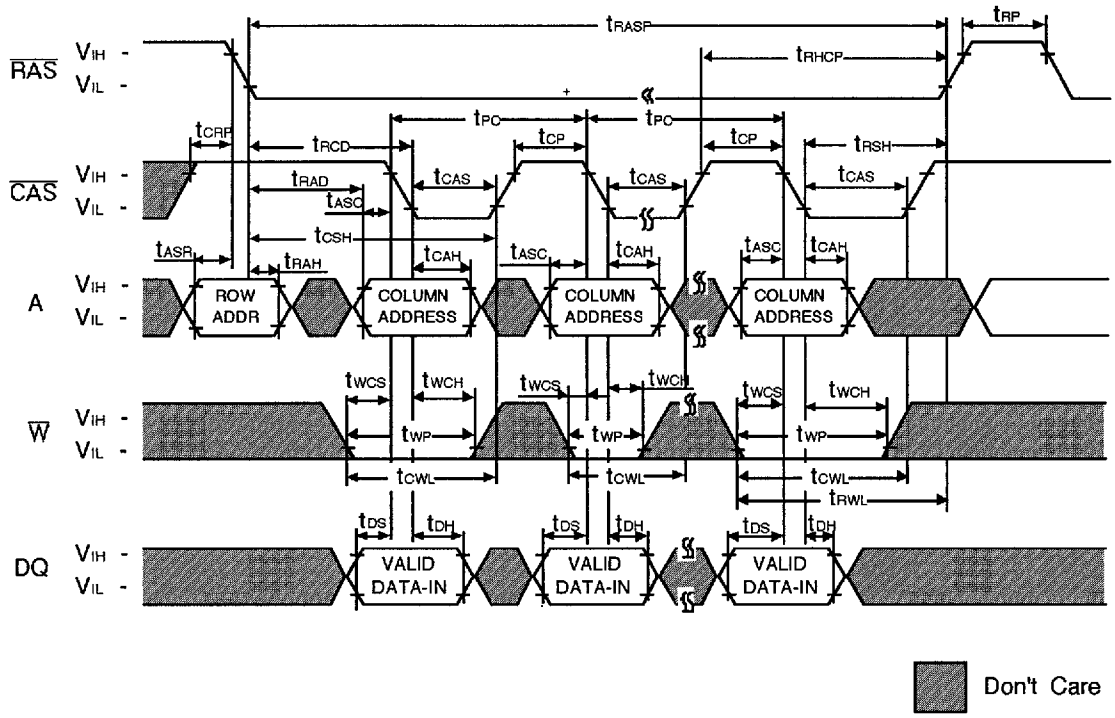
FAST PAGE READ CYCLE

NOTE : D_{OUT} = Open



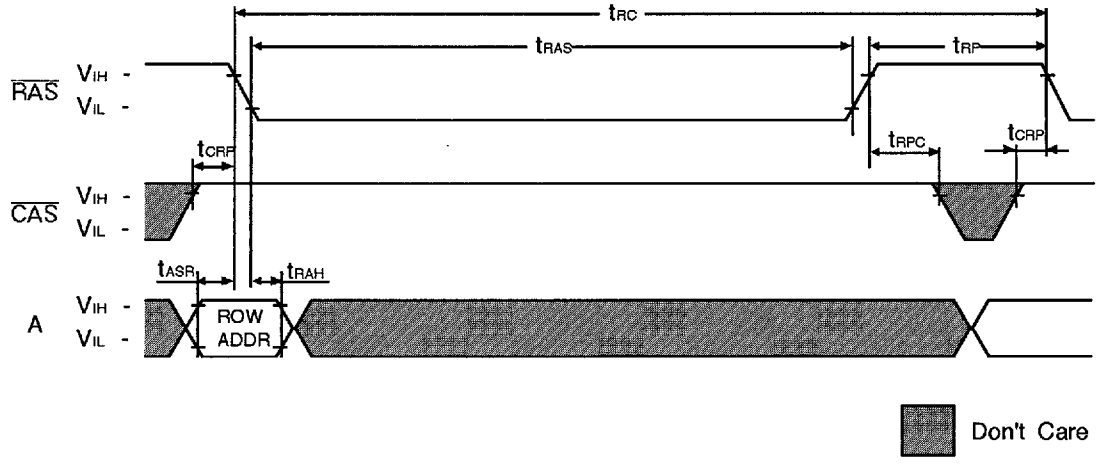
FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



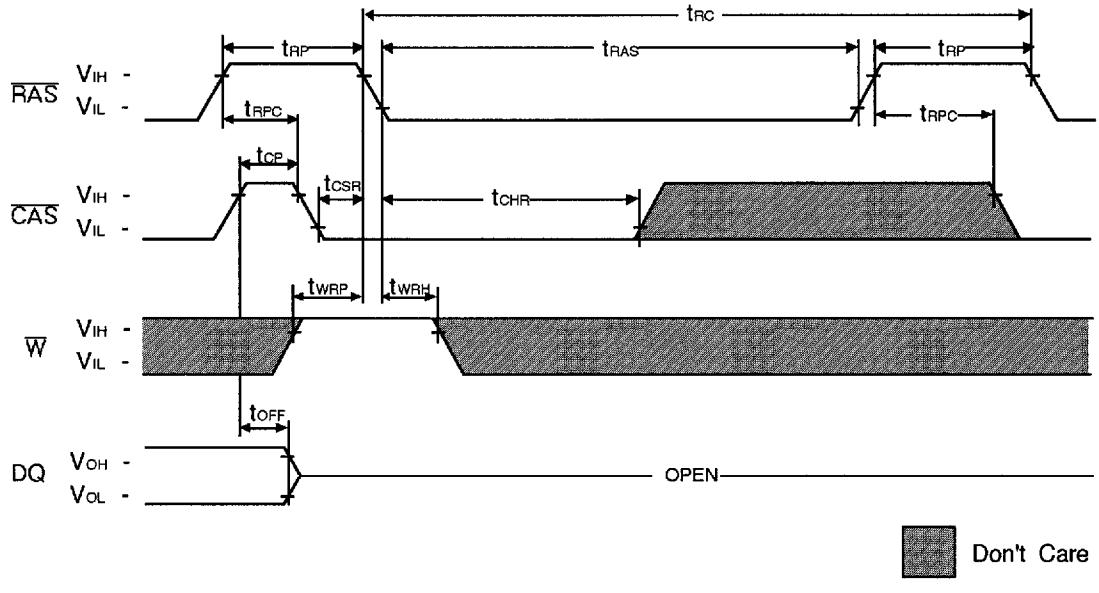
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

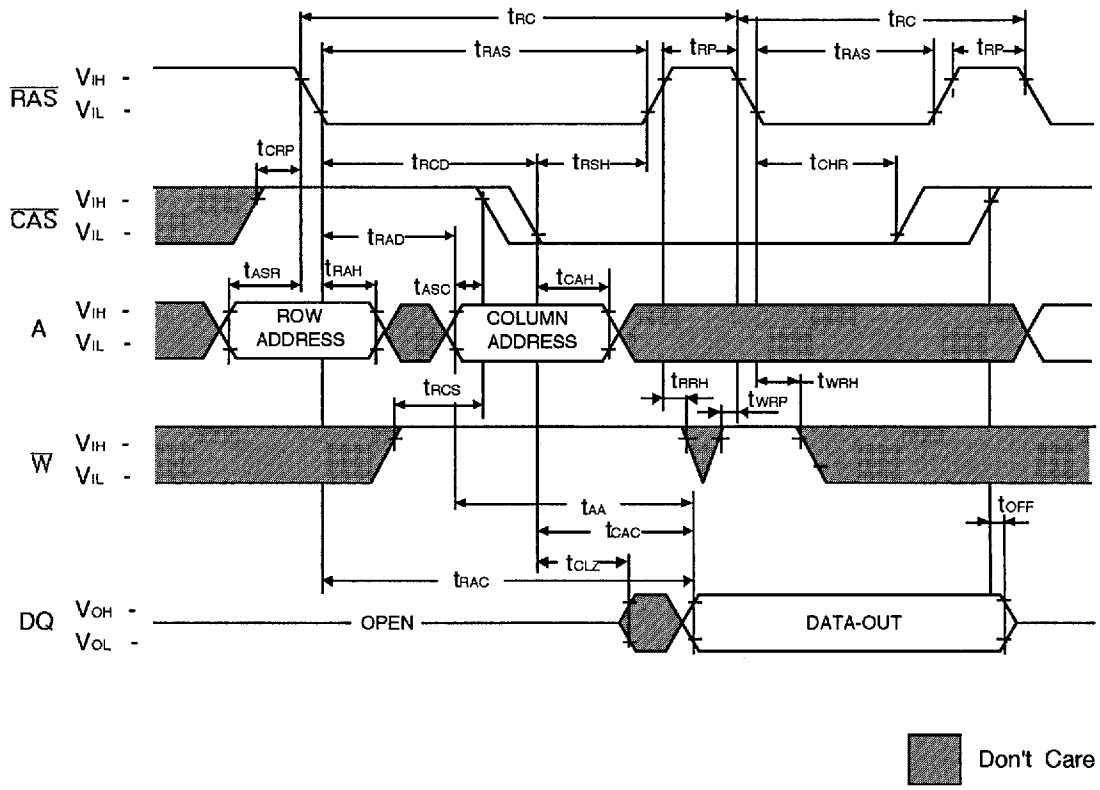


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't Care

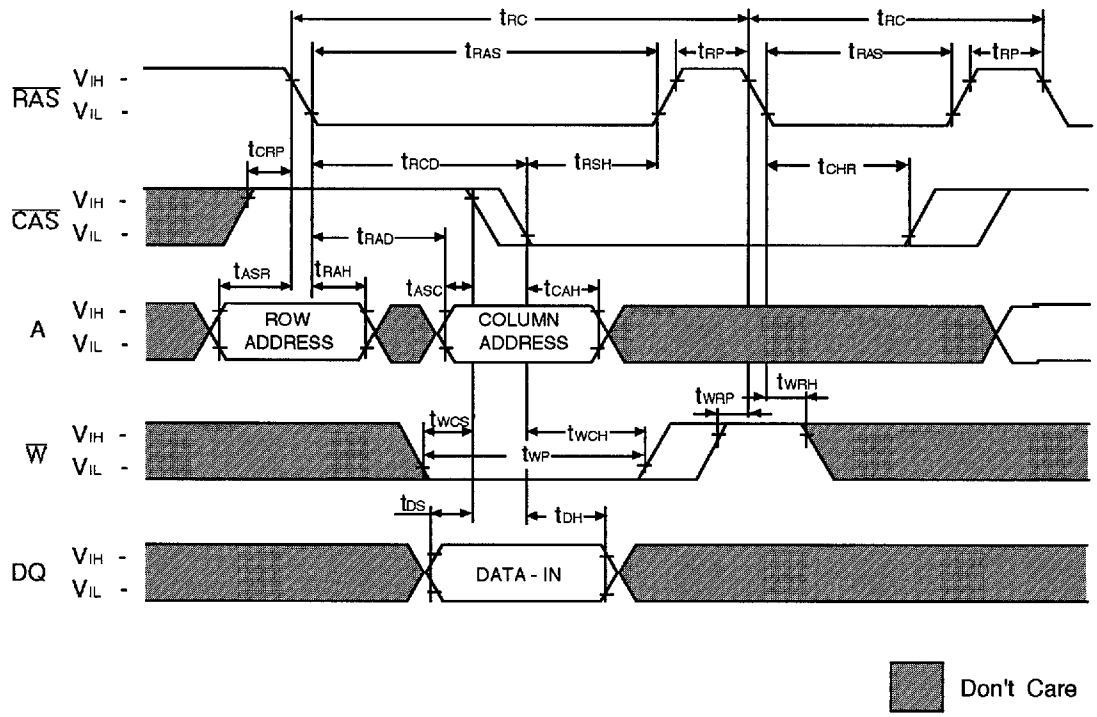


HIDDEN REFRESH CYCLE (READ)

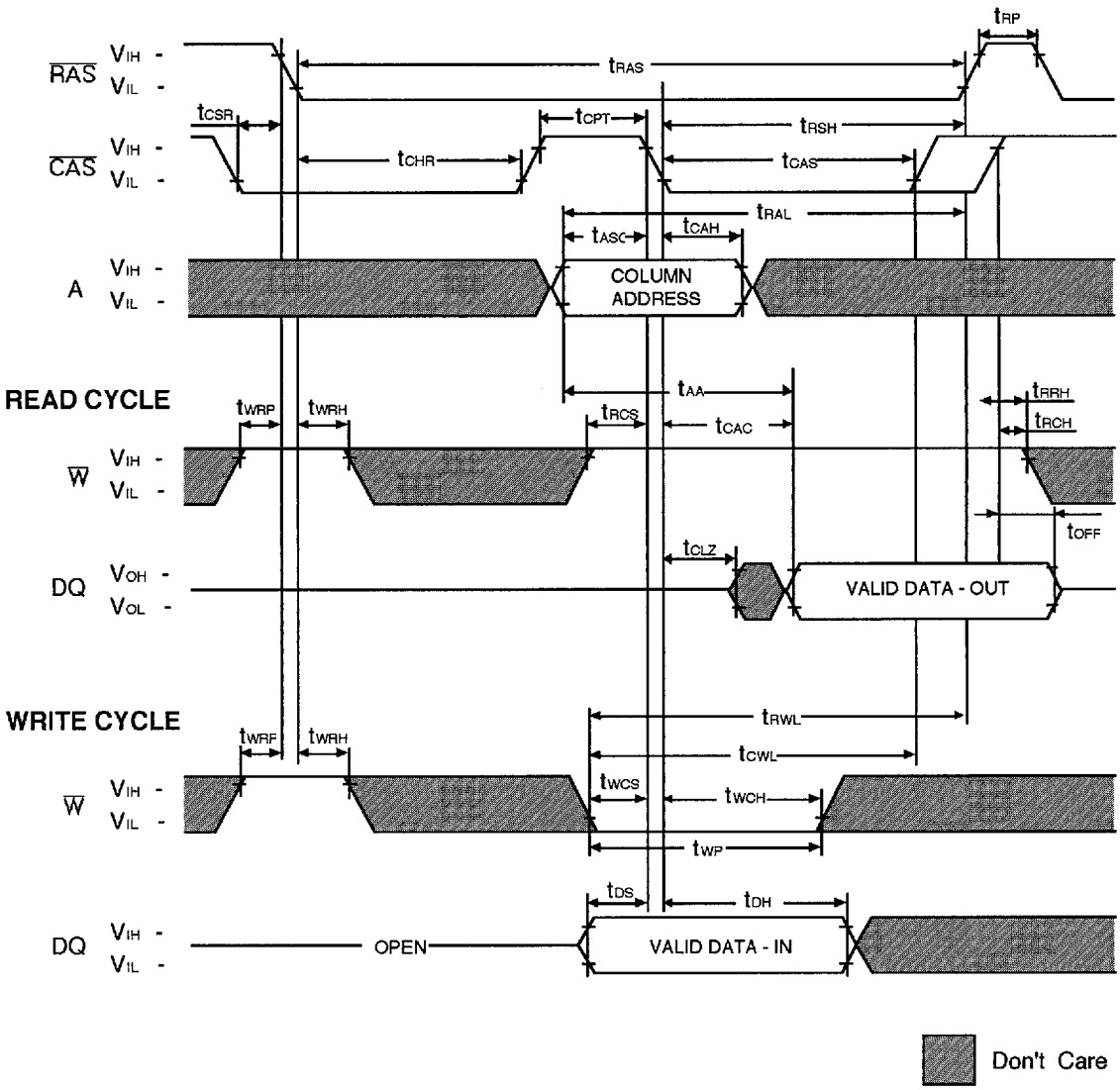


HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN

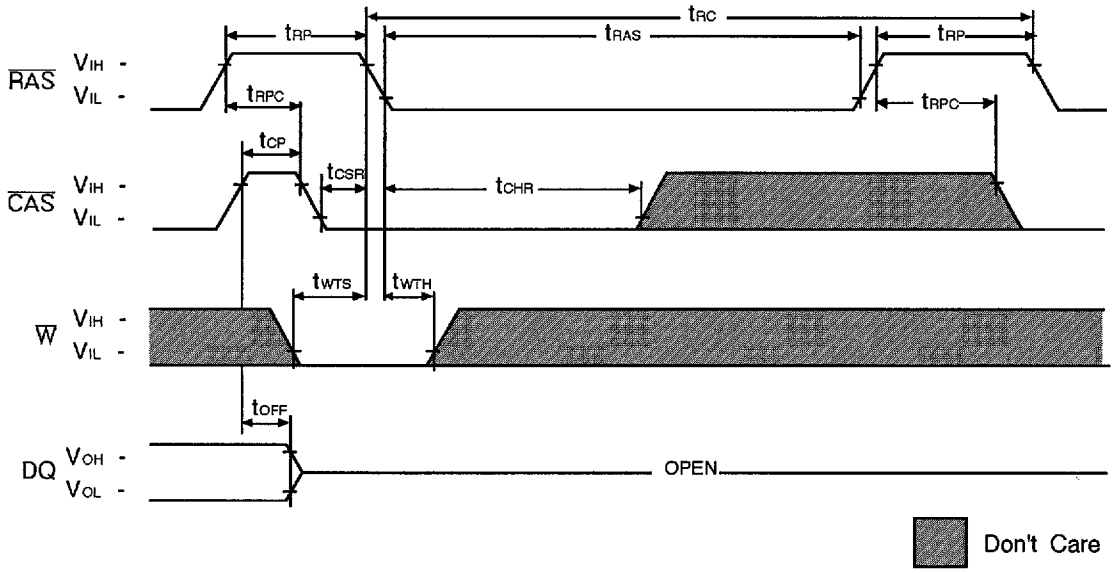


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE

NOTE : $\overline{OE}$, A = Don't Care



CAS-BEFORE-RAS SELF REFRESH CYCLE

NOTE : $\overline{W}$=VIH, $\overline{OE}$, A = Don't Care