KMM5322200BW/BWG Fast Page Mode

2Mx32 DRAM SIMM, 1K Refresh, 5V, using 1Mx16 DRAM

GENERAL DESCRIPTION

The Samsung KMM5322200BW is a 2M bit x 32 Dynamic RAM high density memory module. The Samsung KMM5322200BW consists of four CMOS 1Mx16 bit DRAMs in 42-pin SOJ packages mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22 uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM5322200BW is a Single In-line Memory Module with edge connections and is intended for mounting into 72-pin edge connector sockets.

FEATURES

- Part Identification
  - KMM5322200BW (1024 cycles/16ms Ref, SOJ, Solder)
  - KMM5322200BWG (1024 cycles/16ms Ref, SOJ, Gold)
- Fast Page Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- JEDEC standard PDPin & pinout
- **PCB : Height(750mil), double sided component**

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC
- 6	60ns	15ns	110ns
- 7	70ns	20ns	130ns

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	Vss
4	DQ1	40	$\overline{CAS0}$
5	DQ17	41	$\overline{CAS2}$
6	DQ2	42	$\overline{CAS3}$
7	DQ18	43	$\overline{CAS1}$
8	DQ3	44	$\overline{RAS0}$
9	DQ19	45	$\overline{RAS1}$
10	Vcc	46	NC
11	NC	47	$\overline{W}$
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	Res(A10)	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	Res(A11)	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	$\overline{RAS3}$	69	PD3
34	$\overline{RAS2}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

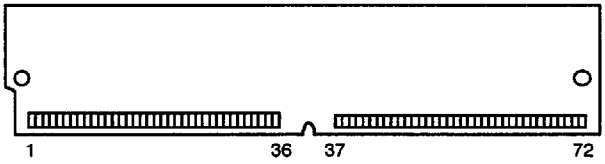
Pin Name	Function
A0 - A9	Address Inputs
DQ0 - DQ31	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
PD1 - PD4	Presence Detect
Vcc	Power (+5V)
Vss	Ground
NC	No Connection
Res	Reserved Pin

PRESENCE DETECT PINS (Optional)

Pin	60NS	70NS
PD1	NC	NC
PD2	NC	NC
PD3	NC	Vss
PD4	NC	NC

*Pin Connection Changing Available

PIN CONNECTIONS (Front View)



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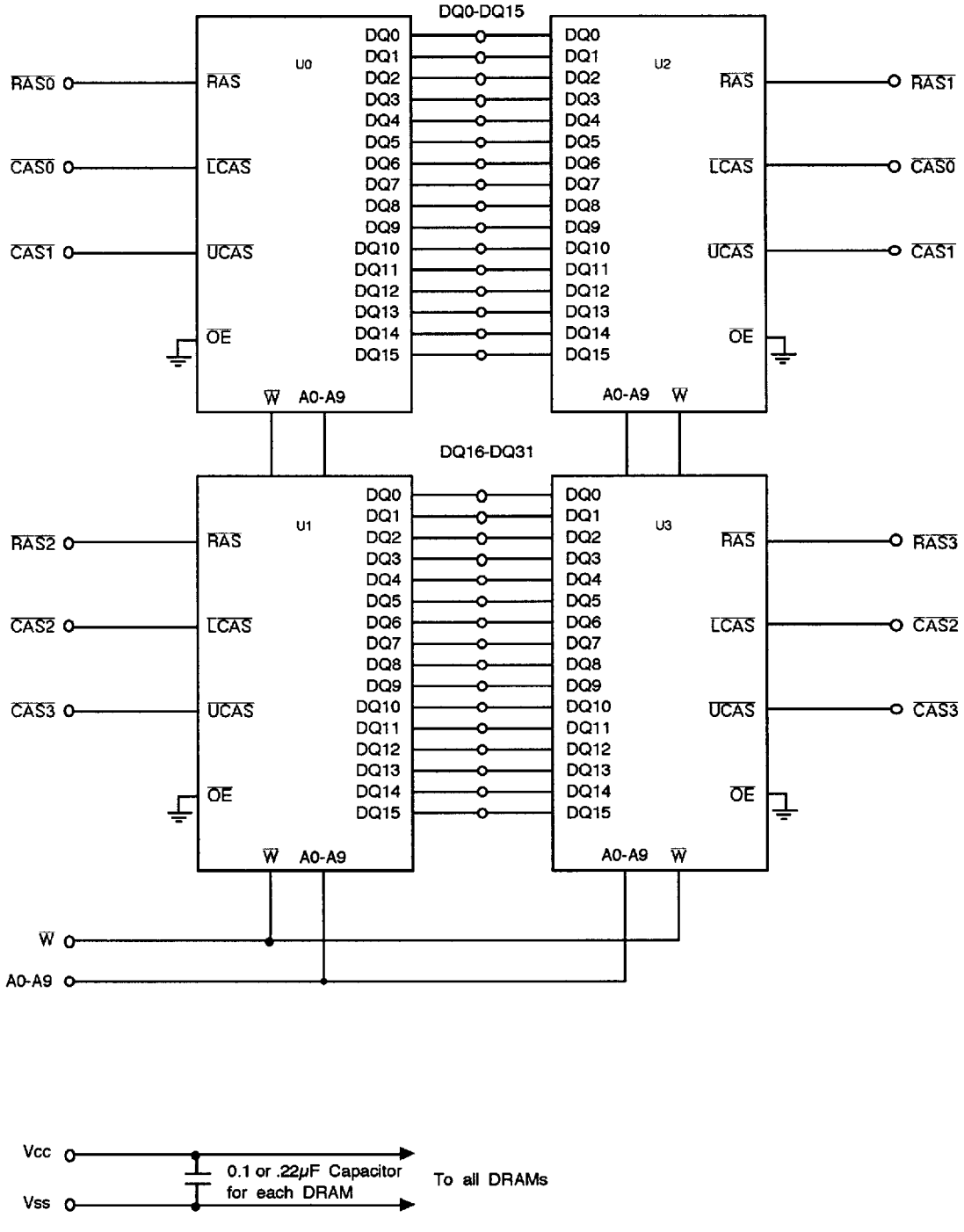
FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN,VOUT	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	Vcc	-1 to +7.0	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	Pd	4	W
Short Circuit Output Current	IOS	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, Ta=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	VIH	2.4	-	Vcc+1 *1	V
Input Low Voltage	VIL	-1.0 *2	-	0.8	V

*1 : Vcc+2.0V/20ns, Pulse width is measured at Vcc.
*2 : -2.0V/20ns, Pulse width is measured at Vss.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Symbol	Speed	KMM5322200BW/BWG		Unit
		Min	Max	
ICC1	- 6	-	304	mA
	- 7	-	284	mA
ICC2		-	8	mA
ICC3	- 6	-	304	mA
	- 7	-	284	mA
ICC4	- 6	-	184	mA
	- 7	-	164	mA
ICC5		-	4	mA
ICC6	- 6	-	304	mA
	- 7	-	284	mA
II(L)		-20	20	μA
IO(L)		-10	10	μA
VOH		2.4	-	V
VOL		-	0.4	V

ICC1 : Operating Current * ($\overline{RAS}$, $\overline{LCAS}$ or $\overline{UCAS}$ Address cycling @tRC=min.)
ICC2 : Standby Current ($\overline{RAS}$=$\overline{LCAS}$=$\overline{UCAS}$=$\overline{W}$=VIH)
ICC3 : $\overline{RAS}$ Only Refresh Current * ($\overline{LCAS}$=$\overline{UCAS}$=VIH, $\overline{RAS}$, Address cycling @tRC=min.)
ICC4 : Fast Page Mode Current * ($\overline{RAS}$=VIL, $\overline{LCAS}$ or $\overline{UCAS}$, Address cycling @tPC=min.)
ICC5 : Standby Current ($\overline{RAS}$=$\overline{LCAS}$=$\overline{UCAS}$=$\overline{W}$=Vcc-0.2V)
ICC6 : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @tRC=min.)
II(L) : Input Leakage Current (Any input 0 ≤ VIN ≤ Vcc+0.5V, all other pins not under test = 0V)
IO(L) : Output Leakage Current (Data out is disabled, 0V ≤ Vout ≤ Vcc)
VOH : Output High Voltage Level (IOH = - 5mA)
VOL : Output Low Voltage Level (IOL = 4.2mA)

* NOTE : ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, address can be changed maximum once while $\overline{RAS}$=VIL. In ICC4, address can be changed maximum once within one page mode cycle, tPC.

CAPACITANCE (Ta=25°C, Vcc=5V, f =1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance [A0-A9]	CIN1	-	35	pF
Input capacitance [W]	CIN2	-	45	pF
Input capacitance [RAS0 ~ RAS2]	CIN3	-	20	pF
Input capacitance [CAS0 ~ CAS3]	CIN4	-	30	pF
Input/Output capacitance [DQ0-31]	CDQ	-	30	pF

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1, 2.)

Test condition : Vih/Vil=2.4V/0.8V, Voh/Vol=2.4V/0.4V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
Random read or write cycle time	tRC	110		130		ns	
Access time from RAS	tRAC		60		70	ns	3,4
Access time from CAS	tCAC		15		20	ns	3,4,5
Access time from column address	tAA		30		35	ns	3,10
CAS to output in Low-Z	tCLZ	0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	ns	6
Transition time (rise and fall)	tT	3	50	3	50	ns	2
RAS precharge time	tRP	40		50		ns	
RAS pulse width	tRAS	60	10K	70	10K	ns	
RAS hold time	tRSH	15		20		ns	
CAS hold time	tCSH	60		70		ns	
CAS pulse width	tCAS	15	10K	20	10K	ns	
RAS to CAS delay time	tRCD	20	45	20	50	ns	4
RAS to column address delay time	tRAD	15	30	15	35	ns	10
CAS to RAS precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	10		15		ns	
Column Address to RAS lead time	tRAL	30		35		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold referenced to CAS	tRCH	0		0		ns	8
Read command hold referenced to RAS	tRRH	0		0		ns	8
Write command hold time	tWCH	10		15		ns	
Write command pulse width	tWP	10		15		ns	
Write command to RAS lead time	tRWL	15		15		ns	
Write command to CAS lead time	tCWL	15		15		ns	
Data-in set-up time	tDS	0		0		ns	9
Data-in hold time	tDH	10		15		ns	9
Refresh period	tREF		16		16	ms	
Write command set-up time	tWCS	0		0		ns	7
CAS setup time (C-B-R refresh)	tCSR	5		5		ns	
CAS hold time (C-B-R refresh)	tCHR	10		10		ns	
RAS precharge to CAS hold time	tRPC	5		5		ns	
Access time from CAS precharge	tCPA		35		40	ns	3
Fast Page mode cycle time	tPC	40		45		ns	
CAS precharge time (Fast page)	tCP	10		10		ns	
RAS pulse width (Fast page)	tRASP	60	200K	70	200K	ns	

AC CHARACTERISTICS (0°C≤Ta≤70°C, Vcc=5.0V±10%. See notes 1, 2.)

Test condition : Vih/Vil=2.4V/0.8V, Voh/Vol=2.4V/0.4V, Output loading CL=100pF

STANDARD OPERATION	Symbol	-6		-7		Unit	Notes
		Min	Max	Min	Max		
$\overline{W}$ to $\overline{RAS}$ precharge time(C-B-R refresh)	tWRP	10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time(C-B-R refresh)	tWRH	10		10		ns	
$\overline{CAS}$ precharge(C-B-R counter test)	tCPT	20		25		ns	

NOTES

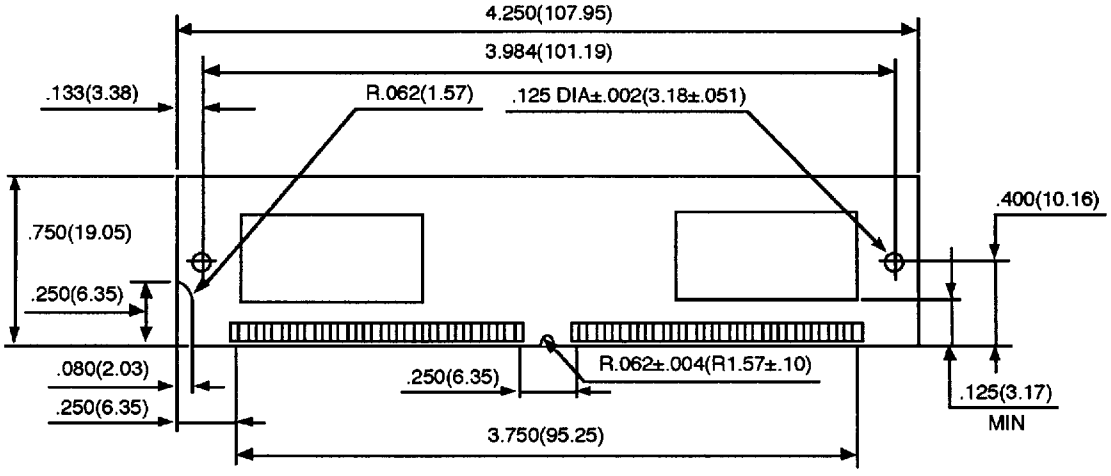
1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min) and VIL(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2TTL loads and 100pF.
4. Operation within the tRCD(max) limit insures that tRAC(max) can be met. tRCD(max) is specified as a reference point only. If tRCD is greater than the specified tRCD(max) limit, then access time is controlled exclusively by tCAC.
5. Assumes that tRCD ≥ tRCD(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenc -ed to VOH or VOL.
7. tWCS is non restrictive operating parameter. It is included in the data sheet as electrical characteristic only. If tWCS≥tWCS(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either tRCH or tRRH must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the tRAD(max) limit insures that tRAC (max) can be met. tRAD(max) is specified as reference point only. If tRAD is greater than the specified tRAD (max) limit, then access time is controlled by tAA.

TIMING DIAGRAM

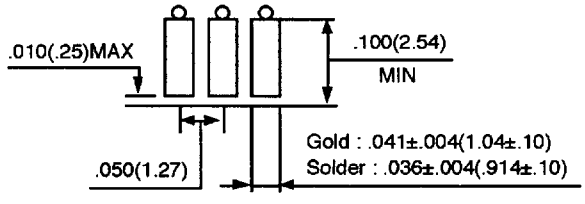
Please refer to attached timing chart (I) !!!

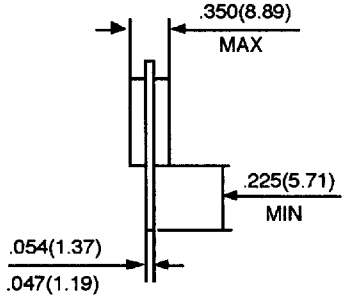
PACKAGE DIMENSIONS (Front View)

Units : Inches (millimeters)



Gold & Solder Plating Lead





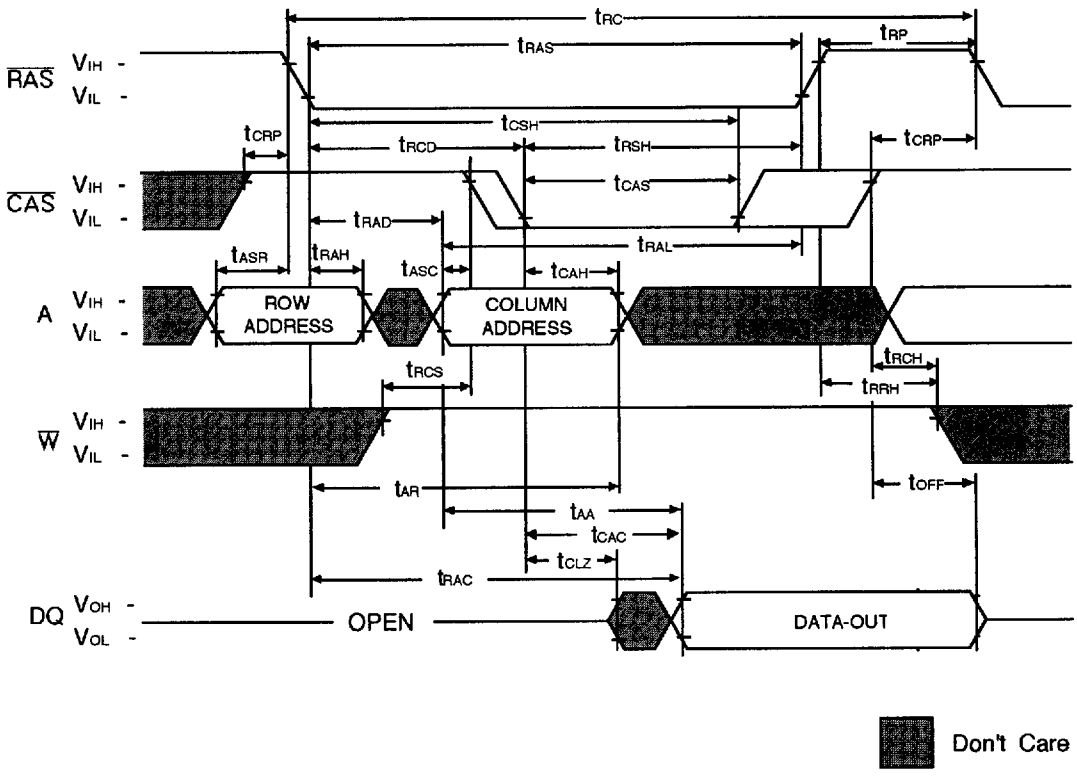
Tolerances : ±.005(.13) unless otherwise specified

NOTE : The used device is 1Mx16 DRAM.
DRAM Part No. : KM416C1200BJ (400 mil)

Revision History
Rev 0.0 : 10 Sep. '95

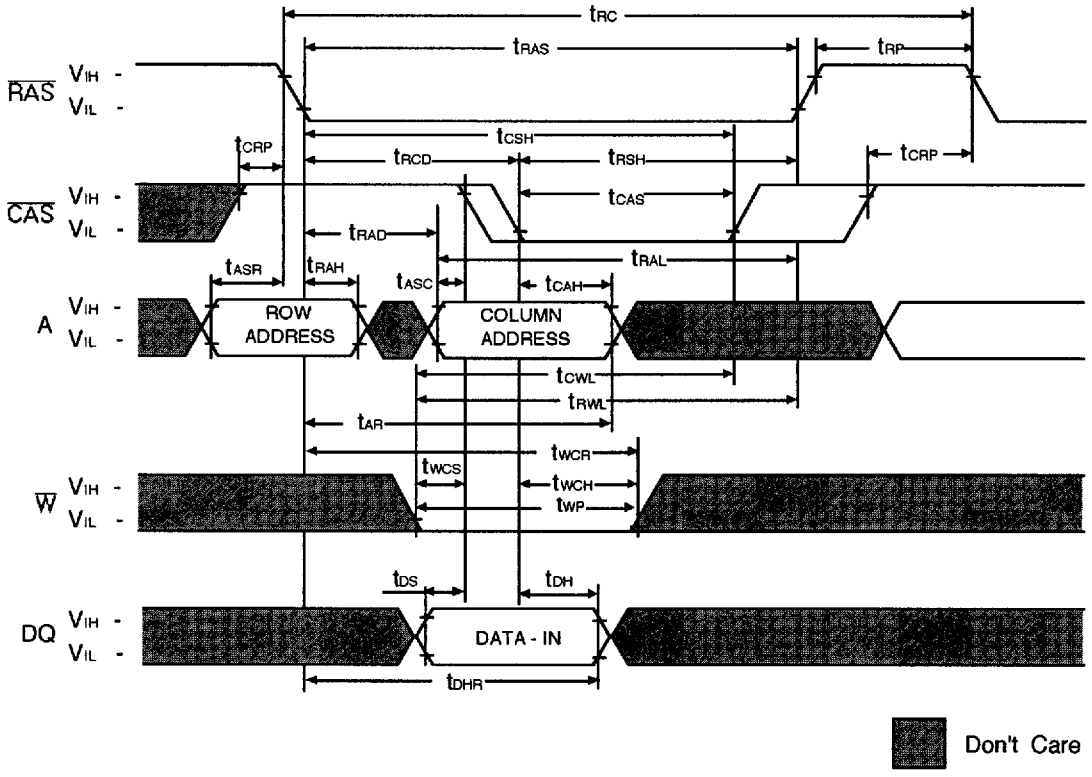
TIMING DIAGRAM

READ CYCLE



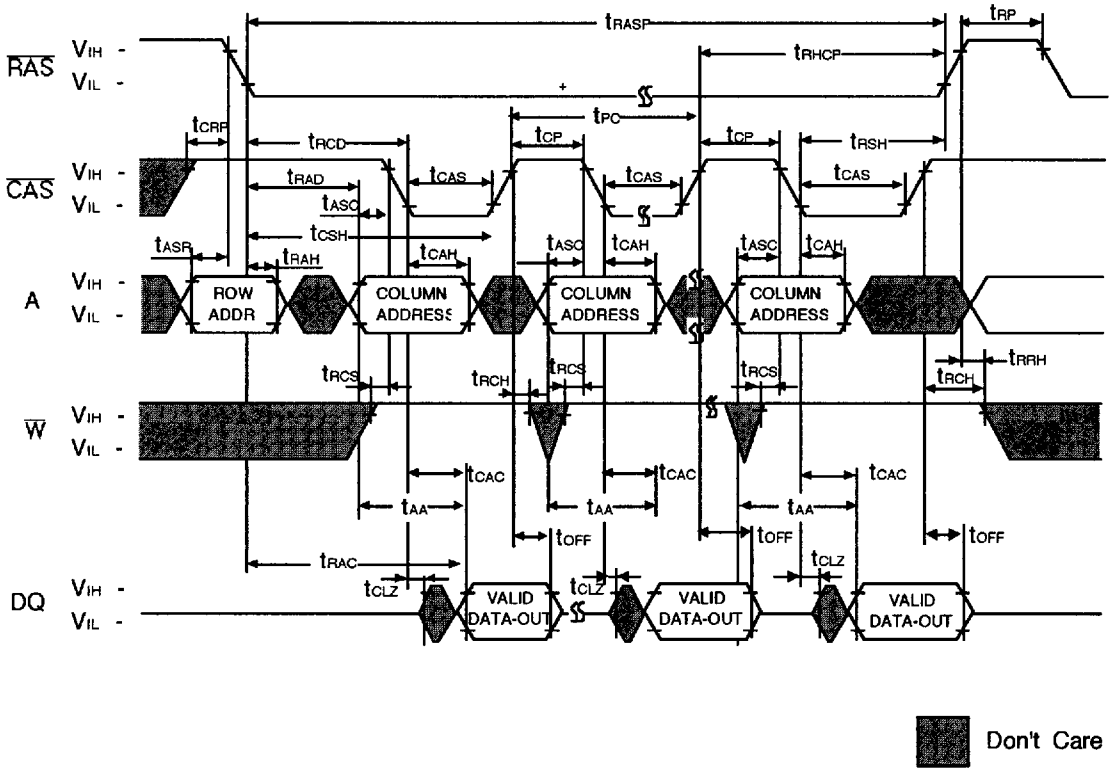
WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = OPEN



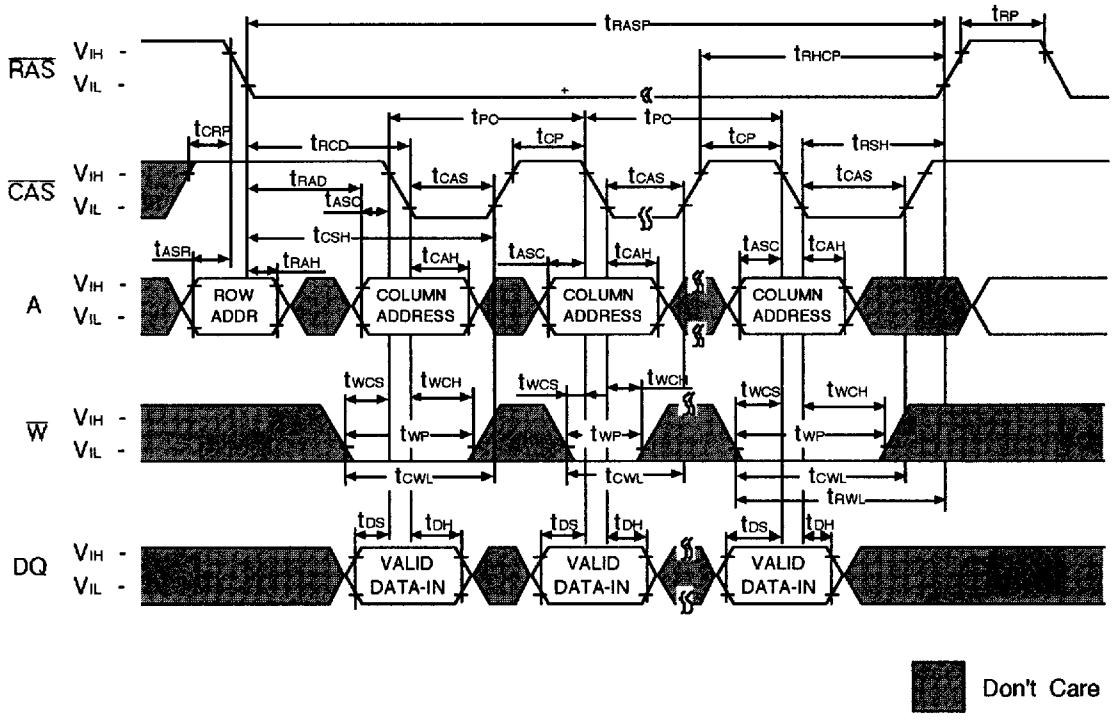
FAST PAGE READ CYCLE

NOTE : D_{OUT} = Open



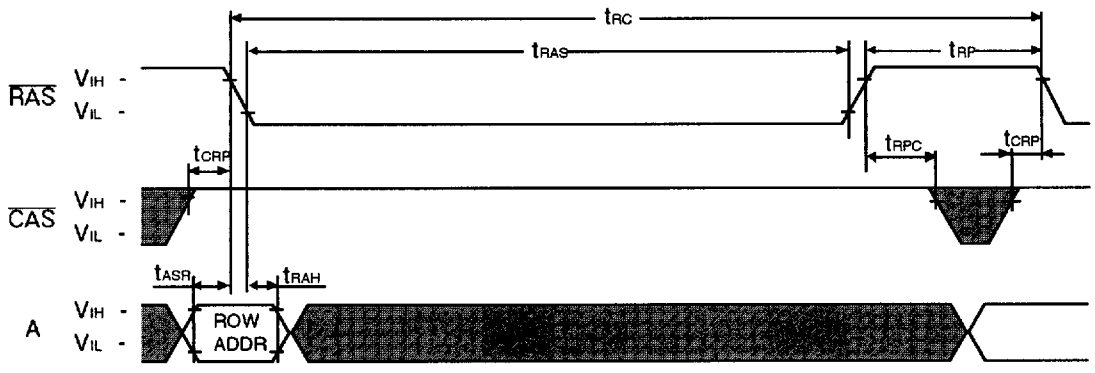
FAST PAGE WRITE CYCLE (EARLY WRITE)

NOTE : D_{OUT} = Open



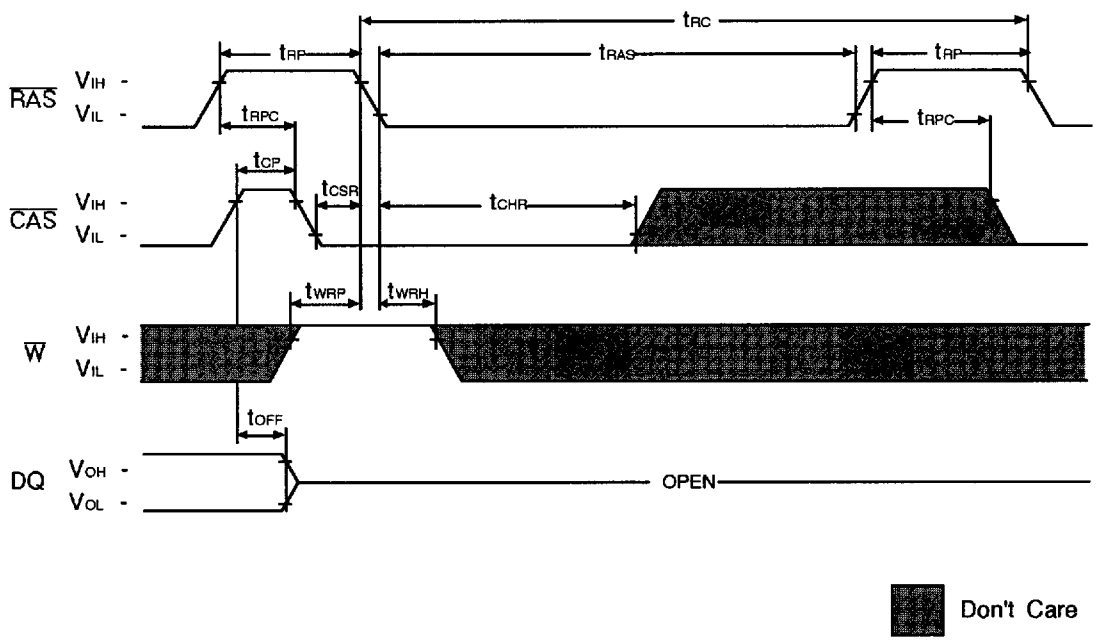
$\overline{RAS}$-ONLY REFRESH CYCLE

NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care
D_{OUT} = Open

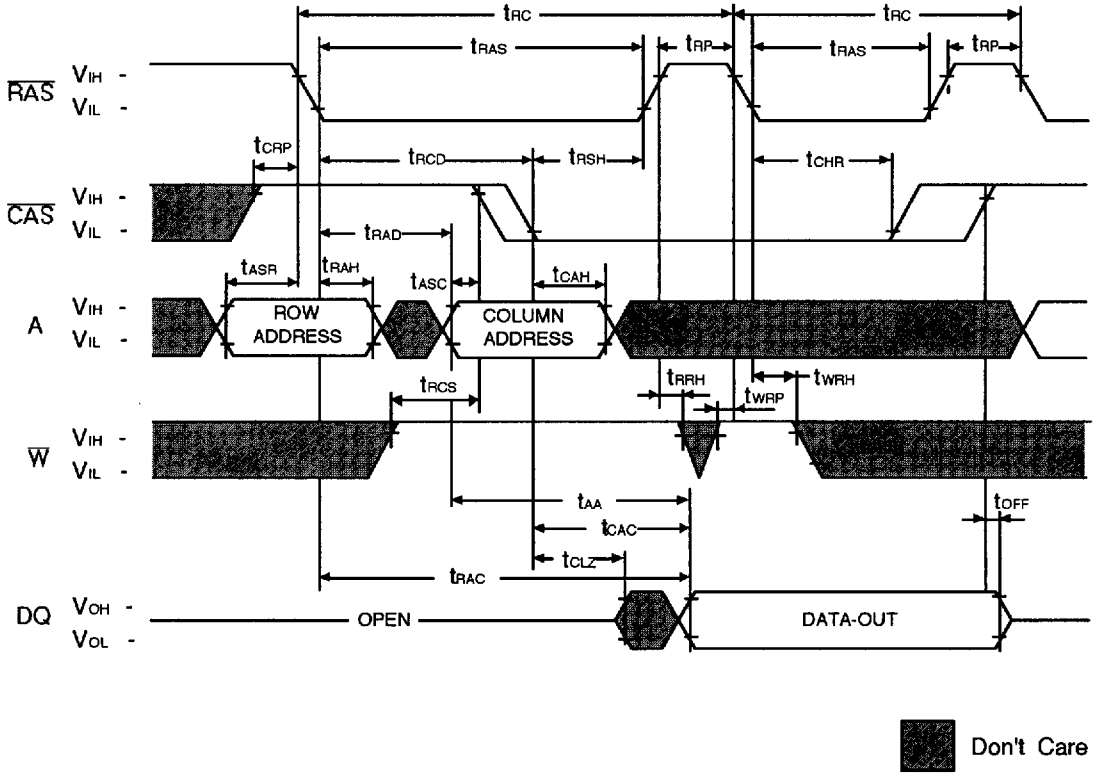


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

NOTE : $\overline{OE}$, A = Don't Care

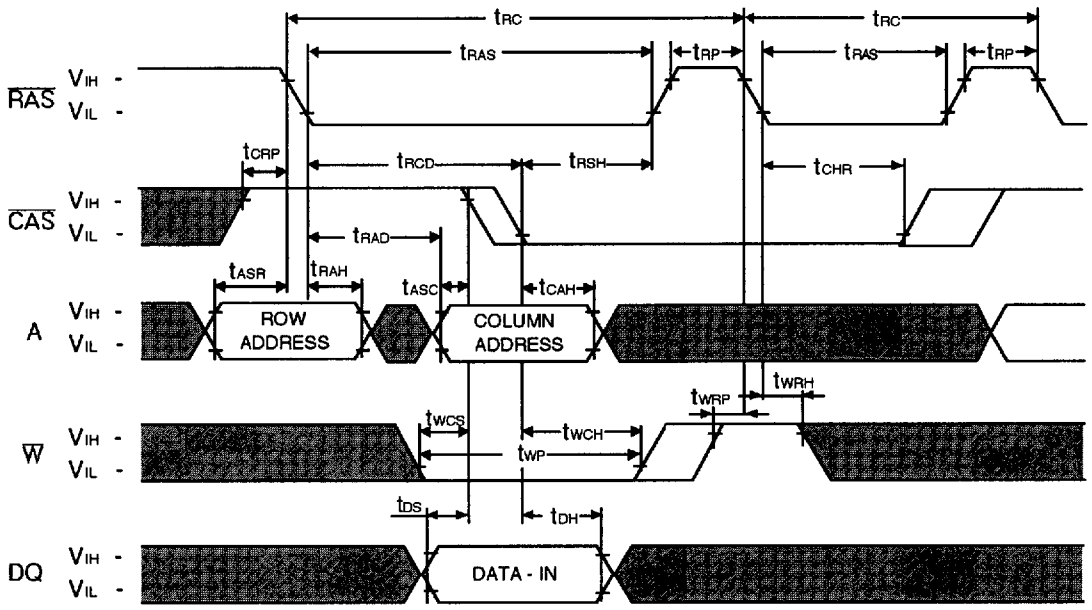


HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

NOTE : D_{OUT} = OPEN



Don't Care

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE