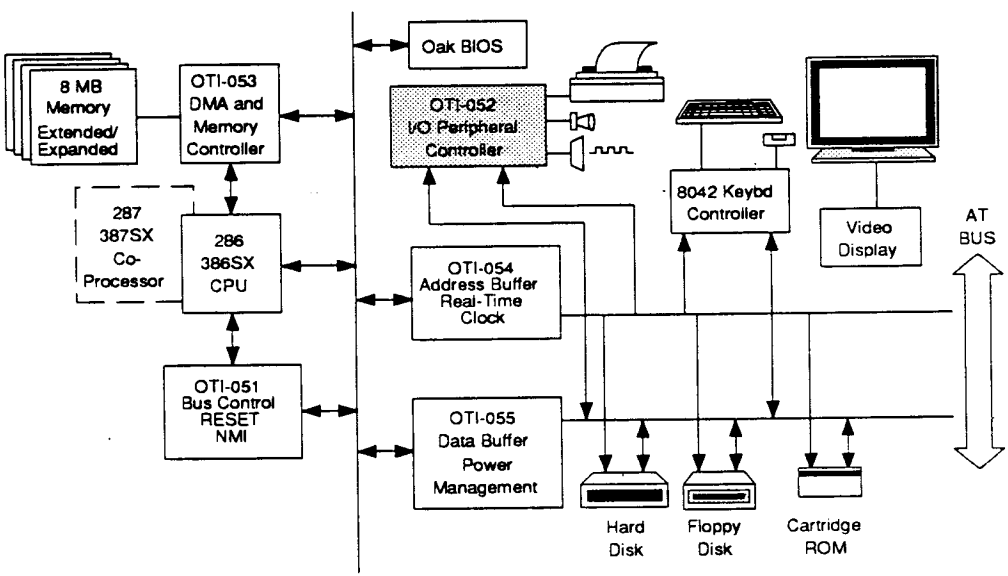
1.0 INTRODUCTION TO THE OTI-052 I/O CONTROLLER

OTI-052 is an integrated I/O peripheral controller. It consists of the following functional blocks:

- Dual 8259 compatible interrupt controller
- 8254 compatible timer/counter
- 16450 compatible serial communication controller
- Parallel port controller
- Chip select logic for floppy disk controller (OTI-033), hard disk subsystem, keyboard controller, and co-processor
- Co-processor interface logic

System Block Diagram



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2.0 PIN-OUT ASSIGNMENT

Table 1. OTI-052 Pin Description

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			***** Bus Interface *****
XDATA7-XDATA0	7-14	I/O	XDATA BUS: bi-directional data lines to/from the I/O channel bus.
SADR9-SADR0	19-22,24-29	I	ADDRESS BUS: from I/O channel. It determines which I/O device the CPU is accessing.
PCAEN	79	I	ADDRESS ENABLE: signal to de-gate the I/O devices from the I/O channel and allow DMA transfers to take place.
IORD-	54	I	I/O READ COMMAND: active low command to instruct the I/O device to drive its data onto the data bus.
IOWR-	53	I	I/O WRITE COMMAND: active low command to instruct the I/O device to read the data present on the data bus.
MEMRD-	52	I	MEMORY READ COMMAND: active low signal to instruct the memory subsystem to drive its data onto the data bus.
MEMWR-	51	I	MEMORY WRITE COMMAND: active low signal to instruct the memory subsystem to read the data present on the data bus.
MREF-	80	I	MEMORY REFRESH REQUEST: active low. It indicates that the system is in the memory refresh cycle.
REFRQT	81	O	REFRESH REQUEST: indicates to the CPU that the DRAM needs refreshing.
ADSEL0	98	I	SELECT FUNCTION 0: is the special select status signal decoder for address range at the current cycle: **SEL0** **FUNCTION** 0 Nothing selected 1 A15 - A10 = 0 (I/O)
VDPMSEL-	99	I	VIDEO ROM CHIP SELECT: is the chip select signal for on-board video ROM address space.
VDRMSEL-	100	I	VIDEO RAM CHIP SELECT: is the chip select signal for on-board video RAM address space.
XBFRD	78	O	X-BUS DIRECTION: active low signal. When this signal is low, data is read from the internal bus to the I/O channel. When this signal is high, data is written from the I/O channel to the internal bus.
RESET	17	I	RESET INPUT: active high signal which is used to reset the internal logic of OTI-052.
			***** Timer Counter *****
SPKOUT	55	O	SPEAKER DATA OUTPUT: speaker output data to be connected to a speaker driver to drive the speaker or beeper.
TIMER2	56	O	TIMER 2 OUTPUT: status signal on 8254 timer channel 2. This signal goes to OTI-051.

Table 1. OTI-052 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
			*** Interrupt Controller ***
IRQ1, IRQ3-12, IRQ14-15	84-90,92-97	I	INTERRUPT REQUEST INPUTS: asynchronous interrupt request inputs to the internal 8259 controllers.
INTR	82	O	INTERRUPT REQUEST: interrupt request to the CPU and is generated whenever a valid IRQ is received.
INTA-	83	I	INTERRUPT ACKNOWLEDGE: is an active low signal from OTI-051 indicating an interrupt acknowledge cycle is in progress.
			*** Parallel Port Interface ***
PD0-PD7	62-65,67-70	I/O	PARALLEL PORT DATA BUS: the bi-directional data lines to the parallel port device. When printer mode is selected, these lines are used as output lines. When input mode is selected, these lines are used as input lines.
ACK-	71	I	PRINTER ACKNOWLEDGE: active low. This pin indicates that the data has been received by the printer.
BUSY	77	I	PRINTER BUSY: indicates that the printer is unable to receive data.
PTPERR	60	I	PRINTER PAPER END OR ERROR: indicates that the end of paper has been detected.
SLCT	76	I	PRINTER SELECT: indicates that the printer is selected.
AUTOFD-	72	O	PRINTER AUTO FEED: active low. It causes the printer to generate a line feed after each line is printed.
ERROR-	75	I	PRINTER ERROR: active low. Indicates that a printer error has occurred.
INIT-	61	O	PRINTER INITIALIZE: active low. It initializes the printer.
SELIN-	74	O	PRINTER SELECT IN: active low. It selects a printer.
STROBE-	59	O	PRINTER STROBE: active low. Its function is to control the "strobe" signal to the printer.
			*** Serial Port Interface ***
CLKSER	39	I	CLOCK INPUT: a 32 MHz TTL clock input.
TXD1	37	O	TRANSMIT DATA 1: the serial output data from UART1.
RXD1	30	I	RECEIVE DATA 1: the serial input data to UART1.
DTR1-	36	O	DATA TERMINAL READY: active low. Notify the MODEM or data set that UART1 is ready to transfer characters.
RTS1-	35	O	REQUEST TO SEND: active low. Handshake signal notifying the MODEM or data set that UART1 is ready to transmit data.
CTS1-	34	I	CLEAR TO SEND: active low. Handshake signal notifying UART1 that the MODEM or dataset is ready to receive data.
DSR1-	33	I	DATA SET READY: active low. The signal indicates that the MODEM or data set is ready to establish the communication link with the UARTS. The CPU can read the UART register to find out the MODEM's ready condition.

Table 1. OTI-052 Pin Description (Continued)

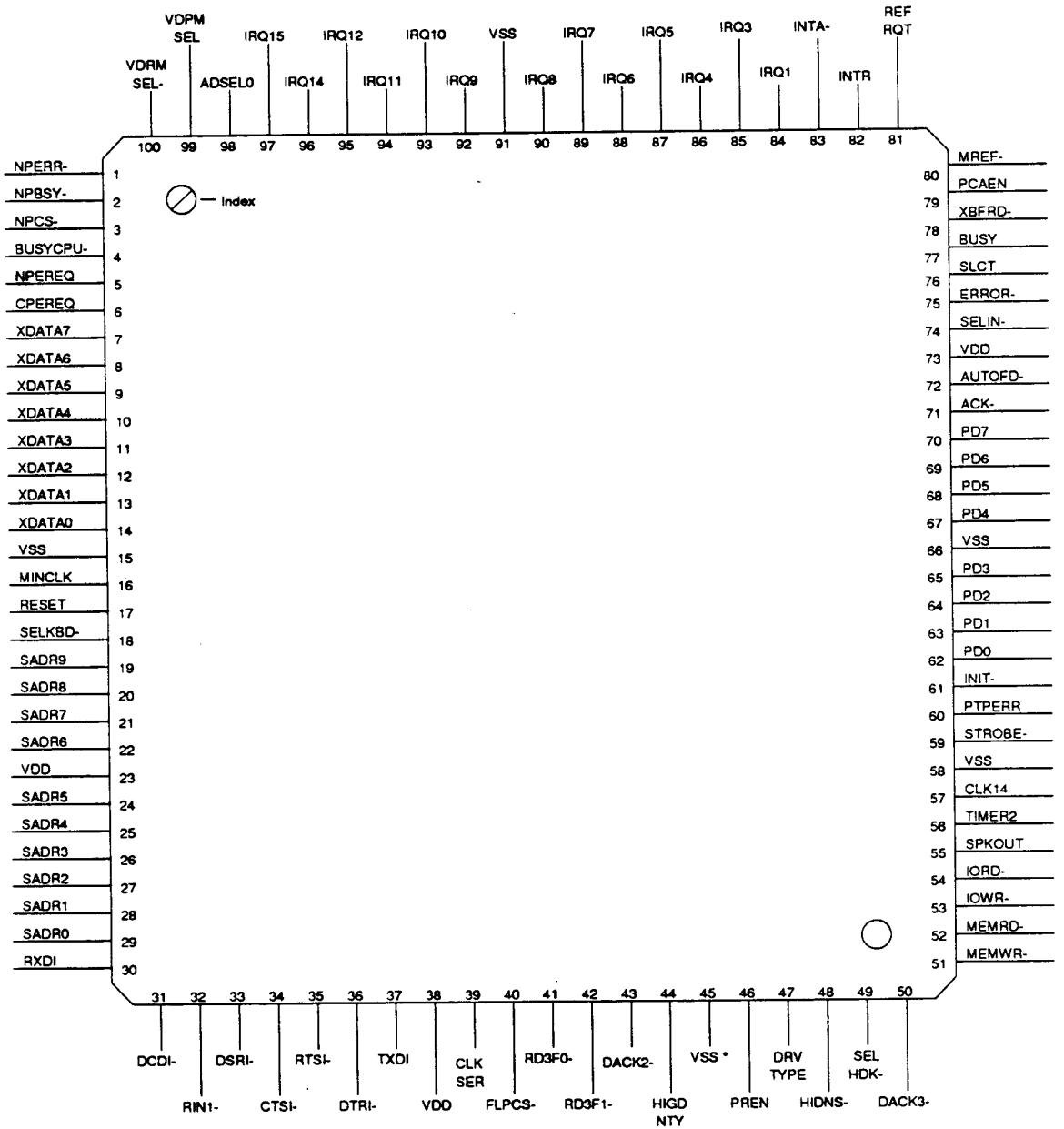
SYMBOL	PIN #	TYPE	NAME and FUNCTION
DCD1-	31	I	CARRIER DETECT: active low. The MODEM or data set uses these pins to notify UART1 that the carrier signal has been detected.
RIN1-	32	I	RING INDICATOR: active low. It notifies UART1 that a telephone ringing signal has been detected by the MODEM or data set.
			***** Keyboard and Mouse Interface *****
SELKBD-	18	O	SELECT KEYBOARD: active low. Indicates the keyboard controller is selected .
			***** Floppy Disk Controller *****
FLPCS-	40	O	FLOPPY SELECT: active low. This pin selects the floppy disk controller (OTI-033).
RD3F0-	41	O	READ RAS PORT A: active low. It enables RAS Port-A.
RD3F1-	42	O	READ RAS PORT B: active low. It enables RAS Port-B.
HIGDNTY	44	O	HIGH DENSITY: high current output to the input of the floppy drive high density media support. This pin supports both AT and Model 30-286 types.
DACK2-	43	I	DMA ACKNOWLEDGE: active low. It indicates that the floppy disk controller has been granted a DMA cycle.
PREN	46	O	PRECOMP: selects the precompensation value for the floppy disk controller.
DRVTYPE	47	O	DRIVE TYPE: controls the data rate for the floppy disk controller.
			***** Hard Disk Controller *****
HDINS-	48	I/O	HARD DISK INSTALLED: active low input indicating that an on-board IBM hard disk is installed. When a Conner's hard disk is installed, this pin is used as one of the chip select output decoding addresses 3F6 and 3F7.
SELHDK-	49	O	HARD DISK SELECT: active low. It selects an on-board hard disk drive for an I/O operation.
DACK3-	50	I	DMA ACKNOWLEDGE: active low. It indicates that the on- board hard disk controller has been granted a DMA cycle.
			***** Co-processor Interfaces *****
NPEREQ	5	I	NUMERICAL PROCESSOR REQUEST: active high. It indicates that the co-processor is requesting an operand transfer. This pin comes from the PEREQ output of the co-processor.
CPEREQ	6	O	CPU REQUEST: active high. It indicates to the CPU that the co-processor is requesting an operand transfer. This pin goes to the CPU to request the transfer.
NPERR-	1	I	NUMERICAL PROCESSOR INTERRUPT: active low. It indicates that an unmasked exception has occurred during a numeric instruction execution when an 80287 interrupt is enabled.
NPBSY-	2	I	NUMERICAL PROCESSOR BUSY: active low. It is connected directly to the BUSY signal of the co-processor.

Table 1. OTI-052 Pin Description (Continued)

SYMBOL	PIN #	TYPE	NAME and FUNCTION
NPCS-	3	O	NUMERICAL PROCESSOR CHIP SELECT: When low, the co-processor is selected for an I/O operation.
BUSYCPU-	4	O	BUSY TO CPU: active low. It is connected directly to the BUSY input of 80286 or 80386SX.
			***** POWER Management *****
MINCLK	16	I	MINUTE CLOCK: minute clock signal from OTI-054.
			***** Others *****
CLK14	57	I	14.318 MHz TTL level clock input signal used to generate internally the clock for 8254.
VSS	15,45,58,66,91	I	GROUND: 5 pins 0V
VDD	23,38,73	I	POWER: 3 pins 5V
PCALE	45	I	PCALE: Signal coming from OTI-054 for interfacing 80287 co-processor with 80386SX CPU. This pin is only valid in OTI-052, rev C or above. For rev A and B of the OTI-052, pin 45 should be tied to VSS.

NOTE: OTI-052 would go into the TEST mode under the following input combination:

RESET = '0'
DACK3- = '0'
DACK2- = '0'



* For rev C and above, this pin is used as PCALE (see pin description for PCALE).

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3.0 OTI-052 FUNCTIONAL DESCRIPTION

OTI-052 functions can be categorized as follows:

1. Interrupt Control Logic
2. Timer Controller
3. Serial Communication Controller
4. Parallel Port Controller
5. Floppy Disk Decode and Control Logic
6. Hard Disk Decode Logic
7. Power Management
8. System Control and Status Registers
9. Co-processor Interface

3.1 Interrupt Control Logic

The interrupt control logic includes two Intel 8259A compatible interrupt controllers. It has 15 levels of interrupt that are handled according to programmed priority in the OTI-052 chip. The following table shows the hardware interrupts and their availability to the I/O channel (PC bus).

Table 2. Availability of Hardware Interrupts to the I/O Channel

Level	OTI-052 chip	System Board	I/O channel
IRQ0	Timer Channel 0	Not available	Not available
IRQ1	Not used	Keyboard interface	Not available
IRQ2	Slave	Not Available	Not available
IRQ3	COM2	Not used	Available
IRQ4	COM1	Not used	Available
IRQ5	Not used	Parallel port 2	Available
IRQ6	Not used	Diskette drive (OTI-033)	Available
IRQ7	Parallel port	Not used	Available
IRQ8	Not used	Real Time Clock	Not Available
IRQ9	Not used	Software redirects to INT 0A(Hex) (IRQ2)	Available
IRQ10	Not used	Not used	Available
IRQ11	Not used	Not used	Available
IRQ12	Not used	Mouse	Not Available
IRQ13	Coprocessor	Not used	Not Available
IRQ14	Not used	Fixed Disk Controller	Available
IRQ15	Not used	Not used	Available

The I/O address for each register in the interrupt controllers is defined in the following table:

Table 3. I/O Addresses for Registers in the Interrupt Controllers

ADDRESS	W/R	Function
		Master Interrupt Controller
		***** Initialization Mode *****
0020	W	initialization command word ICW1
0021	W	initialization command word ICW2, ICW3, ICW4
		***** Operation Mode *****
0021	W	operation control word OCW1
0020	W	operation control word OCW2, OCW3
		***** Read Status Register (Operation Mode) *****
0021	R	interrupt mask register (IMR)
0020	R	interrupt request register (IRR) and interrupt service register (ISR). IRR and ISR are selected through bit 0 and bit 1 in OCW3
		Slave Interrupt Controller
		***** Initialization Mode *****
00A0	W	initialization command word ICW1
00A1	W	initialization command word ICW2, ICW3, ICW4
		***** Operation Mode *****
00A1	W	operation control word OCW1
00A0	W	operation control word OCW2, OCW3
		***** Read Status Register (Operation Mode) *****
00A1	R	interrupt mask register (IMR)
00A0	R	interrupt request register (IRR) and interrupt service register (ISR). IRR and ISR are selected through bit 0 and bit 1 in OCW3

The interrupt acknowledge cycle requires two wait states.

3.2 Timer Controller

The timer controller is compatible with the Intel 8254. It is a programmable interval timer/counter. The function of timer controller is to generate a constant system time and control the tone of the speaker. This controller contains three timer channels. Each channel is described as follows:

Channel 0:

This channel is a general purpose timer providing a constant time base for the operating system. The input clock (CLK IN 0) runs at 1.19 MHz frequency. The enable clock input (GATE 0) is always enabled after power up. The output (CLK OUT 0) of this channel is connected to interrupt channel 0 (IRQ0) of the interrupt controller (8259A).

Channel 1:

This channel is used to control the DRAM refresh cycles. The input clock (CLK IN 1) runs at 1.19 MHz. The enable clock input (GATE 1) is always enabled after power up. The output (CLK OUT 1) of this channel goes to OTI-051 to request a periodic DRAM refresh cycle.

Channel 2:

This channel controls the tone of the speaker. The input clock (CLK IN 2) runs at 1.19 MHz. The enable clock input (GATE 2) is turned on/off by bit 0 of system control register 061(Hex). When bit 0 of I/O PORT 061h is set to one, the frequency of tone is controlled by the counting number in the counter register 2. The output (CLK OUT 2) of this channel is connected to the driver of the speaker. After power on or reset, bit 0 of I/O port 061h is reset to zero. More detailed information will be described in the section on the system control register 061(Hex).

The I/O address for each register in the timer controller is defined below:

ADDRESS	W/R	Function
0040	W/R	counter register 0
0041	W/R	counter register 1
0042	W/R	counter register 2
0043	W	control mode register

The control mode register selects the operation mode for each channel in the timer controller. There are six different modes. They are listed below:

- mode 0: interrupt on terminal count
- mode 1: programmable one-shot
- mode 2: rate generator
- mode 3: square wave rate generator
- mode 4: software triggered strobe
- mode 5: hardware triggered strobe

More detailed information can be found in the Intel 8254 data sheet.

3.3 Serial Communication Controller

The OTI-052 chip incorporates a serial communication controller which can be optionally selected to be COM1 or COM2 through the BIOS set-up menu. The serial communication controller is fully compatible with the NS16450A. It will add and remove start, stop and parity bits. A programmable baud-rate generator allows operation from 50 baud to 56000 baud. These controllers support 5, 6, 7 and 8 bit characters with 1, 1.5 or 2 stop bits. A prioritized interrupt system controls transmitting, receiving, error, and line status as well as data-set interrupt. The clock applied to the serial communication controllers is 1.84 MHZ which is derived from the 32 MHz clock.

Addressing of the accessible registers in the serial communication controllers is shown in the table below.

Table 4. Addressing Registers in Serial Communications Controllers

DLAB	A2	A1	A0	Register
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Flag (read)
X	0	1	1	Byte Format
X	1	0	0	Modem Control
X	1	0	1	Line status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor LSB
1	0	0	1	Divisor MSB

Notes: X = Don't Care
DLAB = Divisor Latch Access Bit

The serial port provides the following RS-232 signals which include modem control interfaces:

- RXD: Receive Data
- CTS: Clear To Send
- DSR: Data Set Ready
- DCD: Data Carry Detect
- RI: Ring Indicator
- TXD: Transmit Data
- DTR: Data Terminal Ready
- RTS: Request To Send

Interrupt of the serial communication controller in COM1 mode is internally connected to the IRQ4 of the interrupt controller in the OTI-052 chip. The I/O address for each register in the serial communication controller in COM1 mode is listed in the following table:

Table 5. I/O Addresses for Registers in Serial Communications Controller in COM1 Mode

ADDRESS	W/R	FUNCTION
03F8	W	transmitter holding register
03F8	R	receive buffer register
03F9	W/R	interrupt enable register
03FA	R	interrupt identification register
03FB	W/R	line control register
03FC	W/R	modem status register
03FD	R	line status register
03FE	R	modem status register
03FF	W/R	scratch register

Interrupt of the serial communication controller in COM2 mode is internally connected to the IRQ3 of the interrupt controller in the OTI-052 chip.

The I/O address for each register in the serial communication controller in COM2 mode is listed in the following table:

Table 6. I/O Address for Serial Communications Controllers in COM2 Mode

ADDRESS	W/R	FUNCTION
02F8	W	transmitter holding register
02F8	R	receive buffer register
02F9	W/R	interrupt enable register
02FA	R	interrupt identification register
02FB	W/R	line control register
02FC	W/R	modem status register
02FD	R	line status register
02FE	R	modem status register
02FF	W/R	scratch register

More detailed information can be found in National's data book.

3.4 Bi-directional Parallel Port Controller

The parallel port controller can be configured to be one of two modes. The first mode is "printer mode." The function of the printer mode is to attach a printer with parallel interface to the system. The second mode is "input mode" that allows the system to receive data through the parallel port from external devices when the direction bit in the printer control register is set to read. The input mode of the parallel port controller is selected by writing a 0 to bit 7 of POS byte 102(Hex). Refer to IBM's documentation for POS register definitions.

There are two output ports and three input ports in the parallel port controller. The following is a detailed description of each port.

Data port:

The data port is an 8-bit port for both the printer mode and input mode. For the printer mode, a write operation to this port immediately presents data to the connector pins. A read operation from this port in the printer port produces the data that was last written to it. In the input mode, a write operation to this port does not affect the output of the data port if the direction bit is set to read. A read operation in the input read mode produces the data on the connector pins from external devices.

Status Port:

The status port is a read-only port for either mode. When an interrupt is pending, the interrupt status bit is set to 0. The following table shows the bit definition of the status port:

Table 7. Bit Definition of the Status Port, Parallel Port Controller

Bit	Function	
7	BUSY-:	When this bit is active, the printer is busy and can not accept data.
6	ACK-:	When this bit is 0, the printer is ready to accept data.
5	PE-:	When this bit is set to 1, the printer has detected the end of the paper.
4	SLCT-:	When this bit is set to 1, the printer has been selected.
3	ERROR-:	When this bit is set to 0, the printer has detected an error condition.
2	IRQ-:	When this bit is set to 0, the printer has acknowledged the previous transfer using the "-ACK" signal.
1	Reserved	
0	Reserved	

Output Control Port:

The Output Control Port is a read or write port. The following table shows the bit definition of the Output Control Port:

Table 8. Bit Definition of the Output Control Port, Parallel Port Controller

Bit	Function	
7	Reserved	
6	Reserved	
5	Direction:	1 to enable read input mode
4	IRQ EN:	When this bit is set to 1, the interrupt logic is enabled.
3	SLCT IN:	This bit controls the "SLCT IN" signal on connector pin 17. When this bit is set to 1, the printer is selected.
2	INIT:	This bit controls the "-INIT" signal on connector pin 16. When this bit is set to 1, the printer starts.
1	AUTO-FD:	This bit controls the "AUTO-FD" signal on connector pin 14. When this bit is set to 1, the printer will automatically line feed after each line is printed.
0	STROBE:	This bit controls the "STROBE" signal on connector pin 1. When this bit is set to 1, data is pulse-clocked into the printer.

An interrupt from the parallel port controller is connected to IRQ7 of the interrupt controller in OTI-052. This port can be configured into either LPT1, LPT2 or LPT3. The I/O address for each register in different port configurations is listed in the following table:

Table 9. I/O Addresses for Parallel Port Controller Registers

PORT NO.	ADDRESS	W/R	Function
LPT1	03BC	W/R	data register
LPT2	0378	W/R	data register
LPT3	0278	W/R	data register
LPT1	03BE	W/R	printer control register
LPT2	037A	W/R	printer control register
LPT3	027A	W/R	printer control register
			b7 - b6 not used
			b5 = Direction
			(1=input, 0=output)
			b4 = enable/disable interrupt
			(1=enable,0=disable)
			b3 = select printer device
			(1=select, 0=not select)
			b2 = start printer device
			(1=stop, 0=start)
			b1 = enable line feed
			(1=enable, 0=disable)
			b0 = data strobe
			(1=data valid, 0=data invalid)
LPT1	03BD	W/R	status register
LPT2	0379	W/R	status register
LPT3	0279	W/R	status register
			b7 = printer busy
			(1=not busy, 0=busy)
			b6 = printer acknowledge
			(1=no-ACK, 0=ACK)
			b5 = end of paper
			(1=no paper, 0=paper)
			b4 = printer selected
			(1=selected, 0=not selected)
			b3 = printer error
			(1=no error, 0=error)
			b2 = IRQ status
			b1-b0 = not used

3.5 Floppy Disk Controller Address Decode and Control Registers

OTI-052 is capable of decoding the I/O address and generating the select signal for the on-board floppy disk controller. OTI-052 can also control the data buffer between the I/O extended bus and the I/O Channel during an I/O cycle or DMA cycle for the floppy disk controller.

RAS A Port and RAS B Port are implemented externally, OTI-052 generates the chip select signal for these two ports.

Table 10. Floppy Disk Controller Address and Cotrol Registers

ADDRESS	W/R	FUNCTION
RAS A PORT		
03F0	R	b7 = IRQ6 b6 = DRQ2 b5 = step (latched) b4 = track 0 b3 = head 1 select b2 = index b1 = write protect b0 = direction
RAS B PORT		
03F1	R	b7 = not used b6 = drive select 1 b5 = drive select 0 b4 = write data (latched) b3 = read data (latched) b2 = write enable (latched) b1 = drive select 3 b0 = drive select 2
DIGITAL OUTPUT REGISTER		
03F2	W	b6-7= reserved b5 = motor enable 1 b4 = motor enable 0 b3 = DMA and interrupt enable b1,b0 = drive select 00 selects drive 0 01 selects drive 1 10 selects drive 2 11 selects drive 3
DIGITAL INPUT REGISTER		
03F7	R	b7 = diskette change b6-b4= reserved b3 = DMA enable b2 = No write precomp b1 = 250 rate select b0 = high density select
CONFIGURATION CONTROL REGISTER		
03F7	W	b7-3 = reserved = 0 b2 = No write precomp b1 = 250 rate select b0 = used only for 1.2M drive

More detailed information on all the floppy control and status registers can be found in the specification on Oak Technology's floppy controller and data separator chip (OTI-033) and in NEC's floppy controller (NEC 765) data sheet.

3.6 Address Decode for Hard Disk Controller

OTI-052 is capable of decoding the I/O address for the on-board hard disk controller and generating the select signal for the controller. OTI-052 can also control the data buffers between the I/O extended bus and I/O Channel during an I/O cycle or DMA cycle for the hard disk controller. The I/O address range for the PS/2 hard disk controller is between 320(Hex) to 32F(Hex). It uses DMA channel 3 for DMA access. OTI-052 also supports IDE-type hard disk drives. The I/O range for IDE-type drives is 1F0-1F7 and 3F6-3F7(Hex).

3.7 Power Management

OTI-052 incorporates several activity monitors, which together with the power management circuits residing in the other chips of the chipset, enable the system designer to design a very power efficient laptop system.

3.8 System Control and Status Registers

These I/O ports reside in OTI-052 and are used to either control the system or provide various system status.

System Control Register PORT B (061h)

The system control register (061h) is used for speaker control, I/O channel check, and memory parity check enable on the system board. This register is a read/write port. However, the port is only writable in OTI-052. When port 61(Hex) is being read, data would be coming from OTI-051. The bit definitions of this register are defined as follows:

ADDRESS	W	Function
0061		
	W	b1=speaker data, enable/disable the output of 8254-timer 2 (1=enable,0=disable,default=disable)
	W	b0=enable/disable 8253-Timer 2 (1=enable,0=disable,default=disable)

Bit 1 is used to gate speaker data. This bit gates the output of timer 2. It can disable the timer's sound source or modify its output. When set to 1, this bit enables the output. When cleared to 0, it forces the output to zero.

Bit 0 is routed to the timer input at GATE 2. When this bit is cleared to 0, the timer operation is halted. This bit and bit 1 (speaker data) control the operation of the timer's sound source.

After power on or reset, this register is cleared.

3.9 Co-processor Interface

OTI-052 supports both the 80287 and the 80387SX co-processors. When an 80286 is used as the CPU, the 80287 is supported. When an 80386SX is used as the CPU, either an 80287 or 80387SX can be used as the co-processor.

OTI-052 decodes I/O address range 0F8-0FF(Hex) for the co-processor. During hardware reset, OTI-052 latches the status of NPERR- from the co-processor into bit 6 of control/status port 2. If the latched bit is low, it implies an 80387SX is used; if the bit is high, an 80287 is assumed. BIOS should then detect the existence of the co-processor and set bit 3 of the system status register 2.

OTI-052 generates IRQ13 and drives BUSYCPU- low when NPERR- is active. And if an 80386SX is used, CPEREQ and NPCS- will be forced high. INTA- signal is used to clear the above latched error condition. BIOS can also write to ports F0 and F1 to clear it. IRQ13 is reset to low only by writing to F0 or F1.

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4.0 ELECTRICAL CHARACTERISTICS

4.1 A.C. Characteristics

Table 11. A.C. Characteristics of OTI-052

A.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	LOADING CAPACITANCE
t1	Timer Output Delay		180	ns	CL=150 pF
t2	IRQ to INTR		90	ns	CL=150 pF
t3	INTAN to XD Valid		150	ns	
t4	XD Invalid from INTAN	5		ns	
t5	Address SETUP Time	50		ns	
t6	SEL0 SETUP Time	40		ns	
t7	WRITE Data SETUP Time	100		ns	
t8	WRITE Data HOLD Time	20		ns	
t9	READ Data Valid from IORDN		100	ns	CL=200 pF
t10	READ Data Float from IORDN	5		ns	CL=200 pF
t11	XBFRDN from READ Command		45	ns	
t12	Chip Selects from Address		40	ns	CL=50 pF
t13	Floppy Port Read Command		40	ns	
t14	Floppy Control from IOWRN		45	ns	
t15	Printer Control from IOWRN		45	ns	CL=150 pF
t16	BUSYCPU from IOWRN		10	ns	
t17	CPEREQ from IOWRN		10	ns	
t18	NPCSN(387SX) from IOWRN		10	ns	
t19	NPCSN(287) from IOWRN		10	ns	
t20	BUSYCPU from NPBSYN		30	ns	
t21	CPEREQ from NPERRN		35	ns	
t22	NPCSN(287) from NPERRN		35	ns	
t23	NPCSN(387SX) from NPERRN		35	ns	

4.2 DC Characteristics

Table 12. DC Characteristics of OTI-052

D.C. Characteristics: TA=0 deg C to 70 deg C, VDD=5V+/-5%, VSS=0V

SYMBOL	PARAMETER	MIN	MAX	UNIT	CONDITION
VOH	Output High Voltage	2.4		V	IOH=400 µA
VOL1	Output Low Voltage		0.45	V	IOL=20 mA, Note 1
VOL2	Output Low Voltage		0.45	V	IOL=16 mA, Note 1
VOL3	Output Low Voltage		0.45	V	IOL=10 mA, Note 1
VOL4	Output Low Voltage		0.45	V	IOL= 8 mA, Note 1
VOL5	Output Low Voltage		0.45	V	IOL= 4 mA, Note 1
VOL6	Output Low Voltage		0.45	V	IOL= 2 mA, Note 1
VIH	Input HIGH Voltage	2.0	VDD+0.5	V	TTL
VIL	Input LOW Voltage	- 0.5	0.8	V	TTL
VIS	Schmitt Input High	2.4	Vdd+0.5	V	Schmitt, Note 2
VIC	CMOS Input High Voltage	3.8	Vdd+0.5	V	CMOS, Note 2
ILI	Input Leakage Current	- 10	10	µA	
OLI	Output Leakage Current	- 10	10	µA	
ICC	Operating Supply Current		30	mA	Input=VDD or VSS No Output Load
CI	Input Capacitance		8	pF	
CO	Output Capacitance		8	pF	
CIO	I/O Capacitance		16	pF	

1. Output Current (IOL) Capabilities:

20 mA :	HIGDNTY, PD0 - PD7
10 mA :	STROBE-, INIT-, AUTOFD-, SELIN-
8 mA :	DATA0-7, SELHDK-, HDINS-
4 mA :	NPCS-, BUSYCPU, CPEREQ, SELKBD-, RTS1-, DTR1-, TXD1,FLPCS-, RD3F0-, RD3F1-, SPKOUT, TIMEOUT2, XBFRD-, REFREQ, INTR
2 mA :	PREN, DRVTYPE, IRQ3,4,7

2. Input Structures:

Schmitt Triggered :	CLKSER, CLK14, MINCLK
CMOS :	-
TTL :	All Others
Input With Pullup :	NPERR-, NPBSY-, RXD1, DCD1-, RIN1-, DSR1-, CTS1-, IRQ

5.0 OTI-052 TIMING DIAGRAMS

FIGURE 2-1.

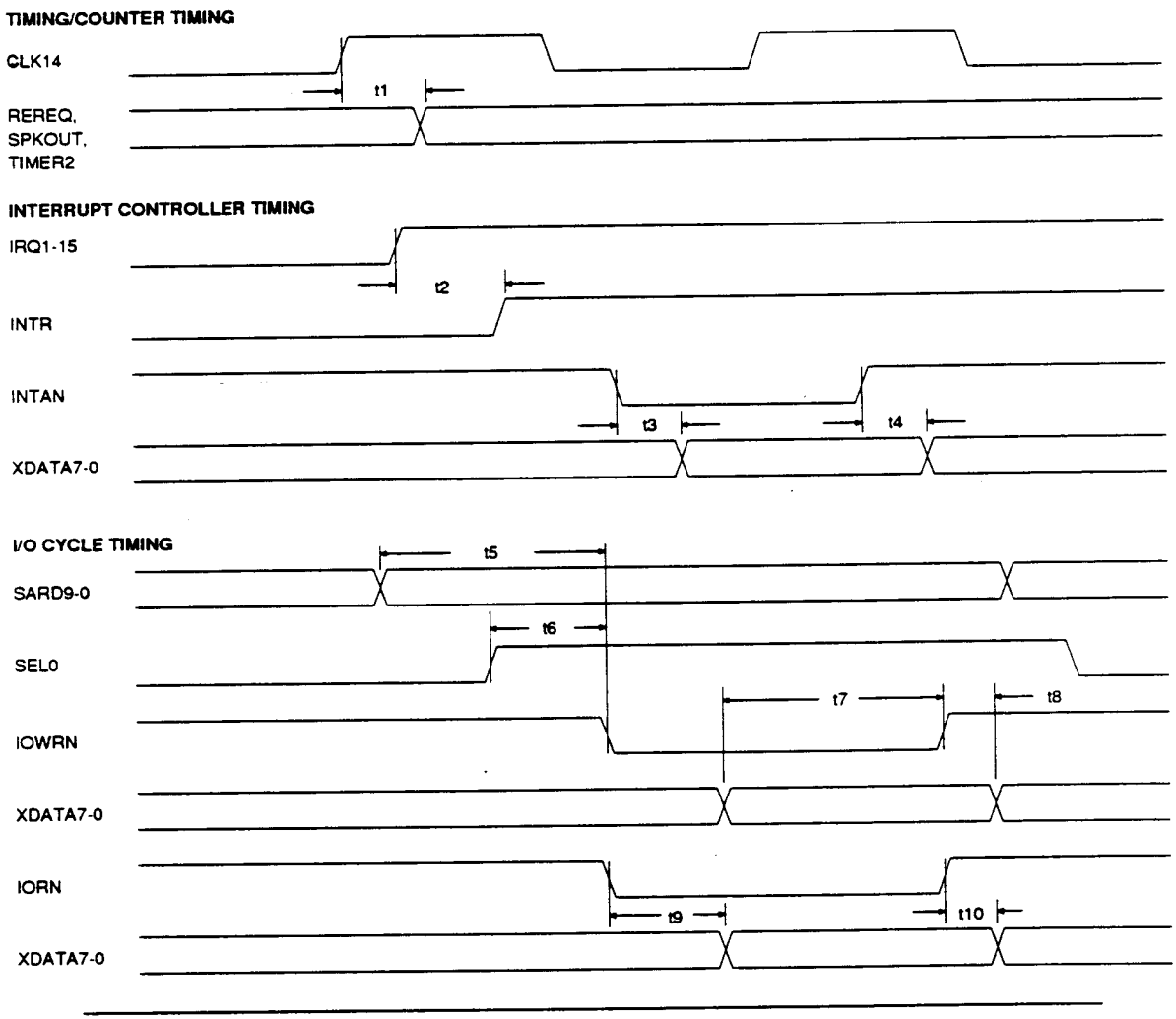

FIGURE 2-2.

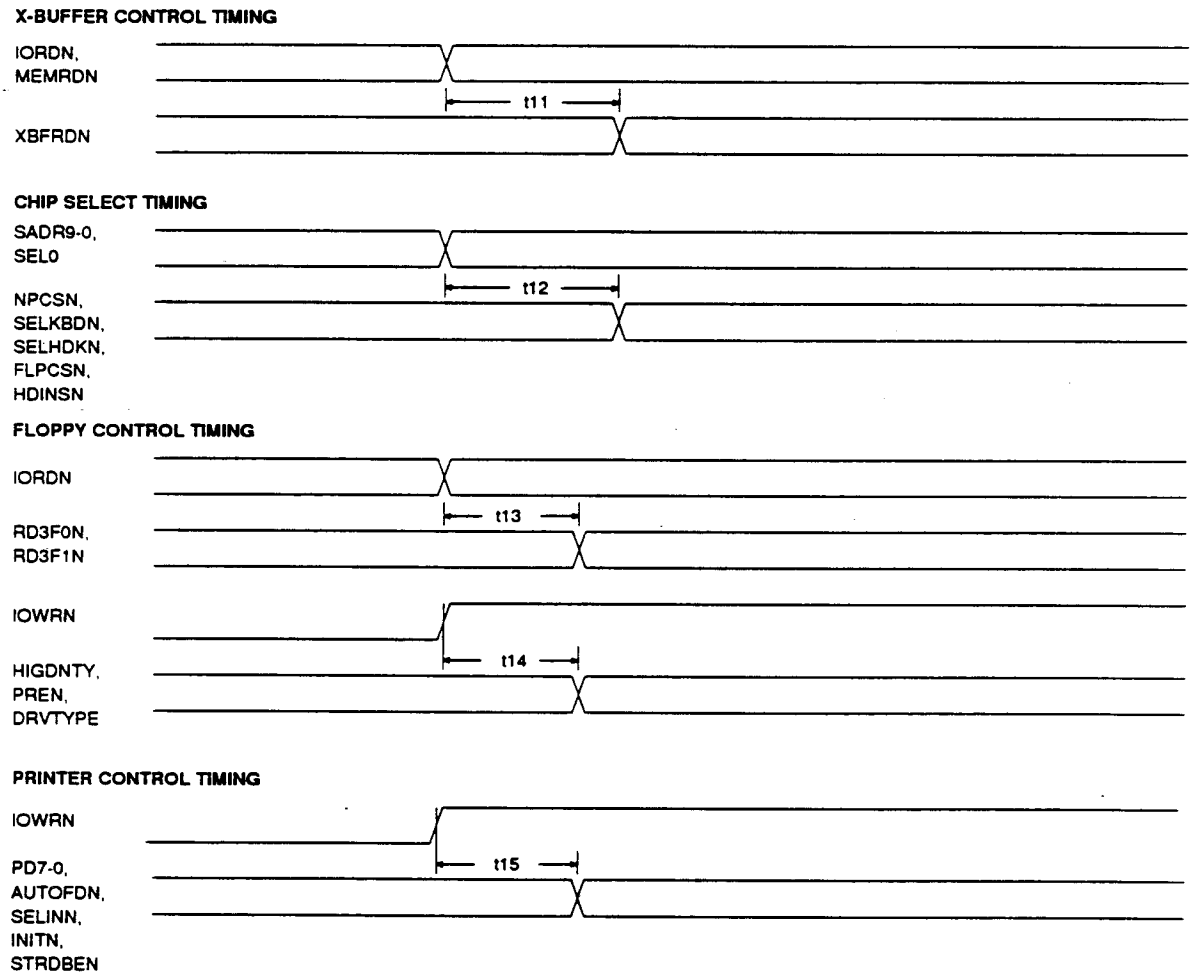

FIGURE 2-3.