DATA SHEET (Rev0.1)

NEC

MOS INTEGRATED CIRCUIT

μPD30133

VR4133™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30133 (VR4133) is one of NEC's VR Series™ RISC (Reduced Instruction Set Computer) microprocessors and it is a high-performance 64-/32-bit microprocessor employing the MIPS™ RISC architecture. The VR4133 uses an ultra-low-power-consumption VR4130™ as the CPU core, and has many peripheral functions such as an Ethernet controller, an IPsec function controller, a DMA controller, serial interface, IrDA interface, real-time clock, memory interface, NS16550-compatible serial interface, and 3-wire clocked serial interface. Configured with these functions, the VR4133 is suitable for embedded systems, especially network systems. The external memory bus width can be selected from 32 bits or 16 bits. This processor supports the PCI bus interface conforming to Rev2.3 as the interface for an external device that requires the module etc. for wireless LAN demands it.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

- **VR4133 Hardware User's Manual (Available in 2003)**
- **VR4100 Series™ Architecture User's Manual (U15509E)**

FEATURES

- Employs 64-bit MIPS architecture
  - Conforms to MIPS III instruction set
  - Optimized 7-stage pipeline
- Supports MIPS16 instruction set
- Supports high-speed product-sum operation (MACC) instructions
- Includes 2-channel 10/100 Mbps Ethernet controllers compliant to IEEE802.3, IEEE802.3u and IEEE802.3x (MII and RMII interface compatible)
- Executes symmetric cryptographic algorithm :DES/Triple-DES/AES, hash function:SHA-1
- Supports five types of operating modes, enabling more effective power-consumption management
- Internal maximum operating frequency: 266 MHz
- On-chip clock generator
- Address space Physical: 32 bits
  Virtual: 40 bits
  Integrates 32 double-entry TLBs
- High-capacity instruction/data separated cache memories
  Instruction: 16 KB
  Data: 16 KB
- Memory controller (ROM, synchronous DRAM (SDRAM), and flash memory supported)
- Supports PCI bus conforming to PCI Rev2.3
- Internal 133MHz SysAD and 66MHz Interface buses
- 7-channel DMA controller
- Serial interface (NS16550 compatible)
- On-chip 3-wire clocked serial interface
- IrDA interface for infrared communication
- Debug serial interface
- Power supply voltage:
  $V_{DD}1$ = 1.35 to 1.65 V (internal)
  $V_{DD}3$ = 3.0 to 3.6 V (external)
- Package: 240-pin plastic FBGA

APPLICATIONS

- Embedded equipment
- Network system, etc.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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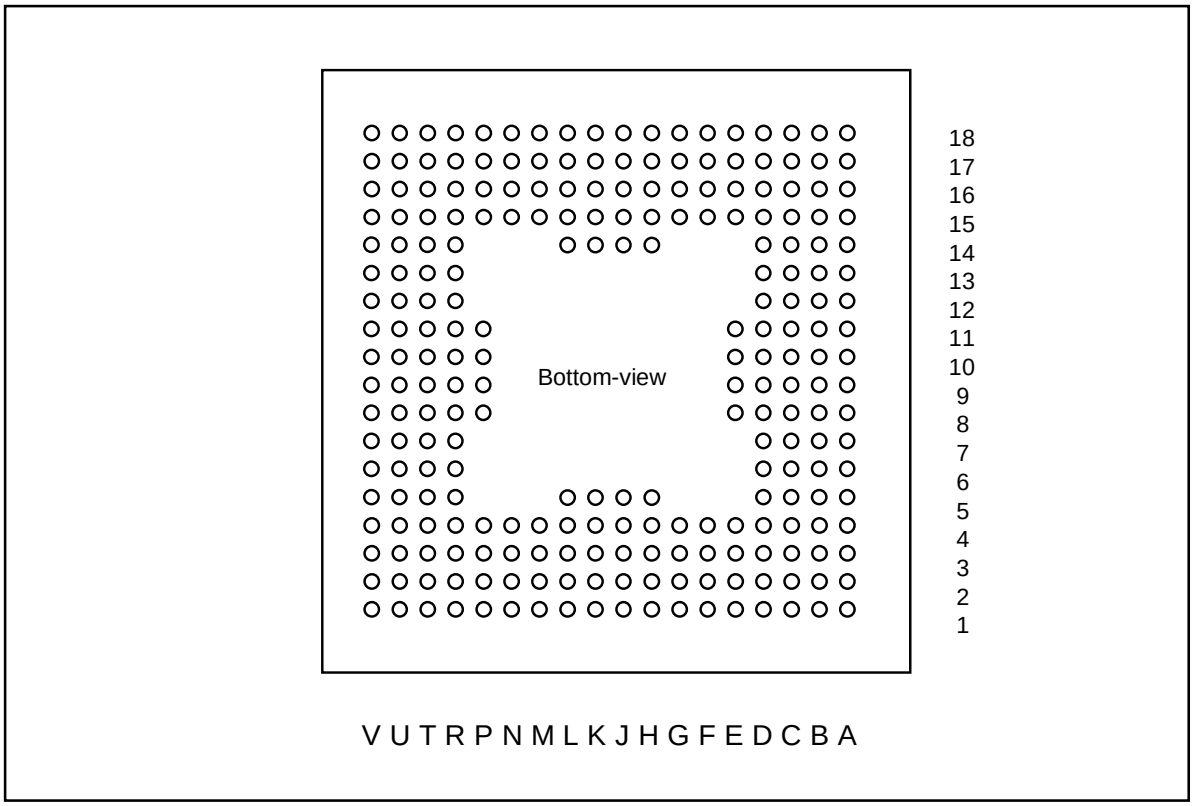
ORDERING INFORMATION

Part Number	Package	Internal Maximum Operating Frequency
μPD30133F1-266-GA3	240-pin plastic FBGA (16 × 16)	266 MHz

PIN CONFIGURATION

- 240-pin plastic FBGA (16 × 16)
  μPD30133F1-266-GA3



(1/3)

No.	Power	Pin name	No.	Power	Pin name
A1	3.3V	AD29	C14	3.3V	GPIO5/M0TXD3/R1TXD1
A2	3.3V	AD28	C15	3.3V	GPIO12/M0MD/R0MD
A3	3.3V	AD23/GPO44	C16	3.3V	GPIO10/M0RXER/R1MDC
A4	3.3V	AD21/GPO42	C17	3.3V	GPIO0
A5	3.3V	AD19/GPO40	C18	3.3V	GPIO9/M0MDC/R0MDC
A6	3.3V	AD16/M1TXEN	D1	3.3V	CBE3
A7	3.3V	AD10/M1RXER	D2	3.3V	CLKRUN
A8	3.3V	AD9/M1RXD3	D3	3.3V	PCLK
A9	3.3V	AD8/M1RXD2	D4	1.5V	VDD
A10	3.3V	AD4/M1MDC	D5	3.3V	AD26/GPO47
A11	3.3V	AD1/M1TXCLK	D6	1.5V	GNDH
A12	3.3V	CLKOUT/M0TXCLK/REFCLK	D7	1.5V	VDDH
A13	3.3V	DAK1/M0TXER/R1TXEN	D8	3.3V	GND33
A14	3.3V	GPO37/M0RXD3/R1RXD1	D9	1.5V	GND
A15	3.3V	GPIO7/M0RXCLK/R1CRSDV	D10	1.5V	GNDH
A16	3.3V	GPIO14/M0TXD0/R0TXD0	D11	3.3V	VDD33
A17	3.3V	GPIO11/M0COL	D12	1.5V	GND
A18	3.3V	M0CRS/R1MD/BIGENDIAN	D13	3.3V	VDD33
B1	3.3V	AD30	D14	1.5V	GNDH
B2	3.3V	CBE1	D15	3.3V	DCTS#/GPO35
B3	3.3V	AD27	D16	3.3V	GPIO01
B4	3.3V	AD22/GPO43	D17	3.3V	DCD#/GPI15
B5	3.3V	AD20/GPO41	D18	3.3V	DDIN/GPO34
B6	3.3V	AD14/M1TXD2	E1	3.3V	GNT0#
B7	3.3V	AD15/M1TXD3	E2	3.3V	GNT1#
B8	3.3V	AD11/M1RXDV	E3	3.3V	DEVSEL#
B9	3.3V	AD07/M1RXD1	E4	3.3V	VDD33
B10	3.3V	AD05/M1MD	E8	3.3V	VDD33
B11	3.3V	AD02/M1COL	E9	1.5V	GND
B12	3.3V	AD00/M1RXCLK	E10	3.3V	GND33
B13	3.3V	SYSEN#/M0RXD2/R1RXD0	E11	1.5V	VDD
B14	3.3V	GPO38/M0RXD0/R0RXD0	E15	3.3V	VDD33
B15	3.3V	GPIO8/M0RXDV/R0CRSDV	E16	3.3V	DRTS#/GPO33/PCIEN
B16	3.3V	GPIO4/M0RXD1/R0RXD1	E17	3.3V	GPIO2
B17	3.3V	GPIO13/M0TXD1/R0TXD1	E18	3.3V	SPOWER
B18	3.3V	GPIO3	F1	3.3V	IRDY#
C1	3.3V	CBE0	F2	3.3V	LOCK#
C2	3.3V	CBE2	F3	3.3V	FRAME#
C3	3.3V	AD31	F4	3.3V	GND33
C4	3.3V	AD25/GPO46	F15	1.5V	GNDH
C5	3.3V	AD17/M1TXER	F16	3.3V	POWER
C6	3.3V	AD24/GPO45	F17	3.3V	DDOUT/GPO32/DBUS32
C7	3.3V	AD13/M1TXD1	F18	3.3V	CLKX1
C8	3.3V	AD18/GPO39	G1	3.3V	PAR
C9	3.3V	AD12/M1TXD0	G2	3.3V	REQ1#
C10	3.3V	AD06/M1RXD0	G3	3.3V	REQ0#
C11	3.3V	AD3/M1CRS	G4	3.3V	GNT2#
C12	3.3V	DRQ1/M0TXD2/R1TXD0	G15	1.5V	AVDD
C13	3.3V	GPO36/M0TXEN/R0TXEN	G16	3.3V	MPOWER

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

Remark # indicates active low.

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No.	Power	Pin name	No.	Power	Pin name
G17	3.3V	POWERON	M18	3.3V	BKTGIO#
G18	3.3V	CLKX2	N1	3.3V	DATA21/GPIO21
H1	3.3V	REQ2#	N2	3.3V	DATA19/GPIO19
H2	3.3V	RST#	N3	3.3V	DATA18/GPIO18
H3	3.3V	PERR#	N4	1.5V	GND
H4	3.3V	SERR#	N15	1.5V	VDDH
H5	1.5V	GNDH	N16	3.3V	HLDAK#/DAK0
H14	3.3V	VDD33	N17	3.3V	JTRST#
H15	3.3V	GND33	N18	3.3V	JTDI/RMODE#
H16	3.3V	RTCRST#	P1	3.3V	DATA17/GPIO17
H17	3.3V	BATTINH/BATTINT#	P2	3.3V	DATA16/GPIO16
H18	3.3V	RTCX2	P3	3.3V	DATA14
J1	3.3V	STOP#	P4	1.5V	GNDH
J2	3.3V	TRDY#	P8	1.5V	VDDH
J3	3.3V	DATA29/GPIO29	P9	3.3V	GND33
J4	1.5V	GND	P10	1.5V	GND
J5	1.5V	GNDH	P11	3.3V	GND33
J14	1.5V	VDD	P15	3.3V	ADD6
J15	3.3V	GND33	P16	3.3V	HLDRQ#/DRQ0
J16	3.3V	RTS#/CLKSEL1	P17	3.3V	JTDO/IRDOUT#
J17	3.3V	GPIO6/SYSDIR	P18	3.3V	JTCK
J18	3.3V	RTCX1	R1	3.3V	DATA13
K1	3.3V	DATA31/GPIO31	R2	3.3V	DATA12
K2	3.3V	DATA30/GPIO30	R3	3.3V	DATA10
K3	3.3V	DATA25/GPIO25	R4	1.5V	GNDH
K4	3.3V	GND33	R5	3.3V	VDD33
K5	3.3V	VDD33	R6	3.3V	VDD33
K14	3.3V	VDD33	R7	3.3V	VDD33
K15	1.5V	GNDH	R8	1.5V	GND
K16	3.3V	JTMS	R9	1.5V	GNDH
K17	3.3V	RSTSW#	R10	3.3V	GND33
K18	3.3V	LEDOUT#/RTCCLKSEL	R11	3.3V	ADD9
L1	3.3V	DATA28/GPIO28	R12	3.3V	ADD8
L2	3.3V	DATA26/GPIO26	R13	3.3V	VDD33
L3	3.3V	DATA20/GPIO20	R14	1.5V	VDD
L4	3.3V	DATA23/GPIO23	R15	1.5V	GNDH
L5	1.5V	VDDH	R16	3.3V	DSR#
L14	1.5V	AGND	R17	3.3V	IRDIN
L15	1.5V	GND	R18	3.3V	CTS#
L16	3.3V	DTR#/CLKSEL0	T1	3.3V	DATA11
L17	3.3V	TXD/CLKSEL2	T2	3.3V	DATA9
L18	3.3V	SIN/JTAGEN	T3	3.3V	DATA6
M1	3.3V	DATA24/GPIO24	T4	3.3V	DATA1
M2	3.3V	DATA27/GPIO27	T5	3.3V	DQM0/LBE0/ADD0
M3	3.3V	DATA22/GPIO22	T6	3.3V	DATA0
M4	3.3V	DATA15	T7	3.3V	SWR#
M15	3.3V	SOUT	T8	3.3V	CS1#
M16	3.3V	SECLK	T9	3.3V	ADD22
M17	3.3V	RXD	T10	3.3V	ADD16

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

Remark # indicates active low.

(3/3)

No.	Power	Pin name	No.	Power	Pin name
T11	3.3V	ADD12	U15	3.3V	ADD3
T12	3.3V	ADD15	U16	3.3V	IOCS0#
T13	3.3V	ADD13	U17	3.3V	RD#
T14	3.3V	ADD10	U18	3.3V	IORDY
T15	3.3V	ADD01/ADD25	V1	3.3V	DATA7
T16	3.3V	ROMCS0#	V2	3.3V	DATA5
T17	3.3V	TESTMODE	V3	3.3V	DATA3
T18	3.3V	WR#	V4	3.3V	SCLK
U1	3.3V	DATA8	V5	3.3V	DQM2/LBE2
U2	3.3V	DATA4	V6	3.3V	CAS
U3	3.3V	DATA2	V7	3.3V	CKE0
U4	3.3V	DQM1/LBE1/UBE	V8	3.3V	CS0#
U5	3.3V	DQM3/LBE3	V9	3.3V	CS3#/ROMCS3#
U6	3.3V	RAS	V10	3.3V	ADD23
U7	3.3V	CKE1	V11	3.3V	ADD19
U8	3.3V	CS2#/ROMCS2#	V12	3.3V	ADD17
U9	3.3V	ADD24	V13	3.3V	ADD14
U10	3.3V	ADD21	V14	3.3V	ADD11
U11	3.3V	ADD20	V15	3.3V	ADD5
U12	3.3V	ADD18	V16	3.3V	ADD2
U13	3.3V	ADD7	V17	3.3V	IOCS1#
U14	3.3V	ADD4	V18	3.3V	ROMCS1#

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

Remark # indicates active low.

PIN IDENTIFICATION

(1/2)

AD(0:31)	: Address/Data Bus
ADD(1:25)	: Address Bus
AGND	: GND for PLL
AVDD	: VDD for PLL
BATTINH	: Battery Inhibit
BATTINT#	: Battery Interrupt Request
BIGENDIAN	: Big Endian
BKTGIO#	: Break Trigger I/O
CAS	: Column Address Strobe
CBE(0:3)	: Command/Byte Enable
CKE(0:1)	: Clock Enable
CLKSEL(0:2)	: Clock Select
CLKOUT	: Clock Output
CLKRUN	: Clock Run
CLKX1	: Clock X1
CLKX2	: Clock X2
CS(0:3)#	: Chip Select
CTS#	: Clear to Send
DAK(0:1)	: DMA Acknowledge
DATA(0:31)	: Data Bus
DBUS32	: Data Bus 32
DCD#	: Data Carrier Detect
DCTS#	: Debug Serial Clear to Send
DDIN	: Debug Serial Data Input
DDOUT	: Debug Serial Data Output
DEVSEL#	: Device Select
DQM(0:3)	: Data Input/ Output
DRQ(0:1)	: DMA Request
DRTS#	: Debug Serial Request to Send
DSR#	: Data Set Ready
DTR#	: Data Terminal Ready
FRAME#	: Cycle Frame
GND33	: Ground
GND, GNDH	: Ground
GNT(0:2)#	: Grant
GPI15	: General Purpose I
GPIO(0:14,16:31)	: General Purpose I/O
GPO(32:47)	: General Purpose O
HLDRQ#	: Hold Request
HOLDAK#	: Hold Acknowledge
IOCS(0:1)#	: I/O Chip Select
IORDY	: I/O Ready
IRDY#	: Initiator Ready
IRDIN	: IrDA Data Input
IRDOUT#	: IrDA Data Output
JTAGEN	: JTAG Enable
JTCK	: JTAG Clock
JTDI	: JTAG Data Input
JTDO	: JTAG Data Output
JTMS	: JTAG Mode Select
JTRST#	: JTAG Reset
LBE(0:3)	: System Bus Byte Enable
LEDOUT#	: LED Output
LOCK#	: Lock
M0COL	: MII Channel 0 Collision
M0CRS	: MII Channel 0 Carrier sense
M0MD	: MII Channel 0 Management Data
M0MDC	: MII Channel 0 Management Clock
M0RXCLK	: MII Channel 0 Receive Clock
M0RXD(0:3)	: MII Channel 0 Receive Data
M0RXDV	: MII Channel 0 Receive Data Valid
M0RXER	: MII Channel 0 Receive Error
M0TXCLK	: MII Channel 0 Transmit Clock
M0TXD(0:3)	: MII Channel 0 Transmit Data
M0TXEN	: MII Channel 0 Transmit Enable
M0TXER	: MII Channel 0 Transmit Error
M1COL	: MII Channel 1 Collision
M1CRS	: MII Channel 1 Carrier sense
M1MD	: MII Channel 1 Management Data
M1MDC	: MII Channel 1 Management Clock
M1RXCLK	: MII Channel 1 Receive Clock
M1RXD(0:3)	: MII Channel 1 Receive Data
M1RXDV	: MII Channel 1 Receive Data Valid
M1RXER	: MII Channel 1 Receive Error
M1TXCLK	: MII Channel 1 Transmit Clock
M1TXD(0:3)	: MII Channel 1 Transmit Data
M1TXEN	: MII Channel 1 Transmit Enable
M1TXER	: MII Channel 1 Transmit Error
MPOWER	: Main Power
PAR	: Parity
PCIEN	: PCI Enable
PCLK	: PCI Clock
PERR#	: Parity Error
POWER	: Power Switch
POWERON	: Power On State
R0CRSDV	: RMII Channel 0 Carrier Sense / Receive Data Valid
R0MD	: RMII Channel 0 Management Data
R0MDC	: RMII Channel 0 Management Clock
R0RXD(0:1)	: RMII Channel 0 Receive Data
R0TXD(0:1)	: RMII Channel 0 Transmit Data
R0TXEN	: RMII Channel 0 Transmit Enable

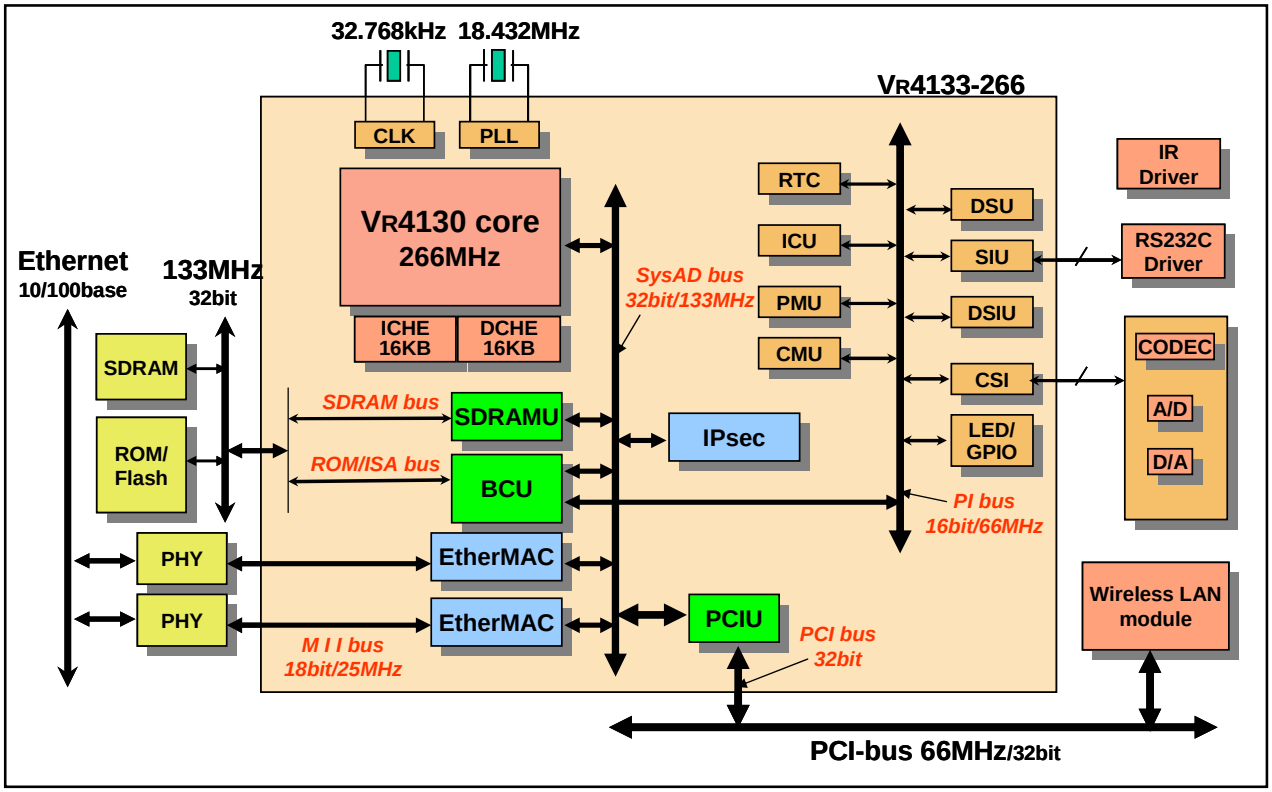
Remark # indicates active low.

(2/2)

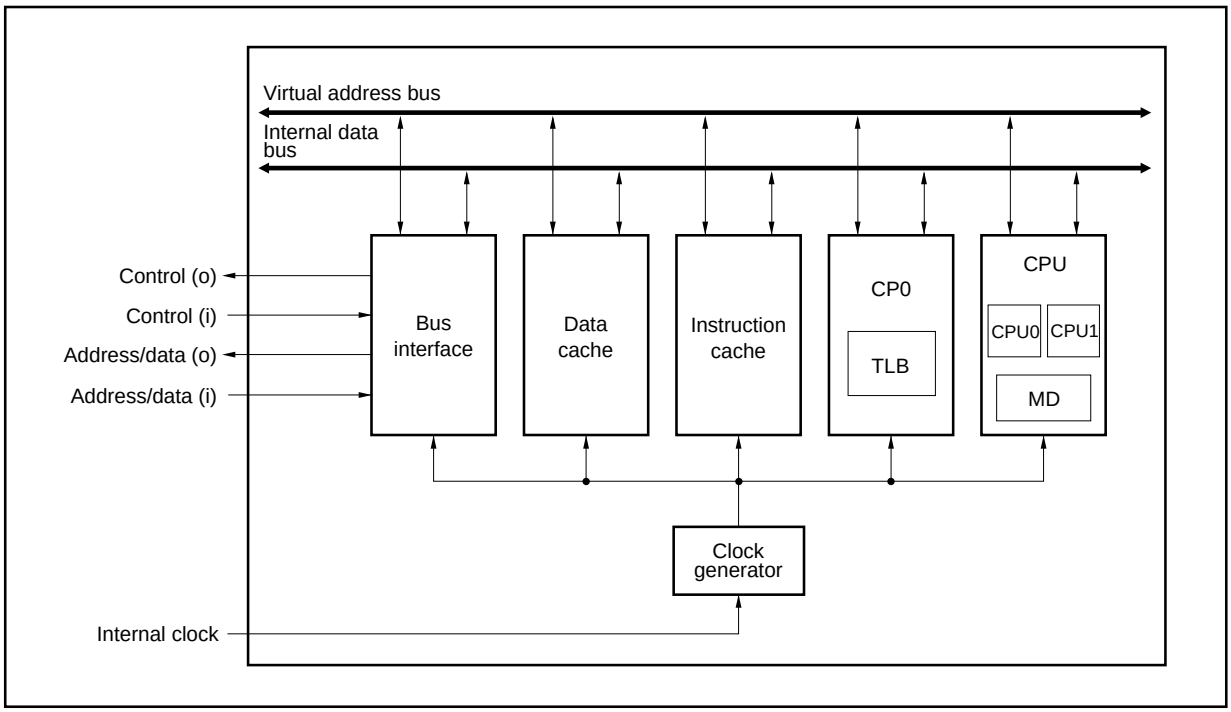
R1CRSDV	: RMII Channel 1 Carrier Sense / Receive Data Valid	RTS#	: Request to Send
R1MD	: RMII Channel 1 Management Data	RxD	: Receive Data
R1MDC	: RMII Channel 1 Management Clock	SCLK	: SDRAM Clock
R1RXD(0:1)	: RMII Channel 1 Receive Data	SECLK	: Clocked Serial Clock
R1TXD(0:1)	: RMII Channel 1 Transmit Data	SEL	: IrDA Module Select
R1TXEN	: RMII Channel 1 Transmit Enable	SERR#	: System Error
RAS	: Row Address Strobe	SIN	: Clocked Serial Input
RD#	: Read	SOUT	: Clocked Serial Output
REQ(0:2)#	: Request	SPOWER	: SDRAM Power Control
REFCLK	: RMII Reference Clock	STOP#	: Target Assert Stop
RMODE#	: Reset Mode	SWR#	: SDRAM Write
ROMCS(0:3)#	: ROM Chip Select	SYSDIR	: System Bus Buffer Direction
RST#	: Reset	SYSEN#	: System Data Enable
RSTSW#	: Reset Switch	TRDY#	: Target Ready
RTCCLKSEL	: Real-time Clock Select	TESTMODE	: Test Mode (**注意** 1)
RTCRST#	: Real-time Clock Reset	TxD	: Transmit Data
RTCX1	: Real-time Clock X1	UBE	: Upper Byte Enable for System Bus
RTCX2	: Real-time Clock X2	VDD33	: Power Supply Voltage
		VDD, VDDH	: Power Supply Voltage
		WR#	: Write

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 System initial setting function

V_R4133 can be changed the function of the pins by the constitution of the system. The changes of these pins become possible by the setting of the initial pin setting or internal registers at the time of the RTC reset.
In V_R4133 is possible that it uses it with the following system constitution (mode).

System constitution	PCI interface	Ether MAC interface for PHY device	Data bus width
Mode A	Use possibility	MII interface (1Channel)	16/32 bus width
Mode B	Use possibility	RMII interface (2 Channel)	16/32 bus width
Mode C	Unusable	MII interface (2 Channel)	16/32 bus width
Mode D	Use possibility	Unusable	16/32 bus width

Also, It can do the setting regarding the following item.

- The CPU core frequency(265.9MHz～133MHz) setting
- The selection of the startup clock (32 KHz, or 18MHz) for V_R4133 at the time of RTC reset
- The endian (little endian, or big endian) setting
- N-Wire / Boundary scan use permission

1.1.1 Initial setting pins function at RTC reset

V_R4133 samples the following pins condition at RTC reset, and setting of initial condition.

- DDOUT/GPO32/DBUS32
- DRTS#/GPO33/PCIEN
- DTR#/CLKSEL0
- RTS#/CLKSEL1
- TXD/CLKSEL2
- LEDOUT#/RTCCLKSEL
- M0CRS/R1MD/BIGENDIAN
- SIN/JTAGEN

Signal	I/O	Function
DDOUT/ GPIO32/DBUS32	I/O	The function differs depending on the operating status. • **During normal operation (output)** DDOUT: This signal functions as the debug serial transmit data signal. • **During RTC reset (input)** DBUS32: This signal functions as the data bus width switching signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Data bus is used with 32-bit width 0: Data bus is used with 16-bit width This signal can be used as a general-purpose output port when not being used as the DDOUT or DBUS32 signal.

Signal	I/O	Function
DRTS#/ GPO33/ PCIEN	I/O	The function differs depending on the operating status. • **During normal operation (output)** DRTS#: This signal functions as the debug serial transmit request signal. • **During RTC reset (input)** PCIEN: This signal functions as the PCI interface enable signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: PCI interface enabled 0: PCI interface disabled (The pin of the PCI interface is used as the pin of the MII (channel.1) interface and GPIO(47:39)) This signal can be used as a general-purpose output port when not being used as the DRTS# or PCIEN signal.
TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0	I/O	The function differs depending on the operating status. • **During normal operation (output)** Signals used for serial communication TxD signal: This is a transmit data signal. It is used when the VR4133 sends serial data to the RS-232-C controller. RTS# signal: This is a transmit request signal. This signal is asserted when the VR4133 is ready to receive serial data from the RS-232-C controller. DTR# signal: This is a terminal equipment ready signal. This signal is asserted when the VR4133 is ready to transmit or receive serial data. • **During RTC reset (input)** Signals (CLKSEL(2:0)) used to set the CPU core operation frequency and internal bus clock frequency. These signals are sampled when the RTCRST# signal changes from low level to high level. For the relationship between the CLKSEL pin setting and each clock frequency, see **Table 1-1 Setting of CLKSEL and Frequency of PClock, VTClock, TClock, and MasterOut (Default Value**).

Table 1-1. Setting of CLKSEL and Frequency of PClock, VTClock, TClock, and MasterOut (Default Value)

CLKSEL(2:0)	PClock (MHz)	VTClock (MHz)	TClock (MHz)	MasterOut (MHz)
111	RFU	RFU	RFU	RFU
110	RFU	RFU	RFU	RFU
101	RFU	RFU	RFU	RFU
100	265.9	66.48	33.24	8.31
011	199.1	66.37	33.18	8.29
010	165.9	55.30	27.65	6.91
001	149.0	49.67	24.83	6.20
000	133.0	66.50	33.25	8.31

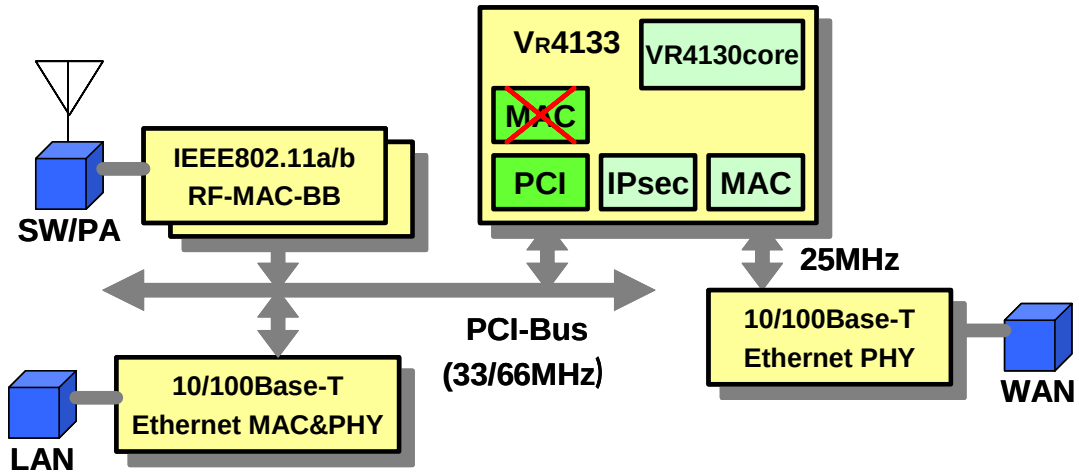
Remark RFU: Reserved for Future Use

Signal	I/O	Function
LEDOUT#/ RTCCLKSEL	Output	The function differs depending on the operating status. • **During normal operation (output)** LEDOUT#: This is an output signal for lighting LED in normal operation mode. • **During RTC reset (input)** RTCCLKSEL: It is the signal that selects the startup clock that uses it at the RTC reset Boot. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Use as the startup clock of 32.768kHz (In the case that it caused Boot with the clock of 32.768KHz, it requires the time for about 2 seconds.) 0: Use as the startup clock of 18.432MHz (The crystal of 32.768kHz does not need to be connected, to use the clock of only 18.432MHz. Therefore, it can activate it in about 100 ms.
M0CRS/R1MD/ BIGENDIAN	I/O	The function differs depending on the operating status. • **During normal operation (output)** **When mode A or C** It becomes the function as a M0CRS pin (input) MII interface (channel 0) carrier sense. It inputs a carrier sense signal from the PHY device connected to the port. If the port is not used, fix M0CRS to the low level. . **When mode B** It becomes the function as a R1MD pin (input/output) RMII interface (channel 1) management data. It is a bidirectional RMII serial management data signal. • **During RTC reset (input)** BIGENDIAN: This signal selects big endian. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Big endian 0: Little endian It doesn't guarantee the action regarding the setting other than the above.
SIN/JTAGEN	Input	The function differs depending on the operating status. • **During normal operation (output)** Clocked serial input signal • **During RTC reset (input)** JTAGEN: The use of N-wire, Boundary scan function and IRDOUT function are permitted. When the RTCRST# signal changes from low to high, this signal is sampled. 1: N-Wire and Boundary scan permit the use. However, the use prohibition of IRDOUT. 0: N-Wire and Boundary scan be the prohibition that uses it. However, the use permission of IRDOUT.

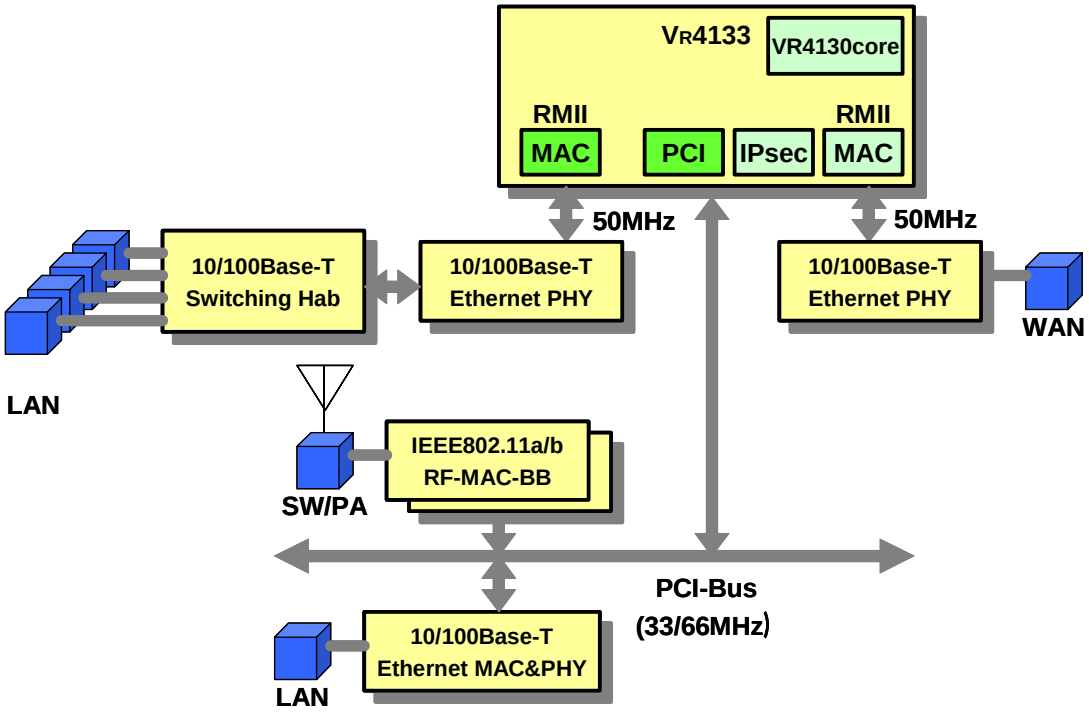
1.1.2 Change of the Ether MAC function

Signal	I/O	Function
DRTS#/ GPO33/ PCIEN	I/O	The function differs depending on the operating status. • **During normal operation (output)** DRTS#: This signal functions as the debug serial transmit request signal. • **During RTC reset (input)** PCIEN: This signal functions as the PCI interface enable signal. When the RTCRST# signal changes from low to high, this signal is sampled. **1: PCI interface use permission condition** In case of, Ethernet (channel 0) controller configuration register's (0x0F001634) and Ethernet (channel 1) controller configuration register's (0x0F001934) MII pin select bit is 0. : Function as CLKOUT pin, GPIO pin and SYSEN pin **=> Mode D (V_R4131 compatible mode)** In case of, Ethernet (channel 0) controller configuration register's (0x0F001634) MII pin select bit is 1, and this register's RMII mode bit is 0. : The PCI pins and MII interface (channel 0) pins become possible and use. **=> Mode A** In case of, Ethernet (channel 0) controller configuration register's (0x0F001634) MII pin select bit is 1, and this register's RMII mode bit is 1, and, Ethernet (channel 1) controller configuration register's (0x0F001934) RMII mode bit is 1. : The PCI pins and RMII interface (channel 0 and 1) pins become possible and use. **=> Mode B** **0: PCI interface use prohibition condition** In case of, Ethernet (channel 0) controller configuration register's (0x0F001634) MII pin select bit is 1, and this register's RMII mode bit is 0, and, Ethernet (channel 1) controller configuration register's (0x0F001934) RMII mode bit is 0. : The GPIO(39:47) pins and MII interface (channel 1) pins become possible and use. **=> Mode C** It doesn't guarantee the action regarding the setting other than the above.

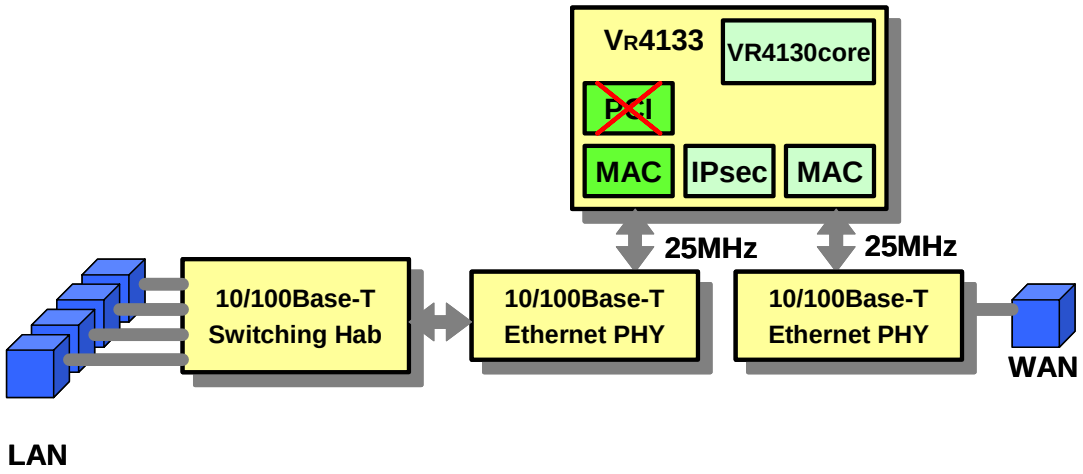
Although the PCI interface becomes possible the use in the case of **mode A**, 1 channel of only the MII interface pin becomes the impossibility that use



Although the PCI interface is use possibility, and, RMII mode Ether MAC becomes possible 2 channel use in the case of **mode B**.



The PCI interface signal is not able to use it in the case of **mode C**. However, Ether MAC (MII mode) be 2 channel use possibility. .



1.2 List of Pin Functions

(1) Memory interface signals (1/3)

Signal	I/O	Function
SCLK	Output	Operation clock for SDRAM
ADD1/ADD25	Output	MSB bit or LSB bit of 25 bit address bus. These signals are used to specify addresses for the VR4133, SDRAM, ROM, and I/O space.
ADD(24:2)	Output	Higher 24 bits or Lower 24 bits of the 25-bit address bus These signals are used to specify addresses for the VR4133, SDRAM, ROM, and I/O space.
DATA(15:0)	I/O	16-bit data bus These signals are used to transfer data between the VR4133 and the SDRAM, ROM, or I/O space.
DATA(31:16)/ GPIO(31:16)	I/O	The function differs depending on the DBUS32 pin setting. • **When DBUS32 = 1** These signals function as the higher 16 bits of the 32-bit data bus. They are used to transfer data between the VR4133 and the DRAM or ROM. • **When DBUS32 = 0** These signals function as general-purpose I/O ports.
CKE(1:0)	Output	Clock enable signals for SDRAM CKE(1:0) supports the following banks. SDRAM bank / CKE(1:0) / 32-bit data bus / 16-bit data bus Bank 3 / CKE1 / CS3#/ROMCS3# / DQM3 Bank 2 / CKE0 / CS2#/ROMCS2# / DQM2 Bank 1 / CKE1 / CS1# / CS1# Bank 0 / CKE0 / CS0# / CS0#
DQM3/LBE3	Output	The function differs depending on the setting of the DBUS32 pin and the connected device. • **When DBUS32 = 1 and** SDRAM or ROM is accessed: This is the byte enable signal for DATA (31:24) of the 32-bit data bus. A 32-bit external I/O device is accessed: This is the byte enable signal for DATA (31:24) of the 32-bit data bus. A 16-bit external I/O device is accessed: This is the CS signal of external I/O device. This signal becomes active when a command is issued for the external I/O device connected to the highest address. . • **When DBUS32 = 0 and** SDRAM is accessed: This is the CS signal for SDRAM. This signal becomes active when a command is issued for the SDRAM connected to the highest address. ROM is accessed: This is the CS signal for ROM. This signal becomes active when a command is issued for the ROM connected to the highest address. External I/O device is accessed: This is the CS signal of external I/O device. This signal becomes active when a command is issued for the external I/O device connected to the highest address.

(2/3)

Signal	I/O	Function
DQM2/LBE2	Output	The function differs depending on the setting of the DBUS32 pin and the connected device. • **When DBUS32 = 1 and** SDRAM is accessed: This is the byte enable signal for DATA (23:16) of the 32-bit data bus. A 32-bit external I/O device is accessed: This is the byte enable signal for DATA (23:16) of the 32-bit data bus. A 16-bit external I/O device is accessed: This is the CS signal of external I/O device. This signal becomes active when a command is issued for the external I/O device connected to the second highest address. • **When DBUS32 = 0 and** SDRAM is accessed: This is the CS signal for SDRAM. This signal becomes active when a command is issued for the SDRAM connected to the second highest address. ROM is accessed: This is the CS signal for ROM. This signal becomes active when a command is issued for the ROM connected to the second highest address. External I/O device is accessed: This is the CS signal of external I/O device. This signal becomes active when a command is issued for the external I/O device connected to the second highest address.
DQM1/LBE1/ UBE	Output	The function differs depending on the connected device. When 32 bits width of ROM or SDRAM is accessed: This is the byte enable signal for DATA (15:8). When a 32-bit external I/O device is accessed: This is the byte enable signal for DATA (15:8). When a 16-bit ROM or external I/O device is accessed (little endian): This is the ADD0 signal of the address bus or ROM bus. When a 16-bit ROM or external I/O device is accessed (big endian): This is the high-byte enable signal of the I/O bus or ROM bus.
DQM0/LBE0/ ADD0	Output	The function differs depending on the connected device. When 32 bits width of ROM or SDRAM is accessed: This is the byte enable signal for DATA (7:0). When a 32-bit external I/O device is accessed: This is the byte enable signal for DATA (7:0). When a 16-bit ROM or external I/O device is accessed (little endian): This is the ADD0 signal of the address bus or ROM bus. When a 16-bit ROM or external I/O device is accessed (big endian): This is the high-byte enable signal of the I/O bus or ROM bus.
CS(1:0)#	Output	Chip select signal for SDRAM
RAS	Output	RAS signal for SDRAM
CAS	Output	CAS signal for SDRAM
GPIO6/SYSDIR	I/O	Direction signal for SDRAM If not used as the SYSDIR signal, this signal can be used as a GPIO pin.
SPOWER	Output	Power supply control signal for SDRAM
RD#	Output	This signal becomes active when a read access is performed for data from the I/O space and ROM.
WR#	Output	This signal becomes active when writing data to the I/O space.
SWR#	Output	This signal becomes active when writing data to SDRAM.

(3/3)

<table>
<tr><th>Signal</th><th>I/O</th><th>Function</th></tr>
<tr><td>ROMCS(1:0)#</td><td>Output</td><td>Chip select signals for ROM</td></tr>
<tr><td>CS(3:2)#/
ROMCS(3:2)#</td><td>Output</td><td>Chip select signals for an expansion SDRAM or expansion ROM
• When using expansion SDRAM
These signals function as CS (3:2)#.
• When using expansion ROM
These signals function as ROMCS (3:2)#.</td></tr>
<tr><td>HLDRQ#/DRQ0</td><td>Input</td><td>The function differs depending on the Contents of the following internal register
HLDEN IORHHEN P2MHHEN M2PHHEN DMAPIN Pin function
1 0 - - 0 HLDRQ#
1 - 0 0 1 HLDRQ#
0 1 - - 0 DRQ0#(I/O-Mem)
0 - 1 0 1 DRQ0#(PCI-Mem)
0 - 0 1 1 DRQ0#(Mem-PCI)
HLDEN bit: bit 2 of BCUCNTREG1 (0x0F00 0000) register
IORHHEN bit: bit 4 of DMAREQREG (0x0F00 0048) register
P2MHHEN bit: bit 3 of PCIDMACTRLREG (0x0F00 0C90) register
M2PHHEN bit: bit 2 of PCIDMACTRLREG (0x0F00 0C90) register
DMAPIN bit: bit 8 of CONTROLREG (0x0F00 004E) register
HLDRQ#: Requests signal for the ownership of System bus and DRAM from external bus master.
DRQ0#: Requests signal for the ownership of DMA function between I/O and memory, or PCI interface and memory.</td></tr>
<tr><td>HLDAK#/DAK0</td><td>Output</td><td>The function differs depending on the Contents of the following internal register
HLDEN IORHHEN P2MHHEN M2PHHEN DMAPIN Pin function
1 0 - - 0 HLDAK#
1 - 0 0 1 HLDAK#
0 1 - - 0 DAK0#(I/O-Mem)
0 - 1 0 1 DAK0#(PCI-Mem)
0 - 0 1 1 DAK0#(Mem-PCI)
HLDEN bit: bit 2 of BCUCNTREG1 (0x0F00 0000) register
IORHHEN bit: bit 4 of DMAREQREG (0x0F00 0048) register
P2MHHEN bit: bit 3 of PCIDMACTRLREG (0x0F00 0C90) register
M2PHHEN bit: bit 2 of PCIDMACTRLREG (0x0F00 0C90) register
DMAPIN bit: bit 8 of CONTROLREG (0x0F00 004E) register
HLDAK#: Acknowledge signal for the ownership of System bus and DRAM from external bus master.
DAK0#: Acknowledge signal for the ownership of DMA function between I/O and memory, or PCI interface and memory.</td></tr>
</table>

(2) I/O device interface signals

Signal	I/O	Function
IOCS(1:0)#	Output	Device chip select signals These signals become active when the VR4133 accesses the I/O device using the ADD bus or DATA bus.
IORDY	Input	Device ready signal Make this signal active in a state in which the I/O device can be accessed from the VR4133.

(3) Clock interface signals

Signal	I/O	Function
RTCX1	Input	This is the 32.768 kHz oscillator's input pin. It is connected to one side of a crystal resonator.
RTCX2	Output	This is the 32.768 kHz oscillator's output pin. It is connected to one side of a crystal resonator.
CLKX1	Input	This is the 18.432 MHz oscillator's input pin. It is connected to one side of a crystal resonator.
CLKX2	Output	This is the 18.432 MHz oscillator's output pin. It is connected to one side of a crystal resonator.
CLKOUT/ M0TXCLK/ REFCLK	I/O	Refer to **(13) Ethernet controller interface signals**.

(4) Battery monitor interface signals

Signal	I/O	Function
BATTINH/ BATTINT#	Input	The function differs depending on the setting of the MPOWER pin. • **When MPOWER = 0** BATTINH function This signal enables/disables activation at power-on. 1: Activation enabled 0: Activation disabled • **When MPOWER = 1** BATTINT# function This is an interrupt signal that is output when the remaining power is low during normal operation. An external circuit checks the remaining battery power. Activate the signal at this pin if voltage sufficient for operation cannot be supplied.

(5) Initialization interface signals

(1/2)

Signal	I/O	Function
MPOWER	Output	This signal indicates that the VR4133 is operating. This signal is inactive in Hibernate mode.
POWERON	Output	This signal indicates that the VR4133 is ready to operate. It becomes active when a power-on factor is detected and becomes inactive when the BATTINH/BATTINT# signal check operation is completed.
POWER	Input	This is the VR4133 activation signal.

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Signal	I/O	Function
RSTSW#	Input	This is the VR4133 reset signal.
RTCRST#	Input	This signal resets the RTC. This pin uses it when the power supply was supplied to the device for the first time. RTCCLKSEL pin is sampled when RTCRST# signal changed into the high level from the low level. The startup time is needed as follows by the condition of pins at the sampling. • **When RTCCLKSEL = 0** 18.432MHz is used the startup clock. (Only about 100ms is required for Booting.) • **When RTCCLKSEL = 1** 32.768kHz is used the startup clock. (About 2 seconds is required for Booting.)

(6) RS-232-C interface signals

Signal	I/O	Function
RxD	Input	This is a receive data signal. It is used when the RS-232-C controller sends serial data to the VR4133.
CTS#	Input	This is a transmit enable signal. Assert this signal when the RS-232-C controller is ready to receive transmission of serial data.
DCD#/GPI15	Input	This is a carrier detection signal. Assert this signal when valid serial data is being received. It is also used as a power-on factor for the VR4133. When this pin is not used for the DCD# signal, this pin can be used as an interrupt detection input for the GIU.
DSR#	Input	This is the data set ready signal. Assert this signal when the RS-232-C controller is ready to transfer serial data between the controller and the VR4133.
TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0	I/O	The function differs depending on the operating status. • **During normal operation (output)** Signals used for serial communication TxD signal: This is a transmit data signal. It is used when the VR4133 sends serial data to the RS-232-C controller. RTS# signal: This is a transmit request signal. This signal is asserted when the VR4133 is ready to receive serial data from the RS-232-C controller. DTR# signal: This is a terminal equipment ready signal. This signal is asserted when the VR4133 is ready to transmit or receive serial data. • **During RTC reset (input)** Signals (CLKSEL (2:0)) used to set the CPU core operation frequency and internal bus clock frequency. These signals are sampled when the RTCRST# signal changes from low level to high level. For the relationship between the CLKSEL pin setting and each clock frequency, see **Table 1-1 Setting of CLKSEL and Frequency of PClock, VTClock, TClock, and MasterOut (Default Value**).

Table 1-1. Setting of CLKSEL and Frequency of PClock, VTClock, TClock, and MasterOut (Default Value)

CLKSEL(2:0)	PClock (MHz)	VTClock (MHz)	TClock (MHz)	MasterOut (MHz)
111	RFU	RFU	RFU	RFU
110	RFU	RFU	RFU	RFU
101	RFU	RFU	RFU	RFU
100	265.9	66.48	33.24	8.31
011	199.1	66.37	33.18	8.29
010	165.9	55.30	27.65	6.91
001	149.0	49.67	24.83	6.20
000	133.0	66.50	33.25	8.31

Remark RFU: Reserved for Future Use

(7) Debug serial interface signals

Signal	I/O	Function
DDIN/GPI34	I/O	Debug serial data input signal. This signal can be used as a general-purpose output port when not being used as the DDIN signal.
DCTS#/GPI35	I/O	Transmit enable signal. Assert this signal when the RS-232-C controller can receive the serial data transmission. This signal can be used as a general-purpose output port when not being used as the DCTS# signal.
DDOUT/GPO32/ DBUS32	I/O	The function differs depending on the operating status. • **During normal operation (output)** DDOUT: This signal functions as the debug serial transmit data signal. • **During RTC reset (input)** DBUS32: This signal functions as the data bus width switching signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Data bus is used with 32-bit width 0: Data bus is used with 16-bit width This signal can be used as a general-purpose output port when not being used as the DDOUT or DBUS32 signal.
DRTS#/GPO33/ PCIEN	I/O	The function differs depending on the operating status. • **During normal operation (output)** DRTS#: This signal functions as the debug serial transmit request signal. • **During RTC reset (input)** PCIEN: This signal functions as the PCI interface enable signal. When the RTCRST# signal changes from low to high, this signal is sampled. 1: PCI interface enabled … **mode A,B,D** 0: PCI interface disabled … **mode C** (The Pins of PCI interface are used for MII interface (channel 1) and GPIO(47:39) function when this mode) This signal can be used as a general-purpose output port when not being used as the DRTS# or PCIEN signal.

(8) IrDA interface signals

Signal	I/O	Function
IRDIN	Input	This is an IrDA serial data input signal. It is used when the serial data is transferred from the IrDA controller to the VR4133. SIR can be used. If the IrDA controller used is a Hewlett Packard Company product, however, this signal should be used only for SIR.
JTDO/IRDOUT#	Output	This is the IrDA serial data output signal. It is used when the serial data is transferred from the VR4133 to the IrDA controller. This signal can be used as a JTAG serial data output signal when JTAG is used.

(9) Clocked serial signals

Signal	I/O	Function
SIN/JTAGEN	Input	The function differs depending on the operating status. • **During normal operation (output)** Clocked serial input signal • **During RTC reset (input)** JTAGEN: The use of N-wire, Boundary scan function and IRDOUT function are permitted. When the RTCRST# signal changes from low to high, this signal is sampled. 1: N-Wire and Boundary scan permit the use. However, the use prohibition of IRDOUT. 0: N-Wire and Boundary scan be the prohibition that uses it. However, the use permission of IRDOUT.
SOUT	Output	Clocked serial output signal
SECLK	Output	Synchronous clock output for the clocked serial interface

(10) General-purpose I/O signals

(1/2)

Signal	I/O	Function
GPIO(3:0)	I/O	Maskable activation factor input signals. These signals can be used as general-purpose I/O ports after activation.
GPIO(5:4)	I/O	General-purpose I/O ports.
GPIO6/SYSDIR	I/O	Refer to **(1) Memory interface signals**.
GPIO(8:7)	I/O	General-purpose I/O ports.
GPIO9/M0MDC/ R0MDC	I/O	Refer to **(13) Ethernet controller interface signals**.
GPIO10/ M0RXER/R1MDC	I/O	Refer to **(13) Ethernet controller interface signals**.
GPIO11/M0COL	I/O	Refer to **(13) Ethernet controller interface signals**.
GPIO12/ M0MD/R0MD	I/O	Refer to **(13) Ethernet controller interface signals**.
GPIO13/ M0TXD1/ R0TXD1	I/O	Refer to **(13) Ethernet controller interface signals**.
GPIO14/ M0TXD0/ R0TXD0	I/O	Refer to **(13) Ethernet controller interface signals**.

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Signal	I/O	Function
DCD#/GPI15	Input	Refer to **(6) RS-232-C interface signals**.
DATA(31:16)/ GPIO(31:16)	I/O	Refer to **(1) Memory interface signals**.
DDOUT/GPO32/ DBUS32	I/O	Refer to **(7) Debug serial interface signals**.
DRTS#/GPO33/ PCIEN	I/O	Refer to **(7) Debug serial interface signals**.
DDIN/GPI34	I/O	Refer to **(7) Debug serial interface signals**.
DCTS#/GPI35	I/O	Refer to **(7) Debug serial interface signals**.

(11) LED interface signal

Signal	I/O	Function
LEDOUT#/ RTCCLKSEL	Output	The function differs depending on the operating status. • **During normal operation (output)** LEDOUT#: This is an output signal for lighting LED in normal operation mode. • **During RTC reset (input)** RTCCLKSEL: It is the signal that selects the startup clock that uses it at the RTC reset Boot. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Use as the startup clock of 32.768kHz (In the case that it caused Boot with the clock of 32.768KHz, it requires the time for about 2 seconds.) 0: Use as the startup clock of 18.432MHz (The crystal of 32.768kHz does not need to be connected, to use the clock of only 18.432MHz. Therefore, it can activate it in about 100 ms.)

(12) PCI Like bus interface signals

(1/3)

Signal	I/O	Function
AD(17:0)	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** Signals used for MII interface (channel 1) pins.
AD(26:18)	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** These signals function as general-purpose I/O ports.
AD(31:27)	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** Please don't use it because it cannot the guarantee of the action.

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Signal	I/O	Function
CBE(3:0)	I/O	• **When mode A, B or D** These are the bus-command/byte-enable signals. In the address phase, bus commands are output, and in the data phase, they operate as the byte-enable signals. • **When mode C** Please don't use it because it cannot the guarantee of the action.
DEVSEL#	I/O	• **When mode A, B or D** This signal is asserted when the target is accessed and continues being asserted until the completion of the transaction. • **When mode C** Please don't use it because it cannot the guarantee of the action.
FRAME#	I/O	• **When mode A, B or D** This signal is asserted when the initiator starts the transaction. It also remains asserted throughout burst transfer. • **When mode C** Please don't use it because it cannot the guarantee of the action.
REQ(2:0)#	Input	• **When mode A, B or D** These signals are asserted when the master sends a request to the VR4133 for the bus mastership. • **When mode C** Please don't use it because it cannot the guarantee of the action.
GNT(2:0)#	Output	• **When mode A, B or D** These signals are asserted when the VR4133 grants bus mastership to the device making the request with the REQ# signal. • **When mode C** Please don't use it because it cannot the guarantee of the action.
IRDY#	I/O	• **When mode A, B or D** This signal is asserted when the initiator is in the data transfer enabled state. • **When mode C** Please don't use it because it cannot the guarantee of the action.
LOCK#	I/O	• **When mode A, B or D** This signal indicates a resource lock. • **When mode C** Please don't use it because it cannot the guarantee of the action.
PAR	I/O	• **When mode A, B or D** This signal outputs a low level if the number of "1" bits from the 36 AD (31:0) and CBE (3:0) signals is even, and a high level if the number is odd. • **When mode C** Please don't use it because it cannot the guarantee of the action.
PERR#	I/O	• **When mode A, B or D** This signal is asserted when a parity error occurs following a parity check by the data-read initiator in the read cycle or the data-write target in the write cycle. • **When mode C** Please don't use it because it cannot the guarantee of the action.

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Signal	I/O	Function
SERR#	I/O	• **When mode A, B or D** This signal is asserted when a fatal error for the system occurs. • **When mode C** Please don't use it because it cannot the guarantee of the action.
STOP#	I/O	• **When mode A, B or D** This signal is asserted when the target requires the initiator to abort the transaction. • **When mode C** Please don't use it because it cannot the guarantee of the action.
TRDY#	I/O	• **When mode A, B or D** This signal is asserted when the target is in the transfer-enabled state. • **When mode C** Please don't use it because it cannot the guarantee of the action.
PCLK	Output	• **When mode A, B or D** This is the PCI bus reference clock. • **When mode C** Please don't use it because it cannot the guarantee of the action.
CLKRUN	I/O	• **When mode A, B or D** This signal controls the clock for power management. • **When mode C** Please don't use it because it cannot the guarantee of the action.
RST#	Output	• **When mode A, B or D** This is the PCI bus reset signal. • **When mode C** Please don't use it because it cannot the guarantee of the action.

(13) Ethernet controller interface signals

(1/8)

Signal	I/O	Function
AD0/M1RXCLK	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXCLK pin (input) MII interface (channel 1) receive clock. It inputs a clock given by the PHY device. When 100Mbps mode : 25MHz When 10Mbps mode : 2.5MHz
AD1/M1TXCLK	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXCLK pin (input) MII interface (channel 1) transmit clock. It inputs a transmit clock necessary for outputting transmit data to a PHY device connected to the port.

(2/8)

Signal	I/O	Function
AD2/M1COL	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1COL pin (input) MII interface (channel 1) collision. It inputs a collision signal detected by the PHY device connected to the port. If the port is not used, fix M1COL to the low level. .
AD3/M1CRS	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1CRS pin (input) MII interface (channel 1) carrier sense. It inputs a carrier sense signal from the PHY device connected to the port. If the port is not used, fix M1CRS to the low level. .
AD4/M1MDC	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1MDC pin (output) MII interface (channel 1) management data clock. It is a transfer clock of MII serial management data.
AD5/M1MD	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1MD pin (input/output) MII interface (channel 1) management data. It is a bidirectional MII serial management data signal.
AD6/M1RXD0	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXD0 pin (input) MII interface (channel 1) receive data. It inputs receive data from the PHY device connected to the port. .
AD7/M1RXD1	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXD1 pin (input) MII interface (channel 1) receive data. It inputs receive data from the PHY device connected to the port. .
AD8/M1RXD2	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXD2 pin (input) MII interface (channel 1) receive data. It inputs receive data from the PHY device connected to the port. .

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Signal	I/O	Function
AD9/M1RXD3	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXD3 pin (input) MII interface (channel 1) receive data. It inputs receive data from the PHY device connected to the port. .
AD10/M1RXER	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXER pin (input) MII interface (channel 1) receive error. This is an input signal to detect an error that occurs in the PHY device connected to the port during reception. If the port is not used, fix M1RXER to the low level. .
AD11/M1RXDV	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1RXDV pin (input) MII interface (channel 1) receive data valid. It indicates that the receive data on M1RXD (3:0) is valid. If the port is not used, fix M1RXDV to the high or the low level. .
AD12/M1TXD0	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXD0 pin (output) MII interface (channel 1) transmit data. It outputs transmit data to the PHY device connected to the port. .
AD13/M1TXD1	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXD1 pin (output) MII interface (channel 1) transmit data. It outputs transmit data to the PHY device connected to the port. .
AD14/M1TXD2	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXD2 pin (output) MII interface (channel 1) transmit data. It outputs transmit data to the PHY device connected to the port. .
AD15/M1TXD3	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXD3 pin (output) MII interface (channel 1) transmit data. It outputs transmit data to the PHY device connected to the port. .

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Signal	I/O	Function
AD16/M1TXEN	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXEN pin (output) MII interface (channel 1) transmit enable. It indicates whether transmit data (M1TXD (3:0)) is valid for each port.
AD17/M1TXER	I/O	• **When mode A, B or D** This is a 32-bit address bus and data bus. In the address phase, addresses are output, and in the data phase, data is output. • **When mode C** It becomes the function as a M1TXER pin (output) MII interface (channel 1) transmit coding error. It indicates that an error has occurred in MAC during transmission.
CLKOUT/ M0TXCLK/ REFCLK	I/O	• **When mode D** This is the clock output to supply an external device. A 9.216 MHz clock is output in the non-Hibernate mode. The clock output stops at low level during Hibernate. • **When mode A or C** It becomes the function as a M0TXCLK pin (input) MII interface (channel 0) transmit clock. It inputs a transmit clock necessary for outputting transmit data to a PHY device connected to the port. • **When mode B** It becomes the function as a REFCLK pin (input) RMII interface (channel 0 and 1) transmit clock. It inputs a transmit clock necessary for outputting transmit data to a PHY device connected to the port.
GPIO9/M0MDC/ R0MDC	I/O	• **When mode D** Maskable activation factor input signals. This signal can be used as general-purpose I/O ports after activation. • **When mode A or C** It becomes the function as a M0MDC pin (output) MII interface (channel 0) management data clock. It is a transfer clock of MII serial management data. • **When mode B** It becomes the function as a R0MDC pin (output) RMII interface (channel 0) management data clock. It is a transfer clock of RMII serial management data.
GPIO12/M0MD/ R0MD	I/O	• **When mode D** Maskable activation factor input signals. This signal can be used as general-purpose I/O ports after activation. • **When mode A or C** It becomes the function as a M0MD pin (input/output) MII interface (channel 0) management data. It is a bidirectional MII serial management data signal. • **When mode B** It becomes the function as a R0MD pin (input/output) RMII interface (channel 0) management data. It is a bidirectional RMII serial management data signal.

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Signal	I/O	Function
GPIO4/M0RXD1/ R0RXD1	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0RXD1 pin (input) MII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. • **When mode B** It becomes the function as a R0RXD1 pin (input) RMII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. .
GPO38/M0RXD0/ R0RXD0	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0RXD0 pin (input) MII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. • **When mode B** It becomes the function as a R0RXD0 pin (input) RMII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. .
GPIO8/M0RXDV/ R0CRSDV	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0RXDV pin (input) MII interface (channel 0) receive data valid. It indicates that the receive data on M0RXD (3:0) is valid. If the port is not used, fix M0RXDV to the high or the low level. • **When mode B** It becomes the function as a R0CRSDV pin (input) RMII interface (channel 0) carrier sense / receive data valid. It shall be asserted by the PHY when the receive medium is non-idle.
GPIO13/ M0TXD1/ R0TXD1	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0TXD1 pin (output) MII interface (channel 0) transmit data. It outputs transmit data to the PHY device connected to the port. • **When mode B** It becomes the function as a R0TXD1 pin (output) RMII interface (channel 0) transmit data. It outputs transmit data to the PHY device connected to the port.
GPIO14/ M0TXD0/ R0TXD0	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0TXD0 pin (output) MII interface (channel 0) transmit data. It outputs transmit data to the PHY device connected to the port. • **When mode B** It becomes the function as a R0TXD0 pin (output) RMII interface (channel 0) transmit data. It outputs transmit data to the PHY device connected to the port.

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Signal	I/O	Function
GPO36/M0TXEN/ R0TXEN	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0TXEN pin (output) MII interface (channel 0) transmit enable. It indicates whether transmit data (M0TXD (3:0)) is valid for each port. • **When mode C** It becomes the function as a R0TXEN pin (output) RMII interface (channel 0) transmit enable. It indicates whether transmit data (R0TXD (3:0)) is valid for each port.
GPIO10/ M0RXER/R1MDC	I/O	• **When mode D** Maskable activation factor input signals. This signal can be used as general-purpose I/O ports after activation. • **When mode A or C** It becomes the function as a M0RXER pin (input) MII interface (channel 0) receive error. This is an input signal to detect an error that occurs in the PHY device connected to the port during reception. If the port is not used, fix M0RXER to the low level. • **When mode B** It becomes the function as a R1MDC pin (output) RMII interface (channel 1) management data clock. It is a transfer clock of RMII serial management data..
M0CRS/R1MD/ BIGENDIAN	I/O	The function differs depending on the operating status. • **During normal operation (output)** **When mode A or C** It becomes the function as a M0CRS pin (input) MII interface (channel 0) carrier sense. It inputs a carrier sense signal from the PHY device connected to the port. If the port is not used, fix M0CRS to the low level. . **When mode B** It becomes the function as a R1MD pin (input/output) RMII interface (channel 1) management data. It is a bidirectional RMII serial management data signal. • **During RTC reset (input)** BIGENDIAN: This signal selects big endian. When the RTCRST# signal changes from low to high, this signal is sampled. 1: Big endian 0: Little endian It doesn't guarantee the action regarding the setting other than the above.
GPO37/M0RXD3/ R0RXD1	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0RXD0 pin (input) MII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. • **When mode B** It becomes the function as a R0RXD0 pin (input) RMII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. .

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Signal	I/O	Function
SYSEN#/ M0RXD2/ R1RXD0	I/O	• **When mode D** It becomes the function as a SYSEN# pin (output) System data bus isolation buffer enable. This becomes “High” level during the cycle of either SDRAM or SyncFlash™ ROM, then becomes “Low” level during other cycle • **When mode A or C** It becomes the function as a M0RXD2 pin (input) MII interface (channel 0) receive data. It inputs receive data from the PHY device connected to the port. • **When mode B** It becomes the function as a R1RXD0 pin (input) RMII interface (channel 1) receive data. It inputs receive data from the PHY device connected to the port. .
GPIO7/ M0RXCLK/ R1CRSDV	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0RXCLK pin (input) MII interface (channel 0) receive clock. It inputs a clock given by the PHY device. When 100Mbps mode : 25MHz When 10Mbps mode : 2.5MHz • **When mode B** It becomes the function as a R1CRSDV pin (input) RMII interface (channel 1) carrier sense / receive data valid. It shall be asserted by the PHY when the receive medium is non-idle.
GPIO5/M0TXD3/ R1TXD1	I/O	• **When mode D** General-purpose I/O ports. • **When mode A or C** It becomes the function as a M0TXD3 pin (output) MII interface (channel 0) transmit data. It outputs transmit data to the PHY device connected to the port. • **When mode B** It becomes the function as a R1TXD1 pin (output) RMII interface (channel 1) transmit data. It outputs transmit data to the PHY device connected to the port.
DRQ1/M0TXD2/ R1TXD0	I/O	• **When mode D** It becomes the function as a DRQ1 pin (input) It works as the request signal of the DMA function. This pin is possible select whether DMA transfer between the IO space and RAM, or PCI and RAM by CONTROLREG (0x0F00004E) of DCU. • **When mode A or C** It becomes the function as a M0TXD2 pin (output) MII interface (channel 0) transmit data. It outputs transmit data to the PHY device connected to the port. • **When mode B** It becomes the function as a R1TXD0 pin (output) RMII interface (channel 1) transmit data. It outputs transmit data to the PHY device connected to the port.

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Signal	I/O	Function
DAK1/M0TXER/ R1TXEN	I/O	• **When mode D** It becomes the function as a DAK1 pin (output) It works as the acknowledge signal of the DMA function. This pin is possible select whether DMA transfer between the IO space and RAM, or PCI and RAM by CONTROLREG (0x0F00004E) of DCU. • **When mode A, B or D** It becomes the function as a M0TXER pin (output) MII interface (channel 0) transmit coding error. It indicates that an error has occurred in MAC during transmission. • **When mode C** It becomes the function as a R1TXEN pin (output) RMII interface (channel 1) transmit enable. It indicates whether transmit data (R1TXD (3:0)) is valid for each port.
GPIO11/M0COL	I/O	• **When mode B or D** Maskable activation factor input signals. This signal can be used as general-purpose I/O ports after activation. • **When mode A or C** It becomes the function as a M0COL pin (input) MII interface (channel 0) collision. It inputs a collision signal detected by the PHY device connected to the port. If the port is not used, fix M0COL to the low level. .

(14) Debug interface signals

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Signal	I/O	Function
JTCK	Input	This is the clock input for JTAG.
JTMS	Input	This is the JTAG mode setting input signal.
JTDI/RMODE#	Input	This is the RMODE#/JTDI alternate function pin. When JTRST# is active, it functions as RMODE#, and when JTRST# is inactive, it functions as JTDI. If a debugging tool is not connected externally, pull up to high level. • **RMODE#: Input** When JTRST# is active, this becomes the reset mode pin. The debug reset initial value is determined according to the level of this signal. Debug reset resets the processor with two kinds of resets: a debug cold reset and debug soft reset. These two resets function in the same way as a cold reset input and a soft reset input from the target system. 0: The debug reset is valid; the CPU core is reset. 1: The debug reset is invalid; the CPU core is not reset. • **JTDI: Input** When JTRST# is inactive this becomes the JTAG data input signal.
IRDOUT#/JTDO	Output	• **When N-Wire cannot be used** IRDOUT: This is the IrDA serial data output signal. • **When N-Wire can be used** JTDO: This is the JTAG data output signal.
JTRST#	Input	This is the JTAG reset signal.

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Signal	I/O	Function
BKTGIO#	I/O	• **BKTGIO#: In the input setting** When JTRST# is inactive and BKTGIO# is in the input setting, BKTGIO# becomes the event trigger/break request input pin. When the event trigger input is valid, if BKTGIO# is made low level, the normal mode user program is aborted, and the processor is forcibly changed to debug mode. If BKTGIO# becomes low level in debug mode, the break request is held pending until the processor returns to normal mode. 0: A break is requested and the processor is forcibly changed to debug mode. 1: The current status of the processor is maintained. • **BKTGIO#: In the output setting** When JTRST# is inactive and BKTGIO# is in the output setting, BKTGIO# becomes the event trigger/break output pin. While the processor is operating in normal mode, if an event is detected upon a match with either of the conditions of the hardware breakpoints (instruction address breakpoint or data access breakpoint), a low level (1 pulse) is output from BKTGIO# as an event trigger, and report of the event detection is sent to the external debugging tool. All the events detected after the last event trigger has been output are sent as one event trigger. If the processor mode is changed to debug mode, the low-level output continues, and none of the as unreported events are sent. 0: Detects a hardware breakpoint. The processor is in debug mode. 1: The processor is in normal mode.
SIN/JTAGEN	Input	The function differs depending on the operating status. • **During normal operation (output)** Clocked serial input signal • **During RTC reset (input)** JTAGEN: The use of N-wire, Boundary scan function and IRDOUT function are permitted. When the RTCRST# signal changes from low to high, this signal is sampled. 1: N-Wire and Boundary scan permit the use. However, the use prohibition of IRDOUT. 0: N-Wire and Boundary scan be the prohibition that uses it. However, the use permission of IRDOUT.

(15) Dedicated V_{DD} and GND signals

V_R4133 has the 1.5V power supply and 3.3V power supply systems. There are the power supply that is not possible the SHUTDOWN (VDDH/GNDH) and is impossible the SHUTDOWN (VDD/GND) at the Hibernate mode, regarding the power supply lines of the 1.5V system. However, please handle and observe all the 1.5V system power supply with VDDH/GNDH, regarding the way that who does not use the Hibernate mode.

Signal	Power Supply[Note]	Function
AVDD	1.5 V	Dedicated V_{DD} for the PLL analog unit
AGND	1.5 V	Dedicated GND for the PLL analog unit
VDD	1.5 V	Normal 1.5 V V_{DD} (It's possible to do the SHUTDOWN at Hibernate mode)
GND	1.5 V	GND for normal 1.5 V system
VDDH	1.5 V	Normal 1.5 V V_{DD} (Please be supplying the power even at Hibernate mode)
GNDH	1.5 V	GND for normal 1.5 V system
VDD33	3.3 V	Normal 3.3 V V_{DD}
GND33	3.3 V	GND for normal 3.3 V system

Note For the actual power supply voltage values, refer to **2. ELECTRICAL SPECIFICATIONS**.

Remark The V_R4133 has two power supplies, but there are no restrictions on the order of supply voltage application.

(16) Other signal

Signal	I/O	Function
M0CRS/R1MD/ BIGENDIAN	I/O	Refer to **(13) Ethernet controller interface signals**.
TESTMODE	input	This pin is used to the test of when that ships it. Therefore, please DON'T use it. As for the processing of the pin, please be directly associated to GND33.

1.3 Pin function for the each pin mode

Pin Name	Mode A (PCI + MII X 1)	Mode B (PCI+RMII X 2)	Mode C (MII X 2)	Mode D (non-MAC)
ADD01/ADD25	ADD(25:0)	ADD(25:0)	ADD(25:0)	ADD(25:0)
ADD02				
ADD03				
ADD04				
ADD05				
ADD06				
ADD07				
ADD08				
ADD09				
ADD10				
ADD11				
ADD12				
ADD13				
ADD14				
ADD15				
ADD16				
ADD17				
ADD18				
ADD19				
ADD20				
ADD21				
ADD22				
ADD23				
ADD24				
CAS	CAS	CAS	CAS	CAS
CKE0	CKE(1:0)	CKE(1:0)	CKE(1:0)	CKE(1:0)
CKE1				
CS0#	CS (1:0)#	CS (1:0)#	CS(1:0)#	CS (1:0)#
CS1#				
CS2#/ROMCS2#	CS2#/ROMCS2#	CS2#/ROMCS2#	CS2#/ROMCS2#	CS2#/ROMCS2#
CS3#/ROMCS3#	CS3#/ROMCS3#	CS3#/ROMCS3#	CS3#/ROMCS3#	CS3#/ROMCS3#
DATA00	DATA(15:0)	DATA(15:0)	DATA(15:0)	DATA(15:0)
DATA01				
DATA02				
DATA03				
DATA04				
DATA05				
DATA06				
DATA07				
DATA08				
DATA09				
DATA10				
DATA11				
DATA12				
DATA13				
DATA14				

DATA15				
DATA16/GPIO16	DATA(31:16)/GPIO(31:16)	DATA(31:16)/GPIO(31:16)	DATA(31:16)/GPIO(31:16)	DATA(31:16)/GPIO(31:16)
DATA17/GPIO17				
DATA18/GPIO18				
DATA19/GPIO19				
DATA20/GPIO20				
DATA21/GPIO21				
DATA22/GPIO22				
DATA23/GPIO23				
DATA24/GPIO24				
DATA25/GPIO25				
DATA26/GPIO26				
DATA27/GPIO27				
DATA28/GPIO28				
DATA29/GPIO29				
DATA30/GPIO30				
DATA31/GPIO31				
DQM0/LBE0/ADD0	DQM0/LBE0/ADD0	DQM0/LBE0/ADD0	DQM0/LBE0/ADD0	DQM0/LBE0/ADD0
DQM1/LBE1/UBE	DQM1/LBE1/UBE	DQM1/LBE1/UBE	DQM1/LBE1/UBE	DQM1/LBE1/UBE
DQM2/LBE2	DQM2/LBE2	DQM2/LBE2	DQM2/LBE2	DQM2/LBE2
DQM3/LBE3	DQM3/LBE3	DQM3/LBE3	DQM3/LBE3	DQM3/LBE3
GPIO06/SYSDIR	GPIO06/SYSDIR	GPIO06/SYSDIR	GPIO06/SYSDIR	GPIO06/SYSDIR
HLDAK#/DAK0	HLDAK#/DAK0	HLDAK#/DAK0	HLDAK#/DAK0	HLDAK#/DAK0
HLDRQ#/DRQ0	HLDRQ#/DRQ0	HLDRQ#/DRQ0	HLDRQ#/DRQ0	HLDRQ#/DRQ0
IOCS0#	IOCS(1:0) #	IOCS(1:0) #	IOCS(1:0) #	IOCS(1:0) #
IOCS1#				
IORDY	IORDY	IORDY	IORDY	IORDY
RAS	RAS	RAS	RAS	RAS
RD#	RD#	RD#	RD#	RD#
ROMCS0#	ROMCS(1:0) #	ROMCS(1:0) #	ROMCS(1:0) #	ROMCS(1:0) #
ROMCS1#				
SCLK	SCLK	SCLK	SCLK	SCLK
SWR#	SWR#	SWR#	SWR#	SWR#
WR#	WR#	WR#	WR#	WR#
BATTINH/BATTINT#	BATTINH/BATTINT#	BATTINH/BATTINT#	BATTINH/BATTINT#	BATTINH/BATTINT#
CLKX1	CLKX1	CLKX1	CLKX1	CLKX1
CLKX2	CLKX2	CLKX2	CLKX2	CLKX2
MPOWER	MPOWER	MPOWER	MPOWER	MPOWER
POWERON	POWERON	POWERON	POWERON	POWERON
RSTSW#	RSTSW#	RSTSW#	RSTSW#	RSTSW#
RTCRST#	RTCRST#	RTCRST#	RTCRST#	RTCRST#
RTCX1	RTCX1	RTCX1	RTCX1	RTCX1
RTCX2	RTCX2	RTCX2	RTCX2	RTCX2
SPOWER	SPOWER	SPOWER	SPOWER	SPOWER
TESTMODE	TESTMODE	TESTMODE	TESTMODE	TESTMODE
POWER	POWER	POWER	POWER	POWER
BKTGIO#	BKTGIO#	BKTGIO#	BKTGIO#	BKTGIO#
JTCK	JTCK	JTCK	JTCK	JTCK

JTDI/RMODE#	JTDI/RMODE#	JTDI/RMODE#	JTDI/RMODE#	JTDI/RMODE#
JTDO/IRDOUT#	JTDO/IRDOUT#	JTDO/IRDOUT#	JTDO/IRDOUT#	JTDO/IRDOUT#
JTMS	JTMS	JTMS	JTMS	JTMS
JTRST#	JTRST#	JTRST#	JTRST#	JTRST#
CTS#	CTS#	CTS#	CTS#	CTS#
DSR#	DSR#	DSR#	DSR#	DSR#
DTR#/CLKSEL0	DTR#	DTR#	DTR#	DTR#
RTS#/CLKSEL1	RTS#	RTS#	RTS#	RTS#
RXD	RXD	RXD	RXD	RXD
TXD/CLKSEL2	TXD	TXD	TXD	TXD
DCD#/GPI15	DCD#/GPI15	DCD#/GPI15	DCD#/GPI15	DCD#/GPI15
DCTS#/GPO35	DCTS#/GPO35	DCTS#/GPO35	DCTS#/GPO35	DCTS#/GPO35
DDIN/GPO34	DDIN/GPO34	DDIN/GPO34	DDIN/GPO34	DDIN/GPO34
DDOUT/GPO32/DBUS32	DDOUT/GPO32	DDOUT/GPO32	DDOUT/GPO32	DDOUT/GPO32
DRTS#/GPO33/PCIEN	DRTS#/GPO33	DRTS#/GPO33	DRTS#/GPO33	DRTS#/GPO33
GPIO00 GPIO01 GPIO02 GPIO03	GPIO(3:0)	GPIO(3:0)	GPIO(3:0)	GPIO(3:0)
IRDIN	IRDIN	IRDIN	IRDIN	IRDIN
LEDOUT#/RTCCLKSEL	LEDOUT#	LEDOUT#	LEDOUT#	LEDOUT#
SECLK	SECLK	SECLK	SECLK	SECLK
SIN/JTAGEN	SIN	SIN	SIN	SIN
SOUT	SOUT	SOUT	SOUT	SOUT
AD00/M1RXCLK	AD(31:00)	AD(31:00)	M1RXCLK	AD(31:00)
AD01/M1TXCLK			M1TXCLK	
AD02/M1COL			M1COL	
AD03/M1CRS			M1CRS	
AD04/M1MDC			M1MDC	
AD05/M1MD			M1MD	
AD06/M1RXD0			M1RXD0	
AD07/M1RXD1			M1RXD1	
AD08/M1RXD2			M1RXD2	
AD09/M1RXD3			M1RXD3	
AD10/M1RXER			M1RXER	
AD11/M1RXDV			M1RXDV	
AD12/M1TXD0			M1TXD0	
AD13/M1TXD1			M1TXD1	
AD14/M1TXD2			M1TXD2	
AD15/M1TXD3			M1TXD3	
AD16/M1TXEN			M1TXEN	
AD17/M1TXER			M1TXER	
AD18/GPO39			GPO39	
AD19/GPO40			GPO40	
AD20/GPO41			GPO41	
AD21/GPO42			GPO42	
AD22/GPO43			GPO43	
AD23/GPO44			GPO44	
AD24/GPO45			GPO45	

AD25/GPO46			GPO46	
AD26/GPO47			GPO47	
AD27			<Internal used>	
AD28			<Internal used>	
AD29			<Internal used>	
AD30			<Internal used>	
AD31			<Internal used>	
CBE0	CBE(3:0)	CBE(3:0)	<Internal used>	CBE(3:0)
CBE1			<Internal used>	
CBE2			<Internal used>	
CBE3			<Internal used>	
DEVSEL#	DEVSEL#	DEVSEL#	<Internal used>	DEVSEL#
FRAME#	FRAME#	FRAME#	<Internal used>	FRAME#
GNT0#	GNT(2:0)#	GNT(2:0)#	<Internal used>	GNT(2:0)#
GNT1#			<Internal used>	
GNT2#			<Internal used>	
IRDY#	IRDY#	IRDY#	<Internal used>	IRDY#
LOCK#	LOCK#	LOCK#	<Internal used>	LOCK#
PAR	PAR	PAR	<Internal used>	PAR
PCLK	PCLK	PCLK	<Internal used>	PCLK
PERR#	PERR#	PERR#	<Internal used>	PERR#
REQ0#	REQ(2:0)#	REQ(2:0)#	<Internal used>	REQ(2:0)#
REQ1#			<Internal used>	
REQ2#			<Internal used>	
STOP#	STOP#	STOP#	<Internal used>	STOP#
TRDY#	TRDY#	TRDY#	<Internal used>	TRDY#
SERR#	SERR#	SERR#	<Internal used>	SERR#
RST#	RST#	RST#	<Internal used>	RST#
CLKRUN	CLKRUN	CLKRUN	<Internal used>	CLKRUN
CLKOUT/M0TXCLK/REFCLK	M0TXCLK	REFCLK	M0TXCLK	CLKOUT
GPIO09/M0MDC/R0MDC	M0MDC	R0MDC	M0MDC	GPIO09
GPIO12/M0MD/R0MD	M0MD	R0MD	M0MD	GPIO12
GPIO04/M0RXD1/R0RXD1	M0RXD1	R0RXD1	M0RXD1	GPIO04
GPO38/M0RXD0/R0RXD0	M0RXD0	R0RXD0	M0RXD0	GPO38
GPIO08/M0RXDV/R0CRSDV	M0RXDV	R0CRSDV	M0RXDV	GPIO08
GPIO13/M0TXD1/R0TXD1	M0TXD1	R0TXD1	M0TXD1	GPIO13
GPIO14/M0TXD0/R0TXD0	M0TXD0	R0TXD0	M0TXD0	GPIO14
GPO36/M0TXEN/R0TXEN	M0TXEN	R0TXEN	M0TXEN	GPO36
GPIO10/M0RXER/R1MDC	M0RXER	R1MDC	M0RXER	GPIO10
M0CRS/R1MD/BIGENDIAN	M0CRS	R1MD	M0CRS	<Internal used>
GPO37/M0RXD3/R1RXD1	M0RXD3	R1RXD1	M0RXD3	GPO37
SYSEN#/M0RXD2/R1RXD0	M0RXD2	R1RXD0	M0RXD2	SYSEN#
GPIO07/M0RXCLK/R1CRSDV	M0RXCLK	R1CRSDV	M0RXCLK	GPIO07
GPIO05/M0TXD3/R1TXD1	M0TXD3	R1TXD1	M0TXD3	GPIO05
DRQ1/M0TXD2/R1TXD0	M0TXD2	R1TXD0	M0TXD2	DRQ1
DAK1/M0TXER/R1TXEN	M0TXER	R1TXEN	M0TXER	DAK1
GPIO11/M0COL	M0COL	GPIO11	M0COL	GPIO11

1.4 Pin Status in Specific States

(1/3)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
AD(31:0)	0	0	0	Hold	Usually action
ADD(24:1)	0	0	0	Hold	Hi-Z
BATTINH/BATTINT#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
BIGENDIAN	Hi-Z	0	0	0	0
BKTGIO#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
CAS	0	0	0	0	Hi-Z
CBE(3:0)	0	0	0	Hold	Usually action
CKE(1:0)	0	0	0	0	Hi-Z
CLKOUT	Hi-Z	Hi-Z	Hi-Z	Usually action	Usually action
CLKRUN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
CS(1:0)#	0	0	1	1	Hi-Z
CS(3:2)#	Hi-Z	Hi-Z	1	1	1
CTS#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DAK(1:0)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
DATA(31:0)	0	0	0	Hold	Hi-Z
DCD#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DCTS#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DDIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DDOUT	Hi-Z	1	1	Hold	Hold
DEVSEL#	Hi-Z	Hi-Z	Hi-Z	Hold	Usually action
DQM(3:0)	0	0	1	Hold	Hi-Z
DRQ(1:0)	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DRTS#	Hi-Z	1	1	Hold	Hold
DSR#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
DTR#	Hi-Z	1	1	Hold	Hold
FRAME#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
GNT(2:0)#	Hi-Z	Hi-Z	Hi-Z	Hold	Usually action
GPIO(3:0)	Hi-Z	Hold	Hold	Hold	Hi-Z
GPIO(5:4)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
GPIO6	0	0	0	Hold	Hi-Z
GPIO(8:7)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
GPIO(12:9)	Hi-Z	Hold	Hold	Hold	Hi-Z
GPIO(14:13)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
GPI15	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

(2/3)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
GPIO(31:16)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
GPO(35:32)	Hi-Z	Hold	Hold	Hold	Hold
GPO(47:36)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
HLDAK#	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
HLDRQ#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IOCS(1:0)#	Hi-Z	Hi-Z	1	Hold	1
IORDY	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRDIN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
IRDOUT#	Hi-Z	Hi-Z	0	0	0
IRDY#	Hi-Z	Hi-Z	Hi-Z	Hold	Usually action
JTCK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTDI	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTDO	Hi-Z	Hi-Z	0	0	0
JTMS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
JTRST#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
LEDOUT#	Hi-Z	Hold	Hold	Hold	Hold
LOCK#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
MPOWER	0	0	1	1	1
PAR	0	0	1	Hold	Usually action
PCLK	0	0	0	Hold	Usually action
PERR#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
POWER	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
POWERON	0	0	0	0	0
RAS	0	0	0	0	Hi-Z
RD#	Hi-Z	Hi-Z	1	Hold	Hi-Z
REQ(2:0)#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
RMODE#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
ROMCS(1:0)#	Hi-Z	Hi-Z	1	1	1
ROMCS(3:2)#	Hi-Z	Hi-Z	1	1	1
RST#	0	0	0	Hold	Usually action
RSTSW#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
RTCRST#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
RTS#	0	0	0	0	0
RxD	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SCLK	0	0	Hold	0	Hi-Z

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

(3/3)

Pin Name	When Reset by RTC	In Hibernate Mode or During HALTimer Shutdown	When Reset by RSTSW	In Suspend Mode	During Bus Hold
SECLK	0	0	1	Hold	Hold
SERR#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
SIN/JTAGEN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
SOUT	0	0	0	0	0
SPOWER	0	**Note.1**	1	1	1
STOP#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
SWR#	0	0	0	Hold	Hi-Z
SYSDIR	0	0	0	Hold	Hold
SYSEN#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
TRDY#	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Usually action
TxD	Hi-Z	1	1	1	1
WR#	Hi-Z	Hi-Z	1	Hold	Hi-Z
TESTMODE	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1COL	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1CRS	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1MD	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1MDC	Hi-Z	Hi-Z	0	0	0
M0/1RXCLK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1RXD(3:0)	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1RXDV	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1RXER	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1TXCLK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M0/1TXD(3:0)	Hi-Z	Hi-Z	0	Hold	Hold
M0/1TXEN	Hi-Z	Hi-Z	0	Hold	Hold
M0/1TXER	Hi-Z	Hi-Z	0	Hold	Hold
REFCLK	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
R0/1MDC	Hi-Z	Hi-Z	0	0	0
R0/1MD	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
R0/1RXD(1:0)	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
R0/1CRSDV	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
R0/1TXD(1:0)	Hi-Z	Hi-Z	Hi-Z	Hold	Hold
R0/1TXEN	Hi-Z	Hi-Z	Hi-Z	Hold	Hold

Notes 1. When SDRAMACT bit of PMUCNTREG (0x0F0000C2) is 1 this pin's condition becomes 1. When the SDRAMACT bit is 0 it becomes 0.

Remark 0: Low level, 1: High level, Hi-Z: High impedance,
Hold: Maintains the status of the preceding Fullspeed mode

1.5 Pin Handling and I/O Circuit Types

(1/3)

Pin Name	Pin Handling	Recommended Connection of Unused Pins
AD(31:0)	–	Leave open
ADD(24:1)	–	–
BATTINH/BATTINT#	Connect to VDD33 direct or via a resistor	Connect to VDD33
BIGENDIAN	Connect to VDD33 or GND via a resistor	–
BKTGIO#	Connect to VDD33 via a resistor	Leave open
CAS	–	Leave open
CBE(3:0)	–	Leave open
CKE(1:0)	–	Leave open
CLKOUT	–	Leave open
CLKRUN	Connect to VDD33 via a resistor	Connect to VDD33 via a resistor
CS(1:0)#	–	Leave open
CS2#/ROMCS2#	–	Leave open
CS3#/ROMCS3#	–	Leave open
CTS#	Connect to VDD33 via a resistor	Connect to VDD33 direct or via a resistor
DATA(15:0)	–	–
DATA(31:16)/GPIO(31:16)	–	Connect to VDD33 or GND via a resistor
DCD#/GPI15	Connect to VDD33 via a resistor	Connect to VDD33 via a resistor
DCTS#/GPO35	Connect to VDD33 or GND via a resistor	Connect to VDD33 or GND via a resistor
DDIN/GPO34	Connect to VDD33 or GND via a resistor	Connect to VDD33 or GND via a resistor
DDOUT/GPO32/DBUS32	Connect to VDD33 or GND via a resistor	–
DEVSEL#	–	Leave open
DQM(3:0)	–	–
DRTS#/GPO33/PCIEN	Connect to VDD33 or GND via a resistor	Connect to VDD33 or GND via a resistor
DSR#	Connect to VDD33 or GND via a resistor	Connect to VDD33 OR GND
DTR#/CLKSEL0	Connect to VDD33 or GND via a resistor	–
FRAME#	–	Leave open
GNT(2:0)#	–	Leave open
GPIO(2:0), GPIO(5:4) , GPIO(14:7) , GPIO(31:16)	Connect to VDD33 or GND via a resistor	Connect to VDD33 or GND via a resistor
GPIO3	Connect to VDD33 via a resistor	Connect to VDD33 or GND via a resistor
GPIO6/SYSDIR	Connect to VDD33 or GND via a resistor	Leave open
GPI15	Connect to VDD33 via a resistor	Connect to VDD33 via a resistor
GPO(33:32)	Connect to VDD33 or GND via a resistor	–

Remarks 1. External handling is not required for the pins with no special directions in the Pin Handling column (–).

2. The pins with no special directions in the Recommended Connection of Unused Pins column are the pins that are always used.

(2/3)

Pin Name	Pin Handling	Recommended Connection of Unused Pins
GPO(35:34)	Connect to VDD33 or GND via a resistor	Leave open
GPO(47:36)	Connect to VDD33 or GND via a resistor	Leave open
HLDAK# /DAK0	–	Leave open
HLDRQ#/DRQ0	–	Leave open
IOCS(1:0)#	–	Leave open
IORDY	Connect to VDD33 or GND via a resistor	Connect to VDD33
IRDIN	Connect to VDD33 or GND via a resistor	Connect to VDD33 OR GND
IRDY#	Connect to VDD33 via a resistor	Leave open
JTCK	Connect to VDD33 or GND via a resistor	Connect to VDD33 OR GND
JTDI/RMODE#	Connect to VDD33 via a resistor	Leave open
JTDO/IRDOUT#	Connect to VDD33 via a resistor	Leave open
JTMS	Connect to VDD33 via a resistor	Leave open
JTRST#	Connect to GND via a resistor	Connect to GND via a resistor
LEDOUT#/RTCCLKSEL	Connect to VDD33 or GND via a resistor	–
LOCK#	Connect to VDD33 via a resistor	Leave open
MPOWER	–	Leave open
PAR	–	Leave open
PCLK	–	Leave open
PERR#	Connect to VDD33 via a resistor	Leave open
POWER	Connect to VDD33	Leave open
POWERON	–	Leave open
RAS	–	–
RD#	–	–
REQ(2:0)#	Connect to VDD33 via a resistor	Leave open
ROMCS(1:0)#	–	–
RST#	–	Leave open
RSTSW#	Connect to VDD33 via a resistor	–
RTCRST#	Connect to VDD33 via a resistor	–
RTS#/CLKSEL1	Connect to VDD33 or GND via a resistor	–
RxD	Connect to VDD33 or GND via a resistor	Connect to VDD33 or GND via a resistor
SCLK	–	–
SECLK	–	Leave open
SERR#	Connect to VDD33 via a resistor	Leave open
SIN/JTAGEN	Connect to VDD33 or GND via a resistor	–
SOUT	–	Leave open
SPOWER	–	Leave open
STOP#	Connect to VDD33 via a resistor	Leave open
SWR#	–	Leave open

Remarks 1. External handling is not required for the pins with no special directions in the Pin Handling column (–).

2. The pins with no special directions in the Recommended Connection of Unused Pins column are the pins that are always used.

(3/3)

Pin Name	Pin Handling	Recommended Connection of Unused Pins
SYSEN#	–	Leave open
TRDY#	Connect to VDD33 via a resistor	Leave open
TxD/CLKSEL2	Connect to VDD33 or GND via a resistor	–
WR#	–	Leave open
M0/1COL	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1CRS	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1MD	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1MDC	–	Leave open
M0/1RXCLK	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1RXD(3:0)	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1RXDV	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1RXER	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1TXCLK	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
M0/1TXD(3:0)	–	Leave open
M0/1TXEN	–	Leave open
M0/1TXER	–	Leave open
REFCLK	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
R0/1MDC	–	Leave open
R0/1MD	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
R0/1RXD(1:0)	Connect to GND via a resistor	Leave open
R0/1CRSDV	Connect to GND via a resistor	Connect to VDD33 or GND via a resistor
R0/1TXD(1:0)	–	Leave open
R0/1TXEN	–	Leave open
TESTMODE	Connect to GND	Connect to GND

Remarks 1. External handling is not required for the pins with no special directions in the Pin Handling column (–).

2. The pins with no special directions in the Recommended Connection of Unused Pins column are the pins that are always used.

2. ELECTRICAL SPECIFICATIONS

This electric characteristic specification may become a change because it is during product development in a present.

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	VDD1	Applies to AVDD, VDD, and VDDH pins	−0.5 to +1.8	V
	VDD3	Applies to VDD33 pins	−0.5 to +4.6	V
Input voltage	VI	It makes 4.6V upper limit.	−0.5 to VDD3 + 0.5	V
Storage temperature	Tstg		−65 to +125	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	VDD1	Applies to AVDD, VDD, and VDDH pins	1.35	1.65	V
	VDD3	Applies to VDD33 pins	3.0	3.6	V
Ambient temperature	TA		−40	+85	°C

Capacitance (TA = 25°C, VDD = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	CI	fC = 1 MHz		10	pF
I/O capacitance	CIO	Unmeasured pins returned to 0 V.		10	pF

DC Characteristics (T_A = –40 to +85°C, V_{DD1} = 1.35 to 1.65 V, V_{DD3} = 3.0 to 3.6 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	IOH = –2 mA	0.8VDD3			V
Output voltage, low	VOL1	IOL = 2 mA			0.4	V
Clock input voltage, high[Note 1]	VIH1		0.8VDD3		VDD3 + 0.3	V
Clock input voltage, low[Note 1]	VIL1		–0.3		0.3VDD3	V
Input voltage, high[Note 2]	VIH2		2.0		VDD3 + 0.3	V
Input voltage, low[Note 2]	VIL2		–0.3		0.3VDD3	V
Input voltage, high[Note 3]	VIH3		0.85VDD3		VDD3 + 0.3	V
Input voltage, low[Note 3]	VIL3		–0.3		0.6	V
Hysteresis voltage[Notes 3, 4]	VH			0.17VDD3		V
Input leakage current	ILI	VDD3 = 3.6 V, VI = VDD3, 0 V			±5	μA
Output leakage current	ILO	VDD3 = 3.6 V, VI = VDD3, 0 V			±5	μA

Notes **1.** Applies to CLKX1, RTCX1, JTCK pin.

2. Except RTCX1, CLKX1, BATTINH/BATTINT#, JTCK, JTRST#, POWER, RSTSW#, TESTMODE, RTCRST# and GPIO(3:0) pins.

3. Applies to BATTINH/BATTINT#, JTCK, JTRST#, POWER, RSTSW#, RTCRST# and GPIO(3:0) pins.

4. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low.

(2/2)

Parameter	Symbol	Condition	MIN.	TYP.[Note 1]	MAX.	Unit
Supply current	IDD1[Note 2]	In Fullspeed mode		250	500	mA
		In Standby mode		T.B.D.	T.B.D.	mA
		In Suspend mode		T.B.D.	T.B.D.	mA
		In Exsuspend mode		T.B.D.	T.B.D.	mA
		In Hibernate mode, VDD1 = 0.0 V, when LED unit is off.		T.B.D.	T.B.D.	μA
	IDD3[Note 3]	In Fullspeed mode		30	60	mA
		In Standby mode		T.B.D.	T.B.D.	mA
		In Suspend mode		T.B.D.	T.B.D.	mA
		In Exsuspend mode		T.B.D.	T.B.D.	mA
		In Hibernate mode, when LED unit is off.		T.B.D.	T.B.D.	μA

Notes **1.** Unless otherwise specified, these are reference values at TA = 25°C, VDD1 = 1.5 V, VDD3 = 3.3 V.

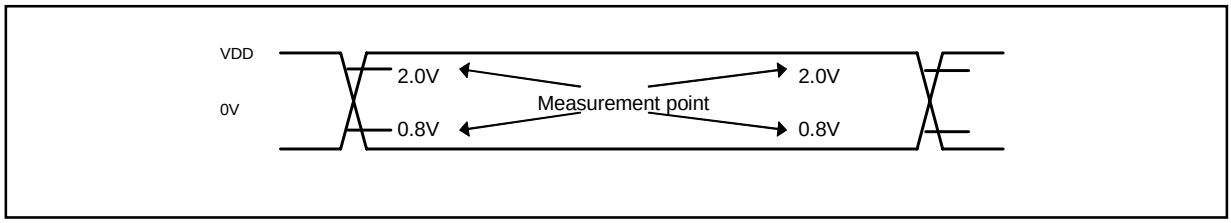
2. Total current flowing to the AVDD, VDD and VDDH pins.

3. Total current flowing to the VDD33 pins.

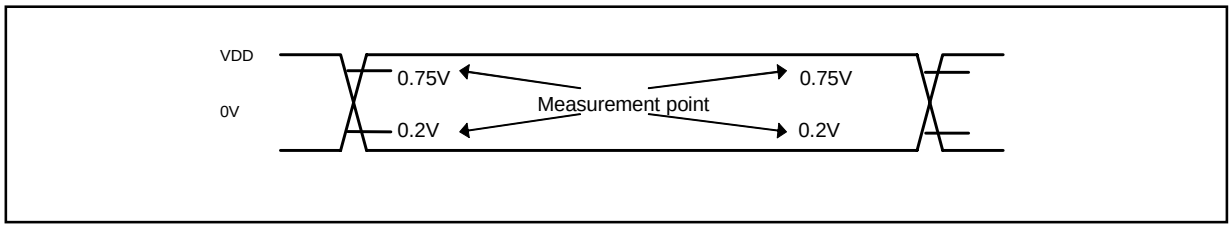
AC Characteristics (T_A = –40 to +85°C)

AC test input waveform

(a) CTS＃, DCD＃/GPI15, DSR＃, HLDRQ＃/DRQ0, IORDY, IRDIN, JTDI/RMODE＃, JTMS, REQ0＃, REQ1＃, REQ2＃, RXD, SIN/JTAGEN, AD0/M1RXCLK, AD1/M1TXCLK, AD2/M1COL, AD3/M1CRS, AD4/M1MDC, AD5/M1MD, AD6/M1RXD0, AD7/M1RXD1, AD8/M1RXD2, AD9/M1RXD3, AD10/M1RXER, AD11/M1RXDV, AD12/M1TXD0, AD13/M1TXD1, AD14/M1TXD2, AD15/M1TXD3, AD16/M1TXEN, AD17/M1TXER, AD[26..18]/GPO(47:39), AD(31:27), BKTGIO＃, CBE(3:0), CLKOUT/M0TXCLK/REFCLK, CLKRUN, DATA(15:0), DATA(31:16)/GPIO(31:16), DCTS＃/GPO35, DDIN/GPO34, DDOUT/GPO32/DBUS32, DEVSEL＃, DRQ1/M0TXD2/R1TXD0, DRTS＃/GPO33/PCIEN, DTR＃/CLKSEL0, FRAME＃, GPIO04/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV, GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, GPO37/M0RXD3/R1RXD1, GPO38/M0RXD0/R0RXD0, IRDY＃, LEDOUT＃/RTCCLKSEL, LOCK＃, M0CRS/R1MD/BIGENDIAN, PAR, PERR＃, RTS＃/CLKSEL1, SERR＃, STOP＃, SYSEN＃/M0RXD2/R1RXD0, TRDY＃, TXD/CLKSEL2

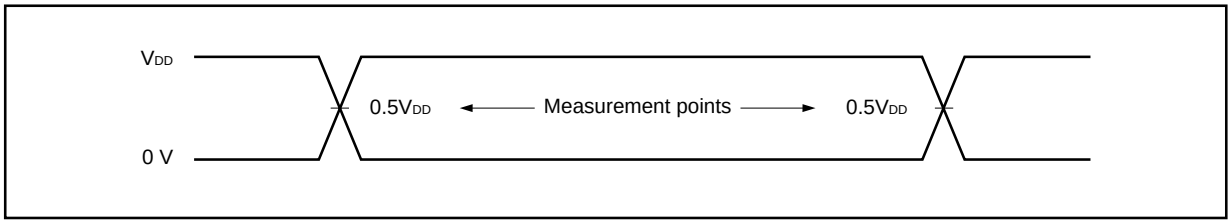


(b) BATTINH/BATTINT＃, JTCK, JTRST＃, POWER, RSTSW＃, RTCRST＃, GPIO(3:0)



AC test output measurement points

AD0/M1RXCLK , AD1/M1TXCLK , AD2/M1COL , AD3/M1CRS , AD4/M1MDC , AD5/M1MD , AD6/M1RXD0 , AD7/M1RXD1 , AD8/M1RXD2 , AD9/M1RXD3 , AD10/M1RXER , AD11/M1RXDV , AD12/M1TXD0 , AD13/M1TXD1 , AD14/M1TXD2 , AD15/M1TXD3 , AD16/M1TXEN , AD17/M1TXER , AD(26:18)/GPO(47:39) , AD(31:27) , BKTGIO＃ , CBE(3:0) , CLKOUT/M0TXCLK/REFCLK , CLKRUN , DATA(15:0) , DATA(31:16)/GPIO(31:16) , DCTS＃/GPO35 , DDIN/GPO34 , DDOUT/GPO32/DBUS32 , DEVSEL＃ , DRQ1/M0TXD2/R1TXD0 , DRTS＃/GPO33/PCIEN , DTR＃/CLKSEL0 , FRAME＃ , GPIO(3:0) , GPIO4/M0RXD1/R0RXD1 , GPIO5/M0TXD3/R1TXD1 , GPIO6/SYSDIR , GPIO07/M0RXCLK/R1CRSDV , GPIO8/M0RXDV/R0CRSDV , GPIO9/M0MDC/R0MDC , GPIO10/M0RXER/R1MDC , GPIO11/M0COL , GPIO12/M0MD/R0MD , GPIO13/M0TXD1/R0TXD1 , GPIO14/M0TXD0/R0TXD0 , GPO37/M0RXD3/R1RXD1 , GPO38/M0RXD0/R0RXD0 , IRDY＃ , LEDOUT＃/RTCCLKSEL , LOCK＃ , M0CRS/R1MD/BIGENDIAN , PAR , PERR＃ , RTS＃/CLKSEL1 , SERR＃ , STOP＃ , SYSEN＃/M0RXD2/R1RXD0 , TRDY＃ , TXD/CLKSEL2 , ADD1/ADD25 , ADD(24:2) , CAS , CKE(1:0) , CS(1:0)＃ , CS(3:2)＃/ROMCS(3:2)＃ , DAK1/M0TXER/R1TXEN , DQM0/LBE0/ADD0 , DQM1/LBE1/UBE , DQM2/LBE2 , DQM3/LBE3 , GNT[2:0]＃ , GPO36/M0TXEN/R0TXEN , HLDAK＃/DAK0 , IOCS(1:0)＃ , JTDO/IRDOUT＃ , MPOWER , PCLK , POWERON , RAS , RD＃ , ROMCS(1:0)＃ , RST＃ , SCLK , SECLK , SOUT , SPOWER , SWR＃ , WR＃



(1) Clock parameters

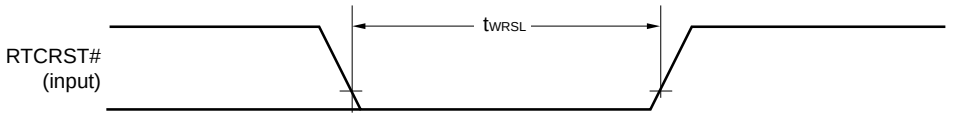
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU core operating frequency	fPCYC	CLKSEL(2:0) = 111 Note 1		RFU		MHz
		CLKSEL(2:0) = 110 Note 1		RFU		MHz
		CLKSEL(2:0) = 101 Note 1		RFU		MHz
		CLKSEL(2:0) = 100		265.9		MHz
		CLKSEL(2:0) = 011		199.1		MHz
		CLKSEL(2:0) = 010		165.9		MHz
		CLKSEL(2:0) = 001		149.0		MHz
		CLKSEL(2:0) = 000		133.0		MHz

Notes 1. Do not set CLKSEL(2:0) = 111, 110, 101.

Remark CLKSEL(2:0): Value set to the TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins after reset

(2) Reset parameters

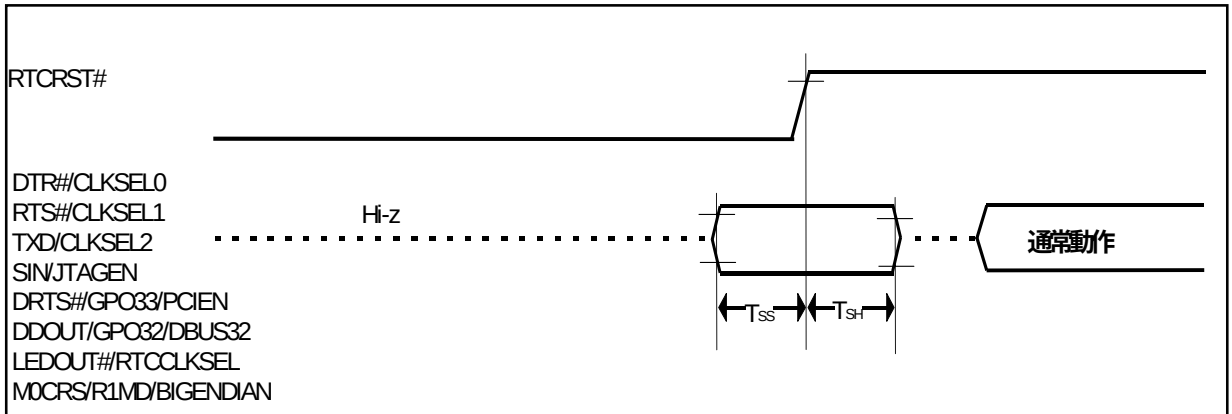
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	tWRSL	Applies to RTCRST# pin	305		μs



Remark For the RTCRST# characteristics at power application, refer to **VR4133 Hardware User's Manual**.

(3) Start-up Initialization parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Set-up time (from RTCRST# ↑)	tSS		91.6		μs
Hold time (from RTCRST# ↑)	tOD		-10		μs



Remark Set the input data level by using a pull-up or pull-down resistor with high resistance.

(4) GPIO interface parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width[Note 1]	t_{INP1}	**Note 2**	326 × N		ns
GPIO input rise time	t_{GPINR1}	**Note 3**		200	ns
	t_{GPINR2}	**Note 4**		10	ns
GPIO input fall time	t_{GPINF1}	**Note 3**		200	ns
	t_{GPINF2}	**Note 4**		10	ns
Output level width	t_{OUTP}	**Note 5**	30		ns

Notes **1.** The N value is set using the IDIV(1:0) bits of the PMUINTRCLKDIVREG register.

IDIV(1:0)	N
11	RFU
10	4
01	8
00	2

2. Applies to the GPIO (3:0), GPIO4/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV , GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, DCD#/GPI15 and DATA(31:16)/GPIO(31:16) pins.

3. Applies to the GPIO (3:0) pins.

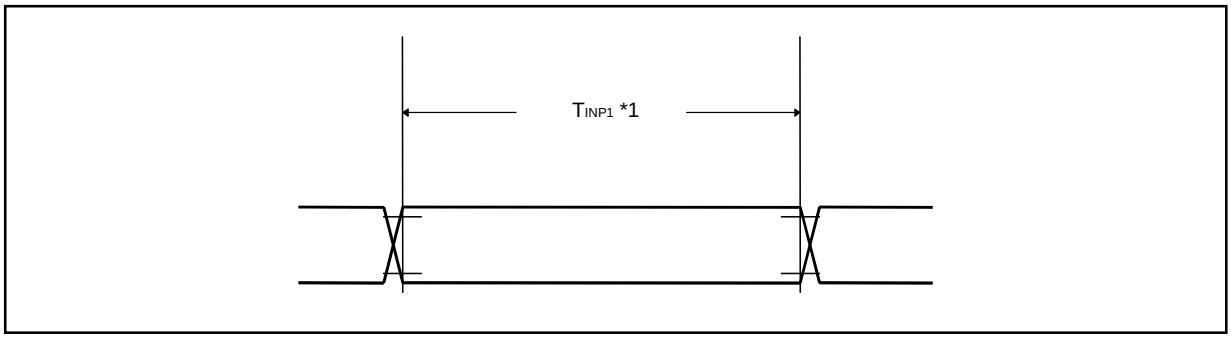
4. Applies to the GPIO4/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV, GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, DCD#/GPI15 and DATA(31:16)/GPIO(31:16) pins.

5. Applies to the GPIO(3:0), GPIO4/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV, GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, DATA(31:16)/GPIO(31:16), DDOUT/GPO32/DBUS32, DRTS＃/GPO33/PCIEN, DDIN/GPO34, DCTS＃/GPO35, GPO36/M0TXEN/R0TXEN, GPO37/M0RXD3/R1RXD1, GPO38/M0RXD0/R0RXD0 and AD(26:18)/GPO(47:39) pins.

Caution These parameters apply when the GPIO4/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV, GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, DCD#/GPI15 , DATA(31:16)/GPIO(31:16) , DDOUT/GPO32/DBUS32, DRTS＃/GPO33/PCIEN, DDIN/GPO34, DCTS＃/GPO35, GPO36/M0TXEN/R0TXEN, GPO37/M0RXD3/R1RXD1 , GPO38/M0RXD0/R0RXD0 , AD(26:18)/GPO(47:39) pin is used as a GPIO signal.

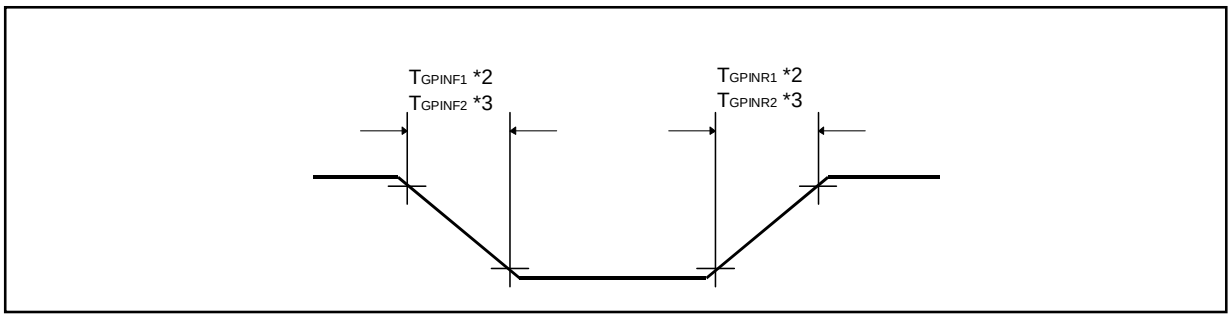
(4) GPIO interface parameters (2/2)

(a) Input level width



note 1. Applies to the GPIO (3:0), GPIO4/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV, GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, DCD#/GPI15 and DATA(31:16)/GPIO(31:16) pins.

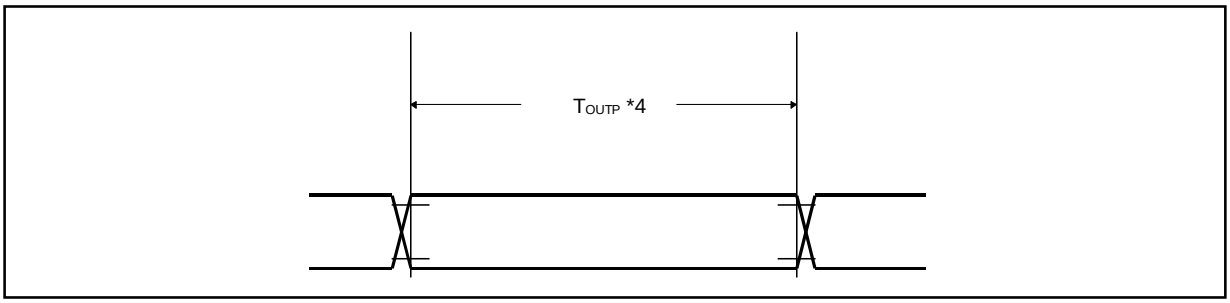
(b) GPIO input rise/fall time



Note 2. Applies to the GPIO (3:0) pins for T_{GPINF1} and T_{GPINR1}.

Note 3. Applies to the GPIO4/M0RXD1/R0RXD1, GPIO5/M0TXD3/R1TXD1, GPIO6/SYSDIR, GPIO7/M0RXCLK/R1CRSDV, GPIO8/M0RXDV/R0CRSDV, GPIO9/M0MDC/R0MDC, GPIO10/M0RXER/R1MDC, GPIO11/M0COL, GPIO12/M0MD/R0MD, GPIO13/M0TXD1/R0TXD1, GPIO14/M0TXD0/R0TXD0, DCD#/GPI15 and DATA(31:16)/GPIO(31:16) pins for T_{GPINF2} and T_{GPINR2}.

(c) Output level width



Note 4. Applies to the GPIO(3:0) , GPIO4/M0RXD1/R0RXD1 , GPIO5/M0TXD3/R1TXD1 , GPIO6/SYSDIR ,GPIO7/M0RXCLK/R1CRSDV , GPIO8/M0RXDV/R0CRSDV , GPIO9/M0MDC/R0MDC , GPIO10/M0RXER/R1MDC , GPIO11/M0COL , GPIO12/M0MD/R0MD , GPIO13/M0TXD1/R0TXD1 , GPIO14/M0TXD0/R0TXD0 , DATA(31:16)/GPIO(31:16) , DDOUT/GPO32/DBUS32 , DRTS＃/GPO33/PCIEN , DDIN/GPO34 , DCTS＃/GPO35 , GPO36/M0TXEN/R0TXEN , GPO37/M0RXD3/R1RXD1 , GPO38/M0RXD0/R0RXD0 and AD(26:18)/GPO(47:39) pins.

(5) Normal ROM parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note.1	tACC		T*G – 9.7		ns
Data access time (from ROMCS(3:0)# ↓) Note.1	t_{CE}		T*G – 9.7		ns
Data access time (from RD# ↓) Note.1	t_{OE}		T*(G–1) –9.7		ns
Data input setup time	t_{DS}		2.8		ns
Data input hold time	t_{DH}		0.7		ns
Active delay time of SYSEN# Note.2	t_{ED}		-（0.5T+5.0）	5.0	ns
Active delay time of SYSDIR# Note.3	t_{DAD}		-5.0	5.0	ns
Inactive delay time of SYSDIR# Note.3	t_{DID}		T-5.0	T+5.0	ns

Note.1 The value of G is set by using the rom2_wait (3:0) bits of the ROMSPEEDREG register. The value of T is set by using the CLKSEL (2:0) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register.

Note.2 Applies to SYSEN#/M0RXD2/R1RXD0 pin.

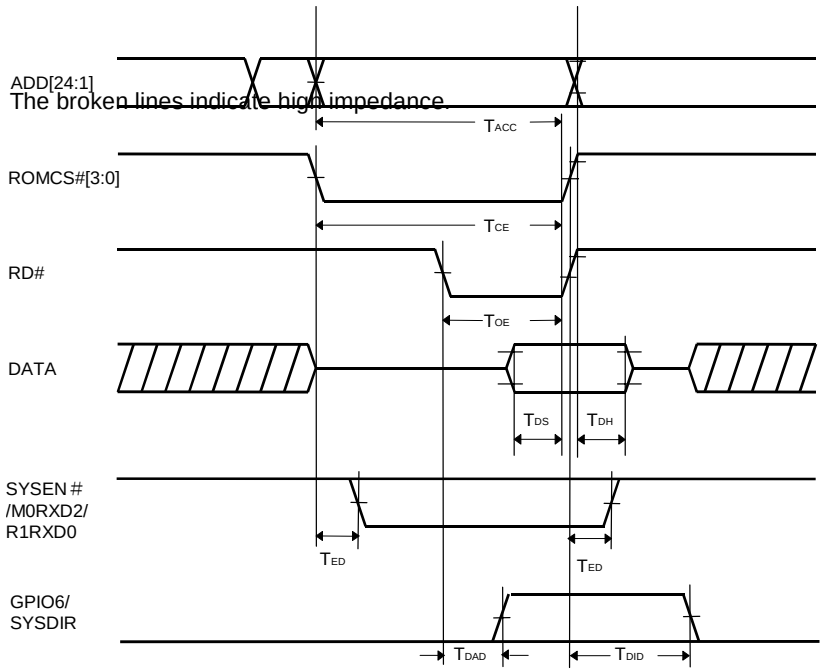
Note.3 Applies to GPIO6/SYSDIR pin.

rom2_wait	G	rom2_wait	G	rom2_wait	G	rom2_wait	G
11111	34	01111	26	01111	18	00111	10
11110	33	01110	25	01110	17	00110	9
11101	32	01101	24	01101	16	00101	8
11100	31	01100	23	01100	15	00100	7
11011	30	01011	22	01011	14	00011	6
11010	29	01010	21	01010	13	00010	5
11001	28	01001	20	01001	12	00001	4
11000	27	01000	19	01000	11	00000	3

VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
101	16.7	RFU	RFU	RFU	RFU	RFU	RFU	RFU
100	15.0	RFU	7.5	11.2	15.0	18.8	22.5	RFU
011	15.0	RFU	10.0	15.0	20.0	25.1	RFU	RFU
010	18.0	RFU	12.0	18.0	24.1	RFU	RFU	RFU
001	20.1	RFU	13.4	20.1	26.8	RFU	RFU	RFU
000	15.0	RFU	15.0	22.5	RFU	RFU	RFU	RFU

Remark As for the value of T, please consult the value of the above table.

(5) Normal ROM parameters (2/2)



Remark The broken lines indicate high impedance.

(6) Page ROM parameters (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note.1]	t_{ACC1}		$T_*G - 9.7$		ns
	t_{ACC2}		$T_*H - 8$		ns
Data access time (from ROMCS(3:0)# ↓)[Note.1,2]	t_{CE}		$T_*G - 9.7$		ns
Data access time (from RD# ↓)[Note.1]	t_{OE}		$T_*(G - 1) - 9.7$		ns
Data input setup time	t_{DS}		2.8		ns
Data input hold time	t_{DH}		0.7		ns
Active delay time of SYSEN#[Note.3]	t_{ED}		-（0.5T+5.0）	5.0	ns
Active delay time of SYSDIR#[Note.4]	t_{DAD}		-5.0	5.0	ns
Inactive delay time of SYSDIR#[Note.4]	t_{DID}		T-5.0	T+5.0	ns

Note.1 The value of G is set by using the rom2_wait (3:0) bits of the ROMSPEEDREG register.
The value of H is set by using the rom4_wait (1:0) bits of the ROMSPEEDREG register.
The value of T is set by using the CLKSEL (2:0) signals (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins) and the VTDIV (2:0) bits of the PMUTCLKDIVREG register.

Note.2 Applies to ADD (3:2) and ADD1/ADD25 pins.

Note.3 Applies to SYSEN#/M0RXD2/R1RXD0 pin.

Note.4 Applies to GPIO6/SYSDIR pin.

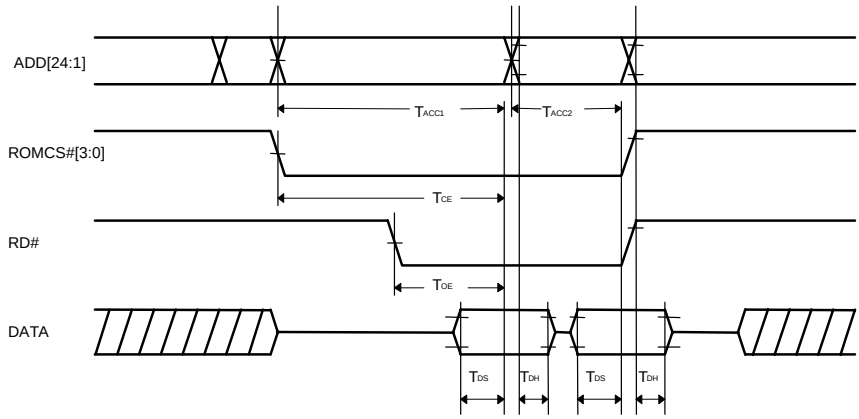
rom2_wait	G	rom2_wait	G	rom2_wait	G	rom2_wait	G
11111	34	01111	26	01111	18	00111	10
11110	33	01110	25	01110	17	00110	9
11101	32	01101	24	01101	16	00101	8
11100	31	01100	23	01100	15	00100	7
11011	30	01011	22	01011	14	00011	6
11010	29	01010	21	01010	13	00010	5
11001	28	01001	20	01001	12	00001	4
11000	27	01000	19	01000	11	00000	3

rom4_wait[1:0]	H
111	9
110	8
101	7
100	6
011	5
010	4
001	3
000	2

VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
101	16.7	RFU	RFU	RFU	RFU	RFU	RFU	RFU
100	15.0	RFU	7.5	11.2	15.0	18.8	22.5	RFU
011	15.0	RFU	10.0	15.0	20.0	25.1	RFU	RFU
010	18.0	RFU	12.0	18.0	24.1	RFU	RFU	RFU
001	20.1	RFU	13.4	20.1	26.8	RFU	RFU	RFU
000	15.0	RFU	15.0	22.5	RFU	RFU	RFU	RFU

Remark As for the value of T, please consult the value of the above table.

(6) Page ROM parameters (2/2)



Remark The broken lines indicate high impedance.

(7) Flash memory mode parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Setup time of ADD (24:1) until ROMCS # (3:0) become 0	T_{AVEL}		0		ns
Setup time of ROMCS # (3:0) until CMD becomes 0	T_{ELCL}		T * I-9.7		ns
CMD low-level width	T_{CLCH}		T * J-9.7		ns
ROMCS # (3:0) hold time (from CMD ↑)	T_{CHEH}		T * K-9.7		ns
ADD (24:1) hold time (from CMD ↑)	T_{CHAX}		T * K-9.7		ns
DATA hold time (from CMD ↑)	T_{CHDX}		T * K-9.7		ns
Setup time of write data until CMD becomes 0	T_{DVCL}		0		ns
Data output setup time (to WR# ↑)	T_{DS}		2.8		ns
Data output hold time (from WR# ↑)	T_{DH}		0.7		ns

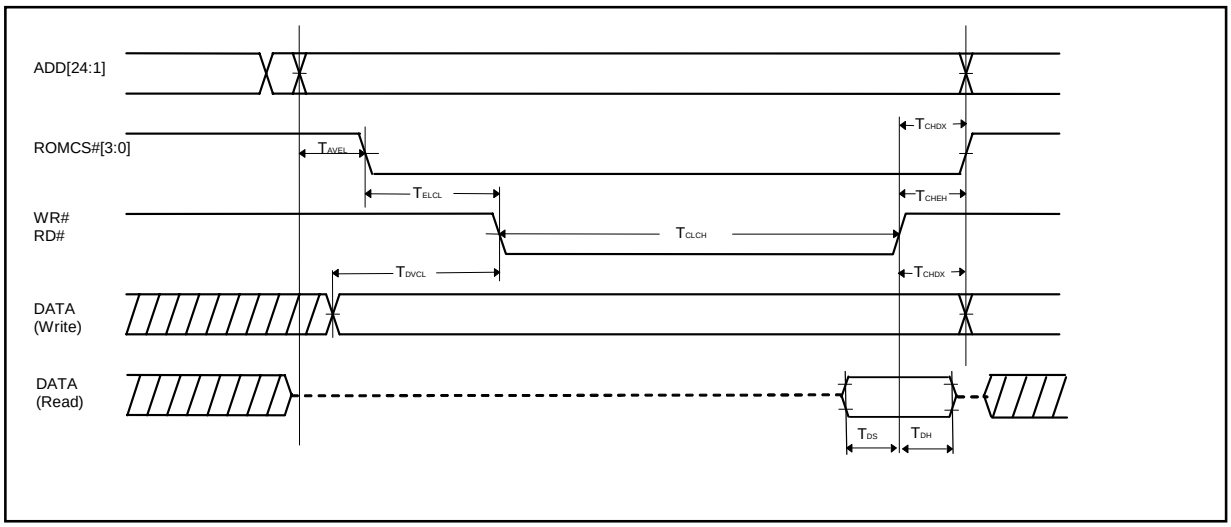
Notes. With the VR4133, the RD# and WR# signals are called the command signals for the LCD interface. When write cycle to the ROM space where corresponds with ROMWEN2 and ROMWEN0 bits of BCUCNTREG1 register is permitted, the access timing is able to be set up by the value of WAIT2 (3:0), WAIT4 (7:0), WAIT5 (3:0) of FLASHSPEEDREG.

Remark CMD shows WR# signal, or RD# signal. Also DATA shows Write data, or Read data.

WAIT2	I	WAIT3	J	WAIT5	K
1111	17	11111111	258	1111, 0011	RFU
.....	....	.....	....	0010	4
0101	7	00001101	13	0001	3
0100	6	.....	....	0000	RFU
0011	5	00000011	6		
0010	4	00000010	5		
0001	3	00000001	4		
0000	RFU	00000000	RFU		

VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
101	16.7	RFU	RFU	RFU	RFU	RFU	RFU	RFU
100	15.0	RFU	7.5	11.2	15.0	18.8	22.5	RFU
011	15.0	RFU	10.0	15.0	20.0	25.1	RFU	RFU
010	18.0	RFU	12.0	18.0	24.1	RFU	RFU	RFU
001	20.1	RFU	13.4	20.1	26.8	RFU	RFU	RFU
000	15.0	RFU	15.0	22.5	RFU	RFU	RFU	RFU

Remark As for the value of T, please consult the value of the above table.


ADD[24:1]
ROMCS#[3:0]
WR#
RD#
DATA
(Write)
DATA
(Read)
TAVEL
TELCL
TCLCH
TDVCL
TCHDX
TCHEH
TCHDX
TDS
TDH

(8) I/O interface parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)[Notes 1, 2]	tAS		T*L-9.7		ns
Address hold time (from command signal ↑)[Notes 1, 2]	tAH		T*O-9.7		ns
Command signal recovery time[Notes 1, 2]	tRY		T*(O+1)-9.7		ns
IORDY sampling start time[Note 2]	tCLR		T*M-9.7		ns
Command signal delay time from IORDY ↑[Notes 1, 2]	tRHCH		T*N-9.7	T*(N + 2) + 9.7	ns
IORDY hold time (from command signal ↑)[Note 1]	tRYZ		0		ns
Data output setup time (to command signal ↓)[Notes 1, 2]	tDSTC		T*(L1)-9.7		ns
Data output setup time (to command signal ↑)[Notes 1, 2]	tDVCH		T*(L+ M+N-1)-9.7		ns
Data output hold time (from command signal ↑)[Notes 1, 2]	tCHDV		T*O		ns
Data input setup time (to command signal ↑)[Note 1]	tDS		2.8		ns
Data input hold time (from command signal ↑)[Note 1]	tDH		0.7		ns
Active delay time of SYSEN#[Note.3]	tED		-（0.5T+5.0）	5.0	ns
Active delay time of SYSDIR#[Note.4]	tDAD		-5.0	5.0	ns
Inactive delay time of SYSDIR#[Note.4]	tDID		T-5.0	T+5.0	ns

Notes **1.** With the VR4133, the RD# and WR# signals are called the command signals for the LCD interface.

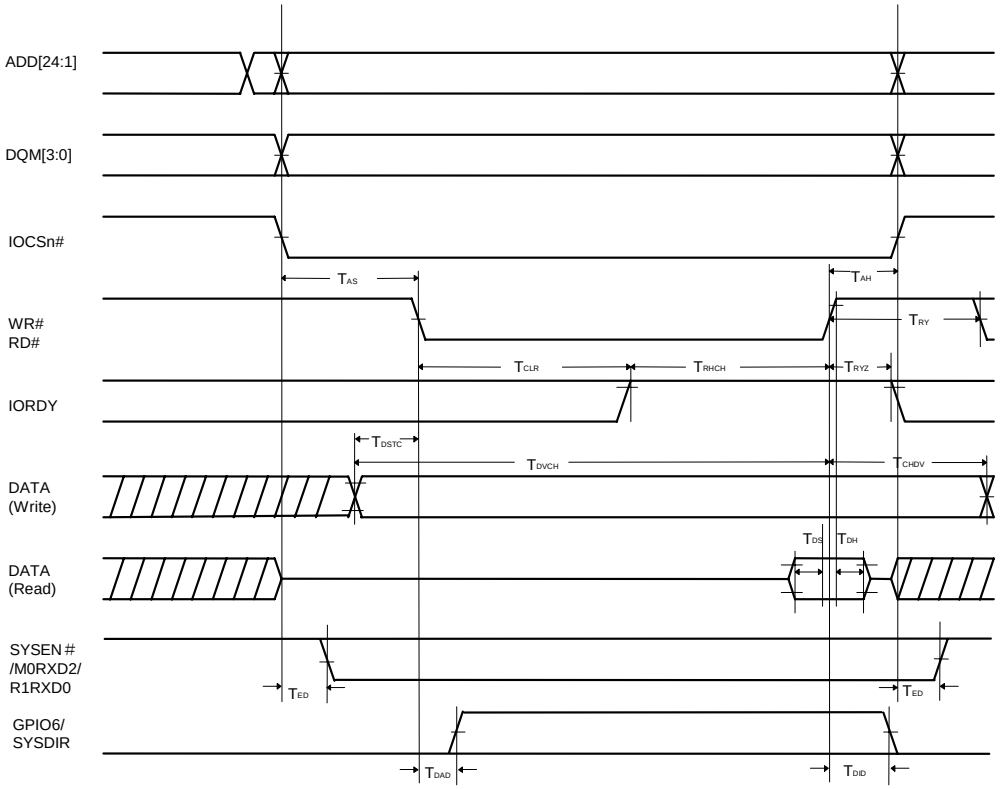
2. The values of L, M, N and O are set by using the ion_1_wait(3:0) bits, ion_2_wait(3:0) bits, ion_3_wait(3:0) bits, and ion_5_wait(1:0) bits, respectively, of the IOnSPEEDREG register. The value of T is set by using the CLKSEL(2:0) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register (n = 0, 1).

	L (IOn_1_wait)	M (Ion_2_wait)	N (IOn_3_wait)
1111	16	14	18
1110	15	13	17
1101	14	12	16
1100	13	11	15
1011	12	10	14
1010	11	9	13
1001	10	8	12
1000	9	7	11
0111	8	6	10
0110	7	5	9
0101	6	4	8
0100	5	3	7
0011	4	2	6
0010	3	1	5
0001	2	0	4
0000	1	-1	3

IOn_5_wait	O
11	4
10	3
01	2
00	1

VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
101	16.7	RFU	RFU	RFU	RFU	RFU	RFU	RFU
100	15.0	RFU	7.5	11.2	15.0	18.8	22.5	RFU
011	15.0	RFU	10.0	15.0	20.0	25.1	RFU	RFU
010	18.0	RFU	12.0	18.0	24.1	RFU	RFU	RFU
001	20.1	RFU	13.4	20.1	26.8	RFU	RFU	RFU
000	15.0	RFU	15.0	22.5	RFU	RFU	RFU	RFU

Remark **As for the value of T, please consult the value of the above table.**



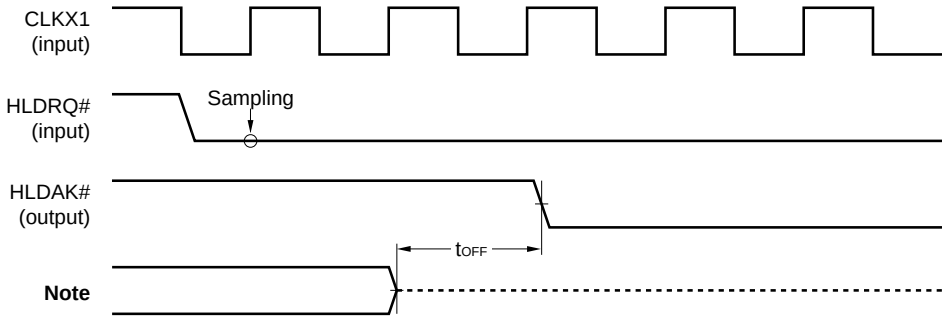
Remark The broken lines indicate high impedance.

(9) Bus hold parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
HLDRQ# input pulse width[Note]	t_{HP}	In Fullspeed/Standby/Suspend mode	271		ns
Data floating delay time	t_{OFF}	In Fullspeed/Standby/Suspend mode	0		ns
Data valid delay time	t_{ON}	In Fullspeed/Standby/Suspend mode	0		ns

Note When the VR4133 receives an input signal of less than 271 ns, the bus hold operation may malfunction. Change the signal input to the HLDRQ# pin to one with a pulse width of 271 ns or more.

(a) Starting bus hold

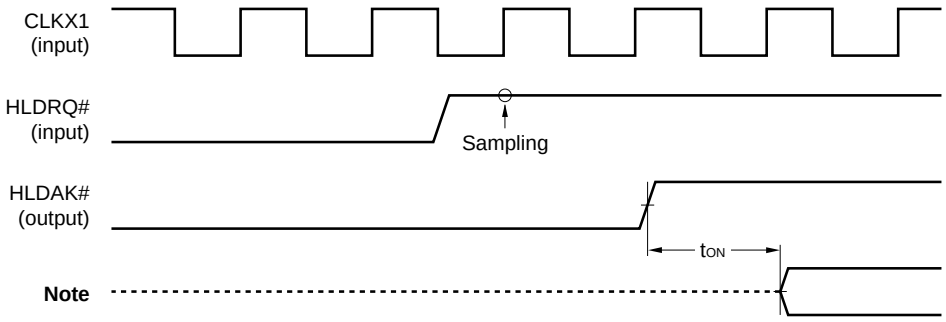


Note Applies to the following pins.

- ADD (24:0), DATA (15:0). CKE (1:0), DQM0/LBE0/ADD0, DQM1/LBE1/UBE, DQM (3:2)/LBE(3:2), CS[1:0]#, RAS, CAS, SCLK, RD#, R#, WR# ins
- GPIO6/SYSDIR pin when the load-reducing buffer direction is controlled by setting the SYSDIR_EN bit of the BCUCNTREG3 register
- DATA (31:16)/GPIO (31:16) pins in 32-bit data bus mode
- CS (3:2)#/ROMCS (3:2)# pins when using the expansion memory space as SDRAM by setting the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register in the 32-bit data bus mode
- SYSEN#/M0RXD2/R1RXD0 pin when the load-reducing buffer enable is controlled by setting the SYSDIR_EN bit and MII pin select bit at Ethernet controller configuration register of channel 0 and Ethernet controller configuration register of channel 1, of the BCUCNTREG3 register

Remark The broken lines indicate high impedance.

(b) Releasing bus hold (HLDRQ#)

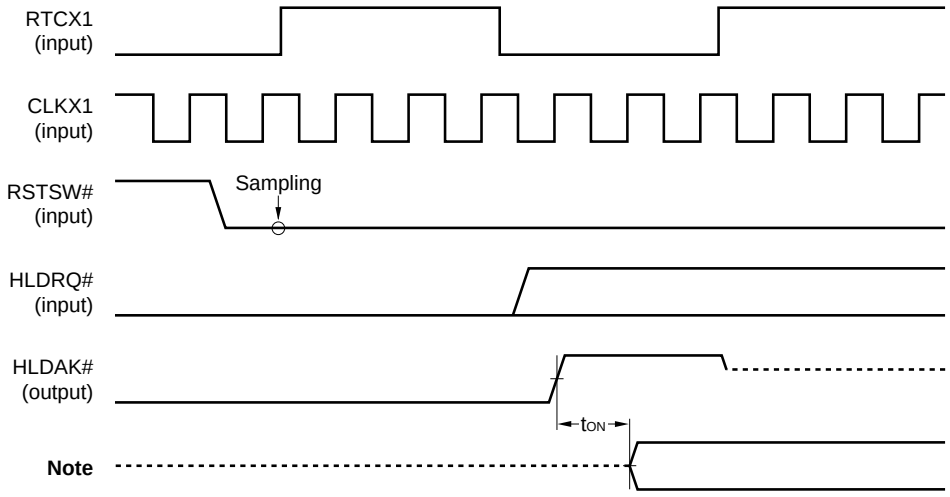


Note Applies to the following pins.

- ADD (24:0), DATA (15:0). CKE (1:0), DQM0/LBE0/ADD0, DQM1/LBE1/UBE, DQM (3:2)/LBE(3:2), CS[1:0]#, RAS, CAS, SCLK, RD#, R#, WR# ins
- GPIO6/SYSDIR pin when the load-reducing buffer direction is controlled by setting the SYSDIR_EN bit of the BCUCNTREG3 register
- DATA (31:16)/GPIO (31:16) pins in 32-bit data bus mode
- CS (3:2)#/ROMCS (3:2)# pins when using the expansion memory space as SDRAM by setting the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register in the 32-bit data bus mode
- SYSEN#/M0RXD2/R1RXD0 pin when the load-reducing buffer enable is controlled by setting the SYSDIR_EN bit and MII pin select bit at Ethernet controller configuration register of channel 0 and Ethernet controller configuration register of channel 1, of the BCUCNTREG3 register

Remark The broken lines indicate high impedance.

(c) Releasing bus hold (RSTSW#)



Note Applies to the following pins.

- ADD (24:0), DATA (15:0). CKE (1:0), DQM0/LBE0/ADD0, DQM1/LBE1/UBE, DQM (3:2)/LBE(3:2), CS[1:0]#, RAS, CAS, SCLK, RD#, R#, WR# ins
- GPIO6/SYSDIR pin when the load-reducing buffer direction is controlled by setting the SYSDIR_EN bit of the BCUCNTREG3 register
- DATA (31:16)/GPIO (31:16) pins in 32-bit data bus mode
- CS (3:2)#/ROMCS (3:2)# pins when using the expansion memory space as SDRAM by setting the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register in the 32-bit data bus mode
- SYSEN#/M0RXD2/R1RXD0 pin when the load-reducing buffer enable is controlled by setting the SYSDIR_EN bit and MII pin select bit at Ethernet controller configuration register of channel 0 and Ethernet controller configuration register of channel 1, of the BCUCNTREG3 register

Remark The broken lines indicate high impedance.

(10) Serial interface parameters

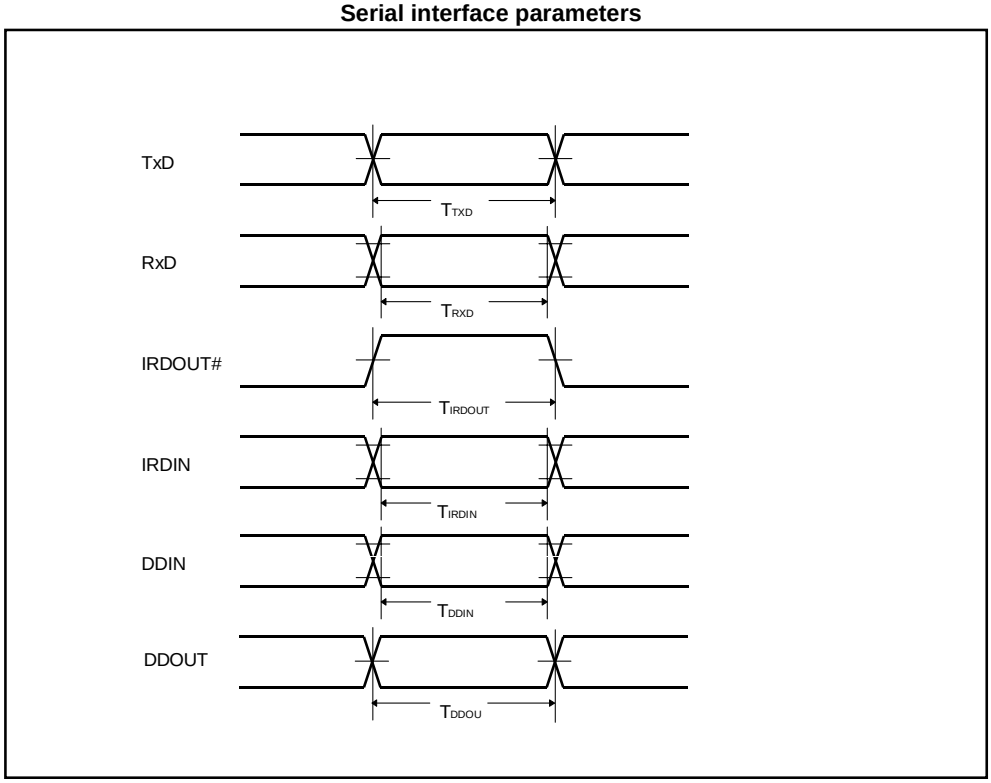
Parameter	Symbol	Condition	MIN.	MAX.	Unit
TXD/CLKSEL2 output pulse width[Note]	tTXD		P– 0.1	P+ 0.1	μs
RXD input pulse width[Note]	tRXD		(9/16)P		μs
JTDO/IRDOUT# high-level output pulse width[Note]	tIRDOUT		(3/16)P– 0.1	(3/16)P+ 0.1	μs
IRDIN input pulse width	tIRDIN		1		μs
DDOUT/GPO32/DBUS32 output pulse width[Note]	tDDOUT		P- 0.1	P+ 0.1	μs
DDIN/GPO35 input pulse width[Note]	tDDIN		(9/16)P		μs

Note N indicates the data transfer cycle per bit, which is determined by the divisor of the baud rate generator that is set with the SIUDLL and SIUDLM registers.

Baud Rate (bits/s)	SIUDLM, SIUDLL	P(μs)
50	23040	20000
75	15360	13333
110	10473	9091
134.5	8565	7435
150	7680	6667
300	3840	3333
600	1920	1667
1200	960	833
1800	640	556
2000	576	500
2400	480	417
3600	320	278
4800	240	208
7200	160	139
9600	120	104
19200	60	52.1
38400	30	26.0
57600	20	17.4
115200	10	8.68
128000	9	7.81
144000	8	6.94
192000	6	5.21
230400	5	4.34
288000	4	3.47
384000	3	2.60
576000	2	1.74
1152000	1	0.868

Remark Baud rate = (18.432 MHz/16)/(value set in the SIUDLM and SIUDLL registers)

Serial interface parameters



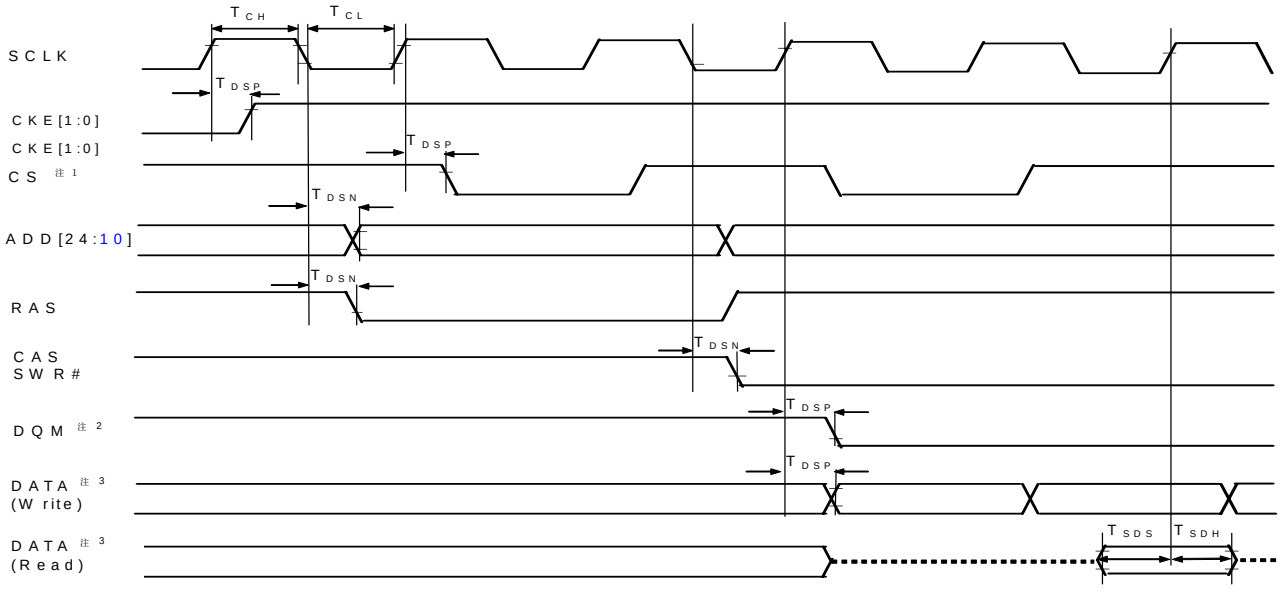
(11) SDRAM interface parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SCLK jitter[Note]	tJitter			3.5	%
SCLK high-level width	t_{CH}		2.5		ns
SCLK low-level width	t_{CL}		2.5		ns
Output delay time (from SCLK ↑)	t_{DSP}		1.1	5.2	ns
Output delay time (from SCLK ↓)	t_{DSN}		-2.0	7.8	ns
Data input setup time	t_{SDS}		1.7		ns
Data input hold time	t_{SDH}		1.8		ns

Note Precision tests have not been performed. Only guaranteed as design characteristics.

Remark The maximum frequency of SCLK is 133 MHz.

SDRAM interface parameters



Notes **1.** The pins to which this signal applies differ depending on the state of the DBUS32 pin and the EXT_ROMCS(1:0) bits of the BCUCNTREG3 register.

When DBUS32 = 0: CS(1:0)#, DQM(3:2)/LBE(3:2)

When DBUS32 = 1 and EXT_ROMCS(1:0) = 11: CS(1:0)#

When DBUS32 = 1 and EXT_ROMCS(1:0) = 10: CS(1:0)#, CS2#/ROMCS2#

When DBUS32 = 1 and EXT_ROMCS(1:0) = 00: CS(1:0)#, CS(3:2)#/ROMCS(3:2)#

2. The pins to which this signal applies differ depending on the state of the DBUS32 pin.

When DBUS32 = 0: DQM1/LBE1/UBE, DQM0/LBE0/ADD0

When DBUS32 = 1: DQM (3:2)/LBE(3:2),DQM1/LBE1/UBE, DQM0/LBE0/ADD0

3. The pins to which this signal applies differ depending on the state of the DBUS32 pin.

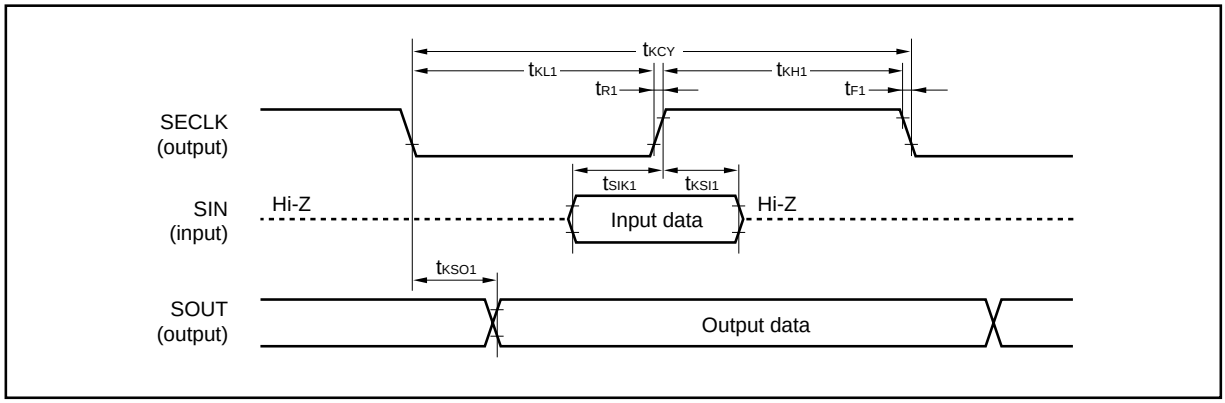
When DBUS32 = 0: DATA (15:0)

When DBUS32 = 1: DATA (31:16)/GPIO(31:16) , DATA(15:0)

Remark The broken lines indicate high impedance.

(12) CSI (clocked serial interface) parameters

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating frequency					9.216	MHz
SECLK clock cycle time	t_{KCY}		108			ns
SECLK high-level width	t_{KH1}		$t_{KCY}/2 - 10$			ns
SECLK low-level width	t_{KL1}		$t_{KCY}/2 - 10$			ns
SECLK rise time	t_{R1}				10	ns
SECLK fall time	t_{F1}				10	ns
SIN input setup time (to SECLK ↑)	t_{SIK1}		30			ns
SIN input hold time (from SECLK ↑)	t_{KSI1}		20			ns
SOUT output delay time (from SECLK ↓)	t_{KSO1}				20	ns



(13) PCI bus interface parameters

Parameter	Symbol	Condition	MIN.	MAX.	Unit
PCLK clock cycle[Notes 1, 2]	tCLK		T*Q		ns
PCLK high-level width[Notes 1, 2]	tCLKH		(T*Q/2)-4		ns
PCLK low-level width[Notes 1, 2]	tCLKL		(T*Q/2)-4		ns
Output valid delay time (from PCLK ↑)[Note 3]	tVAL		T.B.D	6	ns
Delay time from floating to valid (from PCLK ↑)[Note 4]	tON		2		ns
Output floating delay time (from PCLK ↑)[Note 4]	tOFF			14	ns
Data input setup time[Note 5]	tSU		T.B.D		ns
Data input hold time[Note 5]	tDH		0		ns

Notes **1.** Applies to the PCLK pin.

2. The value of Q is set by using the SEL_CLK(1:0) bits of the PCICLKSELREG register, and the value of T is set by using the CLKSEL(2:0) signals (TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0) and the VTDIV(2:0) bits of the PMUTCLKDIVREG register.

SEL_CLK(1:0)	Q
11	3
10	1
01	4
00	2

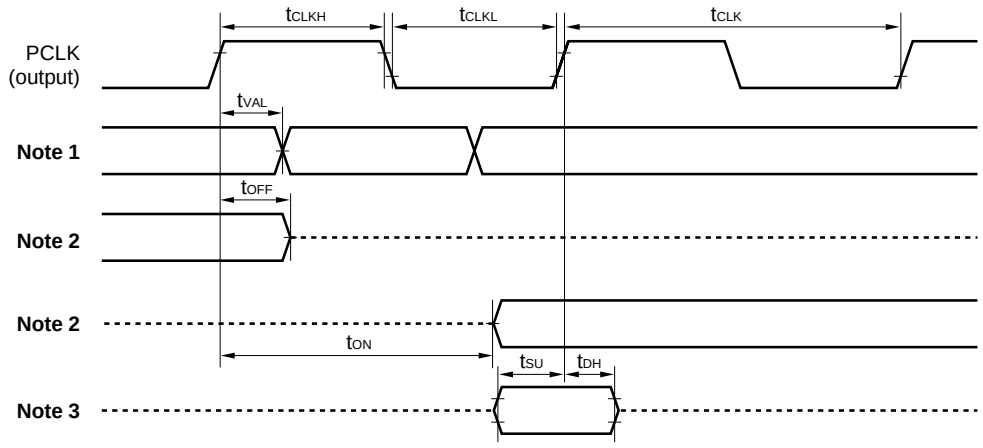
VTDIV(2:0) / CLKSEL(2:0)	000	001	010 (Divided by 2)	011 (Divided by 3)	100 (Divided by 4)	101 (Divided by 5)	110 (Divided by 6)	111
111	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
110	15.0	RFU	RFU	RFU	RFU	RFU	RFU	RFU
101	16.7	RFU	RFU	RFU	RFU	RFU	RFU	RFU
100	15.0	RFU	7.5	11.2	15.0	18.8	22.5	RFU
011	15.0	RFU	10.0	15.0	20.0	25.1	RFU	RFU
010	18.0	RFU	12.0	18.0	24.1	RFU	RFU	RFU
001	20.1	RFU	13.4	20.1	26.8	RFU	RFU	RFU
000	15.0	RFU	15.0	22.5	RFU	RFU	RFU	RFU

3. Applies to the AD(31:27), AD26/GPO47, AD25/GPO46, AD24/GPO45, AD23/GPO44, AD22/GPO43, AD21/GPO42, AD20/GPO41, D19/GPO40, AD18/GPO39, AD17/M1TXER, AD16/M1TXEN, AD15/M1TXD3, AD14/M1TXD2, AD13/M1TXD1, AD12/M1TXD0, AD11/M1RXDV, AD10/M1RXER, AD9/M1RXD3, AD8/M1RXD2, AD7/M1RXD1, AD6/M1RXD0, AD5/M1MD, AD4/M1MDC, AD3/M1CRS, AD2/M1COL, AD1/M1TXCLK, AD0/M1RXCLK, CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, GNT(2:0)# and RST# pins.

4. Applies to the AD(31:27), AD26/GPO47, AD25/GPO46, AD24/GPO45, AD23/GPO44, AD22/GPO43, AD21/GPO42, AD20/GPO41, D19/GPO40, AD18/GPO39, AD17/M1TXER, AD16/M1TXEN, AD15/M1TXD3, AD14/M1TXD2, AD13/M1TXD1, AD12/M1TXD0, AD11/M1RXDV, AD10/M1RXER, AD9/M1RXD3, AD8/M1RXD2, AD7/M1RXD1, AD6/M1RXD0, AD5/M1MD, AD4/M1MDC, AD3/M1CRS, AD2/M1COL, AD1/M1TXCLK, AD0/M1RXCLK, CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP# and TRDY# pins.

5. Applies to the AD(31:27), AD26/GPO47, AD25/GPO46, AD24/GPO45, AD23/GPO44, AD22/GPO43, AD21/GPO42, AD20/GPO41, D19/GPO40, AD18/GPO39, AD17/M1TXER, AD16/M1TXEN, AD15/M1TXD3, AD14/M1TXD2, AD13/M1TXD1, AD12/M1TXD0, AD11/M1RXDV, AD10/M1RXER, AD9/M1RXD3, AD8/M1RXD2, AD7/M1RXD1, AD6/M1RXD0, AD5/M1MD, AD4/M1MDC, AD3/M1CRS, AD2/M1COL, AD1/M1TXCLK, AD0/M1RXCLK, CBE(3:0), DEVSEL＃, FRAME＃, IRDY＃, LOCK＃, PAR, PERR＃, SERR＃, STOP＃, TRDY＃ and REQ(2:0)＃ pins.

PCI bus interface timing



Notes **1.** Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, GNT(2:0)#, and RST# pins.

2. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, and TRDY# pins.

3. Applies to the AD(31:0), CBE(3:0), DEVSEL#, FRAME#, IRDY#, LOCK#, PAR, PERR#, SERR#, STOP#, TRDY#, and REQ(2:0)# pins.

Remark The broken lines indicate high impedance.

(14) Ethernet controller parameters

MII interface mode

Parameter	Symbol	Condition	MIN.	MAX.	Unit
TCLK clock cycle Notes 1	Tcyctx		40	400	ns
RCLK clock cycle Notes 2	Tcycrx		40	400	ns
Output valid delay time (from TXEN ↑)Note 3	Tden		0	25	ns
Output valid delay time (from TXD(3:0) ↑)Note 4	Tdtd		0	25	ns
Output valid delay time (from TXER ↑)Note 5	Tdtxer		0	25	ns
RXDV input setup timeNote 6	Tsdy		10		ns
RXDV input hold timeNote 6	Thdy		10		ns
RXD (3:0) Data input setup timeNote 7	Tsrd		10		ns
RXD (3:0) Data input hold timeNote 7	Thrd		10		ns
RXDER input setup timeNote 8	Tsrxer		10		ns
RXDER input hold timeNote 8	Thrxer		10		ns

Notes
1. Applies to the CLKOUT/M0TXCLK/REFCLK, AD1/M1TXCLK pin.
2. Applies to the GPIO7/M0RXCLK/R1CRSDV, AD0/M1RXCLK pin.
3. Applies to the GPO36/M0TXEN/R0TXEN, AD16/TXEN pin.
4. Applies to the GPIO14/M0TXD0/R0TXD0, GPIO13/M0TXD1/R0TXD1, DRQ1/M0TXD2/R1TXD0, GPIO5/M0TXD3/R1TXD1, AD12/TXD0, AD13/TXD1, AD14/TXD2, AD15/TXD3 pin.
5. Applies to the DAK1/M0TXER/R1TXEN, AD17/M1TXER pin.
6. Applies to the GPIO8/M0RXDV/R0CRSDV, AD11/M1RXDV pin.
7. Applies to the GPO38/M0RXD0/M0RXD0, GPIO4/M0RXD1/R0RXD1, SYSEN#/M0RXD2/R1RXD0, GPO37/M0RXD3/R1RXD1, AD6/M1RXD0, AD7/M1RXD1, AD8/M1RXD2, AD9/M1RXD3 pin.
8. Applies to the GPIO10/M0RXER/R1MDC, AD10/M1RXER pin.

RMII interface mode

Parameter	Symbol	Condition	MIN.	MAX.	Unit
CLKOUT/M0TXCLK/REFCLK clock cycle	Tcyc		20		ns
CLKOUT/M0TXCLK/REFCLK clock jitter	REFjit			50	ppm
CLKOUT/M0TXCLK/REFCLK High/Low-level width	REFhilo		35	65	%
Output valid delay time (from TXD(1:0) ↑)Note 1	Tdtd		0	10	ns
Output valid delay time (from TXEN ↑)Note 2	Tdtxen		0	10	ns
CRSDV input setup timeNote 3	Tsdy		4		ns
CRSDV input hold timeNote 3	Thdy		2		ns
RXD(1:0) input setup timeNote 4	Tsrd		4		ns
RXD(1:0) input hold timeNote 4	Thrd		2		ns

Notes **1.** Applies to the GPIO14/M0TXD0/R0TXD0, GPIO13/M0TXD1/R0TXD1, DRQ1/M0TXD2/R1TXD0, GPIO5/M0TXD3/R1TXD1 pin.

2. Applies to the GPO36/M0TXEN/R0TXEN, DAK1/M0TXER/R1TXEN pin.

3. Applies to the GPIO8/M0RXDV/R0CRSDV, GPIO7/M0RXCLK/R1CRSDV pin.

4. Applies to the GPO38/M0RXD0/M0RXD0, GPIO4/M0RXD1/R0RXD1, SYSEN#/M0RXD2/R1RXD0, GPO37/M0RXD3/R1RXD1 pin.

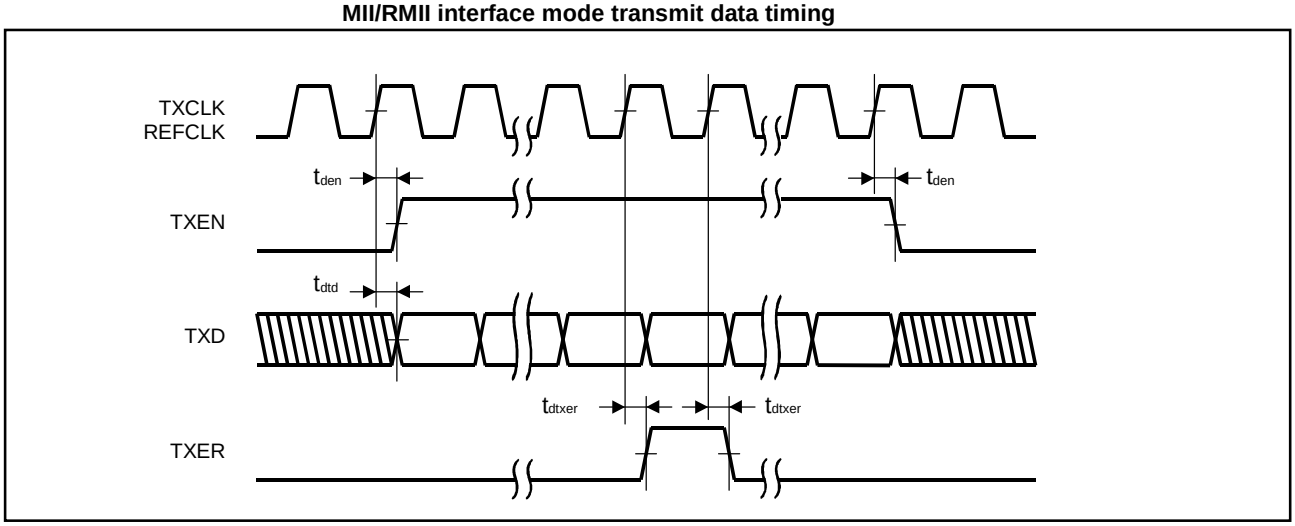
Management interface mode

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MDC clock cycleNote 1	Tcym		400		ns
Output valid delay time (from MD ↑)Note 2	Tdmdo		10		ns
MD data input setup timeNote 2	Tsmdi		10		ns
MD data input hold timeNote 2	Thmdi		10		ns

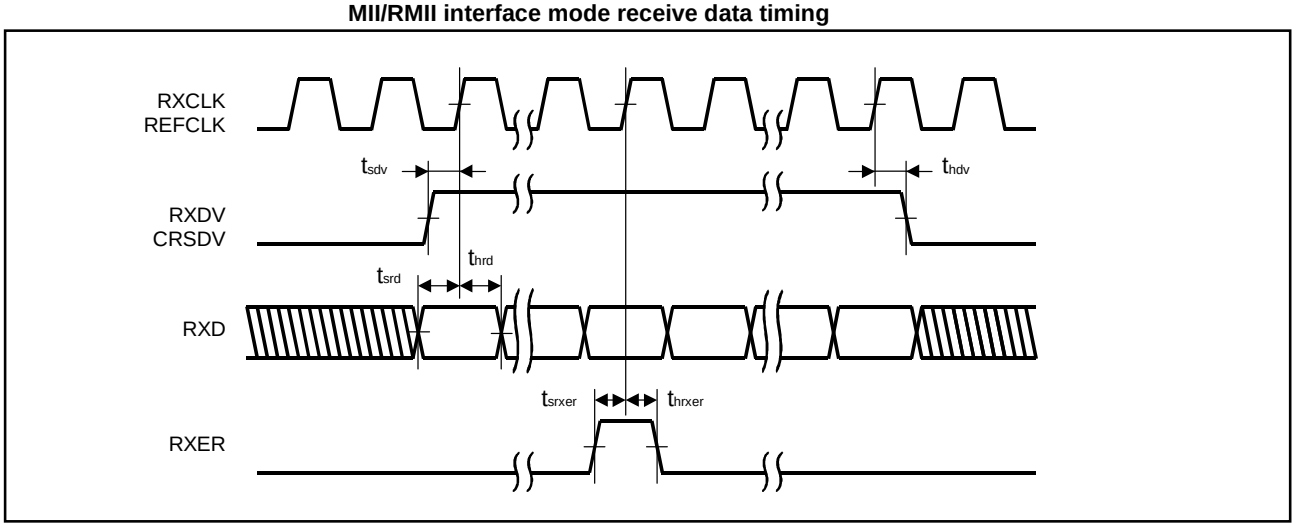
Notes **1.** Applies to the GPIO9/M0MDC/R0MDC, AD4/M1MDC, GPIO10/M0RXER/R1MDC pin.

2. Applies to the GPIO12/M0MD/R0MD, M0CRS/R1MD/BIGENDIAN, AD5/M1MD pin.

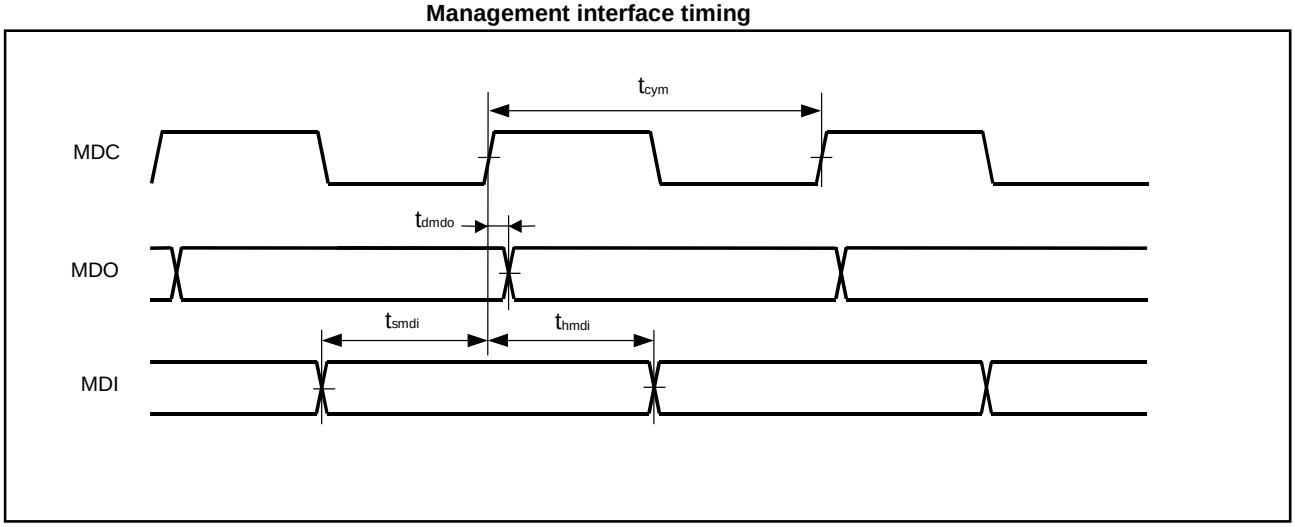
MII/RMII interface mode transmit data timing



MII/RMII interface mode receive data timing



Management interface timing



(15) DMA hardware handshake parameters

DMA function of VR4133 as for the following 3 kinds DRQ/DAK signal hardware handshake control is possible.

PCI space ⇔ DMA transmission of the DRAM space

ROM space ⇔ DMA transmission of the DRAM space

External I/O space ⇔ DMA transmission of the DRAM space

DMA hardware handshake parameters

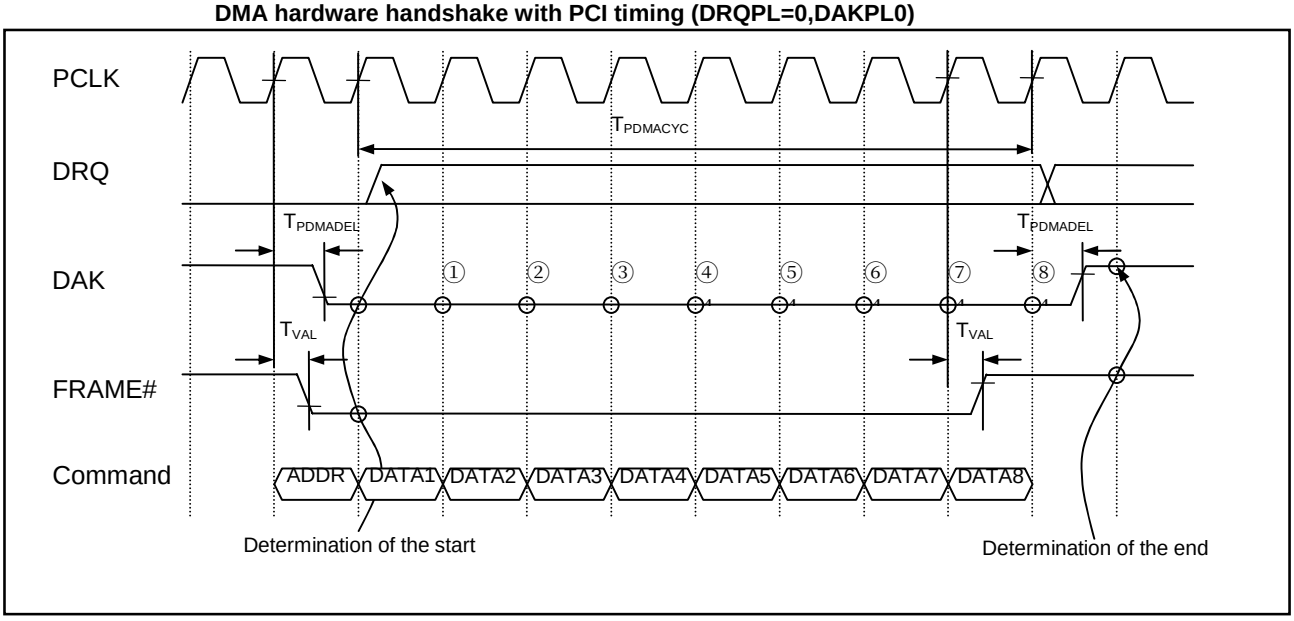
Parameter	Symbol	Condition	MIN.	MAX.	Unit
From FRAME# assertion to the next sampling of DRQ min. time (for PCI-DMA transmission) Notes 1	$T_{PDMACYC}$			8*T*Q	ns
Output valid delay time (from DAK ↑) Note 2	$T_{PDMADEL}$			12	ns
From DAK active to the next sampling of DRQ min. time (for ROM-DMA transmission) Notes 1	$T_{RDMACYC}$			T*(G*R－2)	ns
Output valid delay time (from DAK ↑) Note 2	$T_{RDMADEL}$			12	ns
From DAK active to the next sampling of DRQ min. time (for PageROM-DMA transmission) Notes 1	$T_{PRDMACYC}$			T*(G*S+（H＊(R-S)）-2)	ns
Output valid delay time (from DAK ↑) Note 2	$T_{PRDMADEL}$			12	ns
From DAK active to the next sampling of DRQ min. time (for FlashROM-DMA transmission) Notes 1	$T_{FDMACYC}$			T*(I＋J) *R	ns
Output valid delay time (from DAK ↑) Note 2	$T_{FDMADEL}$			12	ns
From DAK active to the next sampling of DRQ min. time (for External-I/O-DMA transmission) Notes 1	$T_{IDMACYC}$			T*(L-M-N)*R	ns
Output valid delay time (from DAK ↑) Note 2	$T_{IDMADEL}$			12	ns

Page ROM DMA parameters

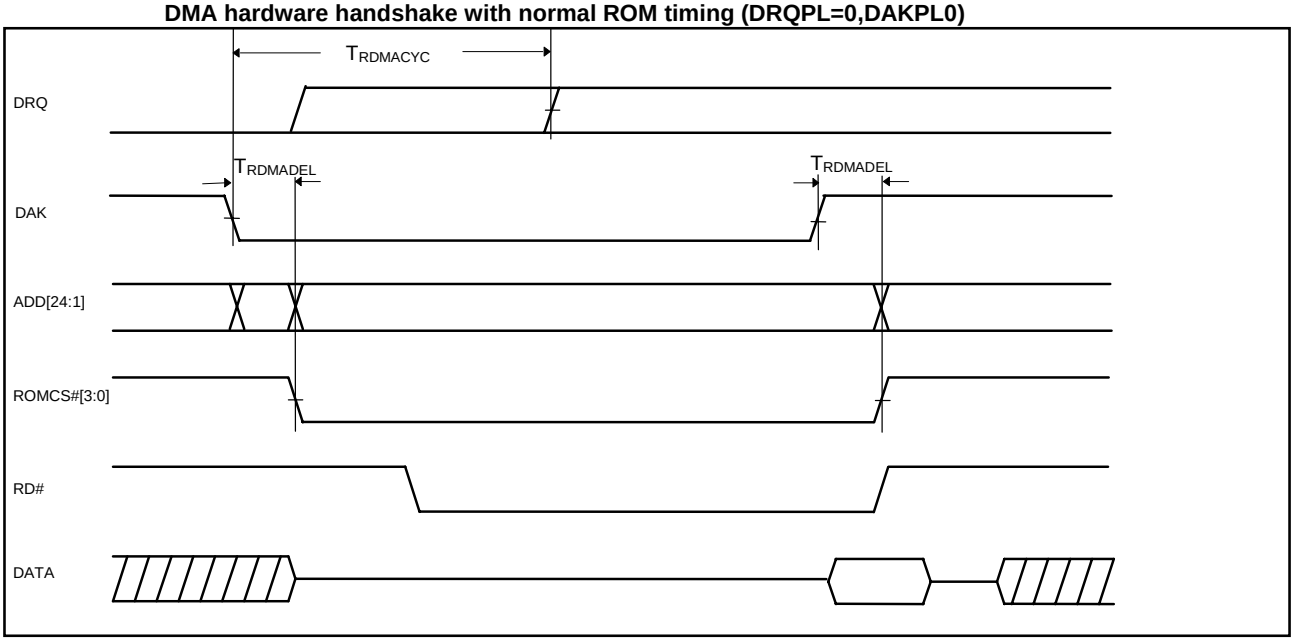
DBUS32	DMABLKS	R
1	10	8
1	01	4
1	00	1
0	10	16
0	01	8
0	00	2

PAGESIZE	DMABLKS	S
10	10	1
10	01	1
10	00	1
01	10	2
01	01	1
01	00	1
00	10	4
00	01	2
00	00	1

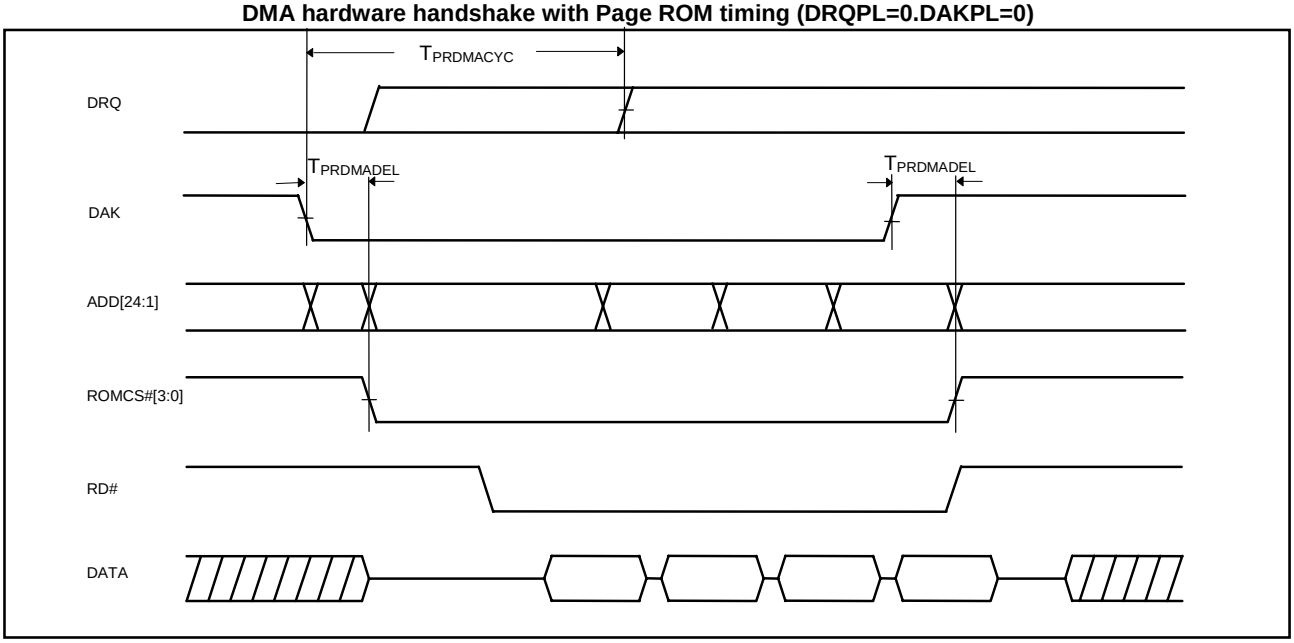
DMA hardware handshake with PCI timing (DRQPL=0,DAKPL0)



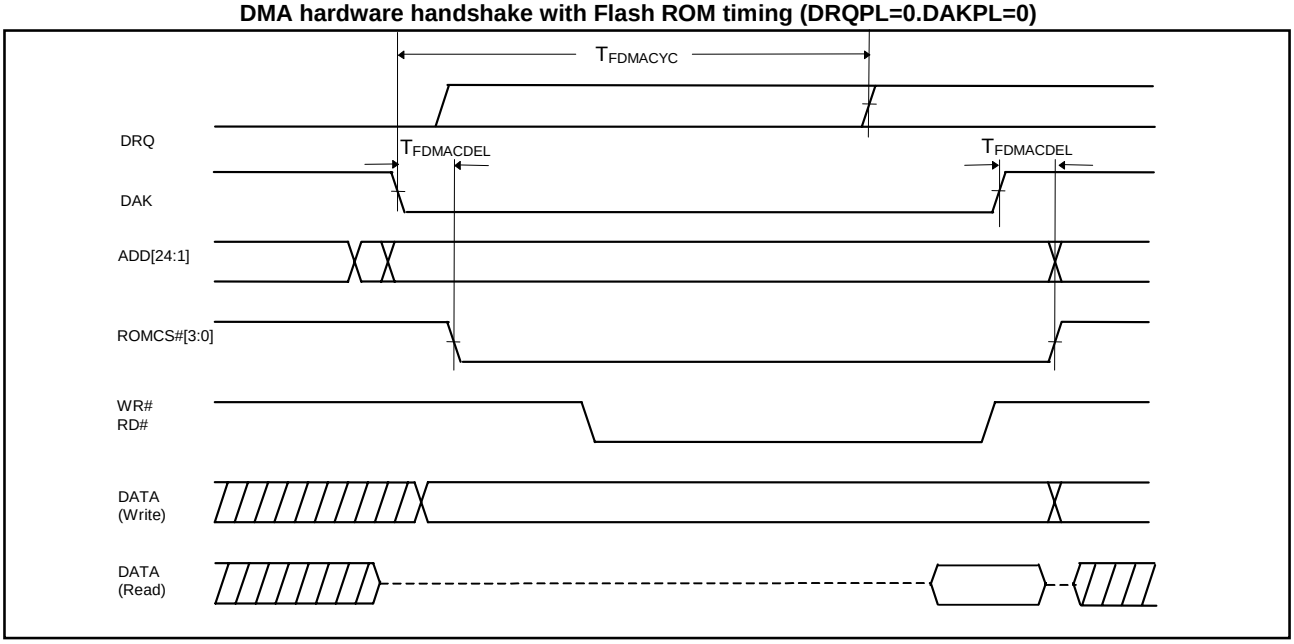
DMA hardware handshake with normal ROM timing (DRQPL=0,DAKPL0)



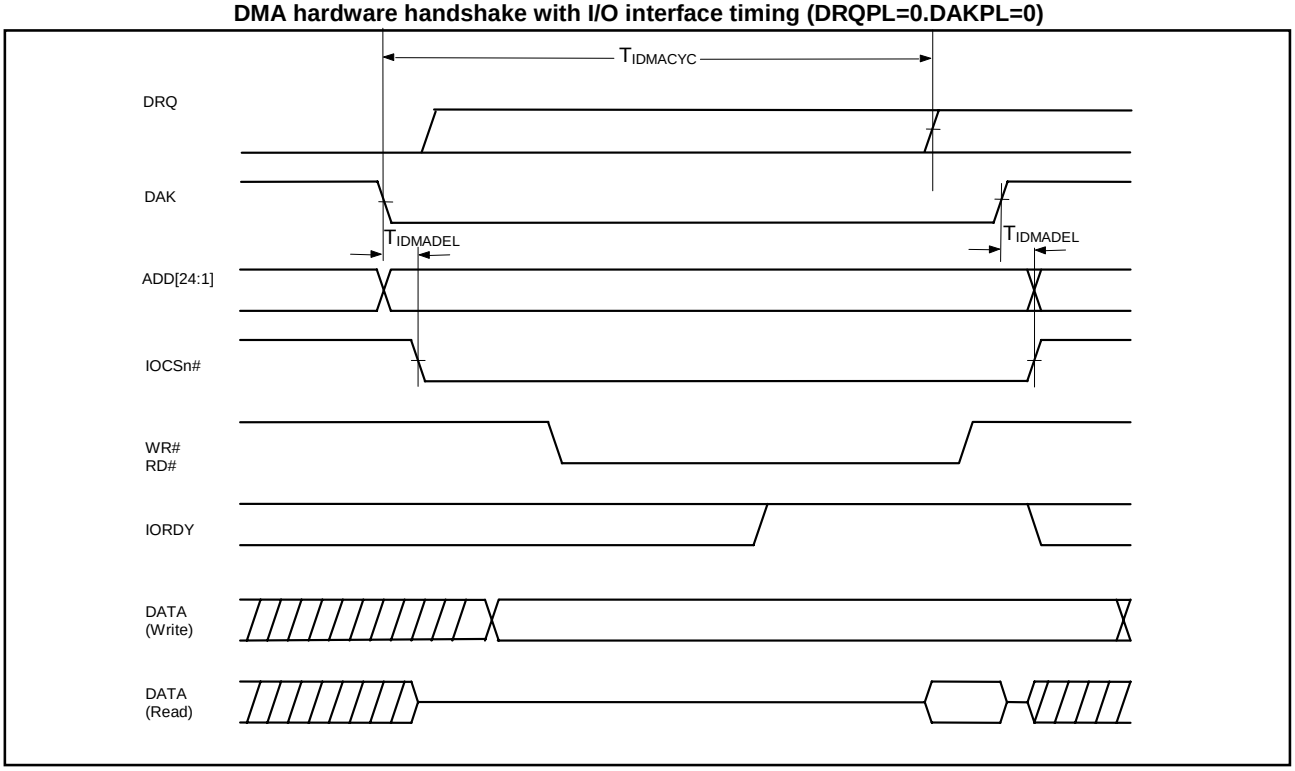
DMA hardware handshake with Page ROM timing (DRQPL=0.DAKPL=0)



DMA hardware handshake with Flash ROM timing (DRQPL=0.DAKPL=0)



DMA hardware handshake with I/O interface timing (DRQPL=0.DAKPL=0)



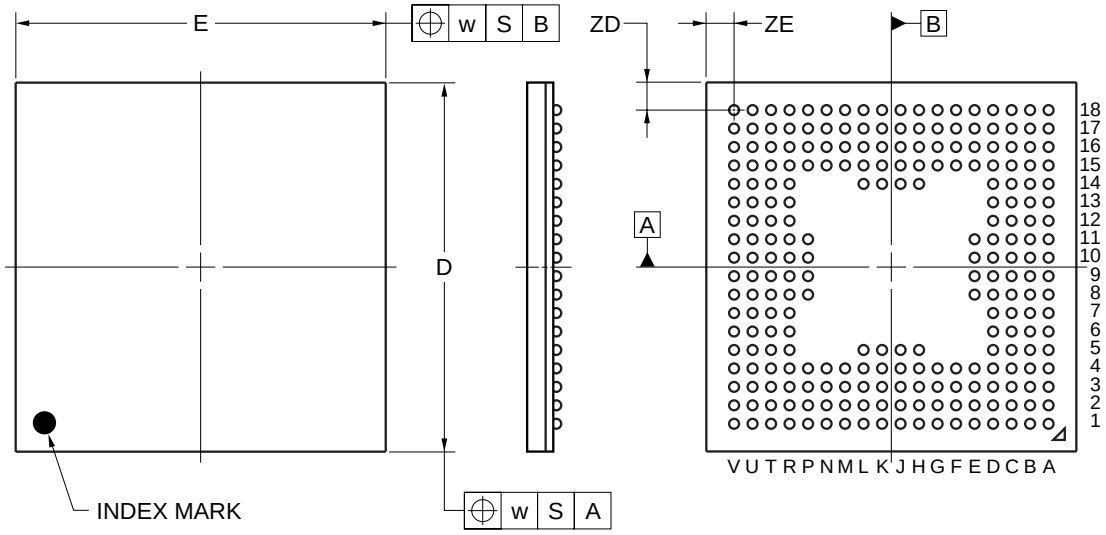
Load Coefficient (Delay Time per Load Capacitance)

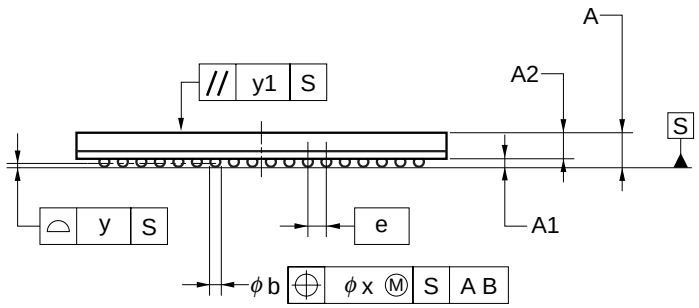
Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

Caution Precision tests have not been performed. Only guaranteed as design characteristics.

3. PACKAGE DRAWING

240ピン・プラスチック FBGA（16x16）外形図





(UNIT:mm)

ITEM	DIMENSIONS
D	16.00±0.10
E	16.00±0.10
w	0.20
A	1.48±0.10
A1	0.35±0.06
A2	1.13
e	0.80
b	$0.50^{+0.05}_{-0.10}$
x	0.08
y	0.10
y1	0.20
ZD	1.20
ZE	1.20

P240F1-80-GA3

4. RECOMMENDED SOLDERING CONDITIONS

The μPD30133 should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 4-1. Surface Mounting Type Soldering Conditions

μPD30133F1-200-GA2: 240-pin plastic FBGA (16 × 16)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: 2 times max., Exposure limit: 3 days[Note] (after that, prebake at 125°C for 20 to 72 hours.)	T.B.D

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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