Interfacing the DP8441 and the 68040

National Semiconductor
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Atilio Canessa
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This application notes assumes that the reader is familiar with the modes of operation of the DP8441 DRAM controller and the 68040 microprocessor. The nature of this application note is to give the system designer an idea of a possible memory configuration. After reading this application note, the system designer must do an analysis for his particular application.

The design's operating frequency is 33 MHz and the design supports page and burst accesses. The design constitutes a complete 128 Megabytes memory system in a 2 bank configuration. The memory array uses 70 ns DRAMs in a 16 Megx1 architecture. Different or more compact memory arrays can be achieved if different DRAMs are used.

The DP8441 performs all housekeeping required by DRAMs. The controller will refresh the memory and it will guarantee precharge times after accesses or refresh cycles. The DP8441 also arbitrates between accesses, refreshes and precharge. The DRAM controller will insert wait states into an access cycle to allow refresh or precharge to take place. The controller will delay a refresh to allow an access in progress to finish.

The DP8441 supports byte, word or double-word writing. This is done through decoding the 68040's A0, A1, SIZ0 and SIZ1 outputs and connect the appropriate $\overline{BE}$ (byte enables) to the $\overline{ECAS}$ inputs in the DP8441. $\overline{ECAS}$ controls the $\overline{CAS}$s to the DRAMs.The DP8441 also supports the 68040 Read-Modify-Write (LOCKED cycle), this is done by connecting the $\overline{LOCK}$ output from the 68040 to $\overline{DISRFSH}$ input on the DP8441. This guarantees that a refresh will not brake a Read-Modify-Write cycle.

RESET AND PROGRAMMING

Resetting the DRAM controller is accomplished by asserting low the $\overline{RESET}$ input for at least 16 clock cycles. The DP8441 must be programmed before accessing the memory. Programming can be done by writing to an I/O address equal to the programming selection. Programming can also be accomplished during the first memory write. In the latter case the CPU writes to an address equal to the programming selection during the first write cycle after power up.

After $\overline{ML}$ negates during the programming cycle, the DP8441 enters a 60 ms initialization period. This period is when the Phase Lock Loop (PLL) locks into place.

The system must wait at least 70 ms before accessing the memory. During this time the DRAM controller performs refreshes to the memory, this makes further ''warm up'' cycles unnecessary.

OPENING ACCESS

A memory access begins when the 68040 outputs a valid address and asserts $\overline{ADS}$. For this design at 33 MHz, the address, the B0 (bank select) and the $\overline{ADS}$ inputs meet the set up times required by the DRAM controller. Three address lines are used to do DRAM $\overline{CS}$. The $\overline{CS}$ setup time is also met.

The DP8441 will split the address from the CPU and will output the row address to the DRAMs. The appropriate $\overline{RAS}$, as decoded by B0, will assert from the next rising clock edge latching the row address into the DRAM. The programmed t_{RAH} will be guaranteed by the controller before switching the internal multiplexor to the column address. The controller latches the column address into the DRAM after meeting the t_{CSC}. The t_{RAH}, t_{CSC} and the time when the controller switches the row address to the column address is guaranteed by the on board delay line based on the PLL.

The controller asserts $\overline{DTACK}$ after the programmed number of wait states to indicate to the CPU that the access can finish. In this design, $\overline{DTACK}$ asserts from the 3rd rising clock edge. The $\overline{DTACK}$ setup time required by the CPU is easily met. At the end of the fourth clock the 68040 will either latch the data into its registers in the case of a read cycle, or it will take the data of the bus in the case of a write cycle. For every access, $\overline{DTACK}$ asserts for one clock period, and $\overline{CAS}$ negates from the same clock edge that $\overline{DTACK}$ negates.

PAGE ACCESSES

Every access finishes when $\overline{DTACK}$ asserts. In this application note, the DRAM controller is programmed in page mode, thus when $\overline{DTACK}$ negates, only CAS negate and $\overline{RAS}$ stays asserted. When the CPU requests a new access (a new address and a new $\overline{ADS}$), if this new access is within the same page as the previous access (same row address), a page hit is detected by the on-board page comparator. When there is a page hit, $\overline{RAS}$ stays asserted and the controller outputs the new column address and asserts $\overline{CAS}$ from the next rising clock edge. In cases when there is a page miss, the DP8441 negates $\overline{RAS}$, meets the programmed number of clock cycles for precharge, and then asserts $\overline{RAS}$ to latch the new row address into memory. In either case $\overline{DTACK}$ will assert and negate after the appropriate number of programmed wait states ($\overline{DATCK}$ for page accesses or for opening accesses).

BURST ACCESSES

The 68040 indicates that it wants to burst when the attributes SIZ0 and SIZ1 are both 1. The system's glue logic decodes SIZ0 and SIZ1 and generates BSTREQ (a simple AND gate is used). BSTREQ asserted makes the DRAM controller to increment the column address every time $\overline{DTACK}$ negates. The DRAM controller will automatically assert $\overline{CAS}$ to latch the new column address into memory. $\overline{CAS}$ precharge is guaranteed by the on-board delay line, and in this design it is programmed to be 10 ns minimum. The DP8441 will burst for as long as BSTREQ is asserted. Every burst access finishes with the assertion and negation of $\overline{DTACK}$.

REFRESH AND PRECHARGE

The DP844l will request a memory refresh every 15 μs. During refresh, $\overline{RAS}$ will be low for 3 clock periods. The controller will also guarantee precharge of 3 clock periods. These timings are enough for 70 ns DRAMs. If the controller is in the middle of a page mode access ($\overline{RAS}$ asserted but no

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real access may be in progress) the controller will keep track of all missed refresh requests. When there is an access out of page, the DRAM controller will burst refresh the memory the number of refresh requests missed. If the in-page access is idle and there is a sixth refresh request, the DRAM controller will automatically finish the access, meet the precharge time, and burst refresh the memory six times.

PROGRAMMING BITS

TABLE I.

R1, R0 0, 1	RAS Low and Precharge Time 3Ts
R3, R2 0, 1	$\overline{\text{DTACK}}$ during Opening Access Will Assert after $\overline{\text{RAS}}$ 2Ts
R5, R4 0, 1	$\overline{\text{DTACK}}$ during Burst Access Will Toggle with $\overline{\text{CAS}}$ 1T
R7, R6 0, 1	$\overline{\text{DTACK}}$ during Page Access Will Assert after $\overline{\text{CAS}}$ 1T
R8, R9 1, 1	Page Size Select to 4096 for 16 Meg DRAMs
R11, R10 0, 1	Wrap around Size Select 4 (00 01 10 11)
C3, C2, C1, C0 0, 1, 0, 0	Divisor Select for DELCLK to Get Close to 2 MHz 15(30/16 = 2)
C5, C4 1, 1	B0 Is Not Used. Staggered Refresh B1 = 1 $\rightarrow$ RAS 0,1 CAS 0,1,4,5 B1 = 1 $\rightarrow$ RAS 2,3 CAS 2,3,6,7

TABLE I. (Continued)

C6 0	Staggered Refresh Selected
C7 0	t_{RAH} = 10 ns
C8 1	Page Miss Output Selected
C9 0	CAS Precharge Time during Burst 1/2T during Read and 1T during Write
C10 0	RAS Only Refresh Selected
C11 0	15 μs Refresh Period
B0 1	DTACK Rising Edge Increments the Column Counter
B1	Page Mode Selected
ECAS0 0	Latch Mode Selected to Be Able to Increment the Column Counter during Burst
ECAS1 1	Burst Request Select Is Active High
ECAS2 0	CAS and DTACK Clock Edge Select Is the Rising Clock Edge

TIMINGS FOR THE 68040 AND THE DP8440/41 INTERFACE DRAM CONTROLLER RUNNING AT 33 MHz

(1) Minimum $\overline{ADS}$ Low Setup Time to CLK High.

1 CLK Period −CLK High to $\overline{TS}$ Asserted (68040)

30.3 ns − 19 ns

11.3 ns The DP8440/41 need only 6 ns

(2) Minimum Address Valid Setup Time to CLK High.

1 CLK Period −CLK High to Address Valid (68040)

30.3 ns − 19 ns

11.3 ns The DP8440/41 need only 10 ns

(3) Minimum $\overline{CS}$ Asserted Setup Time to CLK High.

1 CLK Period − (CLK High to Address Valid + Decoder Delay)

30.3 ns − (19 ns + 7 ns)

30.3 ns − 26 ns

4.3 ns The DP8440/41 need only 4 ns

(4) Wait States through $\overline{TA}$ during Opening Accesses.

(4a) Access Time from RAS

1 CLK Period + CLK High to RAS Asserted (DP8440/41) + DRAM t_{RAC} + Data Setup Time (68040)

30.3 ns + 15 ns + 70 ns + 5 ns

120.3 → 4 CLK Periods (121.2 ns)

(4b) Access Time from CAS

1 CLK Period + CLK to CAS Asserted (DP8440/41) + DRAM t_{CAC} + Data Setup Time (68040)

30.3 ns + 55 ns + 20 ns + 5 ns

110.3 ns → 4 CLK Periods (121.2 ns)

(4c) Access Time from Column Address Valid

1 CLK Period + CLK High to Column Address Valid (DP8440/41) + DRAM t_{AA} + Data Setup Time (68040)

30.3 ns + 51 ns + 35 ns + 5 ns

121.3 ns → 4 CLK Periods (121.2 ns)

From 4a, 4b and 4c, $\overline{DTACK}$ should assert from the 3rd rising CLK edge. Therefore program $\overline{DTACK}$ during opening accesses as 2T.

(5) $\overline{TA}$ Setup Time (68040)

1 CLK Period − $\overline{DTACK}$ Asserted from CLK High

30.3 ns − 12 ns

18.3 ns The 68040 needs only 10 ns

(6) /CAS Precharge during Burst Accesses

Program the DP8440/41 for ½T of CAS precharge. It will guarantee a minimum of 10 ns.

(7) Wait States through $\overline{TA}$ during Burst Accesses.

CLK High to CAS Negated + Max CAS Precharge (½T) + DRAM t_{CAC} + Data Setup Time (68040)

12 ns + 14 ns + 20 ns + 5 ns

41 ns → 2 CLK Periods (60.6 ns), needs 1 Wait State

(8) Wait States through $\overline{TA}$ during Page Accesses

1 CLK Period − (CLK High to CAS Asserted + DRAM t_{CAC} + Data Setup)

30.3 ns − (12 ns + 20 ns + 5 ns)

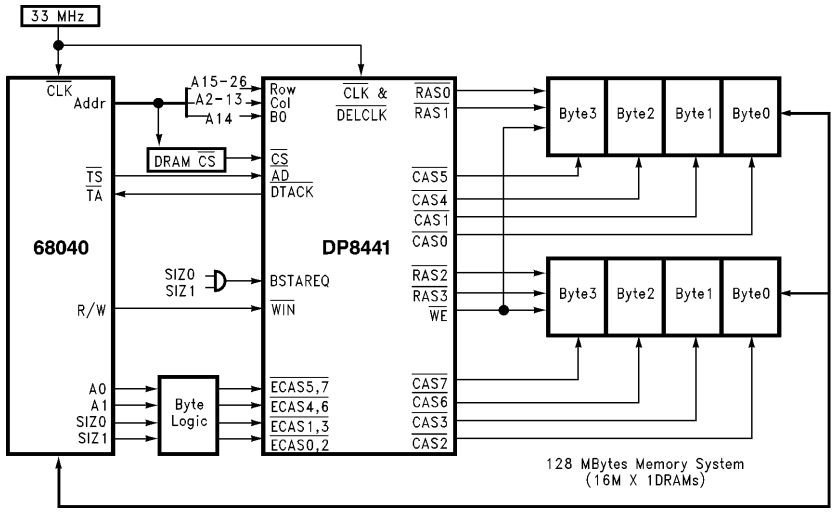
−6.7 ns → 1 Wait State. Page Accesses take 3 CLKs

(9) RAS Low during Refresh

Program the DP8440/41 for 3T of refresh to guarantee 70 ns t_{RAS}. Same number of CLKs for precharge.

Note: The timing analysis was done with preliminary AC specs, prior to final characterization of the DP8440/41. The reader is required to check AC timing from the latest DP8440/41 data sheet.

Interfacing the 68040 and the DP8441 DRAM Controller



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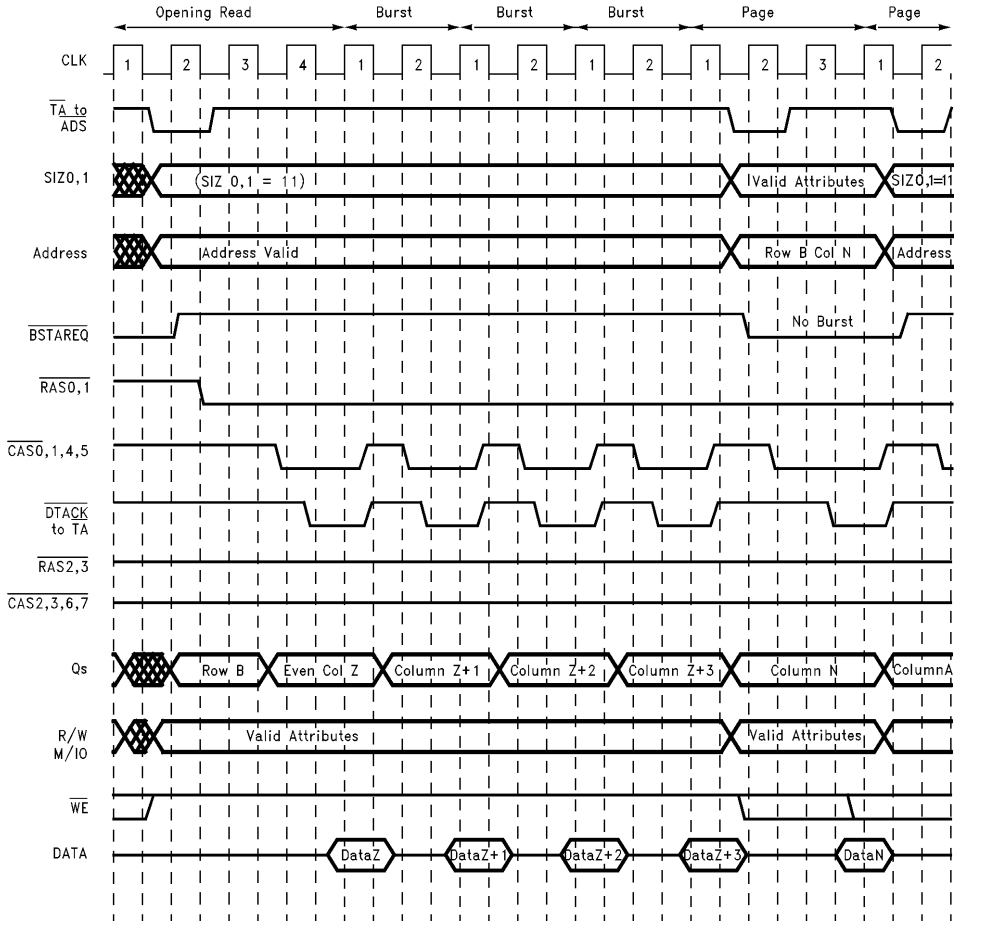
68040 Opening, Burst and Page Accesses,
4-2-2-2 and 3 Ts



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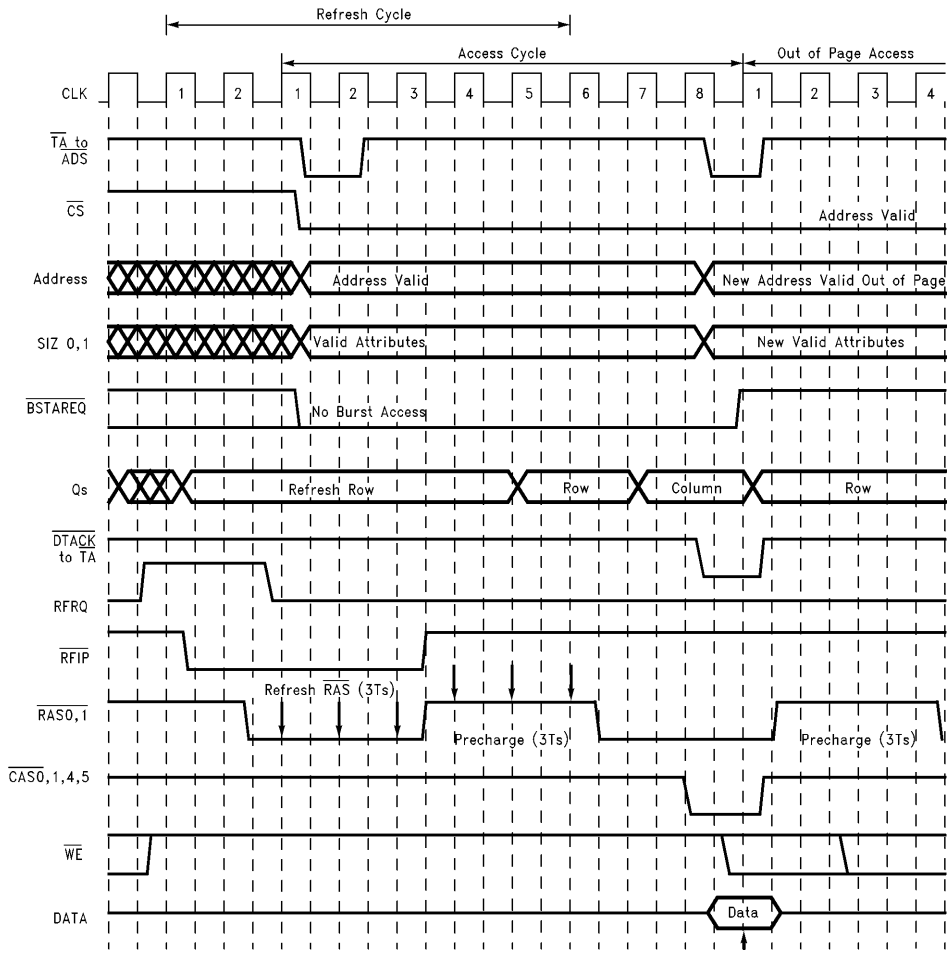
Refresh Cycle and Delayed Access



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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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