DP83902EB-AT PC-AT® Compatible DP83902 ST-NIC™ Ethernet Evaluation Board

National Semiconductor
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OVERVIEW

The National Semiconductor ST-NIC Evaluation Board design provides IBM® AT's and AT Compatibles with Thick Ethernet, Thin Ethernet, and Twisted Pair connections. This low parts count Evaluation Board is compatible with the AT bus and requires only a ½ size slot for insertion. The board uses the DP83902 (ST-NIC) to interface to twisted pair Ethernet. The ST-NIC also has an AUI Port which allows interface to thick wire Ethernet, or thin wire Ethernet by the addition of the DP8392 Coaxial Transceiver Interface (CTI). The dual DMA (local and remote) capabilities of the ST-NIC, along with 16 Kbytes of buffer RAM, allow the entire Network Interface Adapter to appear as a standard I/O Port to the system. The NIC module's local DMA channel buffers packets between the local memory (16 Kbytes of buffer RAM) and the network, while the NIC module's remote DMA channel passes data between the local memory and the system by way of an I/O Port. This I/O Port architecture which isolates the CPU from the network traffic proves to be the simplest method to interface the DP83902 to the system.

HARDWARE FEATURES

- Half-size IBM PC-AT I/O Card Form Factor
- Utilizes DP83902 Serial Network Interface Controller for Twisted Pair (ST-NIC)
- 16 Kbyte on-board Packet Buffer
- Simple I/O port interface to IBM PC-AT
- Interfaces to Thick Ethernet, Thin Ethernet, and Twisted Pair
- Boot EPROM Socket

The detailed schematics for this design are shown at the end of this document.

NETWORK INTERFACE OPTIONS

The evaluation board supports three physical layer options: Thick Ethernet, Thin Ethernet, and Twisted Pair. The block diagram for these interfaces can be seen in *Figure 1*. When using Thick Ethernet, a drop cable is connected to an external transceiver which is in turn connected to a standard Ethernet network, eliminating the need for an internal transceiver. This configuration may be obtained by connecting the pins on JB3 while leaving JB2 open, and connecting JB9 (AUTP) to V_{CC}.

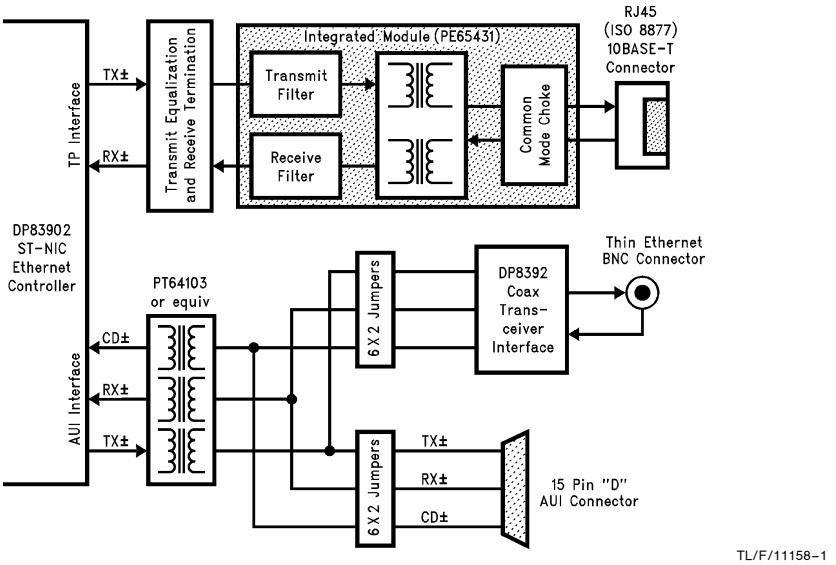

FIGURE 1. Physical Layer Adapter Interface Block Diagram

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When using Thin Ethernet, a transceiver (the CTI) is available on-board to allow the evaluation board to directly connect to the network. This transceiver (the CTI) forms the link between the differential ECL signals of the SNI module and the non-differential ECL signal of the thin-wire coaxial cable. A DC-DC Convertor is provided on the board to supply the CTI with −9V isolated voltage source. The Thin Ethernet solution is made by connecting the pins on JB2, leaving JB3 open and JB9 (AUTP) should be connected to V_{CC}.

When using the Twisted Pair, JB9 (AUTP) needs to be connected to ground. The ST-NIC allows direct connection to the network using the RJ-45 phone jack. The remaining circuitry includes pre-emphasis resistors, a filter, a transformer/filter and a common mode choke. The transformer/filter decouples the DC component and eliminates any possible voltage spikes.

The diagram in *Figure 2* illustrates the layout of the board. It shows the various jumpers, ICs, LEDs, and the connectors for the three physical layer options. The transmit pre-emphasis resistors R27–R30 provide equalization to the twisted pair transmit outputs. This boosts the higher harmonics of the signal in order to compensate for losses in these harmonics over the twisted pair cable. R19 and R20 are 50Ω each and when combined form the required 100Ω termination on the receive side.

BUS INTERFACE

The block diagram, *Figure 3*, illustrates the architecture of the ST-NIC Evaluation Board. The ST-NIC Board as seen by the system appears only to be an I/O port. With this architecture the ST-NIC board has its own local bus to access the board memory. The system never has to intrude further than the I/O ports for any packet data operation. This I/O architecture isolates the system bus and the local bus, thereby preventing interference by the system when the ST-NIC is doing real-time accesses such as transmitting and receiving packets.

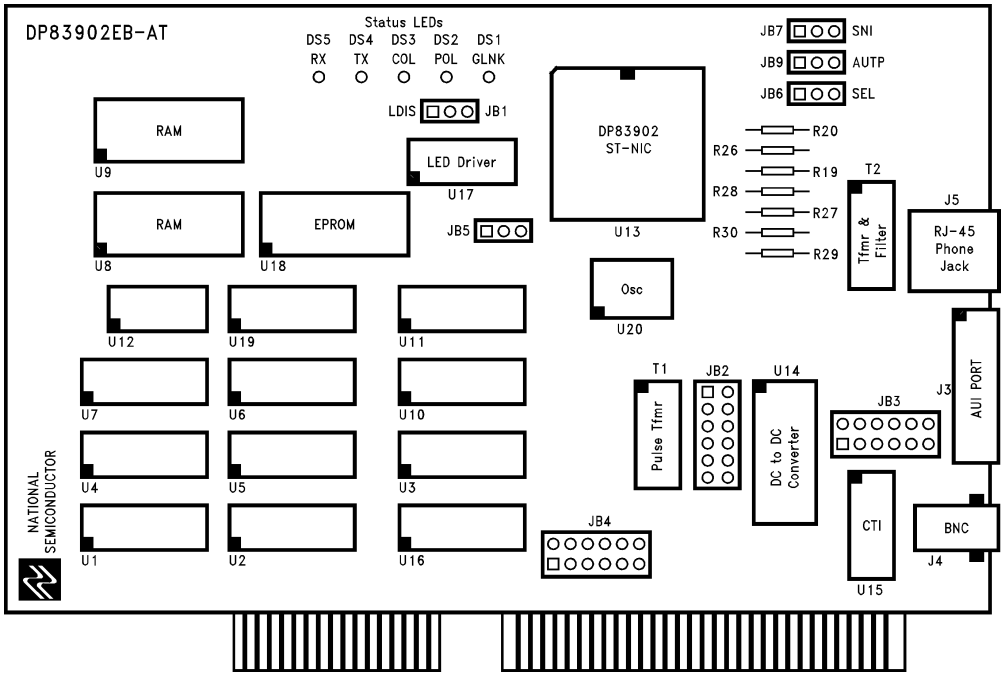

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FIGURE 2. Layout of ST-NIC Evaluation Board

BOARD ARCHITECTURE

I/O Map of ST-NIC Board

The ST-NIC Board requires a 32-byte I/O space to allow for decoding the data buffers, the reset port, and the ST-NIC registers. The first 16 bytes (300h–30Fh) are used to address the ST-NIC registers (8 bits wide) and the next 8 bytes (310h–317h) are used to address the data buffers which are 16 bits wide. Finally, the reset port (also software selectable) may be addressed by 318h–31Fh.

TABLE I. I/O MAP in PC-AT

Address	Part Addressed
300h–30Fh	ST-NIC Chip Select
310h–317h	Data Buffers
318h–31Fh	Reset

Although in the description above the I/O map is positioned at the addresses 300–31F, it may also be placed in the following address spaces: 320–33F, 340–35F, 360–37F. These alternate address spaces may be selected by the two jumper pins JP1 and JP0 (refer to JB4 in *Figure 4* and Appendix A).

DP83902's Local Memory Map

There are only two items mapped into the local memory space. These two items being the 8K x 16 buffer RAM and the ID address PROM. The buffer RAM is used for temporary storage of transmit and receive packets.

TABLE II. ST-NIC's Local Memory Map

7FFFh	RAM
4000h	
3FFFh	PROM
0000h	

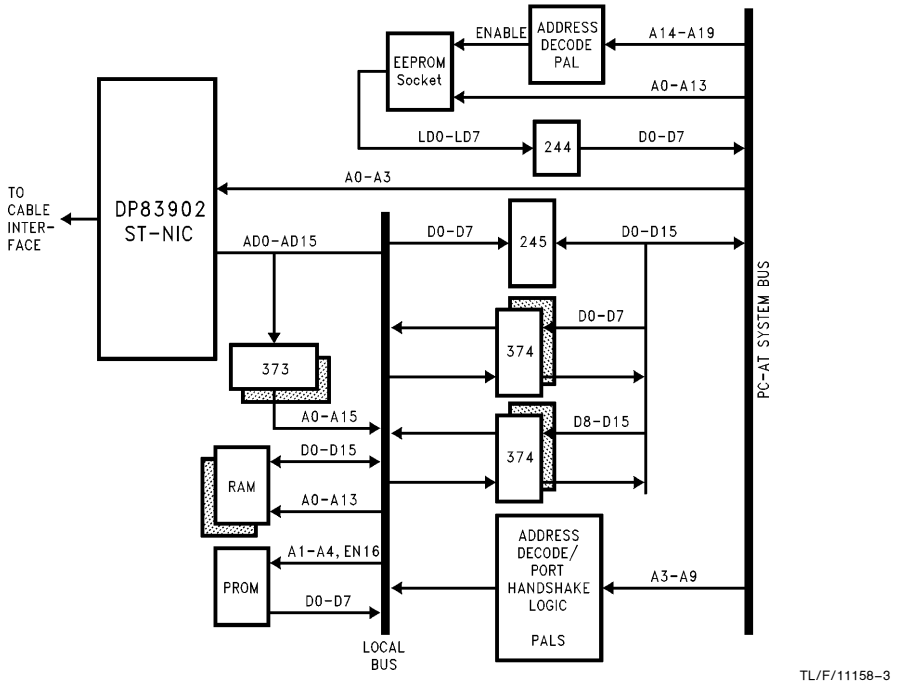

FIGURE 3. Block Diagram of ST-NIC Evaluation Board's System Interface

For transmit packets, the remote DMA puts data from the I/O ports into the RAM and the local DMA moves the data from the RAM to the ST-NIC. For the receive packets, the local DMA carries the data from the ST-NIC to the RAM and the remote DMA moves the data from the RAM to the I/O ports. The ID address PROM (74S288 32 x 8) contains the physical address of the evaluation board. Each PROM holds its own unique physical address which is installed during its manufacture. The PROM also contains some identification bytes that can be checked by the driver software. At the initialization of the evaluation board the software commands the ST-NIC to transfer the PROM data to the I/O Port where it is read by the CPU. The CPU then loads the ST-NIC's physical address registers. The following chart shows the contents of the PROM.

TABLE III. PROM Contents

PROM Location	Location Contents
00h	Ethernet Address 0 (Most Significant Byte)
01h	Ethernet Address 1
02h	Ethernet Address 2
03h	Ethernet Address 3
04h	Ethernet Address 4
05h	Ethernet Address 5
06h–0Dh	00h
0Eh, 0Fh	57h
10h–15h	Ethernet Address 0 thru 5
16h–1Dh	Reserved
1Eh, 1Fh	42h

Data and Address Paths

For the following paragraph, refer to the block diagram shown in *Figure 3*. Twenty address lines from the PC go onto the ST-NIC Board, but only four of them actually go to the ST-NIC. These four addresses along with the NIOR (low-asserted I/O read) or NIOW (low-asserted I/O write) and the CS (ST-NIC chip select signal) allow the PC to read or write to the ST-NIC's registers. If the system wants to read from or write to the ST-NIC registers, the data (only 8 bits) must pass through the 245 buffer. All of the packet data will pass through the I/O ports (the 374's). Each 374 is unidirectional and can only drive 8 bits, therefore it is necessary to have four 374's. Two of which drive data from the ports to the board memory and two of which drive the data from the ports to the AT bus. Even the PROM, which can only be addressed by the ST-NIC, sends its 8 bits of data out through the 374's. When the PROM does this, two of the 374's will be enabled but only the lower 8 bits will be read by the system. The RAM is also accessed by the ST-NIC. However, it is addressed by 14 bits and drives out 16 bits of data. The PALs receive 7 address lines among many other signals such as NIOR, NIOW, NACK, MRD, etc. With these signals the PALs do all of the decodes, such as selecting the ST-NIC Board, the ST-NIC chip, the RAM, and the PROM.

EPROM SOCKET

The EPROM socket is provided so that the user may add an EPROM to the system. This EPROM would normally contain a program and a driver to enable the PC-AT to be booted up through the network. The chips necessary to interface the EPROM to the system are the 27128 (EPROM), a 16L8 (PAL), and a 74ALS244 (buffer). Also, JB5 must be placed in the proper selection as described in the jumper section. The PAL decodes SA14–SA19, along with SMRDC (system memory read), in order to generate the EPROMEN signal. This signal, issued when the PC wants to execute the program stored in the EPROM, enables the EPROM and the 244 buffer.

EVALUATION BOARD OPERATION

The following pages will describe the slave accesses to the ST-NIC and the local DMA and remote DMA operation.

Register Operations

Accesses to the board are register operations to the DP83902, which are done to set up the ST-NIC and to control the operation of the ST-NIC's DMA channels.

REGISTER READ

To begin the register read, the CPU drives the four address lines (SA0–SA3) to the ST-NIC and the SA3–SA9 address lines to the PAL. These address lines are decoded by the PAL in order to generate a chip select to the ST-NIC. The CPU also drives the NIOR line which the ST-NIC sees as the NSRD (slave read). Once the ST-NIC receives this NSRD, it then sends out a high assertion on NACK, acknowledging that it is in slave mode but not yet ready to complete the read. The NACK signal is used by the PAL to assert the IOCHRDY (used to insert wait states) signal false. The ST-NIC then drives out the data from its internal registers to the 245 buffer. The 245 buffer is then enabled and the data is driven onto the AT BUS. When the ST-NIC is ready, it asserts NACK true and the PAL asserts IOCHRDY true. As a result, NIOR is driven high by the CPU, thereby deasserting the NSRD. On the rising edge of the NIOR, the data which is on the AT BUS is latched into the system. The addresses are removed at the same time, causing the ST-NIC chip select to become deasserted, ending the register read cycle.

REGISTER WRITE

To begin the register write, the CPU drives the SA0–SA3 address lines to the ST-NIC and the SA4–SA9 address lines to the PAL. With these address lines, the PAL decodes to 300–30F (the ST-NIC registers) thereby enabling the chip select for the ST-NIC. The CPU then drives the NIOW strobe which the ST-NIC sees as NSWR (slave write). Once the ST-NIC receives this NSWR it sends back a low assertion on NACK to acknowledge that it is in slave mode and ready to perform the write. When the CPU receives this signal, it puts data out onto the AT BUS where it goes into the 245 buffer. The 245 buffer then drives the data to the ST-NIC, but the data is not latched into the ST-NIC until the rising edge of NIOW. The system drives NIOW high, thereby deasserting the NSWR and latching the data. The addresses also are taken away and the chip select then goes high (deasserted). This ends the cycle of the register write.

Remote Transfers

Remote DMA transfers are operations performed by the ST-NIC on the board. These operations occur when the ST-NIC is programmed to transfer packet data between the PC-AT and the card's on-board RAM. These transfers take place through the I/O Port interface.

REMOTE READ

To program the ST-NIC for a remote read, the CPU must make five slave accesses to the ST-NIC. The CPU must write the Remote Start Address (2 bytes), the Remote Byte Count (2 bytes), and issue the Remote DMA Read Command. The addresses and byte count require two transfers because they are both 16 bits, yet only 8 bits can be written per transfer.

Once the ST-NIC has received all of the above data, it drives out BREQ and waits for BACK. The ST-NIC immediately receives BACK because it is tied to the BREQ line. (BREQ can be tied to BACK because there are no other devices contending for the local bus.) After receiving BACK, the ST-NIC drives out the address from which the data is required to be read. This address flows into the 373's and is latched by ADS0. From here, the address flows to the RAM. The RAM waits until it receives MRD from the ST-NIC and then it drives the data into the 374 ports. The 374 ports then latch the data on the rising edge of the PWR strobe from the ST-NIC. PRQ is then sent out by the ST-NIC to let the system know that there is data waiting in the ports.

If the AT reads the I/O ports before the ST-NIC has loaded the 374's, then the port request (PRQ) from the ST-NIC will not yet be driven. This unasserted PRQ signal causes the AT's ready line to be set low, indicating that the ST-NIC has yet to load the data. After the data is in the ports, the system must then read the 374 data ports. This begins with the AT driving out an address which is decoded (inside the PAL) to the data I/O Ports (310–31F). The PAL then drives RACK to the ST-NIC, indicating that the CPU is ready to accept data. This RACK signal then reads the data from the 374 ports onto the AT BUS. The system deasserts NIOR which finishes the cycle.

REMOTE WRITE

Like the remote read, the remote write cycle also begins with five slave accesses into the internal registers. The CPU must write the Remote Start Address (2 bytes), the Remote Byte Count (2 bytes), and issue the Remote DMA Write Command. The ST-NIC then issues a PRQ. The CPU responds by sending an NIOW, indicating that it is ready to write to the ports. The CPU also drives out the address which corresponds to the I/O Ports. This address goes into the PAL and helps to decode to WACK. This WACK signal latches the data into the 374 ports The ST-NIC issues a BREQ and immediately receives a BACK since the two lines are tied together. (BREQ can be tied to BACK because there are no other devices contending for the local bus.) The ST-NIC, upon receiving the BACK, drives out address lines to the 373's. These address lines are latched by ADS0 and then are driven to the RAM. ST-NIC sends out a PRD and a NMWR which drives the data from the 374 ports into the already specified address of the onboard memory. PRD and NMWR are then deasserted and the cycle ends.

Network Transfers

Transfers to and from the network are controlled by the DP83902's local DMA channel which transfers packet data to/from the ST-NIC's internal FIFO from/to the card buffer's RAM.

RECEIVE

The data comes off of the network, is deserialized and is stored in the FIFO inside of the ST-NIC. The ST-NIC then issues a BREQ and immediately receives BACK since the lines are tied together. After receiving BACK, the ST-NIC drives the address lines to the 373's. The 373's are latched by ADS0 and the address is allowed to flow to the RAM. Then the ST-NIC drives out NMWR along with the data from the FIFO. The data flows into the RAM under the address given earlier. The NMWR strobe is then deasserted, ending the cycle.

TRANSMIT

To begin the transmit cycle, the ST-NIC issues a BREQ and waits for the BACK. Since the BREQ and BACK lines are tied together, the BACK signal is received immediately. Upon reception of this signal, the ST-NIC drives out the address to the 373's which latch the address with the ADS0 strobe. The address then flows to the onboard memory. NMRD, driven by ST-NIC, causes the RAM to drive the data out of the given address and into the ST-NIC. The ST-NIC then latches the data into the FIFO on the rising edge of NMRD. This high assertion of NMRD signifies the ending of this cycle. From the FIFO, the data is serialized and transmitted onto the network.

BOARD CONFIGURATION

On the DP83902EB-AT ST-NIC AT board, there are nine jumper blocks as seen in the diagram below. The following pages wiill explain how to configure these jumpers.

Physical Layer

If JB9 is tied to Ground then the twisted pair interface will be selected. If JB2 is closed while JB3 is open, and JB9 is connected to V_{CC}, then the Thin Ethernet option will be selected. And finally if JB3 is closed while JB2 is open, and JB9 is high, then the Thick Ethernet option will be selected. Refer to Appendix A for Jumper settings.

Interrupt Lines, Board Addresses, and EPROM Addresses

On JB4, there are six possible connections. Four of these are to select an interrupt line. The available interrupt lines include INT3, INT4, INT5, and INT9. The last two possible connections, JP1 and JP0, are used to select the base address for the board. However, if JB5 is connected to V_{CC}, then these last two connections select the address of the EPROM also. The possible selections and the jumpers are shown in Appendix A. The factory configuration uses the INT3 line for interrupts and has JP1 and JP0 in the on position.

This factory configuration is shown in *Figure 4*, along with the factory configurations for JB1, JB5, JB6, JB7, JB8, and JB9. The square pin indicates pin 1 of the jumpers.

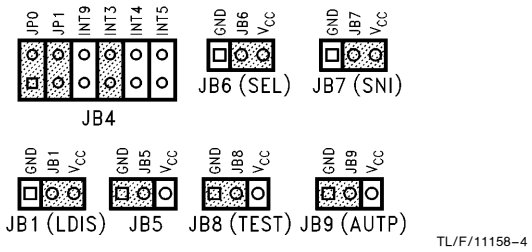

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FIGURE 4. Factory Configuration for JB1, JB4, JB5, JB6, JB7, JB8 and JB9

APPENDIX A

The following tables show all of the various jumper settings. The shaded boxes are the Factory Configuration default settings.

JB1	**High**	**Link Enabled**
	Low	Link Disabled
JB5	High	EPROM Address
	Low	**Base Address**
JB6	**High**	**Tx+ and Tx− are same in idle state**
	Low	Tx+ is positive with respect to Tx− in idle state
JB7	**High**	**Normal Operation**
	Low	ENDEC Module Testing
JB8	High	Internal Function Testing
	Low	**Normal Operation**

JP1	JP0	Base Address	EPROM Address
On	**On**	**300h–31Fh**	C800h
On	Off	320h–33Fh	CC00h
Off	On	340h–35Fh	D000h
Off	Off	300h–37Fh	D400h

JB9	JB2	JB3	Physical Layer Selected
Low	**X**	**X**	**Twisted Pair**
High	On	Off	Thin Ethernet
High	Off	On	Thick Ethernet

INT9	INT3	INT4	INT5	Interrupt Selection
On	Off	Off	Off	Interrupt 9
Off	**On**	**Off**	**Off**	**Interrupt 3**
Off	Off	On	Off	Interrupt 4
Off	Off	Off	On	Interrupt 5

APPENDIX B: PAL® EQUATIONS

PAL # 1 (U1)

In this first PAL, the output signals are NIO16, NIOEN, NSTNICB, and NCSROM. (The N's before the signals indicate that the signal is low asserted.) Since it is necessary to assert NIO16 as soon as possible, this first PAL has been selected to be a 10 ns "D" PAL. The NIO16 signal must be TRI-STATE® when it is not asserted. Therefore, we use an enable signal (NIOEN) which is equal to the decode for the I/O Ports (310–31F) and NAEN high (NAEN high signifies that the system DMA does not have control of the bus). The enable signal (NIOEN) loops back into the PAL to bring NIO16 out of TRI-STATE. The NIO16 signal is set to zero so that whenever it is enabled it will be asserted.

The STNICB signal consists of simple address decodes along with NAEN. The addresses decode to one of four address slots which were mentioned earlier in the board configuration section. The NCSROM is a very simple signal as it consists only of AD14 and NMRD. AD14 comes from the ST-NIC and selects either the PROM (when low) or the onboard RAM (when high).

PAL 1

```
module iodec;
flag '-r1';
title '
date: 9/13/89
functions:
ST-NIC BOARD DECODE, IO16 DECODE, AND CHIP SELECT PROM';
u1 device 'p1618';

"input pins:
NEN16, NAEN, SA9        pin 1, 2, 3;
SA8, SA7, SA6           pin 4, 5, 6;
SA5, SA4, SA3           pin 7, 8, 9;
JP0, JP1, NMRD          pin 13, 14, 15;
A14                     pin 16;
"output pins:
NSTNICB, NIOEN, NIO16   pin 12, 17, 18;
NCSROM                  pin 19;

"constants
    X = .X.;
    Z = .Z.;

equations
NSTNICB = !(!NAEN & SA9 & SA8 & !SA7 & !SA6 & !SA5 & !JP1 & !JP0
          # !NAEN & SA9 & SA8 & !SA7 & !SA6 & SA5 & !JP1 & JP0
          # !NAEN & SA9 & SA8 & !SA7 & SA6 & !SA5 & JP1 & !JP0
          # !NAEN & SA9 & SA8 & !SA7 & SA6 & SA5 & JP1 & JP0);
NIOEN = !(!NAEN & SA9 & SA8 & !SA7 & !SA6 & !SA5 & !JP1 & !JP0
         & !NEN16 & SA4 & !SA3
       # !NAEN & SA9 & SA8 & !SA7 & !SA6 & SA5 & !JP1 & JP0
         & !NEN16 & SA4 & !SA3
       # !NAEN & SA9 & SA8 & !SA7 & SA6 & !SA5 & JP1 & !JP0
         & !NEN16 & SA4 & !SA3
       # !NAEN & SA9 & SA8 & !SA7 & SA6 & SA5 & JP1 & JP0
         & !NEN16 & SA4 & !SA3);
NCSROM = !(!A14 & !NMRD);
enable NIO16 = !NIOEN;
       NIO16 = 0;
end iodec;
```

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PAL #2

In this PAL there are eight outputs: NRESET, NSOUT, NRDYEN, NIOCHRDY, NCS, NRACK, NWACK and INTO. The first two outptus (NRESET and NSOUT) are part of an R–S flip flop as shown below:

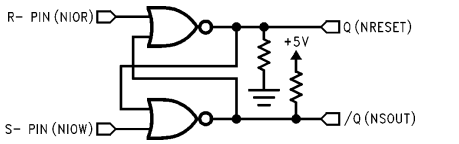

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FIGURE 5. RS Flip-Flop

NRESET is given by the NOR of the high asserted R-input pin and the NSOUT signal. NSOUT is given by the NOR of the high asserted S-input pin and the NRESET signal. The NOR gates are enabled by the low assertion of NRSTDRV. When the system first boots up, it will disable the NOR gates by asserting the RSTDRV signal. But due to the pull-up and pull-down resistors, the output <NRESET, NSOUT> will be set to <0, 1>. Once RSTDRV becomes deasserted, the output will remain at <0, 1>. The only way to get out of reset is to assert the S-pin high which is done by an NIOW and an address decode to 318–31F. After the system has booted up, the ST-NIC may be reset through software. This would be done by setting the R-pin high with an NIOR and an address decode to 318–31F. To escape from reset, we once again set the S-pin high with an NIOW and address decode of 318–31F. The above description of logic is also shown in Truth Table VII.

TABLE IV. R–S Flip Flop Truth Table

R (NIOR)	S (NIOW)	Q (NRESET)	$\overline{Q}$ (NSOUT)
0	0	0	1
0	1	1	0
0	0	1	0
1	0	0	1
0	0	0	1
0	1	1	0

By using the NIOR and NIOW which are never asserted at the same time, this insures that the R-pin and the S-pin will never be asserted at the same time. The next two signals (NRDYEN and NIOCHRDY) are quite similar to NIOEN and NIO16 in PAL#1. All of the decode takes place in the enable signal (NRDYEN). This decode consists of addresses 300–30F without NACK or the addresses 310–318 without PRQ. If the NRDYEN signal is asserted, then NIOCHRDY will be driven low. At all other times, the NIOCHRDY strobe will be in TRI-STATE. This PAL must also be a 10 ns ''D'' PAL.

NCS is decoded by NSTNICB (from PAL #1) along with the low assertion of SA4 and either NIOR or NIOW. Its decode is in the address range of 300–30F. The last two signals are NRACK and NWACK. NRACK occurs with an address decode to 310–318, an NIOR, and a PRQ. The NWACK signal only differs from the NRACK by the NIOR/NIOW signal and therefore consists of an address decode to 310–31F, an NIOW and a PRQ. INT is just sent through the PAL to be buffered. The buffered signal which comes out of the PAL is INTO.

PAL 2

```
module reset;
flag '-r1';
title '
date: 9/13/89
functions:
RESET LATCH, STNIC SELECT, IOCHRDY, RACK, WACK,
BUFFER INTERRUPT';
u2 device 'p16l8';

"input pins:
NSTNICB, NIOW, NIOR     pin 1, 2, 3;
RSTDRV, NACK, PRQ       pin 4, 5, 6;
SA4, SA3, INT           pin 7, 8, 9;

"output pins:
INTO, NRACK, NWACK      pin 12, 13, 14;
NRESET, NSOUT, NRDYEN   pin 15, 16, 17;
NIOCHRDY, NCS           pin 18, 19;

"constants
    X = .X.;
    Z = .Z.;

equations
NCS = !(!NSTNICB & !NIOR & !SA4 # !NSTNICB &!NIOW &!SA4);
NRACK = !(!NSTNICB & PRQ & !NIOR & SA4 & !SA3);
NWACK = !(!NSTNICB & PRQ & !NIOW & SA4 & !SA3);
NRDYEN = !(!NSTNICB & !NIOR & !SA4 & NACK
         # !NSTNICB & !NIOW & !SA4 & NACK
         # !NSTNICB & !PRQ & !NIOR & SA4 & !SA3
         # !NSTNICB & !PRQ & !NIOW & SA4 & !SA3);
enable NIOCHRDY =!NRDYEN;
       NIOCHRDY = 0;
enable NRESET = !RSTDRV;
       NRESET = !(!NSTNICB & !NIOR & SA4 & SA3 # NSOUT);
enable NSOUT = !RSTDRV;
       NSOUT = !(!NIOW # NRESET);
INTO = INT;
end reset;
```

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PAL #3

The third PAL only does a decode to enable the optional EPROM. This decode consists of an address decode to C800h, CC00h, D000h, or D400h depending on JP1 and JP0 as shown in the board configuration section. JP2 must also be jumpered for selection of the EPROM. NAEN, a low asserted signal should be high to indicate that the DMA does not have control of the bus and the NSMRDC signal should be asserted high since the CPU is doing a system memory read.

PAL 3

```
module epromdec;
flag '-r0';
title '
date: 9/13/89
function:
EPROM DECODE';

u16 device 'p16l8';

"input pins:

A0, A13, EN16           pin 1, 2, 3;
SMRDC, SA19, SA18       pin 4, 5, 6;
A17, SA16, SA15         pin 7, 8, 9;
A14, NAEN, JP2          pin 11, 13, 14;
P0, JP1                 pin 15, 16;

"output pins:

EPROMEN                 pin 19;
A013                    pin 12;

"constants
    X = .X.;

equations

NEPROMEN = !(SA19 & SA18 & !SA17 & !SA16 & SA15 & !SA14 & !NAEN
         & JP2 & !JP1 & !JP0 & !NSMRDC
      # SA19 & SA18 & !SA17 & !SA16 & SA15 & SA14 & !NAEN
         & JP2 & !JP1 & JP0 & !NSMRDC
      # SA19 & SA18 & !SA17 & SA16 & !SA15 & !SA14 & !NAEN
         & JP2 & JP1 & !JP0 & !NSMRDC
      # SA19 & SA18 & !SA17 & SA16 & !SA15 & SA14 & !NAEN
         & JP2 & JP1 & JP0 & !NSMRDC);

A013 = !(!A0 & EN16 # !A13 & !EN16);

end epromdec;
```

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APPENDIX C: BILL OF MATERIALS FOR DP83902EB-AT ST-NIC ETHERNET ADAPTER

CAPACITORS

C1, C20	.01 µF	50V	10%	Monolythic
C3	4.7 µF	25V	20%	Tantalum
C4	0.01 µF	1 KV	10%	Ceramic Disk
C5	0.01 µF	50V	10%	Ceramic Disk
C9..C10	0.01 µF	50V	20%	Monolythic
C11	0.75 pF	1 KV		Spark Gap
C12..C19	0.01 µF	50V	20%	Monolythic
C20	4.7 µF	25V	20%	Tantalum
C21	4.7 µF	25V	20%	Tantalum
C22..C29	0.01 µF	50V	20%	Monolythic
C30..C32	4.7 µF	25V	20%	Tantalum
C33..C37	0.01 µF	50V	20%	Monolythic
C38..C42	4.7 µF	25V	20%	Tantalum

RESISTORS

R1..R3	10K	1/4W	5%
R4..R6	4.7K	1/4W	5%
R7..R10	39.2	1/4W	1%
R11	1M	1/2W	5%
R12, R13	270	1/4W	5%
R14..R17	1.5K	1/4W	5%
R18	1K	1/4W	1%
R19..R20	TBD	1/4W	1%
R21	420	1/4W	5%
R22..R25	430	1/4W	5%
R26	4.7K	1/4W	5%
R27..R30	TBD	1/4W	1%
R31..R34	4.7K	1/4W	5%

IC's

U1, U2	16L8D	PAL
U16	16L8B	PAL
U3	74ALS245	
U4..U7	74ALS374	
U8, U9	HM6264	8K x 8 STATIC RAM 100 ns
U10, U11	74AS373	
U12	74S288	PROM
U13	DP83902	ST-NIC
U15	DP8392	CTI
U17	74HC04N	
U18	27128	EPROM (not supplied on board)
U19	74ALS244	
U20	20 MHz 0.01%	Crystal Oscillator

Note:

ETHERNET ID PROM ADDRESS ASSIGNMENT:
Registration Authority for ISO/IEC 8802-3
c/o The Institute of Electrical and Electronics Engineers
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08055-1331
(908) 562-3812

MAGNETICS (TRANSFORMER, FILTER, CHOKE, DC-DC CONVERTOR, ETC.)
See Section 5 of databook, Ethernet Magnetics Vendors

SPARK GAP SUPPLIERS:
0.75 pFkV Spark Gap

Mallory Part# ASR75A
(317) 856-3731

Mepco/Centralab Part# S758X44000NAZAA
Available from: Philips Components Discrete Product Division
(602) 820-2225

MAGNETICS

U14 PM7102 VALOR DC-DC Convertor.
T1 PE64103 Pulse Engineering
T2 RX and TX Filter & Transformer. Pulse Engineering PE65431.

MISCELLANEOUS

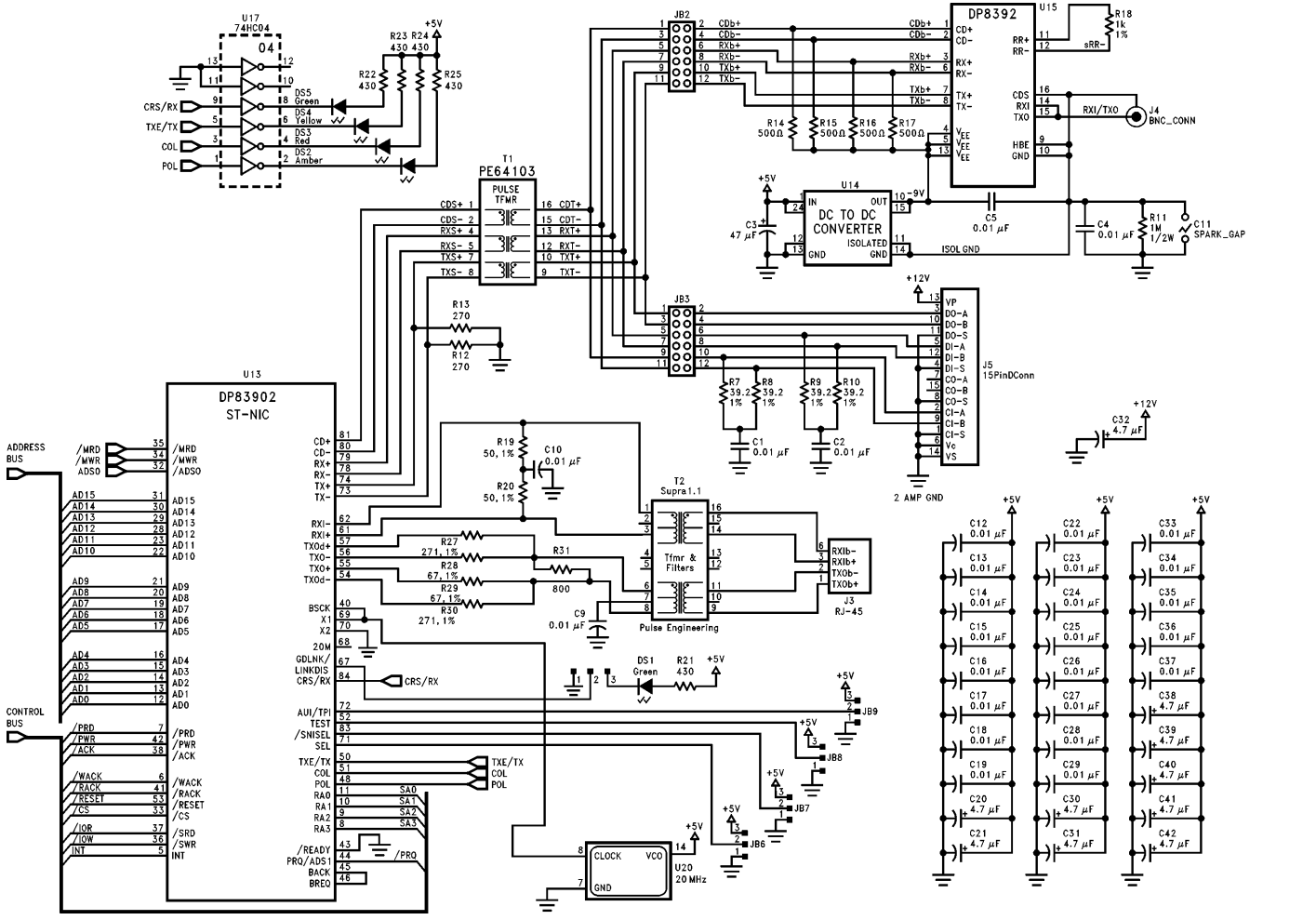
DS1	GREEN	5mm LOW CURRENT LED	CURRENT=I_F=3.5m
DS2	AMBER	5mm LOW CURRENT LED	CURRENT=I_F=3.5 mA
DS3	RED	5mm LOW CURRENT LED	CURRENT=I_F=2.0 mA
DS4	YELLOW	5mm LOW CURRENT LED	CURRENT=I_F=2.0 mA
DS5	GREEN	5mm LOW CURRENT LED	CURRENT=I_F=3.5 mA
JB1	1x3	SHUNT BLOCK WITH .1" SPACING BETWEEN PINS	
JB2	2x6	SHUNT BLOCK WITH .1" SPACING BETWEEN PINS	
JB3	2x6	SHUNT BLOCK WITH .1" SPACING BETWEEN PINS	
JB4	2x6	SHUNT BLOCK WITH .1" SPACING BETWEEN PINS	
JB5-JB9	1x3	SHUNT BLOCK WITH .1" SPACING BETWEEN PINS	

SOCKETS/MECHANICAL

S1-S3	20 PIN	0.3" DUAL IN-LINE FOR U1, U2, U16 (PAL)
S4	28 PIN	DUAL IN-LINE SOCKET FOR U18 (EPROM)
S5	84 PIN	PLCC SOCKET FOR U13 (ST-NIC) AMP SOCKET
S8	BRACKET FOR MOUNTING IN PC-AT, SLOT	
	G44 Basic Blank,	
J3	RJ-45 CONNECTOR AMP 520252-4	
J4	BNC CONNECTOR RT/A Low Pro Amp 227161-7	
J5	15 PIN D CONNECTOR Female AMP 747247-4 (or 747845-4)	
	MAXCON SUB D Slide Lock MDA 51220-1	

BOARD ATTACHMENT COMPONENTS

1) Screw: Bind Head Slotted 4-40 x .250, Steel, (90277A106)
2) Washer: Lock Ext #4, Zinc/Steel, (91114A005)
3) Washer: Flat #4, Zinc-CRS, (90126A005)



TL/F/11158–11

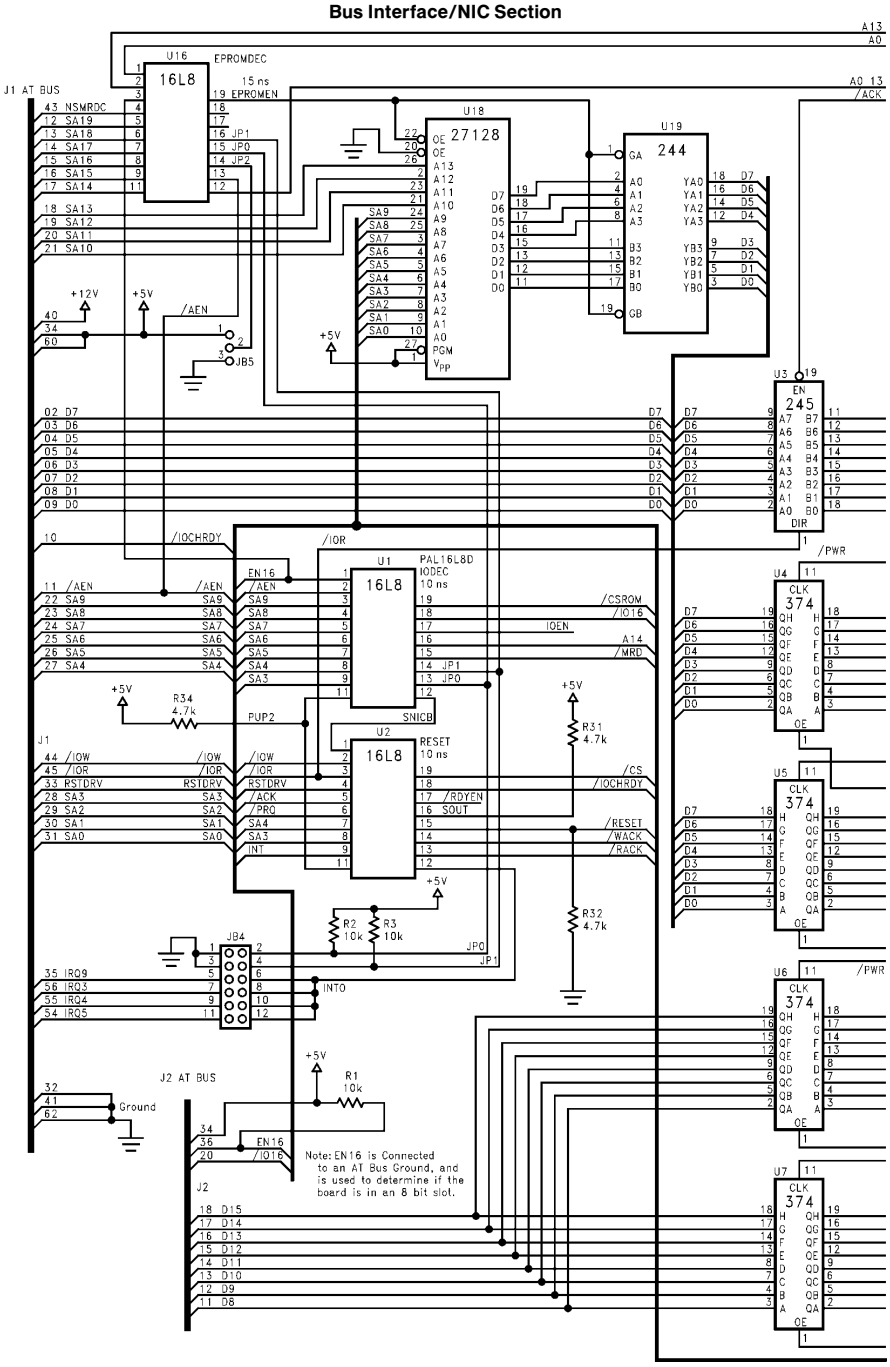
Note: All resistors to be 5%, ¼W unless otherwise indicated

Note: Capacitors 39 to 42 are for the V_{CC} signals off of the AT Bus.

DP83902EB-AT PC-AT Ethernet Evaluation Board

APPENDIX D

Bus Interface/NIC Section

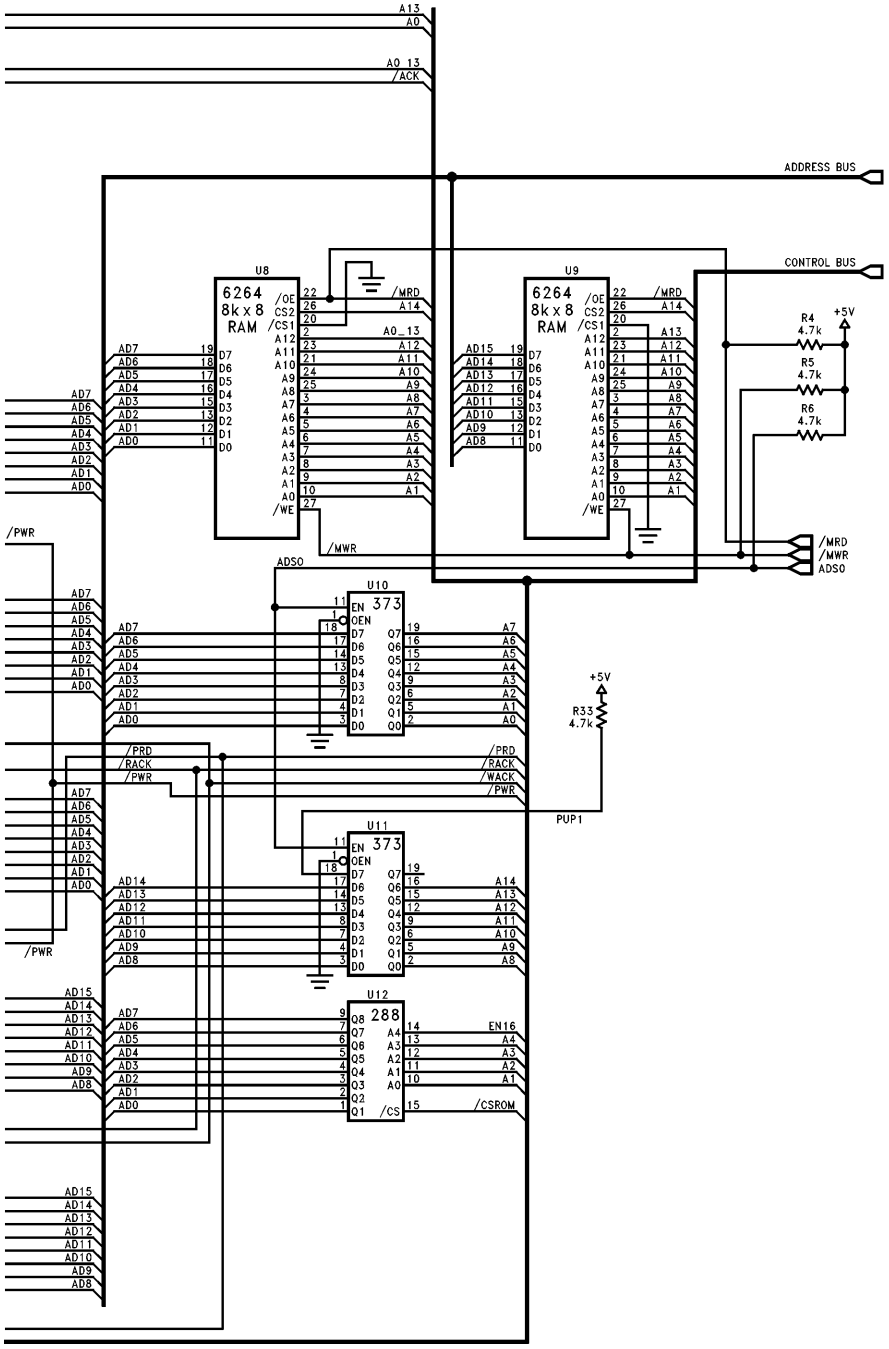


TL/F/11158–9

Note: All resistors to be 5%, ¼W unless otherwise indicated

Note: EN16 is actually a ground signal on the AT Bus J2 Connector. This signal is used to determine whether 8- or 16-bit mode should be used.

DP83902EB-AT ST-NIC Ethernet Evaluation Board Schematic
(Bus Interface/NIC Section)



TL/F/11158–10

DP83902EB-AT ST-NIC Ethernet Evaluation Board Schematic (Continued)
(Bus Interface/NIC Section)

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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