Signals in the Futurebus+ Backplane

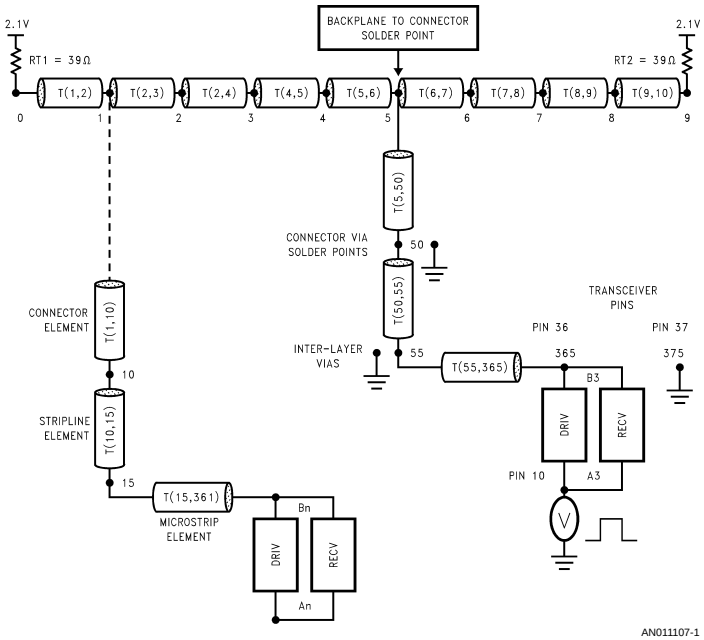
National Semiconductor
Application Note 738
Stephen Kempainen
January 1991

The Futurebus+ backplane is a complex electrical environment that consists of many circuit elements. The modeling of such an environment can become time consuming and expensive. The Futurebus+ Electrical Task Group Expert Team has detailed the circuit elements in their SPICE simulation. An average Futurebus+ simulation contains over 10,880 individual elements and gobbles 8 CPU hours on a single user VAX 8650. This note is an attempt to simplify the circuit model and gain an intuitive understanding of interactive signal path elements. The elements are investigated by probing at individual impedance breaks that are considered significant. Waveforms of the signal will be correlated with the TDR signals from the same signal paths. An investigation of ground signal variations and crosstalk measurements is included because of relevance to signal measuring in this environment. The relation between the crosstalk, ground bounce and the signal path impedance will be pursued to see their combined effect on the noise margin.

The interconnect effects on the electrical signal become critical in high speed multilayer board design such as Futurebus+. PCB traces must be treated as transmission lines due to the rapid transition times of the signal. Analyzing PCB traces uncovers the impedance mismatches caused by seemingly harmless corner geometries, parasitic and crossover effects, and inter-layer vias. The impedance mismatches also affect crosstalk coupling and signal reflections which are a major concern due to the large chunk of noise margin they may consume. To demonstrate how these circuit elements affect the signal, this article will follow a signal from the transceiver as it propagates into the backplane.

FUTUREBUS+ BACKPLANE AND BOARD MODEL

Figure 1 models the signal path from a transceiver in one board, through the backplane, to a transceiver in another board. Both of the boards are mounted in a ten slot backplane. The dashed line to one module indicates it can be removed or moved around to different locations for this analysis. It is the receiver and it is seen as a load by the driver module. To first emphasize the driver module stub effects alone, the receiver is not inserted into the backplane. This focuses the driver response to only the transmission line elements. This model can be generalized to any backplane. However, it is derived from specific equipment used to obtain these waveforms. The backplane is provided by Bicc-Vero Electronics, No. 819-304105E. It uses 39Ω, surface mount, termination resistors and has a 1 inch spacing between the slots (soft metric). The board is provided by Hybricon. It is a Futurebus+ Wire-Wrappable Board 6U x 280mm. The part number is 031-126-10. The board is laid out (eight layers) for the National Semiconductor Futurebus+ Chip Set transceivers and can accommodate 64 data bits.



Model of the Futurebus+ backplane with two daughter boards; one in slot 1, and one in slot 5 with an input signal at pin 10.

FIGURE 1.

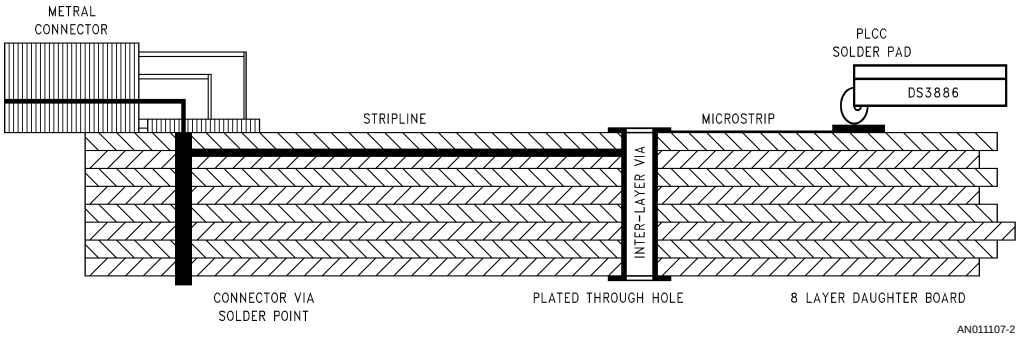


FIGURE 2. Eight Layer Daughter Board, Side View

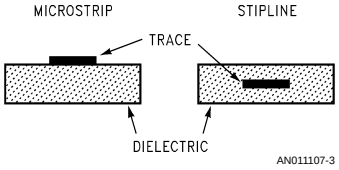


FIGURE 3. PCB Track Cross Section

Figure 2 is a cross section of the Hybricon board showing the signal path of the DS3886 Latched Data Transceiver, pin-36. The illustration emphasizes the physical impedance differences of the transmission path elements. Examination of the Time Domain Reflection response of the signal path is a good way to "electrically see" these differences.

TIME DOMAIN REFLECTION

TDR uses a step generator to apply a positive going impulse to the signal path being investigated. The step has a very fast rise time of 35 ps and a 200 mV amplitude. The step travels down the path at the propagation velocity of the line. If there are impedance mismatches in the signal path, part of the incident wave will be reflected. The reflected wave is then algebraically added to the incident wave at the point where the mismatch occurs. The total voltage wave appears on the oscilloscope as a road map to the impedance breaks encountered by the propagating step.

A quick review of reflection coefficient (ρ) fundamentals will be helpful to intuitively understand the effects of signal path impedance breaks. Then, investigating three load impedance conditions will suffice. For all cases, the TDR generates the step from a 50Ω source and it is carried by a cable with characteristic impedance, Z_O = 50Ω, to the device under test, DUT. First case is if the DUT were a 50Ω load, then ρ would be 0 and the wave on the scope would appear as a straight line after the step, no reflected wave added to the incident.

$$\rho = (Z_L - Z_O)/(Z_L + Z_O) = 0 \text{ for } Z_L = Z_O$$

Z_O = cable characteristic impedance

Z_L = load impedance

The equation for adding the reflected wave, Er, to the incident wave, Ei, is as follows.

$$E = Ei + Er, \text{ where } Er = Ei(\rho)$$

The second case is infinite load impedance as in *Figure 4*. ρ is equal to +1 in this case and the reflected wave equals the incident wave. The total wave is then double the incident, *Figure 5*. Now consider when the incident wave hits an inductive impedance. The current can't change instantaneously so the load momentarily appears as an open due to the increased impedance. The ρ = +1 at t = 0 in *Figure 6*. Reflected voltage is ideally the same as the incident voltage for that moment. As the inductor current builds exponentially, the impedance drops toward zero, *Figure 6*. The voltage a long time after t = 0 is determined by resistance in series with the inductor. As t goes to infinity, the reflection coefficient is $\rho = (R - Z_O)/(R + Z_O)$, where R = series resistance of the inductive load.

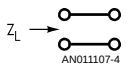


FIGURE 4.

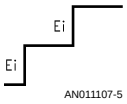


FIGURE 5.

FIGURE 6.

The third case is zero load impedance as in *Figure 7*. ρ = −1 and the reflected wave is subtracted from the incident wave leaving no voltage. Expanding on this idea, when the incident wave hits a capacitive impedance, the capacitor won't accept a sudden voltage change. No change in voltage ap-

pears as a short circuit instantaneously and ρ = −1 at t = 0. The capacitor voltage builds exponentially and the impedance rises to a level determined by the shunt resistive component of the load, *Figure 9*. The final value of ρ is again $(R - Z_O)/(R + Z_O)$, only R = shunt resistance of the capacitive load.

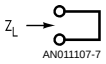


FIGURE 7.

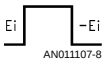


FIGURE 8.

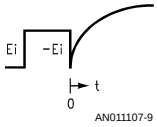


FIGURE 9.

TDR AND IMPULSE ENERGY

Another way to look at TDR results is by considering the energy contained in the step impulse. This energy is transmitted over a non ideal medium so there are losses, but for short distances it is not unrealistic to consider the energy of the pulse to be constant. Now consider the capacitive impedance break; increasing capacitance reduces the characteristic impedance.

$$V/I = Z_O = \sqrt{(L_O/C_O)} \text{ where:}$$

L_O = inductance per unit length

C_O = capacitance per unit length

Since the energy of the pulse remains constant and the voltage and the impedance drop, the current must increase proportionally to the lowered voltage. This increased current charges the capacitor at a time constant that is determined by Z_O in parallel with the shunt R to the capacitor. As the capacitor stores the energy, the current drops off and the capacitor appears as an open circuit after a long steady state condition.

TDR SYSTEM ERRORS

The extremely fast rise time of the step impulse is important to TDR analysis. Since the leading edge of the incident step is made up almost entirely of high frequency components, it accentuates the small reactive impedance mismatches of a signal path. As the step travels down a non-ideal transmission line, the higher frequencies are attenuated by skin effect losses and dielectric losses. This distorts the step, and is called cable loss. The degraded rise time limits the accuracy of reflection measurements through a multiple discontinuity signal path. TDR measures each succeeding discontinuity with less accuracy, because the transmitted step degrades and multiple reflections occur. The stub of a daughter board qualifies as a multiple discontinuity path, so the resulting waveforms must be analyzed as such.

TDR AND FUTUREBUS+ SIGNAL STUBS

With this in mind, an analysis of the TDR waveforms of the signal path can be performed. *Figure 10* and *Figure 11* show the artwork for two signal path traces. The actual path length is 64mm. *Figure 10* is the path used for all the waveforms gathered in this analysis and *Figure 11* is a path for comparison of the TDR responses. The apparent similarity of the artwork does not show the electrical differences of the paths while the TDR waveforms do. *Figure 13* and *Figure 15* include the waveforms from these two signal paths that are similar but different enough to demonstrate some characteristics. The signal path from pin 36 of the DS3886 goes through connector B-b-16 as designated by the Futurebus+ standard, *Figure 12*. This path is included in both figures. Also in both figures is the reflection from just the SMA connector that is used to launch the step impulse into the signal path. It is terminated with a 50Ω load. The inductance of the SMA leads can be seen by the sharp increase in impedance. The return to the 50Ω level is then illustrating the first case in the TDR review for the ρ = 0 situation.

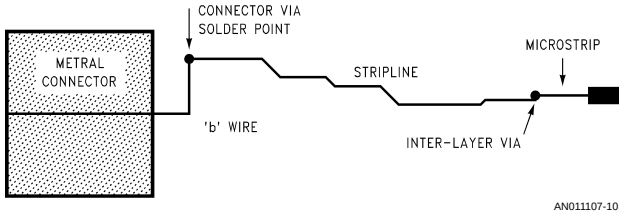


FIGURE 10. Signal Path B-b-16

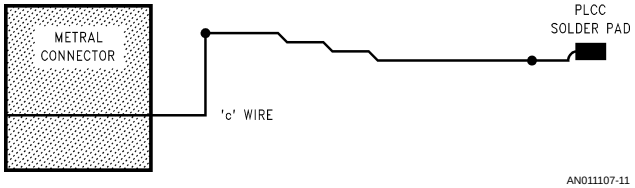


FIGURE 11. Signal Path B-c-16

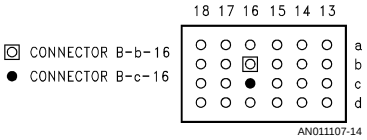


FIGURE 12. Signal Connector Block B, Rows 13 to 18

Figure 13 shows the effect of launching the TDR step into the solder pad. The first inductive bump is the error introduced by the SMA launching mechanism. The inductance of the microstrip follows the dip in impedance (capacitive solder pad). The path impedance is raised to 75Ω by both signal paths, *Figure 15*. Notice how the longer microstrip in *Figure 10* adds distance to the inductive bump compared to the waveform from the shorter microstrip in *Figure 11*. Then notice that the inter-layer via causes a capacitive drop in impedance. The stripline impedance settles in at about 60Ω for both of the paths. The next dip is the capacitance of the connector via solder point followed by the inductive increase of the connector wires. Notice that the longer "c" wire increases the impedance more than the "b" wire. Finally, the step hits the open end of the connector and the signal voltage doubles which indicates the ρ = 1 situation.

Figure 14 is included to show how the degradation of the incident wave through the multiple impedance mismatches of the signal path affects impedance level measurement. The TDR impulse is launched into the connector end of the path rather than the solder pad end. The difference is best seen in how the impedance of the connector is much greater when the high frequency components of the incident wave have not been attenuated by the previous impedance mismatches. The connector launch displays an impedance of 90Ω rather than the small increase that is shown in the end of the launch from the solder pad. *Figure 14* also shows the capacitance of the transceiver mounted on the solder pad that is charging to the open state at the time constant rate.

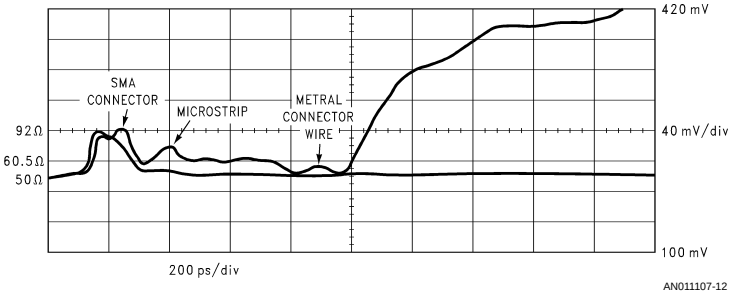


FIGURE 13. Two TDR Waveforms, 50Ω Termination and Path B-b-16

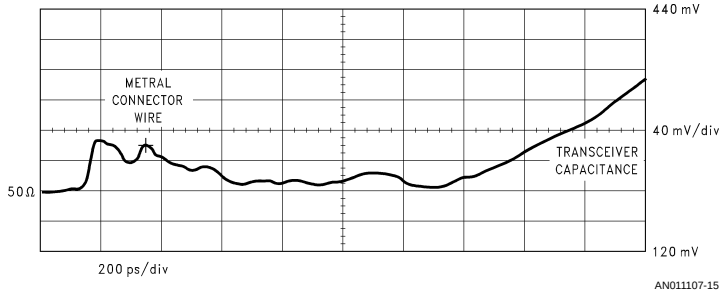


FIGURE 14. TDR Launch into Connector B-b-16 with DS3886 Mounted On Board

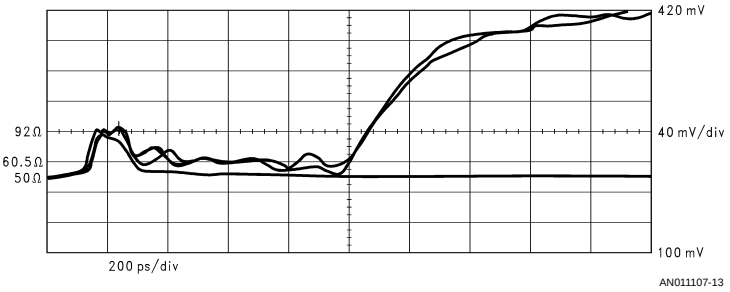
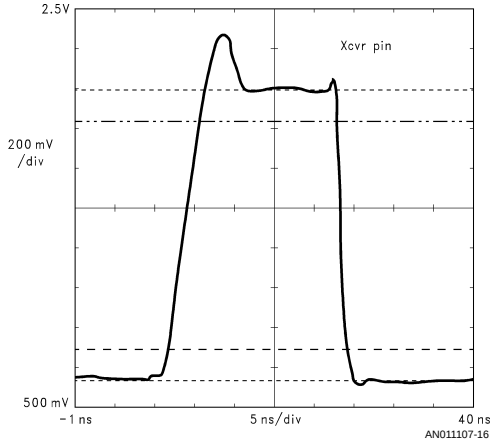


FIGURE 15. Three TDR Waveforms

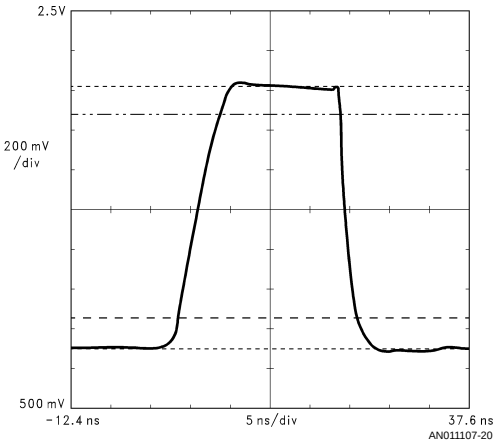
THE TRANSCEIVER IN THE UNLOADED BACKPLANE

The transmitting transceiver is mounted in slot 5, *Figure 1*. Pin 36 is named B3 in both the DS3883, 9 Bit Data Transceiver, and the DS3886, the Latched Data Transceiver which is used in this application. Pin 37 is the B3 GND pin, the BTL ground for B3 (see section on BTL, QGND, and logic GND). The signal waveform in *Figure 16* is obtained by probing the circuit with a low inductance ground tip at these two pins. The signal displays a rapid fall time, large overshoot and minimal undershoot. This signal is different than that obtained from bench testing with minimal jig inductance and capacitance, *Figure 17*. That waveform shows slower fall time and no overshoot. There are a couple of reasons for these backplane circuit responses. The first being the microstrip circuit element, T(55,365). Physically, this element is a very narrow microstrip between the solder pad and the inter-layer via. The relatively high inductance of this microstrip, shown in *Figure 14*, inhibits the sudden change in current presented by rapid transition times. This initially appears as a large impedance mismatch which makes the reflection coefficient (ρ) approach +1 instantaneously. The effect of ρ is to speed the slew rate on the fall time and extend the overshoot on the rising edge. The different response of the two edges is due to the active pull down and the passive pull up.



Rise 3.881 ns	Fall 1.346 ns	Max 2.37800 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 616.000 mV	Over Shoot 19.4787 %	Under Shoot 1.37174 %	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST06	Pan/ Zoom on

FIGURE 16.



Rise 5.410 ns	Fall 2.348 ns	Min 780.000 mV	Measure-ment	Distal 90% Proximal 10%
Max 2.13600 V	Over Shoot 1.52207 %	Under Shoot 1.67428 %	Statistics Comp & Def Continuous	Remove Wfm 1 ST05

FIGURE 17. Bench Test Jig Waveform

The second reason is the path inductance and line delay of the backplane, daughter board, and the termination scheme. The transmitter pull down transistor is turned on with a very large base current needed to supply 80 mA collector current. This collector current is supplied by the termination resistor which is located at some electrical distance (backplane and daughter board paths) from the transistor. As the transistor experiences a hard turn on, it initially sees what appears to be an open circuit. The momentary open circuit causes the overshoot and fast falling edge. This is due to the inductance and delay of the signal path preventing the current from changing immediately at the collector of the transistor. This inductance limits the driver slew rate control at the transceiver pin. Bench testing of the same part shows a fall time 1 ns longer than the daughter board fall time. The difference in fall times under test conditions are due to load proximity and availability of almost instantaneous current on the test jig. The rise time is much slower because it is a passive pull up and is controlled by the exponentially decaying current due to the inductance.

Another look at the waveform will show that there is an increase in voltage just prior to the high to low transition. This is also due to the large, fast voltage change at the base to the output transistor. The voltage step is coupled through from the base to the collector by the Miller capacitance. This small spike only shows up in the backplane environment for the same reasons as already explained.

IMPEDANCE MISMATCHES

The next probe is at the inter-layer via points of the signal line and ground line. Labeled point 55 in *Figure 1*. These vias present a relatively large capacitive impedance to the signal. The capacitance of the plated through hole (PTH) via has been estimated as high as 1.1 pF by Hybricon down to 0.75 pF by the Futurebus+ Expert Team. This is also the point at which the microstrip trace changes to a stripline trace. The capacitance of a PCB track varies directly with track length and width, but inversely with the dielectric thickness. Typically, this corresponds to about a 50% increase in capacitance from outer to inner layer for an eight layer board. As seen by the TDR investigation, the path impedance drops from 75Ω to 60Ω at this point, *Figure 13*. Thus, the stripline circuit element, T(50,55), can be characterized by an increase in the capacitance per unit length.

Figure 18 illustrates the damping of the overshoot and undershoot that is caused by the capacitive reactance. The fall time is increased by the capacitance. This can be intuitively understood by considering the capacitive impedance break of *Figure 9*. This has a counter balance affect on the path inductance so the needed current is available. Initially, the load appears as a short circuit because the capacitance will not accept an immediate change in the voltage. The ρ at the impedance mismatch then initially approaches −1. The quick charging of the capacitance pulls the slew rate out of a nose dive and limits the undershoot. The rise time shows a slight increase, but the resolution of the scope comes into play for times less than 150 pico seconds.

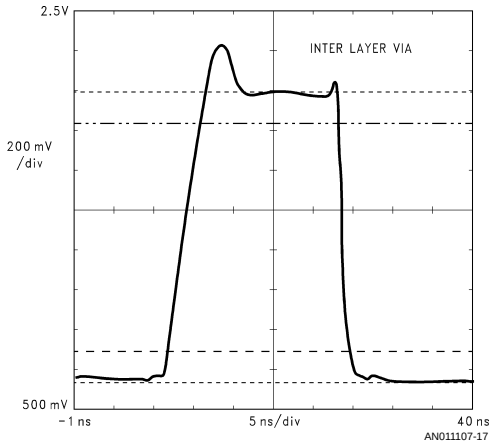
The third major impedance mismatch of the signal path occurs at the PTH to Metral connector solder point. Point 50 in *Figure 1*. The ground reference for the low inductance tip is the solder point for an adjacent connector ground pin. The circuit element for the connector is modeled by T(5,50). A SPICE model is provided by DuPont, the connector manufacturer. The TDR waveform clearly shows the capacitance of the solder filled PTH lowering the impedance to 50Ω, *Figure 13*. The same figure then shows the connector wire pre-

sents an inductive impedance increase for the signal. *Figure 19* shows considerable overshoot damping. It also shows an increase in rise time and fall time. The multiple discontinuities to this point have degraded the initial rise time of the signal so that the overall effect is that of line loss. The passive pull up accentuates only the resistive portion of the impedance rather then the reactive.

Notice the reflection that is well defined at the bottom of the falling edge. A closer examination of *Figure 16* shows that this same reflection is present in an attenuated form. The peak of this reflection is about 2 ns from the point where the signal crosses into an undershoot state. The delay per unit length, t_{pd}, of the unloaded backplane depends on the relative magnetic permeability, μ_r, the relative dielectric permittivity, ϵ_r, and the speed of light, c.

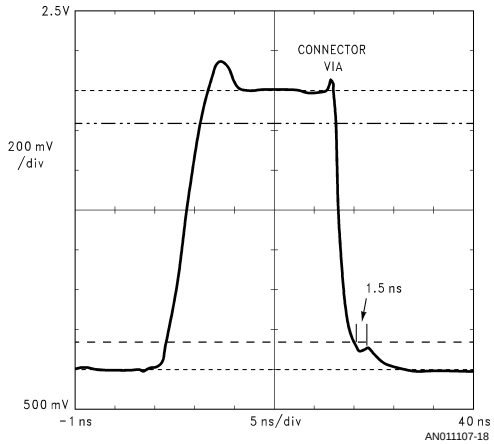
$$t_{pd} = \frac{\sqrt{\mu_r \epsilon_r}}{c}$$

With ϵ_r = 4.7 and μ_r = 0.99, then t_{pd} = 0.18 ns/in. So a round trip of 10 in., slot 5 to slot 0 and back, will be a delay of about 1.8 ns. This is almost exactly the delay of the reflected pulse at the connector solder point in *Figure 19*. The delay is measured from the falling edge tangent line. The period of this pulse is about 1.5 ns which is a frequency of 667 MHz.



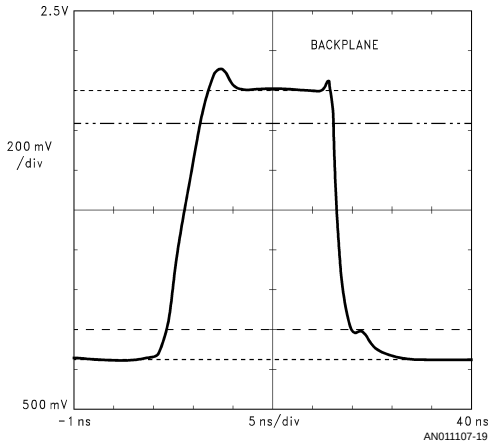
Rise 4.000 ns	Fall 1.689 ns	Max 2.34200 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 652.000 mV	Over Shoot 16.8056 %	Under Shoot 555.556 m%	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST05	Pan/ Zoom on

FIGURE 18.



Rise 4.457 ns	Fall 2.410 ns	Max 2.26200 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 696.000 mV	Over Shoot 11.1270 %	Under Shoot 570.613 m%	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST07	Pan/ Zoom on

FIGURE 19.



Rise 4.688 ns	Fall 2.898 ns	Max 2.21600 V	Measure-ments	Distal 90% Proximal 10%	
Min 742.000 mV	Over Shoot 8.43195 %	Under Shoot 591.716 m%	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST010	

FIGURE 20.

ENTERING THE BACKPLANE

After the connector, the signal reaches the backplane environment. The signal has been transformed by the daughter board path. Besides the impedance factors, the skin effect losses have rounded top and bottom portions of the edges. The probe points are at the solder points of the Metral connectors to the backplane PTH. The waveform in *Figure 20* was obtained at the slot where the board is inserted, just on the backplane side of the connector from the previous figure. The connector increases the fall time by 500 ps and damps the overshoot. The increase in fall time here appears to be a result of the reflected pulse increasing in amplitude. As the incident wave propagates further down the backplane the same damping of overshoot and increase in transition times occurs. The backplane characteristics are dependent on the loading that is present in the form of inserted boards with transceivers.

THE LOADED BACKPLANE

The distributed capacitive loading of the backplane has significant effects on the signal. The position of the loads with respect to the driving board will determine how the reflections add to degrade the signal. The worst case is when the reflections cut into the noise margin; i.e., the reflections that are positive going on the low output and negative going on the high output. The investigative results show that reflections in the high state never go below the 2.1V level by more than 50 mV. The problem on the high end occurs when the bus is fully loaded. At 20 MHz and fully loaded, the rising edge becomes rounded, *Figure 21*.

The worst bite into the noise margin was found in the case of 2 loads, 12 pF each, in specific slots on the backplane. The driver in slot 5 and the loads in slot 6 and 0 caused sustained ringing with a peak amplitude of 200 mV into the noise mar-

gin low. The case is shown in *Figure 22*. It should be noted that the period of the ringing in *Figure 22* is about 2 ns. This corresponds to a frequency of 500 MHz. This presents a demand on test equipment to pick up these high frequency signals.

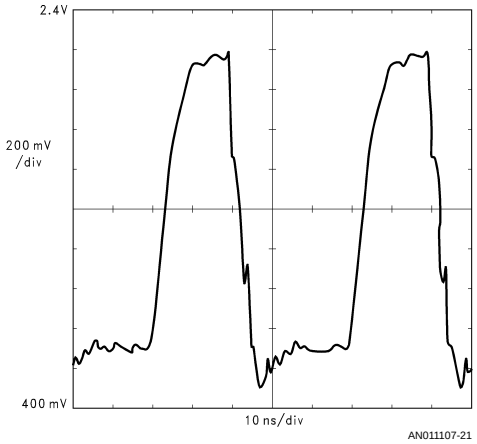
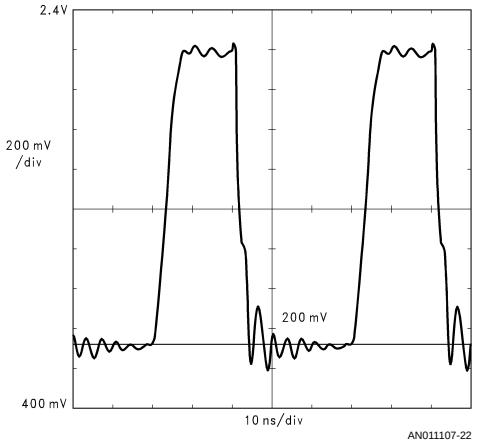


FIGURE 21. Backplane Probed at Driver = Slot 5, 10 pF to 12 pF Loads in Every Slot



Rise 4.938 ns	Fall 3.603 ns	Max 2.21200 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 598.000 mV	Over Shoot 1.64384 %	Under Shoot 8.90411 %	Statistics Comp & Def Continuous	Remove Wfm 3 ST013	Pan/ Zoom on

FIGURE 22. Backplane Probed at Driver = Slot 5, 12 pF Loads in Slots 0 and 6

GIGA HERTZ BANDWIDTH

A 400 MHz probe and scope would not pick up all of the frequency components of this ringing. Because of the high frequency components that comprise this signal, all of the measurements done by National Semiconductor on the Futurebus+ chip set are obtained by using the Tektronix P6204 FET probe and 11A72 amplifier mounted in the 11403 digitizing oscilloscope. This combination has a bandwidth of 1 GHz.

Figure 23 is included to show how a single load of 12 pF will cause different reflections depending on where it is inserted with relation to the driving transceiver. The line delay is evident when the reflection from the adjacent load appears before the reflection from the far end load. The different loading positions will determine the waveform shape and how it will encroach on the noise margin.

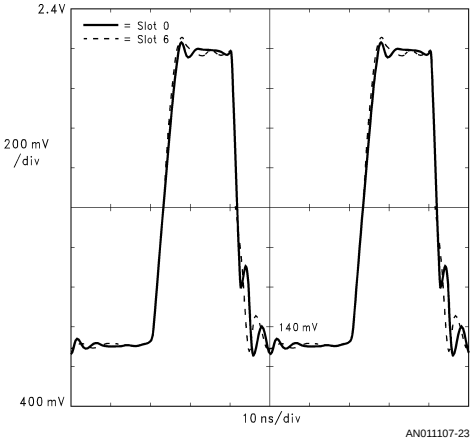


FIGURE 23. Backplane Probed at Driver = Slot 5

WHY ALL THE DIFFERENT GROUNDS?

There are three different types of gound pins on the National Semiconductor Futurebus+ Chip Set. They are the logic ground (GND), the BTL grounds (B0GND–B8GND) and the bandgap reference ground for receiver threshold (QGND). All of these ground reference pins are isolated inside of the chip to limit the interference from high current switching transients. Outside the chip, the bandgap reference ground should be connected to the backplane ground through a quiet channel. The isolation purpose is so the receiver input threshold will follow the same reference as the signals coming off the backplane. The other grounds should be tied to the board ground plane to prevent ground loop currents inside the chip.

FUTUREBUS+ TRANSCEIVER GROUND BOUNCE

A single transceiver can have up to 9 BTL channels switching at the same time. If each channel sinks 80 mA, there is substantial current switching taking place. The combination of the ground lead inductance and finite resistance of the current return paths cause voltage drops and rises to occur along this path that are proportional to the changing current.

$$V = L\,(di/dt)$$

where V = amplitude of the ground bounce

L = inherent inductance of signal and ground trace

The DS3886 Latched Data Transceiver mounted in the Hybricon proto board was used to investigate the amount of ground shift that is experienced in the Futurebus+ environment.

Eight channels are connected to the same input so that they are switching simultaneously. The ninth channel, B3 (located between the other eight), is driven to the asserted state and used as a reference. Six other data transceivers were also on the board and allowed to switch at random (open driver inputs). The Futurebus+ connector pin layout uses 1 of every 3 pins as a ground pin. The Hybricon board links all these pins to the board ground plane as they enter through the Metral connector. The transceiver BTL ground pins are mounted to the solder pad and then traverse a microstrip track to a PTH via to make ground plane contact. The microstrip adds inductance to the ground path but is necessary for even heating to solder the chip package to the thermally isolated pad.

PROBING THE GROUND

The backplane ground plane is used as a reference to investigate all of the ground differences in the circuit. It is accessed through a ground tab connector on the Metral power connector module. *Figure 24* shows the idle backplane noise at the top of the picture. The GHz probe with a short, low inductance alligator clip ground was used to probe two of the empty slot ground tabs. There was no transceiver activity for this situation. The second from the top waveform is the same probe position only eight transceiver channels are now switching. Large disturbances in the signal occur at the time that eight channels are all going from high to low, the time of substantial active current change. Notice how the low to high transition does not create the same sort of voltage spike on the ground signal. This is because the collapsing current doesn't have a large *di/dt.*

The same backplane ground reference was used for all of the measurements in *Figure 24*. The third pattern was obtained probing the daughter board ground plane close to the Metral connector between the switching transceiver and the backplane. The disturbances are muted in this case by the bypass capacitors of the board. The board is decoupled by 4–180 µF and 14–0.1 µF capacitors. The next waveform is from the same ground plane but it is probed at the via that connects the microstrip from the transceiver BTL ground pin to the board ground plane. This waveform is a slightly attenuated version of the waveform seen on the non switching ground pin. This is because the waveform seen at the B3GND pin is coming from the board ground plane! The inductance of the microstrip and the lead frame inside the package increase the overshoot and the undershoot of the ground bounce. The worst ground disturbance is measured at one of the switching channel BTL ground pins. This is as expected from interior transceiver noise caused by the hard turn on of the output transistor creating very rapid build and collapse of current.

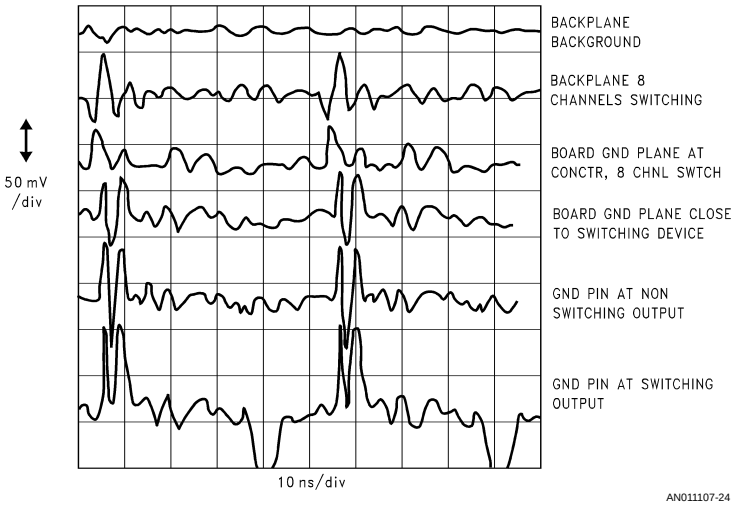


FIGURE 24.

CROSSTALK IN THE FUTUREBUS+ ENVIRONMENT

The crosstalk problem has received a lot of attention. There is the potential for significant forward and backward crosstalk due to the high speed signals, multiple transmission path media, and the density of the signal lines. These are the simplified equations relating the contributing factors.

V_{bkwd} = (V_a/t_r) $(\ell/2t_\ell)$ $(C_CZ + L_C/Z)$
= backward coupled voltage to victim line

V_{frwd} = (V_a/t_r) $(\ell/2)$ $(C_CZ - L_C/Z)$
= forward coupled voltage to victim line

V_a = aggressor signal amplitude

t_r = aggressor signal transition time

ℓ = line length

t_ℓ = line delay

Z = line impedance

C_C = capacitive coupling due to electric field

L_C = inductive coupling due to magnetic field

Both types of crosstalk are directly proportional to the amplitude, and inversely proportional to the transition times of the aggressor signal. The capacitive and inductive coupling affect both types of crosstalk. In backward crosstalk they add together and are multiplied by the aggressor amplitude to give a same polarity pulse to the victim. In forward crosstalk, the quantity $(C_CZ - L_C/Z)$ is multiplied by the aggressor am-

plitude to give a pulse of either polarity depending on the relative size of the coupled reactances. The connector does present a special problem due to the open wire configuration. The inherent inductance of the open wires and the proximity in the Metral connector are favorable situations for crosstalk. Not modeled in the above equations but still a factor is the signal wave velocity differences. Forward crosstalk also results from velocity differences of an aggressor signal due to the conductive medium contacting substances of different dielectric constants. The microstrip line is such a medium that contacts both air and epoxy glass. This creates an energy pulse that will couple electrostatically to the victim. For these reasons, crosstalk was investigated in two different ways.

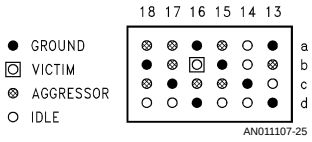


FIGURE 25. Module B, Section 3, Used in Crosstalk Measurements. The Victim Line is Labeled B-b-16

Futurebus+ standards committees set up the pin designations on the Metral connector so that there is one ground pin for every 2 signal carrying pins. The worst case then is the situation where 1 signal pin can be surrounded by 5 signal pins and 3 ground pins as in *Figure 25*. The Expert Team tested crosstalk using a switching line as victim and measured the difference between 0 and 5 aggressors at a receiving module. *Figure 26* shows these same tests for DS3886.

The driver module is located in slot 7 and two receiver modules are in slots 0 and 9. As mentioned in the section on reflections, this is the worst configuration for cutting into the noise margin. It is also a long length for the parallel backplane tracks to cross couple. The signal line ST2 was used as the victim and ST0–ST7 as the aggressors. *Figure 26* shows the falling edges at the driver and receiver pins for the two conditions, only the victim switching and then all aggressors and the victim switching. The largest amount of induced voltage onto the victim line is 50 mV. This is the same result as the Expert Team.

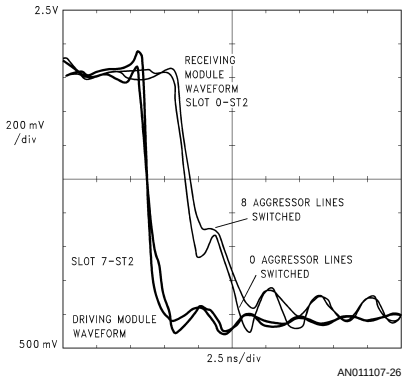


FIGURE 26.

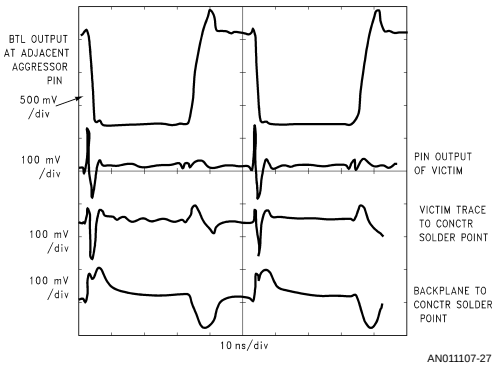
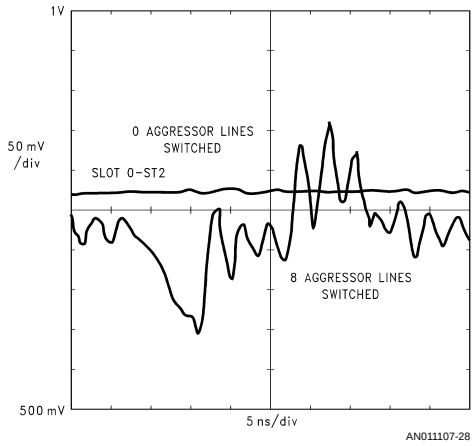


FIGURE 27. Victim Is Only Asserted, 8 Aggressor Channels Switching

Figure 27 shows results of a different way of investigating the crosstalk than the Futurebus+ Expert Team method. The victim line was held in the asserted state while 8 aggressor

lines were switching. The top waveform is the aggressor signal. The three lower waveforms are the victim signal probed at daughter board impedance points. The figure shows that the victim experiences a 100 mV pulse into the noise margin at the high to low transition of all the aggressors. This case is measured on the backplane at the same slot as the driver. A demonstration of the high inductance of the Metral connector is the inversion of the induced signal through the connector. The inductance of the connector is large enough to give the forward crosstalk an inverted pulse at this point. In an actual data transmission, the crosstalk concern would be at the input to the receiving transceiver. The slowing of the edge rates by the time they reach a receiver on another board will further reduce the magnitude of the crosstalk. *Figure 28* shows the signal at the same receiver input pin with no aggressors and with 8. The coupled voltage intrusion to the noise margin is 85 mV.



Rise 466.7 ps	Fall 435.0 ps	Min 590.000 mV	Measure- ments	Horz Mag 1 x Horz Pos Gr Opts	
Max 862.000 mV	Frequency 274.3 MHz		Statistics Comp & Def Continuous	Remove Wfm 2 ST014	Pan/ Zoom On

FIGURE 28. Crosstalk Voltage at Receiver with 8 Aggressor Lines Compared to 0 Aggressors

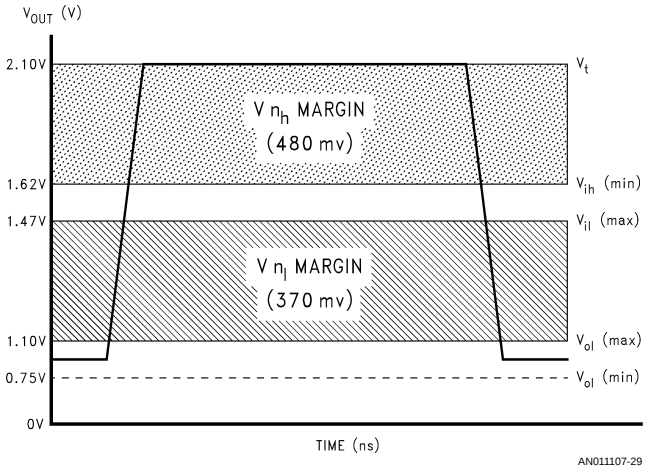


FIGURE 29.

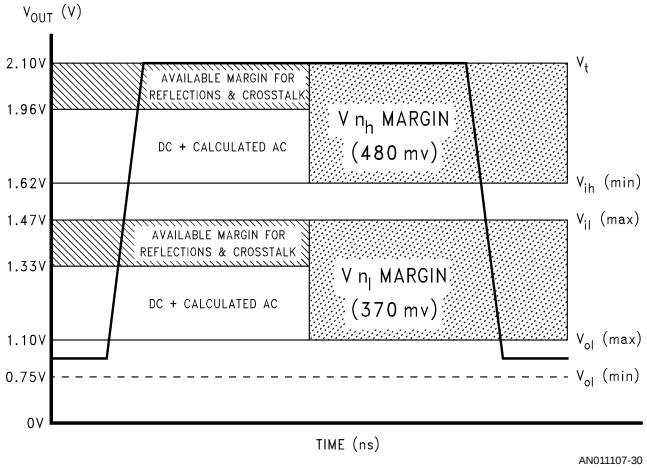


FIGURE 30. (all slots loaded)

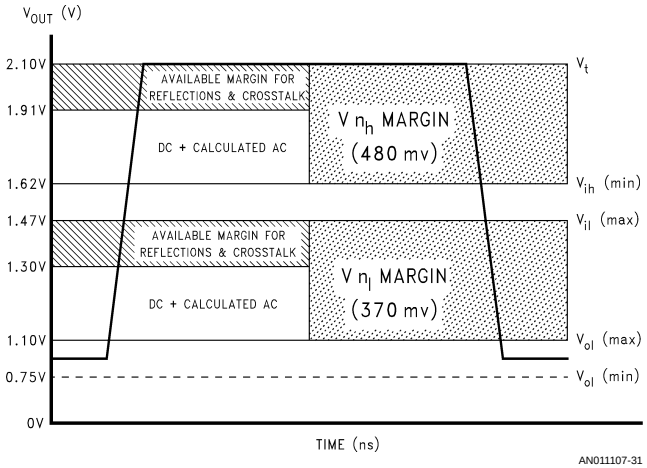


FIGURE 31. slots 0 to 6 loaded

CONCLUSION

The Futurebus+ environment presents impedance mismatches to the high speed data signals. These circumstances make the measurement of the signals dependent on where they are measured. The fast edge rates of the signals have high frequency components that compose a large part of the waveform and can not be ignored. For these reasons, National Semiconductor uses 1000 MHz bandwidth test equipment, and specially designed low impedance test jigs for all of the data sheet specifications.

The placement of modules in a partially loaded backplane is crucial to the magnitude of the ringing. The equal distribution of the modules in the backplane appears to be the best condition for the lowest magnitude ringing.

Figure 29 shows the noise margins for BTL. *Figure 30* shows the allocation of the noise margin for a fully loaded backplane and partially loaded in *Figure 31* according to the Futurebus+ Expert Team. They have done extensive simulations that are reported in the Interim Report presented on September 14, 1990. This investigation of the reflections and crosstalk will be compared to their findings.

Figure 26 shows the combination of worst case crosstalk and reflections that were found in this investigation. The crosstalk added to the reflections to cut into the noise margin low by 100 mV. The 100 mV intrusion is deduced from the fact that the incident edge has a distinct edge at the 1.2V level. This is within the allowed 170 mV range in the Expert Team analysis of the partially loaded backplane, *Figure 31* . This investigation also showed that the fully loaded backplane produced lower magnitude reflections than the partially loaded backplane. The measurements collected here support the Expert Teams allowance of only 140 mV for reflections and crosstalk in the fully loaded backplane, *Figure 30*.

The National Semiconductor DS3886 Latched Data Transceiver maintained signal integrity in the Futurebus+ Back-

plane environment under severe operating conditions. Worst case situations of crosstalk, stub length and ground bounce combined with a transmission speed of 40 MBaud were used to test the DS3886 in real backplane operating conditions. The incident edge of the BTL signal consistently crossed the receiver threshold without a problem.

REFERENCES

1. *The Multilayer Printed Circuit Board Handbook,* J.A. Scarlett, Electromechanical Publications, Ayer, Scotland, 1985.
2. *TDR Fundamentals,* Application Note 62, Hewlett Packard, April, 1988.
3. *FAST Applications Handbook,* National Semiconductor Corporation, 1987.
4. *Handbook of Printed Circuit Design, Manufacture, Components and Assembly,* Giovanni Leonida, Electromechanical Publications, Ayer, Scotland, 1981.
5. Interim Report of the Electrical Task Group Expert Team … Futurebus+ Modeling and Noise Margin Results, Raytheon and DEC, Sept. 14, 1990.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179