A/D Converters Easily Interface with 70 Series Microprocessors

National Semiconductor
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Abstract: *This application note describes techniques for interfacing parallel I/O and serial I/O 8-bit A/D converters to the INS8070 series of microprocessors. A detailed hardware and software interface example is provided for each type of A/D.*

As examples, the INS8073 is used to interface with the parallel I/O ADC0804, and the INS8072 is used with the serial I/O ADC0833.

INTRODUCTION

The INS8070 series of microprocessors is designed for compact, low cost control, data acquisition, and processing applications. Up to 2.5k-bytes of ROM and 64 bytes of RAM are available on-chip. The INS8073 is a programmed version of the INS8072 with a Tiny Basic microinterpreter on-chip. The microinterpreter executes source code directly, thus avoiding the need to translate the source code into machine language. This approach allows users to develop system software without using a development system and gives a greater flexibility for design changes.

The ADC0801 series, the ADC0808 series, and the ADC0816 series are CMOS 8-bit successive approximation A/D converters that include TRI-STATE® latched outputs and control logic for parallel I/O. These A/Ds can be mapped into memory space or they can be controlled as I/O devices. The ADC0801 series includes a differential input and span adjust pin, while the ADC0808 and ADC0816 series include an 8- or 16-channel multiplexer with latched control logic.

The ADC0831 series, on the other hand, are CMOS 8-bit successive approximation A/D converters with serial I/O. In addition to the single analog input ADC0831 in an 8-pin miniDIP, they offer 8, 4, or 2-channel analog multiplexed inputs. Serial output data can be selected as either MSB or LSB first. The channel assignment of the multiplexers is accomplished with a 4-bit serial input word preceded by a leading "1" start bit.

The ADC0801, ADC0802, ADC0803, ADC0804 parallel I/O A/Ds and the ADC0833 serial I/O A/D are designed to work with a 2.5V fixed reference for a 0V to 5V analog input range. The full 8 bits of resolution can be encoded over any smaller analog voltage range by applying one half of the desired full-scale analog input voltage value to the $V_{REF}/2$ pin.

The ADC0805, ADC0808, ADC0809, ADC0816, ADC0817 parallel I/O A/D converters and the ADC0831, ADC0832, ADC0834, and ADC0838 serial I/O A/D converters are designed to operate ratiometrically with the system transducers. A ratiometric transducer is a conversion device whose output is proportional to some arbitrary full-scale value. The actual value of the transducer's output is not important, but the ratio of this output to the full-scale reference is important. Also, these parts are designed to use a 5V fixed reference.

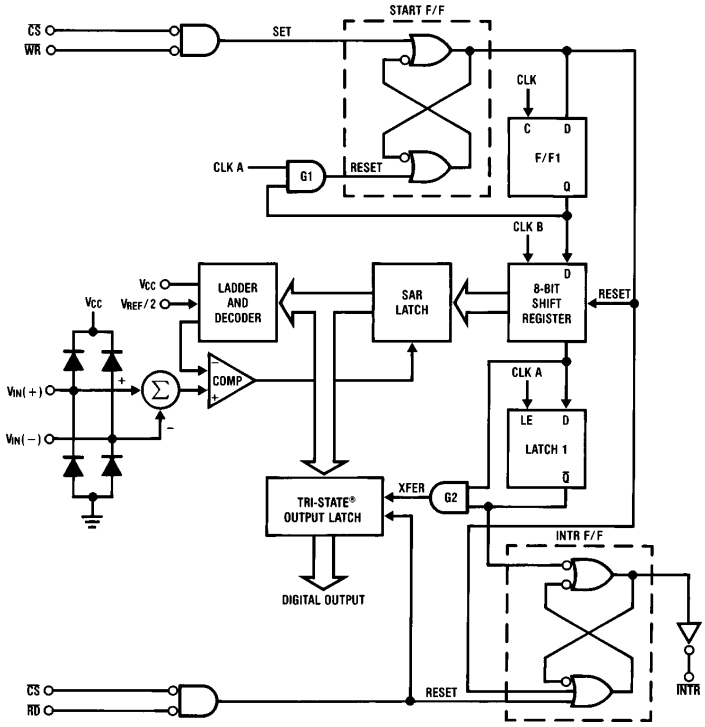

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FIGURE 1. ADC0804 Internal Block Diagram

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All of these A/D converters operate from a standard 5V power supply, and are available in accuracies over the temperature range of $\pm\frac{1}{2}$ LSB or ± 1 LSB including full-scale, zero scale, and non-linearity errors.

ADC0804 IMPLEMENTATION EXAMPLE

Theory of Operation

The converter is started by forcing $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) (see *Figure 1*) which resets the 8-bit shift register, resets the INTR F/F and sets F/F1, which is at the input end of the 8-bit shift register. When the set signal of the start F/F goes low (either $\overline{WR}$ or $\overline{CS}$ is high), the 8-bit shift register then shifts in a ''1'' from F/F1, which starts the conversion process. After the ''1'' is clocked through the 8-bit shift register, it appears as the input to Latch 1. The ''1'' output from the shift register causes the 8-bit output of the SAR latch to transfer to the TRI-STATE output latches. When Latch 1 is subsequently enabled, the Q output makes a high-to-low transition which sets the INTR F/F. An inverting buffer then supplies the $\overline{INTR}$ output signal. When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will reset the INTR F/F and will enable the TRI-STATE buffer latch output onto the 8-bit data bus.

1k-byte of external RAM is provided in the INS8073 system, in which the first 256 bytes are used to store the microinterpreter's variables, stacks and buffers. The remainder of the RAM is used to store data and the interface program. The A/D is mapped into the memory space of the INS8073 system at address 3000 HEX. External RAMs are located from 1000 HEX to 13FF HEX. A DM74LS138 address decoder is used to generate the chip select signals for the A/D and the RAM. It also provides a signal to enable a DM74LS368 TRI-STATE HEX buffer which provides the baud rate setting at location FD00 HEX. The read and write strobe signals of the A/D and the processor are tied together, and the $\overline{INTR}$ signal of the A/D is tied to the SENSE B input of the INS8073.

The microinterpreter has built-in I/O routines to serially interface with an RS-232 terminal. The INS8073 F1 flag should be inverted and buffered to provide an RS-232 level. Similarly, the INS8073 will accept serial input data, buffered to TTL level without inversion, on its SA input. DS1488/DS1489 quad line driver/receiver chips are used for TTL/RS-232 buffering. Baud rate can be selected by matching the two jumpers, J1 and J2, (see *Figure 2*), with the table below. A ''0'' signifies that the jumper is missing, and a ''1'' means that it is installed.

J1	J2	Baud Rate
0	0	4800
0	1	1200
1	0	300
1	1	110

Details of both hardware and software interface are given below and in *Figure 2*. A Tiny Basic subroutine, along with an Assembly Language subroutine, are illustrated. The microprocessor starts the A/D, reads, and stores the results of 16 successive conversions. The 16 data bytes are stored at location 13D0 HEX to 13DF HEX. The Assembly Language subroutine can be called by issuing a ''LINK'' statement in Tiny Basic. It performs the same function as the Tiny Basic subroutine, except it will execute faster. The Tiny Basic subroutine takes about 60 ms to execute; the Assembly Language subroutine takes only 96 μs (plus conversion time).

TINY BASIC INTERFACE SUBROUTINE

```
100 REM   SUBROUTINE TO START A/D AND STORE DATA INTO MEMORY
110 REM   C IS THE COUNTER FOR THE NUMBER OF DATA BYTES STORED
120 REM   D POINTS TO THE 1ST DATA ADDRESS
130 C=16
140 D=#13D0
150 @ #3000=A                          :REM  START A/D
160 A=STAT AND #20                     :REM  LOOP UNTIL SENSE B GOES LOW
170 IF A<>0 THEN GO TO 160             :REM  (CONVERSION COMPLETED)
180 @ D=@ #3000                        :REM  INPUT CONVERTED DATA
190 D=D+1                              :REM  INCREMENT DT ADDRESS
200 C=C-1                              :REM  CHECK WHETHER 16 CONVERSIONS
210 IF C>0 THEN GO TO 150              :REM  ARE DONE OR NOT
220 RETURN
```

INS8072 ASSEMBLY CODE INTERFACE SUBROUTINE

```
; THIS SUBROUTINE IS TO BE CALLED BY TINY BASIC THROUGH A ''LINK'' STATEMENT
BEGIN:  PLI   P2,=13DOH     ;P2 POINTS TO A 1ST BYTE ADDRESS
        PLI   P3,=3000H     ;P3 POINTS TO A/D
        LD    A,=0FH        ;SET CONVERSION COUNTER TO 15
        ST    A, COUNT      ;COUNTER ADDRESS
START:  ST    A, 0, P3      ;START A/D
WAIT:   LD    A, S          ;WAIT FOR SENSE B INPUT TO GO LOW
        AND   A,=20H        ;(CONVERSION COMPLETED)
        BNZ   WAIT
        NOP
        LD    A, 0, P3      ;INPUT CONVERTED DATA
        ST    @ 1, P2       ;STORE DATA IN MEMORY
        DLD   A, COUNT      ;DECREMENT COUNTER. IF NOT DONE,
        BP    START         ;DO ANOTHER CONVERSION
        POP   P3            ;RESTORE P2 AND P3 FOR TINY BASIC
        POP   P2
        RET                 ;RETURN TO TINY BASIC
```

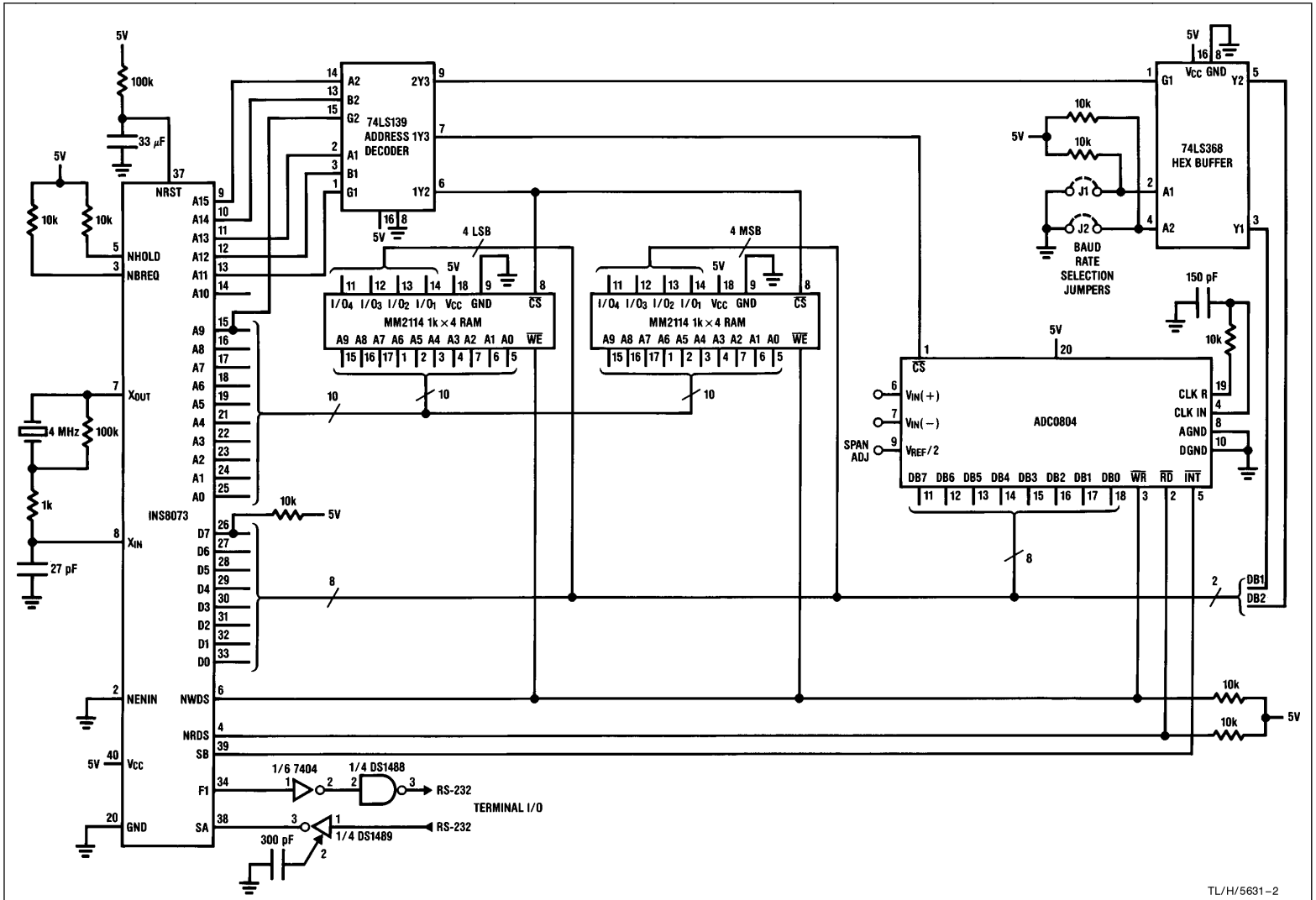

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FIGURE 2. ADC0804–INS8073 Microprocessor Interface

ADC0833 IMPLEMENTATION EXAMPLE

Theory of Operation

The three flag outputs (F1, F2, F3) and a sense input (SA or SB) are all that is required to interface the ADC0833 and the 70 series family microprocessor (see *Figure 3*). The AND S, = XX and the OR S, = XX instructions set up the status register to produce the proper output signals (D1, CLK, $\overline{CS}$). The input is derived by loading the status register into the accumulator and masking all but the necessary bit.

The ADC0833 is selected by setting $\overline{CS}$, CLK, and DI low. After setting a counter to account for the 4-bit MUX address and the start bit, the data is shifted out, serially. This is accomplished by testing the carry bit after each shift and modifying FI accordingly (see Tables I and II and *Figure 4*). Once the leading sentinel bit and all four MUX address bits are clocked in, the A/D input is disabled and DO is enabled. One clock pulse is required to sync the output with the falling clock edge; the falling clock edge is used to clock data out. Each of eight successive input loops load the status register into the accumulator and the masks to determine whether the input was a ''1'' or ''0''. After ascertaining which, the result is loaded into the accumulator and the program successively shifts left (for a ''0''), or shifts left and adds a ''1'' (for a ''1''). A digitized byte is formed representing the analog input (see *Figures 5* and *6*).

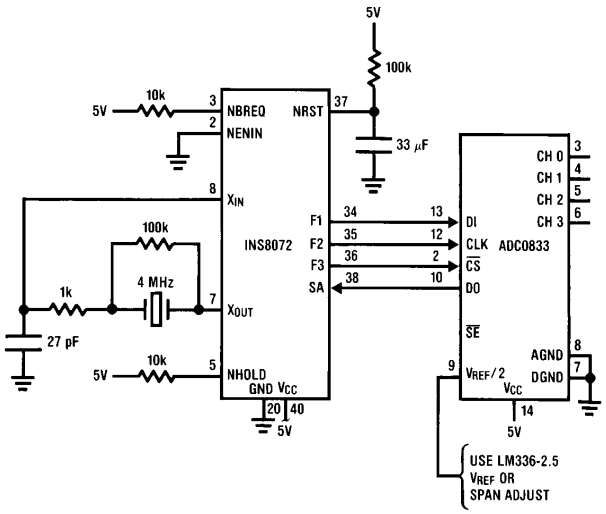

FIGURE 3. A/D Conversion Circuit for Single-Ended MSB First Mode

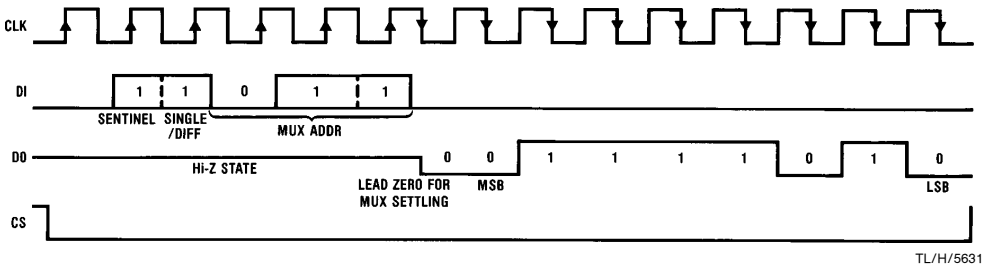

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FIGURE 4. Example I/O Transaction (A/D Output = 7A; Channel 2, Single-Ended Selected)

TABLE I. SINGLE-ENDED MUX MODE

LSB		MSB	S/D	Start	Single-Ended				HEX Code
					0	1	2	3	
1	0	0	1	1	+				13
1	1	0	1	1			+		1B
1	0	1	1	1		+			17
1	1	1	1	1				+	IF

TABLE II. DIFFERENTIAL MUX MODE

LSB		MSB	S/D	Start	Differential				HEX Code
					0	1	2	3	
1	0	0	0	1	+	−			11
1	1	0	0	1			+	−	19
1	0	1	0	1	−	+			15
1	1	1	0	1			−	+	1D

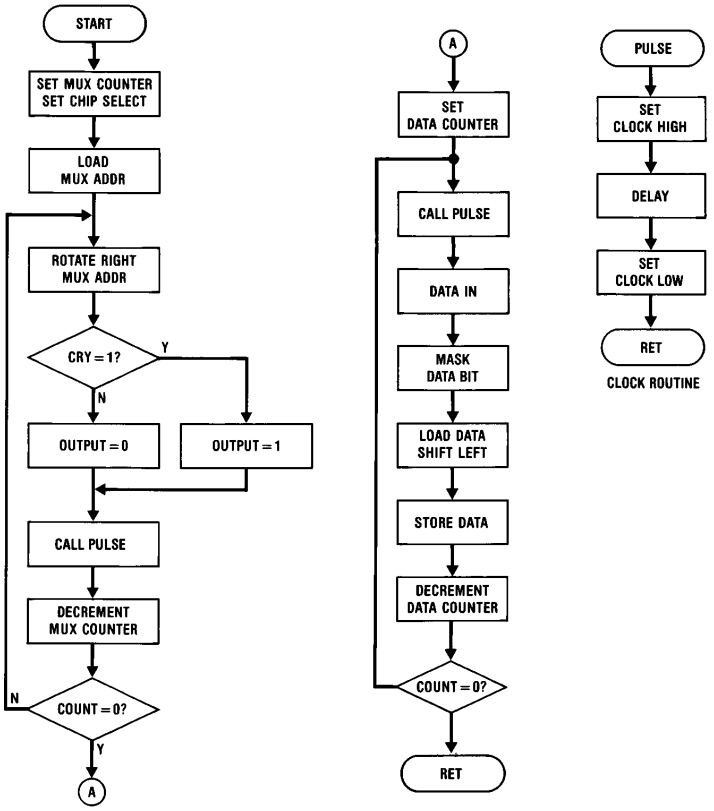

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FIGURE 5. A/D Conversion Flow Chart

```
START:   AND    S, = 0F0H       ;SET CS = 0, CLK = 0
         LD     A, = 5
         ST     A, CNTR ADDR    ;SET UP MUX ADDR COUNTER
         LD     A, = 0
         ST     A, RESLT ADDR   ;CLEARS RESULT LOCATION
         LD     A, = MUX ADDR   ;LOAD MUX ADDR AND SENTINEL BIT
         JMP    LOOPS
LOOP 1:  XCH    A, E            ;RESTORE MUX ADDR REMAINDER
LOOP 5:  RRL    A               ;ROTATE BIT 0 INTO CARRY
         XCH    A, E            ;SAVE MUX ADDR REMAINDER
         LD     A, S            ;LOAD STATUS REG
         BP     ZERO            ;IF CARRY NOT SET, OUTPUT = "0"
ONE:     OR     S, = 02         ;SET F1 = 1 (D1 = 1)
         JMP    CONT
ZERO:    AND    S, = 0F0H       ;SET F1 = 0 (DI = 0)
CONT:    CALL   PULSE           ;PULSE CLK 0 ⟶ 1 ⟶ 0
         DLD    A1 CNTR ADDR    ;DECR AND LOAD COUNTER
         BNZ    LOOP 1          ;BRANCH IF COUNT = 0
         LD     A, = 08         ;SET UP DATA BIT COUNTER
LOOP 2:  CALL   PULSE           ;PULSE CLOCK 0 ⟶ 1 ⟶ 0
         LD     A, S            ;LOAD STATUS REG
         AND    A, = 01         ;DETERMINE IF DATA = "1"
         BZ     IN0             ;IF ACC = 0, GO TO IN0
         LD     A, RESLT ADDR   ;LOAD CURRENT RESULT
         SL     A               ;SHIFT RESULT LEFT
         ADD    A, = 1          ;ENTER LATEST DATA BIT
         JMP    GO              ;
IN0:     LD     A, RESLT ADDR   ;LOAD RESULT
         SL     A               ;SHIFT RESULT LEFT, BIT 0 = 0
GO:      ST     A, RESLT ADDR   ;STORE CURRENT RESULT
         DLD    A, CNTR ADDR    ;DECR AND LOAD DATA COUNTER
         BNZ    LOOP 2          ;IF COUNTER ≠ 0, CONT
         RET
PULSE:   OR     S, = 04         ;SET F2 = 1 (CLK = 1)
         NOP                    ;DELAY
         AND    S, = 0FBH       ;SET F2 = 0 (CLK = 0)
         RET
```

FIGURE 6. Single-Ended A/D Conversion Program

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