CMOS D/A Converters Match Most Microprocessors

National Semiconductor
Application Note 275
James B. Cecil
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With double buffering, 8, 9, and 10-bit multiplying units are useful for microprocessor control of gain and attenuation.

A new family of complementary MOS multiplying digital-to-analog converters has arrived on the scene and promises to make microprocessor interfacing truly universal. The double-buffered MICRO-DAC™ units eliminate many common problems, bridging the way to a host of new applications that include microprocessor-controlled gain, attenuation, and multiplication.

The proliferation of the microprocessor in electronic circuits has brought with it an equal proliferation of microprocessor-compatible D/A converters. Many of these converters, however, have shortcomings in that they often require additional external components to be truly microprocessor-compatible. Furthermore, depending on a converter's resolution and data format, a designer is sometimes forced to adopt additional interfacing circuitry for total microprocessor compatibility. Transient output voltage errors can occur during the updating of a 10-bit D/A converter from an 8-bit microprocessor bus, when the two words are transferred to the converter. Left-justified (fractional binary) and right-justified (positionally weighted binary) D/A converter data formats require different interfacing schemes. All of these problems must be considered in interfacing a microprocessor and a D/A unit.

TWO LEVELS OF BUFFERING

The MICRO-DAC family of multiplying D/A converters consists of 8, 9, and 10-bit accurate units designed to interface directly with the 8080, 8048, 8085, Z-80, and other popular microprocessors. The converters appear to the microprocessor as a memory location or as an input/output port and require no interfacing logic. Each has two levels of input buffers—an input latch and a register (*Figure 1*).

The converter's register holds the digital data undergoing conversion, while the input latch is kept busy acquiring new input data. The digital input data is used to update the D/A converter. The double buffering feature allows 10 bits of microprocessor data to be assembled from 2 data bytes. It also prevents the analog output from changing while the digital input word is updated.

Even when used with 16-bit microprocessors, the double buffering feature is necessary for the simultaneous updating of many D/A converters. Double buffering establishes the proper conditions for the next test or lets new system parameters be set up at the same time.

Two groups of MICRO-DAC converters are available. The DAC1000, DAC1001, and DAC1002 are 24-pin units with 10, 9, and 8-bit accuracy levels, respectively. Each contains all of the necessary logic functions for interfacing with right-justified and left-justified microprocessor data. The DAC1006, DAC1007, and DAC1008 20-pin units are designed for left-justified data at accuracy levels of 10, 9, and 8 bits, respectively.

All the members of this family of multiplying D/A converters feature standard chip select (CS) and write (WR) microprocessor control signals. Data on the microprocessor bus can be written into the D/A converter in a standard write cycle.

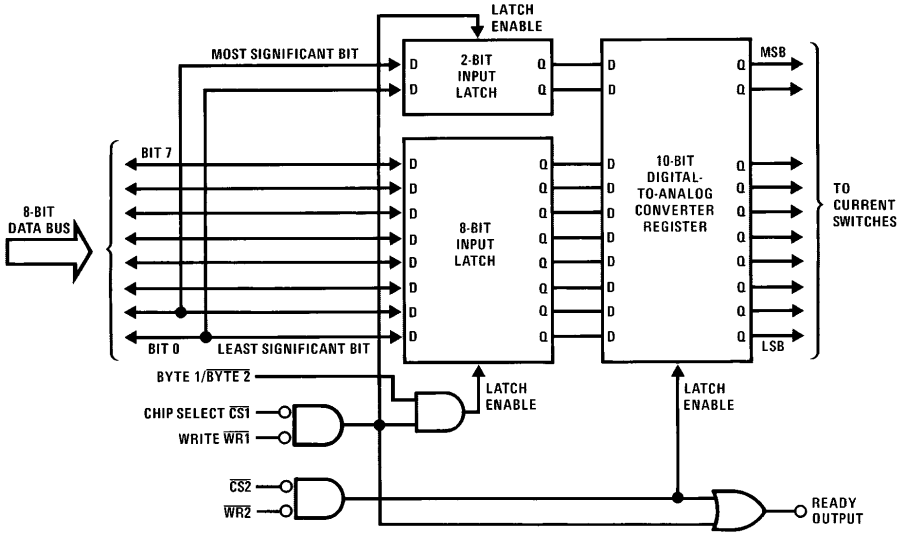

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FIGURE 1. Double buffered. The MICRO-DAC family of 8, 9, and 10-bit digital-to-analog converters has two levels of input buffers—an input latch and a register. They are designed to interface with 8080-, 8048, 8085, Z-80, and other popular microprocessors, with no interfacing logic.

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HANDLING THE DIFFERENT DATA FORMATS

Different data formats exist for many D/A converter products, all of which must be readily handled when interfacing with a microprocessor. Left-justified (fractional number $\times$ V_{REF}) and right-justified (positional number $\times$ $V_{REF}/1,024$) are the main ones. Initially, converter manufacturers favored a left-justified approach in which the most significant bit was labeled bit 1. Newer converters have changed to the right-justified approach to match the data format of microprocessor data buses. Nevertheless, the left-justified approach is still widely used. As previously mentioned, the MICRO-DAC family can readily handle left- and right-justified data formats with no additional interfacing circuitry.

When a MICRO-DAC converter uses either an 8-bit (two write cycles) or a 16-bit (one write cycle) data bus, all 10 locations of the converter's input latch are enabled on the first write cycle from the microprocessor. Depending on the data format, the next write cycle, if used, overwrites 2 of the 10 locations at the proper data rate.

Digital data is transferred from the input latch to the register internally in one of three ways: automatically when the second write byte occurs; through microprocessor control, which allows the updating of several D/A converters if this is necessary; and through the use of an external strobe.

The converter's CMOS logic levels are made compatible with those of TTL by a special biasing circuit that uses the parasitic NPN bipolar transistor available on a CMOS chip. The bipolar transistor supplies a base-emitter voltage (V_{BE}) that acts as a reference for the converter's digital inputs. It supplies an input threshold voltage of 2 V_{BE} that has the same amplitude as that of TTL devices.

Details of the biasing circuit are shown in *Figure 2*. Note that the reference N-channel field-effect transistor, Q1, is tied in a feedback loop so as to have its gate voltage biased at a level of V_{THN}, causing it to conduct the 60 μA shown in its drain circuit. The three NPN transistors in the loop add a voltage of 3 V_{BE} to V_{THN}. The output emitter-follower, Q2, causes a loss of V_{BE}, thus producing a voltage reference of 2 V_{BE} + V_{THN} for use by all of the logic input circuits. Each of the input stages has FETs like Q3, whose source has the digital input applied to it and whose geometry is the same as that of FET Q1. Like Q1, Q3 also has 60 μA of current feeding its drain. When the logic input voltage equals 2 V_{BE}, Q3 conducts, thereby pulling the input of a standard CMOS inverter to a low level. This 2 V_{BE} threshold continues to be independent of the D/A converter's supply voltage. 2 V_{BE} is the logic threshold voltage of standard TTL gates.

ACHIEVING HIGH ACCURACY

The design of the MICRO-DAC's resistor network is simple, even though it provides high levels of converter accuracy. *Figure 3* shows the current switching inverted R-2R ladder used, which consists of passive components.

The operation of the ladder network requires that all of the 2R legs connect to a 0V, or ground, level. This means that the external operational amplifier shown must have a minimal offset voltage. Only 1 mV of offset voltage can introduce a 0.01% linearity error into the converter's operation. Operational amplifiers like National's LM308A series are available with low offset voltages, and they require no zero adjustments.

When zero adjustment of the operational amplifier's offset voltage is required, a 1 kΩ resistor can be temporarily switched in between the converter's $I_{OUT\ 1}$ terminal (which is tied to the amplifier's negative input terminal) and ground. No DC balancing resistance should be used in the operational amplifier's grounded positive input terminal, since it may create errors. The operational amplifier, a BI-FET™ LF356 (made with bipolar and field-effect transistors), has a low input bias current which makes it an ideal choice for use as a current-to-voltage converter. The amplifier's offset voltage should be adjusted with a digital input of all zeros to force $I_{OUT\ 1}$ of the converter to a zero current level. The manually switched-in resistor provides a DC gain of about 15 to the offset voltage and makes the zeroing easier to sense. The converter chip provides the feedback resistor for good initial matching as well as for tracking over temperature.

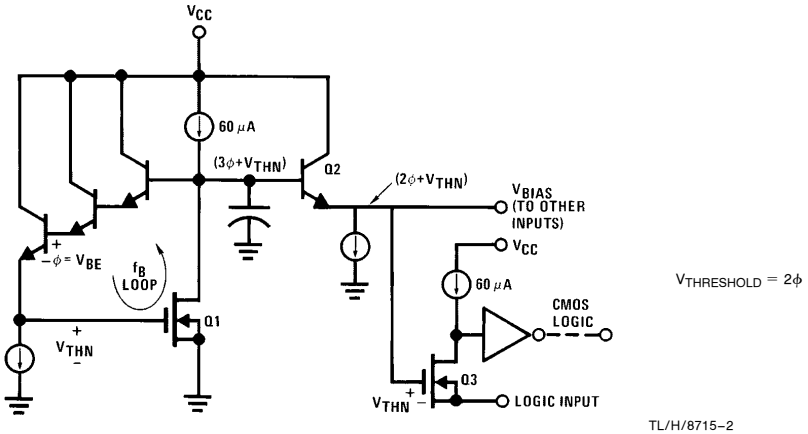

FIGURE 2. Threshold. This basic logic threshold loop provides the biasing for the MICRO-DAC family of MOS D/A converters to interface with TTL voltage levels. This circuit uses the parasitic bipolar structure, which delivers an input threshold of 2 V_{BE} to the biasing circuit.

LOOKING AT THE INSIDE

An examination of the internal details of the single-pole, double-throw current-mode switches employed in the converters shows that the N-channel FETs' gates are driven from the D/A converter's supply voltage. In contrast to a 5V supply, a 15V level reduces the FETs' on-resistances and thereby improves the converter's performance.

MICRO-DAC converters are relatively stable in gain and linearity during variations in the 15V supply voltage. For example, a drop in supply voltage all the way down to 5V results in a gain error of only −0.1%. Even smaller is the change in linearity error for the same supply voltage swing—just −0.005%.

The usefulness of a D/A converter can be determined by the magnitude of the linearity errors resulting from changes in the reference voltage. For applications, like multiplication, that require small values of reference voltage, small linearity errors are essential. In the case of the MICRO-DAC converters, reducing the reference voltage from 10V to 1V results in a worst-case linearity error change of approximately 0.005%.

Figure 4 shows a typical application of a MICRO-DAC as a unipolar voltage output device. This circuit inverts the negative reference voltage to a positive output, with a maximum value of 1,023/1,024 of the reference voltage multiplied by V_{REF}. The BI-FET operational amplifier used is an LF356 that slews and settles within 3 μs.

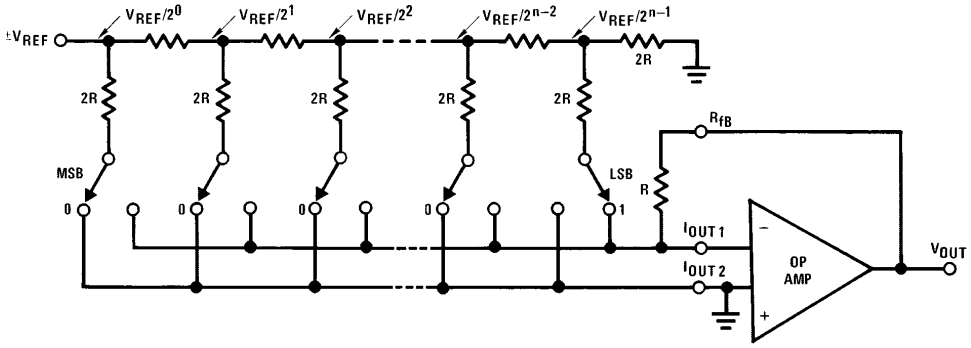

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FIGURE 3. Ladder. The current-switching, current-mode R-2R resistor ladder of the MICRO-DAC family of D/A converters is simple, yet provides high levels of converter accuracy. The external operational amplifier is chosen for minimal offset voltage for the least converter linearity error.

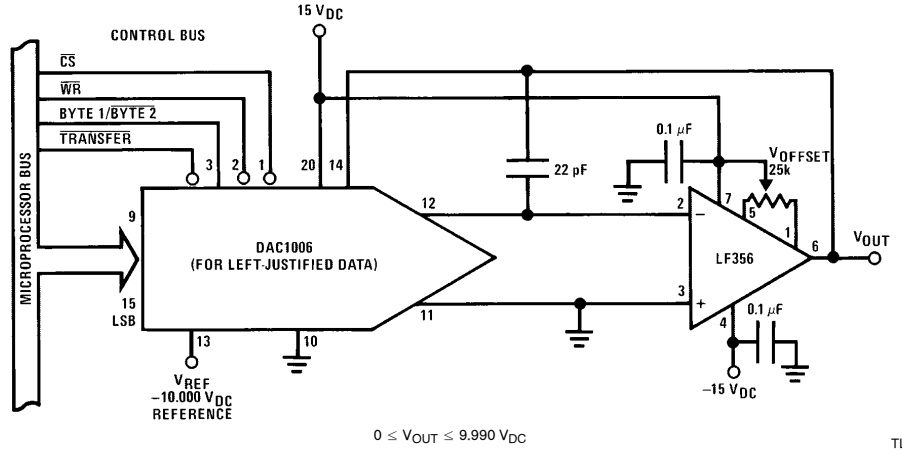

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FIGURE 4. Unipolar. In a typical unipolar application, a MICRO-DAC D/A converter inverts the negative reference voltage to a positive one. The positive output is 1,023/1,024 of the negative reference voltage multiplied by 9.990 V_{DC}. The output amplifier slews within 3 μs.

Operating the MICRO-DAC's R-2R resistor ladder in a voltage switching mode as shown in *Figure 5* gives a faster slewing and settling time—1.8 μs. The ladder is being used backwards. The reference voltage that is derived from the LM336 reference diode is applied to the $I_{OUT\ 1}$ pin. An output voltage is produced at the converter's pin 15 where the reference voltage was previously located in *Figure 4*. This output voltage ranges from 0 to (1,023/1,024) (2.49 V_{DC}). The LF356 operational amplifier used supplies a gain of a little more than 4 for an overall output voltage ranging from 0 to 1 LSB less than 10V (or 9.990 V_{DC}). The two compensating diodes at the ends of the full-scale adjustment potentiometer on the LM336 reference improve the temperature stability of the reference voltage.

For a bipolar output voltage, the circuit in *Figure 6* may be used. The bipolar output voltage results from adding or subtracting the reference voltage from the converter's output voltage.

The output of operational amplifier 1 ranges from 0 to $-1{,}023/1{,}024 \times V_{REF}$ (or $-9.990\ V_{DC}$). This voltage is then applied to operational amplifier 2, where a gain of -2 doubles the voltage range. A $-10\ V_{DC}$ offset voltage at the output of operational amplifier 2 is provided by adding the converter's reference voltage to the amplifier's input. Resistors R1, R2, and R3 in the circuit of operational amplifier 2 must stay matched even during temperature changes for the circuit of *Figure 6* in order to work properly.

The bipolar converter of *Figure 6* is adjusted by first entering a digital code composed of all zeros into the D/A converter. Next, the offset potentiometer of operational amplifier 1 is adjusted for a zero amplifier output voltage and then the offset potentiometer of operational amplifier 2 is adjusted for an amplifier output voltage of $-10{,}000\ V_{DC}$. Finally, a digital code of all 1s is applied, and the 500Ω potentiometer, in series with R_{fB} of the D/A converter, is adjusted for an output voltage of 9.98 V_{DC}. This voltage is $V_{REF} - 1$ LSB, where 1 LSB $= V_{REF}/512$.

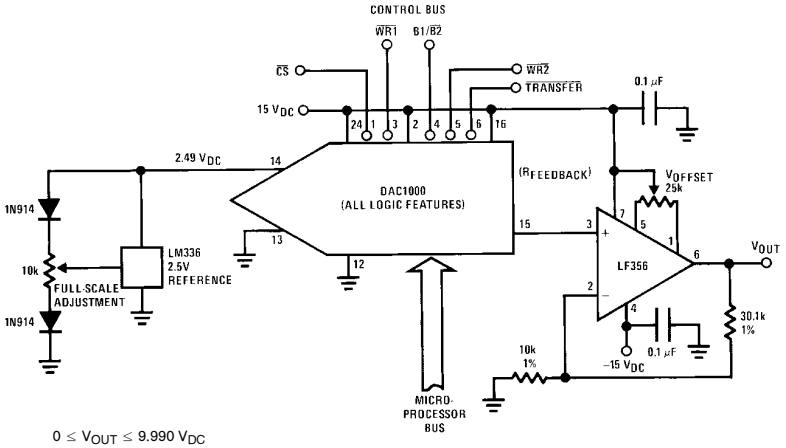

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FIGURE 5. Voltage mode. Operating the MICRO-DAC D/A converter's resistor ladder in a voltage-switching mode provides a faster slewing and settling time (1.8 μs) than that of *Figure 4*. Note that the D/A converter's R-2R ladder is being used backwards.

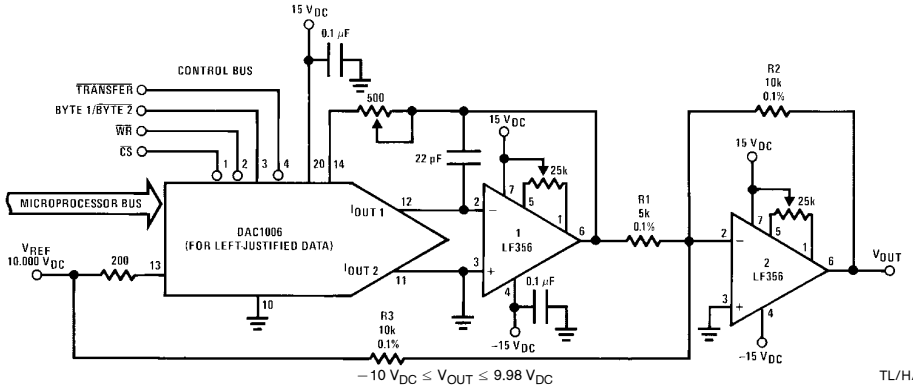

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FIGURE 6. Bipolar. By adding and subtracting the MICRO-DAC D/A converter's reference voltage from its output voltage, a bipolar output results. For this circuit to work properly, however, resistors R1, R2, and R3 in the circuit of op amp 2 must stay matched during temperature changes.

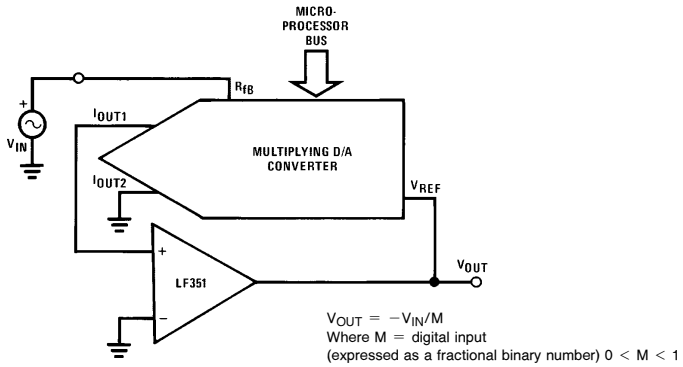

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FIGURE 7. Control. A MICRO-DAC D/A converter can be used for microprocessor control of an amplifier circuit. Since the converter has 4-quadrant multiplication capability, AC and DC signals can be handler. The feedback resistors referred to but not shown is in the converter.

USING THE MICROPROCESSOR FOR CONTROL

The MICRO-DAC multiplying D/A converter can be used in a microprocessor-controlled amplifier circuit as the feedback element for the amplifier *(Figure 7).* Since the converter has 4-quadrant multiplication capability, both AC and DC signals can be handled. The feedback resistor (not shown) is the internal one on the D/A converter's chip.

The D/A converter in *Figure 7* automatically provides an output voltage that causes the current from the converter's $I_{OUT\ 1}$ terminal to the V_{REF} terminal to equal the input current, $V_{IN}R_{fB}$. Note that when the microprocessor provides data to the D/A converter with the LSB set to a 1, a relatively large value of the reference voltage is needed to balance the input current. This value corresponds to the maximum gain of $-1{,}024$. The minimum gain of $-1{,}024/1{,}023$ is obtained for a D/A converter digital input of all 1s. In all, 1,023 gain steps are provided.

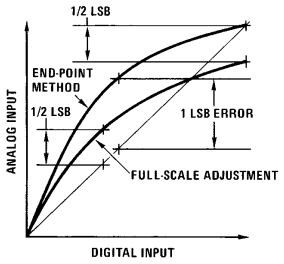
The addition of another amplifier in the converter's $I_{OUT\ 2}$ leg produces a microprocessor-controlled amplifier and attenuator. Compared with the gain of the circuit that appears in *Figure 7*, the gain here is noninverted and ranges from 0 to 1,022.

END POINT VS BEST-STRAIGHT-LINE

To maximize their product yields, manufacturers of digital-to-analog converters like to use a best-straight-line linearity guarantee. Unfortunately, this method is based on iteration of the zero and full-scale converter adjustments, so that errors are optimally split and equidistant from a straight line. To the converter user, a best-straight-line specification means that the D/A converter must undergo a sophisticated adjustment procedure for its linearity to be proven. Furthermore, each D/A converter has a different best-straight-line fit, making it necessary to adjust every one of them individually.

Another way to specify converter linearity is by an end-point method. For a current output converter, the offset voltage of the current-to-voltage output amplifier is first adjusted for 0V output. Then the converter is adjusted with a full-scale input digital code to produce a full-scale output voltage. This simple technique ensures that each of the 10-bit unit's 1,024 steps are within the stated linearity specification. Further, a pretrimmed output amplifier can be used to eliminate the zero offset adjustment, leaving only the full-scale adjustment.

The differences between the best-straight-line and end-point specification techniques are shown in the illustration (below), where a D/A converter with an error of 1 least significant bit is shown failing the end-point linearity test. Note that by readjusting the converter's full-scale output, the D/A converter's error is optimally split on either side of the ideal line in a best-straight-line fit, which is a time-consuming procedure, particularly when done on a large number of individual converters. For many an application where the D/A converter is already mounted on a printed circuit board, the end-point adjustment of zero and full-scale is much less time-consuming. Furthermore, this end-point procedure is a more stringent guarantee of converter linearity than the best-straight-line approach. The end-point method is used for D/A converters in the MICRODAC family.



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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408