COMMERCIAL

MRTL

INTEGRATED CIRCUITS

LOW-POWER
AND
MEDIUM-POWER

MC700 SERIES

MILLIWATT AND MEDIUM-POWER

COMMERCIAL MRTL

INTEGRATED CIRCUITS

In this series of MRTL logic circuits, medium and low-power devices are combined and specified for compatible application in commercial usages. Medium-power devices have loading factors normalized for compatibility with low-power for ease of mixing the two power levels in a system.

INDEX

DEVICE		POWER	PACKAGE
GATES			
MC703	3-Input Gate	MRTL	F,G
MC707	4-Input Gate	MRTL	F,G
MC710	Dual 2-Input Gate	mW MRTL	F,G
MC711	4-Input Gate	mW MRTL	F,G
MC714	Dual 2-Input Gate	MRTL	F,G
MC715	Dual 3-Input Gate	MRTL	F,G
MC717	Quad 2-Input Gate	mW MRTL	F
MC718	Dual 3-Input Gate	mW MRTL	F,G
MC719	Dual 4-Input Gate	mW MRTL	F
MC724	Quad 2-Input Gate	MRTL	F
MC725	Dual 4-Input Gate	MRTL	F
MC728	5-Input Gate	mW MRTL	F,G
MC729	5-Input Gate	MRTL	F,G
MC792	Triple 3-Input Gate	MRTL	F
MC793	Triple 3-Input Gate	mW MRTL	F
BUFFERS			
MC700	Buffer	MRTL	
MC709	Buffer	mW MRTL	F,G
MC781	Dual Buffer	mW MRTL	G
MC788	Dual 3-Input Buffer	MRTL	F
MC798	Dual 2-Input Buffer	mW MRTL	F
MC799	Dual Buffer	MRTL	F,G.
INVERTERS			
MC727	Quad Inverter	MRTL	F,G
MC789	Hex Inverter	MRTL	F
EXPANDERS			
MC721	Dual 2-Input Expander	mW MRTL	F,G
MC785	Quad 2-Input Expander	MRTL	F
MC786	Dual 4-Input Expander	MRTL	F

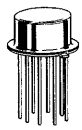
DEVICE		POWER	PACKAGE
COUNTER ADAPTERS			
MC701	Counter Adapter	MRTL	G
ADDERS			
MC704	Half Adder	MRTL	F,G
MC708	Half Adder	mW MRTL	F,G
MC712	Half Adder	mW MRTL	F,G
MC775	Dual Half Adder	MRTL	F
HALF-SHIFT REGISTERS			
MC705	Half-Shift Register with Inverter	MRTL	F,G
MC706	Half-Shift Register without Inverter	MRTL	F,G
MC783	Dual Half-Shift Register with Inverter	MRTL	F
MC784	Dual Half-Shift Register without Inverter	MRTL	F
FLIP-FLOPS			
MC702	R-S Flip-Flop	MRTL	G
MC713	Type D Flip-Flop	mW MRTL	F,G
MC720	J-K Flip-Flop	mW MRTL	F,G
MC722	J-K Flip-Flop	mW MRTL	F,G
MC723	J-K Flip-Flop	MRTL	F,G
MC726	J-K Flip-Flop	MRTL	F,G
MC774	J-K Flip-Flop	MRTL	G
MC776	Dual J-K Flip-Flop	mW MRTL	F
MC778	Dual Type D Flip-Flop	mW MRTL	F
MC782	J-K Flip-Flop	mW MRTL	G
MC790	Dual J-K Flip-Flop	MRTL	F
MC791	Dual J-K Flip-Flop	MRTL	F

NUMERICAL INDEX
(Functions and Characteristics)

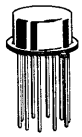
V_{CC} = 3.6 V ±10%, T_A = 25°C

Function	Type ① +15 to +55°C	Case	Output Loading Factor Each Output	Propagation Delay t_{pd} ns typ	Total Power Dissipation mW typ/pkg
MRTL					
Buffer	MC700	601, 606	80	20	25/50 ②
Counter Adapter	MC701	601	16	22	80
R-S Flip-Flop	MC702	601	13	14	32
3-Input NOR Gate	MC703	601, 606	16	12	28/7.5 ②
Half Adder	MC704	601, 606	16	14	65
Half-Shift Register	MC705	601, 606	13	22	75
Half-Shift Register (w/o Inverter)	MC706	601, 606	13	22	52
4-Input NOR Gate	MC707	601, 606	16	12	30/7.5 ②
Dual 2-Input NOR Gate	MC714	601, 606	16	•12	50/15 ②
Dual 3-Input NOR Gate	MC715	603, 606	16	12	55/15 ②
J-K Flip-Flop	MC723	601, 606	10	30	91/79 ④
Quad 2-Input NOR Gate	MC724	607	16	12	100/30 ②
Dual 4-Input NOR Gate	MC725	607	16	12	60/15 ②
J-K Flip-Flop	MC726	603, 606	16	35	100/86 ④
Quad Inverter	MC727	603, 606	16	12	87/30 ②
5-Input NOR Gate	MC729	601, 606	16	12	33/7.5 ②
Quad Exclusive OR Gate	MC771	607	16	12	28
J-K Flip-Flop	MC774	601	16	35	100/86 ④
Dual Half Adder	MC775	607	16	20	120
Dual Half Shift Register	MC783	607	13	22	140
Dual Half Shift Register w/Inverter	MC784	607	13	22	100
Quad 2-Input Expander	MC785	607	–	12	20/ – ②
Dual 4-Input Expander	MC786	607	–	12	20/ – ②
Dual 3-Input Buffer, non-inverting	MC788	607	80	24	145/56 ②
Hex Inverter	MC789	607	16	12	130/15 ②
Dual J-K Flip-Flop	MC790	607	10	35	182/158 ④
Dual J-K Flip-Flop	MC791	607	16	40	190/160 ④
Triple 3-Input NOR Gate	MC792	607	16	12	82/24 ②
Dual Full Adder	MC796	607	16	60	225
Dual Full Subtractor	MC797	607	16	60	225
Dual Buffer	MC799	603, 606	80	20	50/100 ②
Hex Expander	MC9719	607	–	12	13/ – ②
mW MRTL					
Half Adder	MC708	601, 606	4	60	19/12.5 ②
2-Input Buffer	MC709	601, 606	30	57	7.0/23 ②
Dual 2-Input NOR Gate	MC710	601, 606	4	27	10/2.5 ②
Dual 4-Input OR/NOR Gate	MC711	601, 606	4	60	8.0/5.5 ②
Half Adder	MC712	601, 606	4	66	15.5/10.5 ②
Type D Flip-Flop	MC713	601, 606	3	75	24/17.5 ③
Quad 2-Input NOR Gate	MC717	607	4	27	20/5.0 ②
Dual 3-Input NOR Gate	MC718	603, 606	4	27	12/2.5 ②
Dual 4-Input NOR Gate	MC719	607	4	27	13/2.5 ②
J-K Flip-Flop	MC720	601, 606	2	50	20.5/14.5 ④
Dual 2-Input Gate Expander	MC721	601, 606	–	27	3.0/ – ②
J-K Flip-Flop	MC722	603, 606	4	70	24/20 ④
5-Input NOR Gate	MC728	601, 606	4	27	7.5/1.0 ②
Dual J-K Flip-Flop	MC776	607	2	50	41/29 ④
Dual Type D Flip-Flop	MC778	607	3	60	48/35 ③
Dual Buffer	MC781	601	2	57	14/46 ②
J-K Flip-Flop	MC782	601	2	80	23/21 ④
Triple 3-Input NOR Gate	MC793	607	4	27	18/3.5 ②
Dual 2-Input Buffer	MC798	607	30	57	14/46 ②
Quad 2-Input Expander	MC9721	607	–	27	20/ – ②

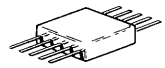
① G suffix denotes Metal Can, F suffix denotes Flat Package; i.e., MC718G = Metal Can, MC718F = Flat Package.
② Inputs High/Inputs Low.
③ Direct Set and Direct Clear Low, All Other Inputs High/All Inputs Low
④ Only Clock Input High/Inputs Low



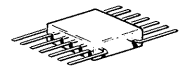
G SUFFIX
METAL PACKAGE
CASE 601
TO-99



G SUFFIX
METAL PACKAGE
CASE 603
TO-100

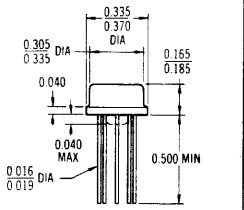


F SUFFIX
CERAMIC PACKAGE
CASE 606
TO-91

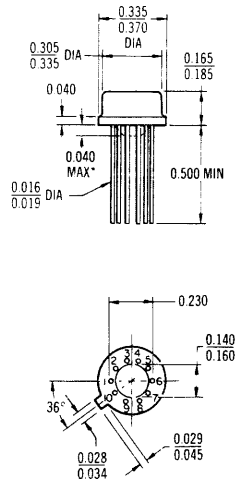


F SUFFIX
CERAMIC PACKAGE
CASE 607
TO-86

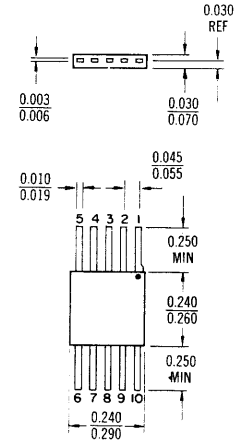
OUTLINE DIMENSIONS



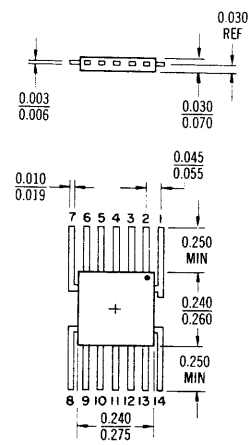
Pin 4 connected to case.



Pin 5 connected to case.



Lead 1 identified by color dot or by shoulder on lead. All leads electrically isolated from package.



Lead 1 identified by color dot or by elbow on lead. All leads electrically isolated from package.

TEST CONDITION TOLERANCES $V_{BOT} = \pm 10$ mV $V_{CC} = \pm 10$ mV $V_{in} = \pm 2$ mV $V_R = \pm 1\%$ $V_{on} = \pm 2$ mV $V_{off} = \pm 2$ mV

GENERAL RULES

- Testing tables shown in the MC900/800 MRTL and the MC908/808 mW MRTL sections of this volume may be utilized for testing MC700F and G commercial series devices. Pin number configurations are the same. MC700 series forcing functions and test limits are shown on the following page.
- The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the output.
- For ease of mixing MRTL and mW MRTL in the same system, the loading factors are normalized in accordance with the input currents being driven.
- Any number of gates may be paralleled; the input loading is increased by 1/4 load if only one gate is connected to V_{CC}.
- When paralleling gates with V_{CC} connected, a maximum of 4 outputs may be paralleled, increasing the input loading factor by 2.33.
- If the counter adapter is paralleled with another circuit, the output drive capability must be reduced by two loads. The reason for this drive reduction is the 1280-ohm resistance that connects the output terminals on the counter adapter.
- All unused input pins should be returned to ground.
- EXPANDER RULES:
  1. The MC785F, MC786F and MC9719F MRTL expanders can be used to expand medium-power MRTL output nodes only.
  2. When using the MC785F, MC786F or MC9719F subtract 0.5 from the output loading factor of the medium-power MRTL expanded gate for each expander node that is connected; also increase the input loading factor of the medium-power expanded gate by a factor of 1.33.

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Logic Input Voltage		±4.0	Vdc
Power Supply Voltage (Pulsed ≤ 1 second)		+12	Vdc
Operating Temperature Range MC700G/F Series	T_A	+15 to +55	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Milliwatt MRTL			MRTL			Unit
	+15°C	+25°C	+55°C	+15°C	+25°C	+55°C	
I_{A3}	0.420	0.420	0.420	–	–	–	mAdc min
I_{A4}	0.570	0.570	0.570	–	–	–	mAdc min
I_{A10}	–	–	–	1.65	1.65	1.65	mAdc min
I_{A13}	–	–	–	2.15	2.15	2.03	mAdc min
I_{A16}	–	–	–	2.65	2.65	2.5	mAdc min
I_{AB}	5.0	5.0	5.0	13.5	13.75	12.5	mAdc min
I_{CEX}	50	50	100	225	225	250	μAdc max
I_{in}	0.150	0.150	0.150	0.500	0.500	0.470	mAdc max
2 I_{in}	0.300	0.300	0.300	1.0	1.0	0.94	mAdc max
V_{out}	0.400	0.300	0.320	0.400	0.300	0.320	Vdc max
V_{CE}	0.220	0.230	0.320	0.300	0.290	0.320	Vdc max
TEST CONDITIONS							
V_{BOT}	1.8	1.8	1.8	1.8	1.8	1.8	Vdc
V_{CC}	3.6	3.6	3.6	3.6	3.6	3.6	Vdc
V_{in}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_{off}	0.475	0.460	0.430	0.475	0.460	0.430	Vdc
V_{on}	0.865	0.850	0.800	0.865	0.850	0.800	Vdc
V_R*	4600	4800	5000	640	640	640	Ohms

*Resistor value to V_{CC}

DEFINITIONS

I_{A2}, I_{A3}, I_{A4}, I_{A5}, I_{A10}, I_{A13}, I_{A16} Minimum available output current from a device with an output loading factor of 2, 3, 4, 5, 10, 13, and 16 respectively. Output voltage not to fall below the value of V_{on}.

I_{AB} Minimum available output current from a buffer. Output voltage not to fall below the value of V_{on}.

I_{AM} The maximum available current from the output of a Dual Gate.

I_{CEX} Collector current of a circuit when V_{in} is applied to the output pin and V_{off} is applied to the input pins.

I_{in} Maximum input current drawn by one input of a gate with V_{in} applied. All other gate inputs are returned to V_{BOT}.

1.8 I_{in} Current drawn from the V_{in} supply by the Toggle pin of the Flip-Flop.

2 I_{in} Maximum input current drawn by one input of a device with 2 bases internally tied together.

I_L Isolation leakage current.

I_O Output load current.

V_{BOT} A high value voltage applied to an input of a device to insure saturation of the driven transistor.

V_{CC} Supply voltage.

$V_{CE(sat)}$ Maximum saturation voltage with V_{BOT} applied to the input.

V_{in} Minimum high level voltage applied to the input of a device.

V_{LL} A supply voltage low enough to allow flow of leakage currents only.

V_{off} The maximum voltage which may be applied to an input terminal without turning the transistor on.

V_{on} The minimum voltage which may be applied to an input terminal that will turn the transistor on.

V_{out} The maximum output voltage with V_{on} applied to the input.

V_R Value of external resistor connected to V_{CC} for test purposes.
V_{RH} = highest node resistor value
V_{RL} = lowest node resistor value

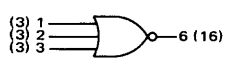
COMMERCIAL MRTL DEVICES AVAILABLE IN METAL CANS

The logic diagrams on these pages describe the MC700 Series Commercial MRTL integrated circuits available in metal cans, and permit quick selection of those circuits required for the implementation of a commercial system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical package power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal). Medium-power devices have loading factors normalized for compatability with the low-power devices for ease of mixing the two power levels in a system.

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the unit. Loading data are valid over the temperature range of +15 to +55°C, with V_{CC} = 3.6 V ±10%. For the TO-99 metal can, V_{CC} is applied to pin 8, with ground connected to pin 4. For the TO-100 metal can, V_{CC} is applied to pin 10, with ground connected to pin 5.

GATES

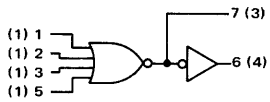
MC703G 3-Input Gate
(medium-power)



$6 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 28 mW (Input High)
7.5 mW (Inputs Low)

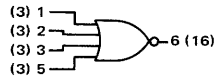
MC711G 4-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 3 + 5}$
$6 = 1 + 2 + 3 + 5$

t_{pd} = 60 ns
P_D = 8.0 mW (Input High)
5.5 mW (Inputs Low)

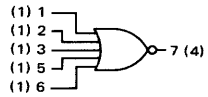
MC707G 4-Input Gate
(medium-power)



$6 = \overline{1 + 2 + 3 + 5}$

t_{pd} = 12 ns
P_D = 30 mW (Input High)
7.5 mW (Inputs Low)

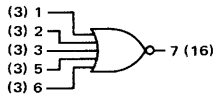
MC728G 5-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 27 ns
P_D = 7.5 mW (Input High)
1.0 mW (Inputs Low)

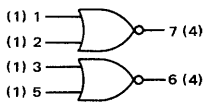
MC729G 5-Input Gate
(medium-power)



$7 = \overline{1 + 2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 33 mW (Input High)
7.5 mW (Inputs Low)

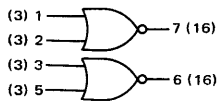
MC710G Dual 2-Input Gate
(milliwatt)



$7 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 10 mW (Input High)
2.5 mW (Inputs Low)

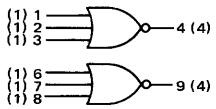
MC714G Dual 2-Input Gate
(medium-power)



$7 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 50 mW (Input High)
15 mW (Inputs Low)

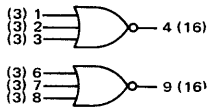
MC718G Dual 3-Input Gate
(milliwatt)



$4 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

MC715G Dual 3-Input Gate
(medium-power)

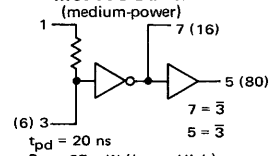


$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

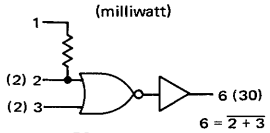
BUFFERS

MC700G Buffer
(medium-power)



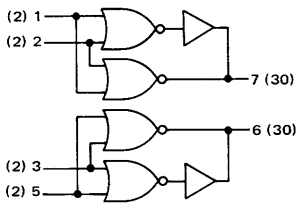
t_{pd} = 20 ns
P_D = 25 mW (Input High)
50 mW (Inputs Low)

MC709G Buffer
(milliwatt)



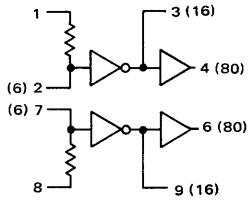
t_{pd} = 57 ns
P_D = 7.0 mW (Input High)
23 mW (Inputs Low)

MC781G Dual Buffer
(milliwatt)



7 = $\overline{1 + 2}$
t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

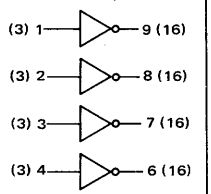
MC799G Dual Buffer
(medium-power)



3 = $\overline{2}$
4 = $\overline{2}$
t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

INVERTER

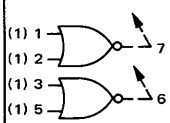
MC727G Quad Inverter
(medium-power)



9 = $\overline{1}$
t_{pd} = 12 ns
P_D = 87 mW (Input High)
30 mW (Inputs Low)

EXPANDER

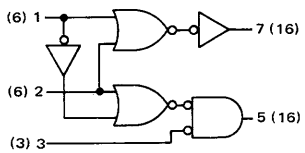
MC721G
Dual 2-Input Expander
(milliwatt)



t_{pd} = 27 ns
P_D = 3.0 mW (Input High)

COUNTER ADAPTER

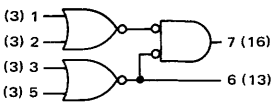
MC701G Counter Adapter
(medium-power)



7 = 1 + 2
5 = ($\overline{1}$ + 2) $\overline{3}$
t_{pd} = 22 ns
P_D = 80 mW

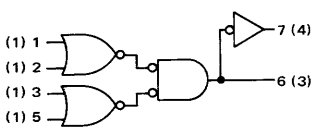
HALF ADDERS

MC704G Half Adder
(medium-power)



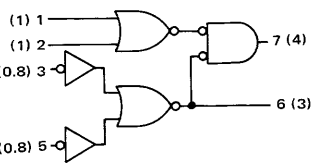
IF: 3 = $\overline{1}$, & 5 = $\overline{2}$
THEN: 6 = 1 • 2
7 = 1 • $\overline{2}$ + $\overline{1}$ • 2
7 = (1 + 2) (3 + 5)
6 = $\overline{3 + 5}$
t_{pd} = 14 ns
P_D = 65 mW

MC712G Half Adder
(milliwatt)



7 = (1 + 2) (3 + 5)
6 = $\overline{1}$ • $\overline{2}$ + $\overline{3}$ • $\overline{5}$
t_{pd} = 66 ns
P_D = 15.5 mW (Input High)
10.5 mW (Inputs Low)

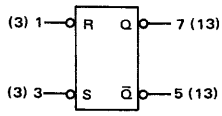
MC708G Half Adder
(milliwatt)



7 = ($\overline{3}$ + $\overline{5}$)
6 = (1 + 2) ($\overline{3}$ + $\overline{5}$)
t_{pd} = 60 ns
P_D = 19 mW (Input High)
12.5 mW (Inputs Low)

FLIP-FLOPS

MC702G R-S Flip-Flop
(medium-power)



t_{pd} = 14 ns
P_D = 32 mW

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC722 and MC726 only

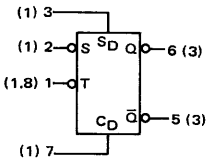
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1}	
S	C	Q	$\bar{Q}$
1	1	Q_n	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n⑤

1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC713G Type D Flip-Flop
(milliwatt)



t_{pd} = 75 ns
P_D = 24 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
17.5 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

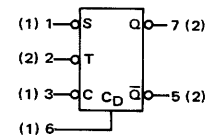
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

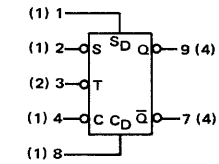
1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
   0 = low state
   1 = high state
   t_n = time period prior to negative transition of pulse
   t_{n+1} = time period subsequent to negative transition of clock pulse

MC720G J-K Flip-Flop
(milliwatt)



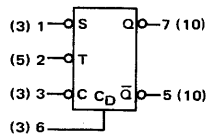
t_{pd} = 50 ns
P_D = 20.5 mW (Only Clock Input High)
14.5 mW (Inputs Low)

MC722G J-K Flip-Flop
(milliwatt)



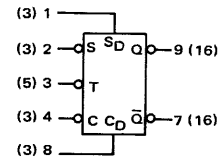
t_{pd} = 70 ns
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

MC723G J-K Flip-Flop
(medium-power)



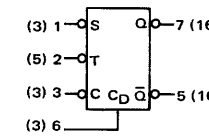
f_{Tog} = 4.0 MHz
t_{pd} = 30 ns
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC726G J-K Flip-Flop
(medium-power)



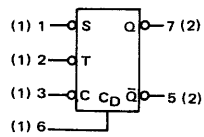
f_{Tog} = 4.0 MHz
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

MC774G J-K Flip-Flop
(medium-power)



t_{pd} = 35 ns
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

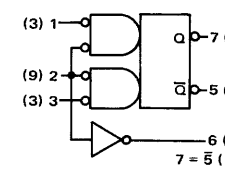
MC782G J-K Flip-Flop
(milliwatt)



t_{pd} = 80 ns
P_D = 23 mW (Only Clock Input High)
21 mW (Inputs Low)

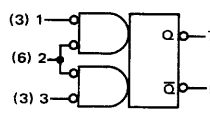
HALF-SHIFT REGISTERS

MC705G Half-Shift Register
(medium-power)



$7 = \overline{5\ (1 + 2)}$
$5 = \overline{7\ (2 + 3)}$
$6 = \bar{2}$
t_{pd} = 22 ns
P_D = 75 mW

MC706G Half-Shift Register
(without inverter—medium-power)



$7 = \overline{5\ (1 + 2)}$
$5 = \overline{7\ (2 + 3)}$
t_{pd} = 22 ns
P_D = 52 mW

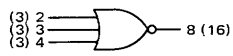
COMMERCIAL MRTL DEVICES AVAILABLE IN FLAT PACKAGES

The logic diagrams shown on these pages describe the MC700 Series Commercial MRTL integrated circuits available in flat packages, and permit quick selection of those circuits required for implementation of a commercial system design. Pertinent information such as logic equations, truth tables, typical propagation delay time (t_{pd}), typical power dissipation (P_D), pin numbers, input loading, and fan-out is shown for each device. The package pin number is shown adjacent to the terminal end. The number in parenthesis indicates the input loading factor (when on the circuit input terminal) or load driving ability – fan-out – (when on the circuit output terminal). Medium-power devices have loading factors normalized for compatability with the low-power devices for ease of mixing the two power levels in a system.

The number of load circuits that may be driven from an output is determined by the output loading factor and the sum of all input loading factors for the circuits connected to that output. The summation of the input loading factors should not exceed the stated drive capability of the unit. Loading data are valid over the temperature range of +15 to +55°C, with V_{CC} = 3.6 V ±10%. For the TO-91 flat package, V_{CC} is applied to pin 10, with ground connected to pin 5. For the TO-86 flat package, V_{CC} is applied to pin 14, with ground connected to pin 7.

GATES

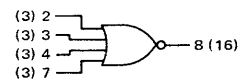
MC703F 3-Input Gate
(medium-power)



$8 = \overline{2 + 3 + 4}$

t_{pd} = 12 ns
P_D = 28 mW (Input High)
7.5 mW (Inputs Low)

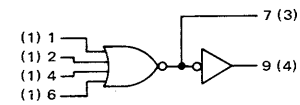
MC707F 4-Input Gate
(medium-power)



$8 = \overline{2 + 3 + 4 + 7}$

t_{pd} = 12 ns
P_D = 30 mW (Input High)
7.5 mW (Inputs Low)

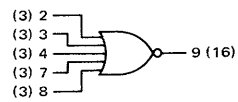
MC711F 4-Input Gate
(milliwatt)



$7 = \overline{1 + 2 + 4 + 6}$
$9 = 1 + 2 + 4 + 6$

t_{pd} = 60 ns
P_D = 8.0 mW (Input High)
5.5 mW (Inputs Low)

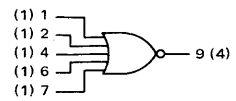
MC729F 5-Input Gate
(medium-power)



$9 = \overline{2 + 3 + 4 + 7 + 8}$

t_{pd} = 12 ns
P_D = 33 mW (Input High)
7.5 mW (Inputs Low)

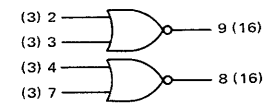
MC728F 5-Input Gate
(milliwatt)



$9 = \overline{1 + 2 + 4 + 6 + 7}$

t_{pd} = 27 ns
P_D = 7.5 mW (Input High)
1.0 mW (Inputs Low)

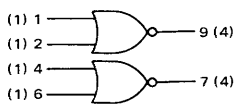
MC714F Dual 2-Input Gate
(medium-power)



$9 = \overline{2 + 3}$

t_{pd} = 12 ns
P_D = 50 mW (Input High)
15 mW (Inputs Low)

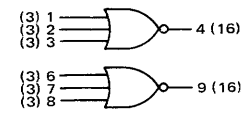
MC710F Dual 2-Input Gate
(milliwatt)



$9 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 10 mW (Input High)
2.5 mW (Inputs Low)

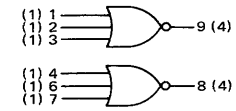
MC715F Dual 3-Input Gate
(medium-power)



$4 = \overline{1 + 2 + 3}$

t_{pd} = 12 ns
P_D = 55 mW (Input High)
15 mW (Inputs Low)

MC718F Dual 3-Input Gate
(milliwatt)



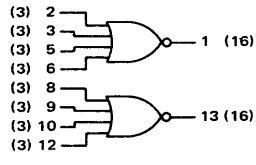
$9 = \overline{1 + 2 + 3}$

t_{pd} = 27 ns
P_D = 12 mW (Input High)
2.5 mW (Inputs Low)

(continued)

GATES (continued)

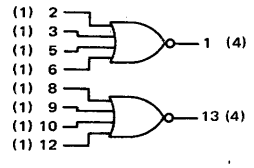
MC725F Dual 4-Input Gate
(medium-power)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 60 mW (Input High)
15 mW (Inputs Low)

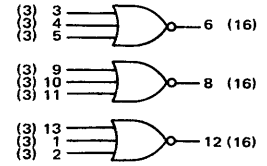
MC719F Dual 4-Input Gate
(milliwatt)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 27 ns
P_D = 13 mW (Input High)
2.5 mW (Inputs Low)

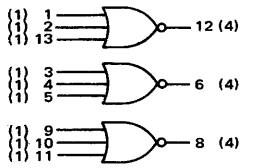
MC792F Triple 3-Input Gate
(medium-power)



$6 = \overline{3 + 4 + 5}$

t_{pd} = 12 ns
P_D = 82 mW (Input High)
24 mW (Inputs Low)

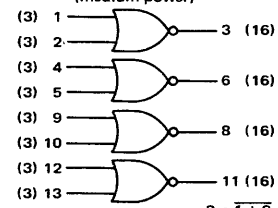
MC793F Triple 3-Input Gate
(milliwatt)



$12 = \overline{1 + 2 + 13}$

t_{pd} = 27 ns
P_D = 18 mW (Inputs High)
3.5 mW (Inputs Low)

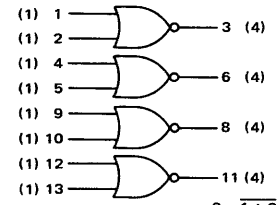
MC724F Quad 2-Input Gate
(medium-power)



$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 100 mW (Input High)
30 mW (Inputs Low)

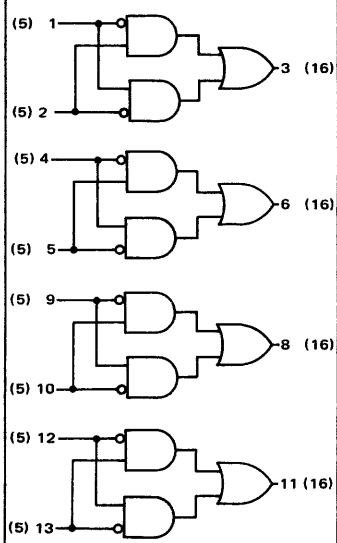
MC717F Quad 2-Input Gate
(milliwatt)



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
5.0 mW (Inputs Low)

MC771F Quad Exclusive "OR" Gate
(medium-power)

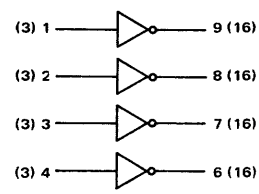


$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns
P_D = 87 mW

INVERTERS

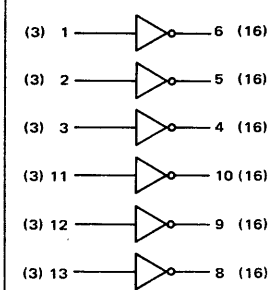
MC727F Quad Inverter
(medium-power)



$9 = \overline{1}$

t_{pd} = 12 ns
P_D = 87 mW (Input High)
30 mW (Inputs Low)

MC789F Hex Inverter
(medium-power)

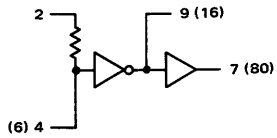


$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 130 mW (Input High)
15 mW (Inputs Low)

BUFFERS

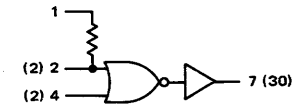
MC700F Buffer
(medium-power)



$9 = \overline{4}$
$7 = \overline{4}$

t_{pd} = 20 ns
P_D = 25 mW (Input High)
50 mW (Inputs Low)

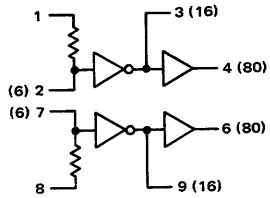
MC709F BUFFER
(milliwatt)



$7 = \overline{2 + 4}$

t_{pd} = 57 ns
P_D = 7.0 mW (Input High)
23 mW (Inputs Low)

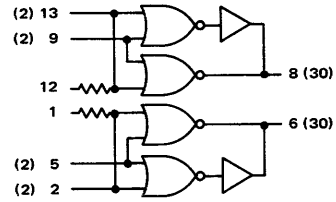
MC799F Dual Buffer
(medium-power)



$3 = \overline{2}$
$4 = \overline{2}$

t_{pd} = 20 ns
P_D = 50 mW (Input High)
100 mW (Inputs Low)

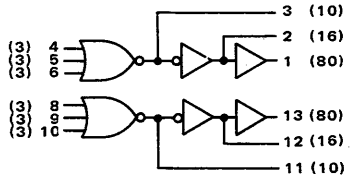
MC798F Dual 2-Input Buffer
(milliwatt)



$8 = \overline{9 + 13}$

t_{pd} = 57 ns
P_D = 14 mW (Input High)
46 mW (Inputs Low)

MC788F Dual 3-Input Buffer
(non-inverting—medium-power)



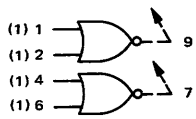
t_{pd} = 24 ns
P_D = 145 mW (Input High)
56 mW (Inputs Low)

$3 = \overline{4 + 5 + 6}$
$2 = 4 + 5 + 6$
$1 = 4 + 5 + 6$

Outputs 1, 2 or 3 may not be used simultaneously.
Outputs 11, 12, or 13 may not be used simultaneously.

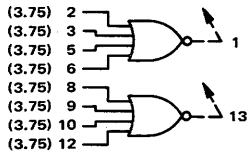
EXPANDERS

MC721F Dual 2-Input Expander
(milliwatt)



t_{pd} = 27 ns
P_D = 3.0 mW (Input High)

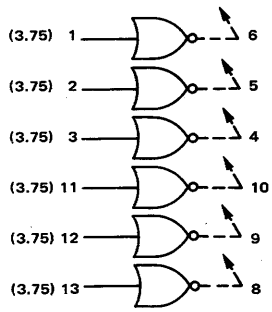
MC786F Dual 4-Input Expander
(medium-power)



$1 = \overline{2 + 3 + 5 + 6}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

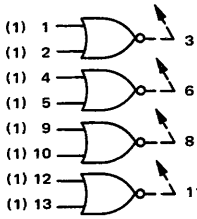
MC9719F Hex Expanders
(medium-power)



$6 = \overline{1}$

t_{pd} = 12 ns
P_D = 13 mW (Input High)
Negligible (Inputs Low)

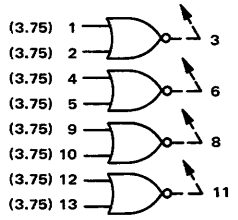
MC9721F Quad 2-Input Expander
(milliwatt)



$3 = \overline{1 + 2}$

t_{pd} = 27 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

MC785F Quad 2-Input Expander
(medium-power)

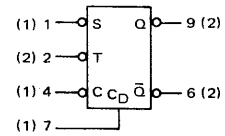


$3 = \overline{1 + 2}$

t_{pd} = 12 ns
P_D = 20 mW (Input High)
Negligible (Inputs Low)

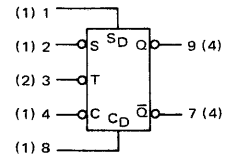
FLIP-FLOPS

MC720F J-K Flip-Flop
(milliwatt)



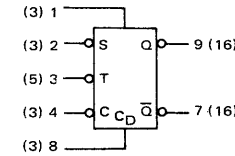
t_{pd} = 50 ns
P_D = 20.5 mW (Only Clock Input High)
14.5 mW (Inputs Low)

MC722F J-K Flip-Flop
(milliwatt)



t_{pd} = 70 ns
P_D = 24 mW (Only Clock Input High)
20 mW (Inputs Low)

MC726F J-K Flip-Flop
(medium-power)



f_{Tog} = 4.0 MHz
t_{pd} = 35 ns
P_D = 100 mW (Only Clock Input High)
86 mW (Inputs Low)

J-K FLIP-FLOP TRUTH TABLES

DIRECT INPUT OPERATION ① MC722 and MC726 only

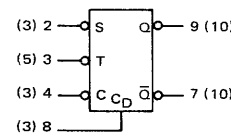
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③ all types

t_n ④		t_{n+1} ④	
S	C	Q	$\bar{Q}$
1	1	Q_n ⑤	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n ⑤

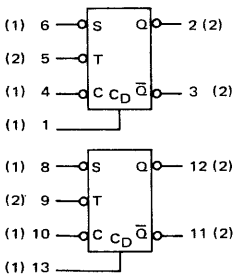
1. Clock (T) to remain unchanged.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
4. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
5. Q_n is the state of the Q output in the time period t_n.

MC723F J-K Flip-Flop
(medium-power)



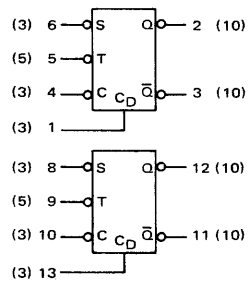
f_{Tog} = 4.0 MHz
t_{pd} = 30 ns
P_D = 91 mW (Only Clock Input High)
79 mW (Inputs Low)

MC776F Dual J-K Flip-Flop
(milliwatt)



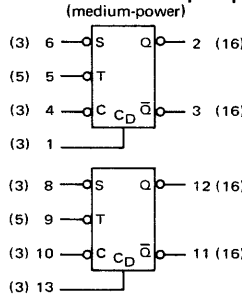
t_{pd} = 50 ns f_{Tog} = 3.0 MHz min
P_D = 41 mW (Only Clock Input High)
29 mW (Inputs Low)

MC790F Dual J-K Flip-Flop
(medium-power)



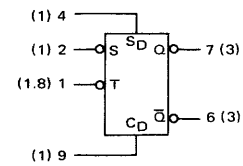
t_{pd} = 35 ns f_{Tog} = 4.0 MHz
P_D = 182 mW (Only Clock Input High)
158 mW (Inputs Low)

MC791F Dual J-K Flip-Flop
(medium-power)



t_{pd} = 40 ns
P_D = 190 mW (Only Clock Input High)
160 mW (Inputs Low)

MC713F Type D Flip-Flop
(milliwatt)



t_{pd} = 75 ns
P_D = 24 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
17.5 mW (All Inputs Low)

DIRECT INPUT OPERATION ①

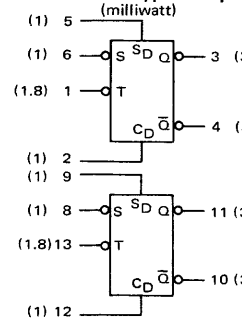
S_D	C_D	Q	$\bar{Q}$
0	0	②	②
1	0	1	0
0	1	0	1
1	1	0	0

CLOCKED INPUT OPERATION ③

t_n	t_{n+1}	
S	Q	$\bar{Q}$
1	1	0
0	0	1

1. Clock (T input) must be high.
2. The output state will not change when the input state goes from $S_D = \bar{C}_D$ to $S_D = C_D = 0$. The output state cannot be predetermined in the case where the input goes from $S_D = C_D = 1$ to $S_D = C_D = 0$.
3. Direct inputs (C_D and S_D) must be low.
   0 = low state
   1 = high state
   t_n = time period prior to negative transition of pulse
   t_{n+1} = time period subsequent to negative transition of clock pulse

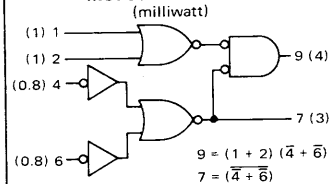
MC778F Dual Type D Flip-Flop
(milliwatt)



t_{pd} = 60 ns f_{Tog} = 1.0 MHz
P_D = 48 mW (Direct Set and Direct Clear Inputs Low, All other Inputs High)
35 mW (All Inputs Low)

HALF ADDERS

MC708F Half-Adder
(milliwatt)

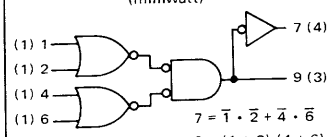


$9 = (1 + 2)(\overline{4} + \overline{6})$

$7 = (\overline{\overline{4} + \overline{6}})$

t_{pd} = 60 ns
P_D = 19 mW (Input High)
12.5 mW (Inputs Low)

MC712F Half-Adder
(milliwatt)

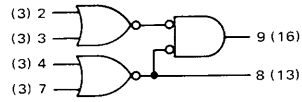


$7 = \overline{1} \cdot \overline{2} + \overline{4} \cdot \overline{6}$

$9 = (1 + 2)(4 + 6)$

t_{pd} = 66 ns
P_D = 15.5 mW (Input High)
10.5 mW (Inputs Low)

MC704F Half Adder
(medium-power)



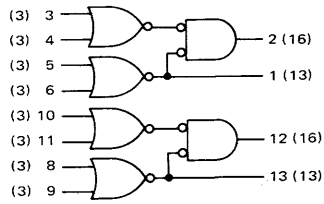
$9 = (2+3)(4 + 7)$

$8 = \overline{4 + 7}$

IF: $4 = \overline{2}$, & $7 = \overline{3}$
THEN: $8 = 2 \cdot 3$
$9 = 2 \cdot \overline{3} + \overline{2} \cdot 3$

t_{pd} = 14 ns
P_D = 65 mW

MC775F Dual Half Adder
(medium-power)



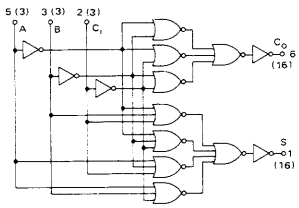
$2 = (3 + 4)(5 + 6)$

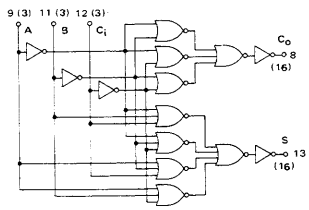
$1 = \overline{5 + 6}$

t_{pd} = 20 ns
P_D = 120 mW

FULL ADDER

MC796F Dual Full Adder





$C_o = ABC_i + AB\overline{C_i} + A\overline{B}C_i + \overline{A}BC_i$

$S = ABC_i + AB\overline{C_i} + A\overline{B}\overline{C_i} + \overline{A}B\overline{C_i}$

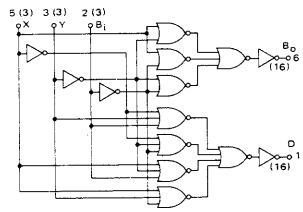
t_{pd} = 60 ns
P_D = 225 mW

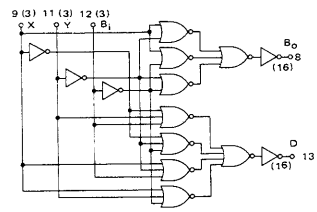
TRUTH TABLE

Input Logic Level			Output Logic Level	
A	B	C_i	S	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FULL SUBTRACTOR

MC797F Dual Full Subtractor





$D = YXB_i + Y\overline{X}\overline{B_i} + \overline{Y}X\overline{B_i} + \overline{Y}\overline{X}B_i$

$B_o = \overline{Y}\overline{X}B_i + Y\overline{X}\overline{B_i} + Y\overline{X}B_i + YXB_i$

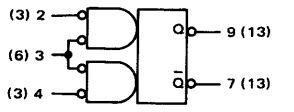
t_{pd} = 60 ns
P_D = 225 mW

TRUTH TABLE

Input Logic Level			Output Logic Level	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

HALF-SHIFT REGISTERS

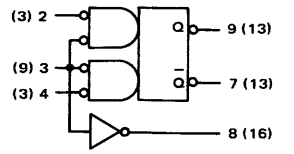
MC706F Half-Shift Register
(without inverter—medium-power)



t_{pd} = 22 ns
P_D = 52 mW

$9 = \overline{7}\,(2 + 3)$
$7 = \overline{9}\,(3 + 4)$

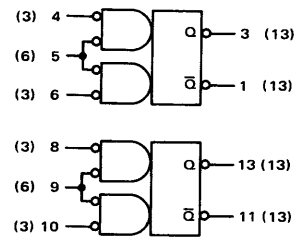
MC705F Half-Shift Register
(with inverter—medium-power)



t_{pd} = 22 ns
P_D = 75 mW

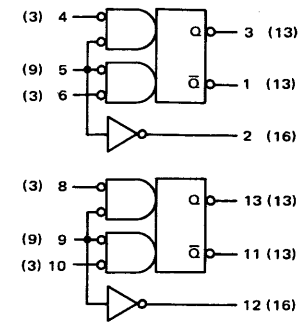
$9 = \overline{7}\,(2 + 3)$
$7 = \overline{9}\,(3 + 4)$
$8 = \overline{3}$

MC784F Dual Half-Shift Register
(without inverter—medium-power)



$3 = \overline{1}\,(4 + 5)$
$1 = \overline{3}\,(6 + 5)$
t_{pd} = 22 ns
P_D = 100 mW

MC783F Dual Half-Shift Register
(with inverter—medium-power)



$3 = \overline{1}\,(4 + 5)$
$1 = \overline{3}\,(6 + 5)$
t_{pd} = 22 ns
P_D = 140 mW