A. General Description —

HT–6560B is a VL_Bus Enhanced IDE Controller which provides a control logic and data path between 486, 386 VL_Bus and IDE drives. The HT–6560B is fully compatible with the ANSI ATA revision 4a specification for IDE hard disk operation and VESA VL_Bus revision 1.0 specification for local bus PC drives. The HT–6560B is a high performance and fully design for IDE application. At the host CPU interface, HT–6560B provides a posted write and pre-fetched read fully 32 bits data path. It can operate up to 50 MHz and zero wait-state cycle. Double word read and write operations are provided. It also allows concurrent IDE and CPU memory operations to maximize system performance. Flexible IDE drive interface timing selection. Power on reset latch the adequate IDE active and recovery time into configuration register. HT–6560B also allows you to detect IDE performance and change the configuration register by software program.

B. Features —

- Pin-to-pin backward compatible with HT–6560A VL_Bus IDE controller
- IDE interface to 486 and 386 DX/SX local bus
- VESA VL_Bus rev 1.0 compatible
- Connects directly to VL_Bus and IDE interface, no extra TTL needed
- Supports 16 bits and 32 bits data transfer
- Supports pipeline pre-fetched data reads and posted writes for concurrent disk and host operations
- Supports 4 layer R/W FIFO (32 bits × 4)
- Supports two IDE channels, up to 4 IDE drivers
- Supports ATAPI CD ROM and TAPE DRIVER protocal
- Direct interface to all hard disk drives that are ANSI ATA compatible
- Programmable command active and cycle time
- Supports IOCHRDY in PIO mode
- Supports mode 3, mode 4 PIO data transfer
- 100-pin PQFP package
- Software driver supported

C. Block Diagram —

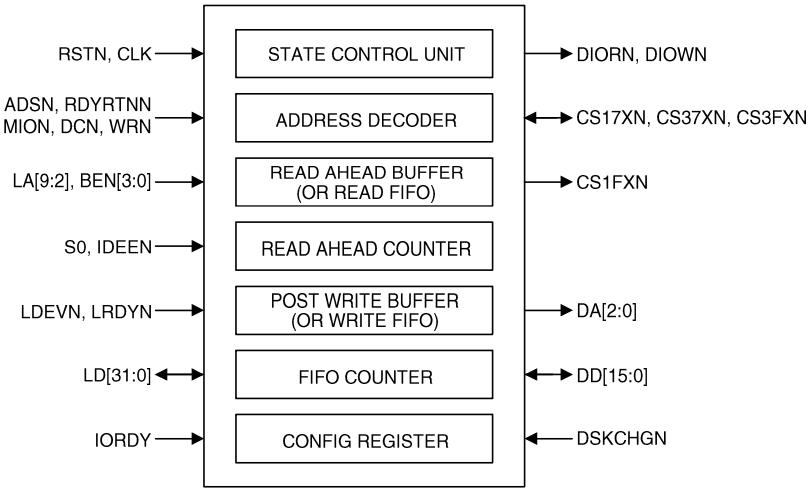
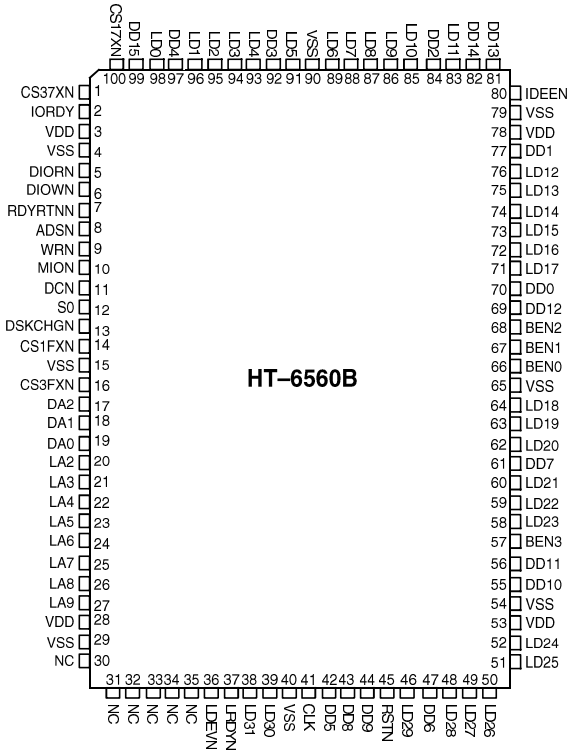


Fig.1

D. Pin Assignment —



E. Pin Description —

Pin No.	Pin Name	I/O	Description
1	CS37XN	I/O	Secondary drive chip select 3 is normally an active low output pin to select the control block registers in the drive. During power on reset, this is an input pin to set DIORN/DIOWN cycle time and sampled on the rising edge of RSTN.
2	IORDY	I	This signal is negated to extend the host transfer cycle of any host command or data register access when the drive is not ready to respond to a data transfer request. When IORDY is not negated, IOCHRDY is in a high impedance state.
3,28,53,78	VDD	—	+5V POWER.
4,15,29,40,54, 65,79,90	VSS	—	GROUND.
5	DIORN	O	Drive I/O read is an active low output which enables data to be read from the drive. The duration and repetition rate of DIORN cycles is determined by the type of IDE drive and programmed by HT–6560B.
6	DIOWN	O	Drive I/O write is an active low output which enables data to be written to the drive. The duration and repetition rate of DIOWN cycles is determined by the type of IDE drive and programmed by HT–6560B.
7	RDYRTNN	I	Ready return is an active low signal which indicates the end of the current host CUP transfer.
8	ADSN	I	Address strobe is an active low input signal which indicates that there is a valid address and command on the bus.
9	WRN	I	Write (active high) or read (active low) is an input which distinguishes between write and read cycles.
10	MION	I	Memory (active high) or I/O (active low) is an input which distinguished between momory and I/O cycles.

Pin No.	Pin Name	I/O	Description
11	DCN	I	Data (active high) or control (active low) is an input which is used to distinguish between I/O and interrupt or halt cycles.
12	S0	I	Primary or secondary I/O port selection input. Level low for primary, level high for secondary I/O port.
13	DSKCHGN	I	Disk change is an input which comes from floopy diskette drive connector pin 34.
14	CS1FXN	I/O	Primary drive chip select 1 is active low output pin to select the command block registers in the drive.
16	CS3FXN	I/O	Primary drive chip select 3 is normal an active low output pin to select the control block registers in the drive. During power on reset, this is an input pin to set DIORN/DIOWN cycle time and sampled on the rising edge of RSTN.
17	DA2	I/O	Drive address, bit 2 is an output to the IDE connector for register selection in the drive.
18	DA1	I/O	Drive address, bit 1 is an output pin to the IDE connector for register selection in the drive.
19	DA0	I/O	Drive address, bit 0 is an output pin to the IDE connector for register selection in the drive.
20~27	LA2~LA9	I	These are the host address bits 2 through 9 from the host address bus.
30~35	NC	—	No connection pins.
36	LDEVN	O	Local device is an active low output which indicates that the current host CPU command cycle is a valid HT–6560B address.
37	LRDYN	Tri-O	Local ready is an active low output which indicates that the current host CPU transfer has completed. As the current cycle is completed, the LRDYN will immediately pull low and remain active for one T-state.

Pin No.	Pin Name	I/O	Description
38,39,46,48~52, 58~60,62~64, 71~76,83,85~89 ,91,93~96,98	LD31~LD0	I/O	Host data is the 32 bits bi-directional data bus which connects to the host CPU LD[7:0] define the lowest data byte while LD[31:24] define the most significant data byte. The active bytes on a CPU transfer are specified by the BEN[3:0] signals. The LD bus is normally in high impedance state and is driven only after T2 state of HT–6560B read cycles.
41	CLK	I	VL_Bus clock.
42~44,47,55,56, 61,69,70,77,81, 82,84,92,97,99	DD15~DD0	I/O	Drive data bus, bits 15 through 0, are the 16 bits bi-directional data bus which connects to the IDE drive. DD[7:0] define the lowest data byte while DD[15:8] define the most significant data byte.
45	RSTN	I	System reset is an active low input.
57,66~68	BEN3~0	I	Byte enable bits 0 through 3 from the host CPU address bus. These inputs are active low and specify which bytes will be valid for host read/write data transfers.
80	IDEEN	I	IDE enable is an active high input which enable the HT–6560B for drive operation. Low input which disables HT–6560B.
100	CS17XN	I/O	Secondary drive chip select 1 is normally an active low output pin to select the control block registers in the drive. During power on reset, this is an input pin for test and sampled on the rising edge of RSTN.

F. Absolute Maximum Ratings —

Parameter		Symbol	Minimum	Maximum	Unit
Supply Voltage		V_{DD}	–0.5	6	V
Input/Output Voltage		V_I,V_O	V_{SS}–0.5	V_{DD}+0.5	V
Storage Temperature	Plastic	T_{STG}	–40	125	°C
Temperature Under Bias	Plastic	T_{BIAS}	–40	85	°C

G. Recommended Operating Conditions —

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage for Normal Input	V_{IH}	2.2	—	—	V
Input Low Voltage for Normal Input	V_{IL}	—	—	0.8	V
Operating Temperature	T_A	0	25	70	°C

H. DC Characteristics —

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DDS}	Power Supply Current	Steady state.	—	—	0.2	mA
V_{OH1}	Output High Voltage for Normal Output (LD[31:0])	I_{OH}=2.5mA		4.5		V
V_{OH2}	Output High Voltage for Driver Output (DD[15:0], DA[2:0], CS1FXN, CS3FXN, CS17XN, CS37XN, DIORN, DIOWN, LDEVN, LRDYN)	I_{OH}=4.5mA		4.5		V
V_{OL1}	Output Low Voltage for Normal Output (LD[31:0])	I_{OL}=8mA		0.5		V
V_{OL2}	Output Low Voltage for Driver Output (DD[15:0], DA[2:0], CS1FXN, CS3FXN, CS17XN, CS337XN, DIORN, DIOWN, LDEVN, LRDYN)	I_{OL}=11mA		0.5		V
R_P	Input Pull-Up Resistor			440K		Ω
R_N	Input Pull-Down Resistor			255K		Ω

I. Functional Description —

The HT–6560B contains seven major blocks as shown in fig.1. They are state control unit, address decoder, read ahead buffer (read FIFO), read ahead counter, posted write buffer (write FIFO), FIFO counter and configuration register.

The state control unit contains a state machine which controls all of the read/write timing and data swapping between CPU and IDE drives. The address decoder connects to VL_Bus directly, decodes valid address of the HT–6560B configuration register and IDE drive registers. Read ahead buffer (or read FIFO) and posted write buffer (or write FIFO) which can accelerate the data read/write speed. User can set the command active and recovery time to optimize the IDE performance by programming the configuration register. In addition to, you can detect and set primary or secordary IDE port through the configuration register.

1. Restet Initialization

Siganl Name	Signal State During Reset
CS1FXN	1
CS3FXN	Hight-Impedance
CS17XN	Hight-Impedance
CS37XN	Hight-Impedance
LDEVN	1
DIOWN	1
DIORN	1
LRDYN	High-Impedance
DA[2:0]	1
LD[31:0]	High-Impedance
DD[15:0]	High-Impedance

2. Host Interface

a. CPU cycle definition:

MION	DCN	WRN	Address Space	IDE Cycle
0	1	0	1F0h-1F7h and 3F6h-3F7h for primary drive. 170h-177h and 376h-377h for secondary drive.	DIORN CYCLE
0	1	1	1F0h-1F7h and 3F6h-3F7h for primary drive. 170h-177h and 376h-377h for secondary drive.	DIOWN CYCLE
0	0	0	Don't care.	NOP
0	0	1	Don't care.	NOP
1	0	0	Don't care.	NOP
1	0	1	Don't care.	NOP
1	1	0	Don't care.	NOP
1	1	1	Don't care.	NOP

b. HT–6560B write data operation:

CPU Write Byte Enable				HT–6560A Input Data			
BEN3	BEN2	BEN1	BEN0	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]
0	0	0	0	valid	valid	valid	valid
0	1	1	1	valid	X	X	X
1	0	1	1	X	valid	X	X
1	1	0	0	X	X	valid	valid
1	1	0	1	X	X	valid	X
1	1	1	0	X	X	X	vaild

c. HT–6560B read data operation:

CPU Read Byte Enable				HT–6560B Output Data			
BEN3	BEN2	BEN1	BEN0	LD[31:24]	LD[23:16]	LD[15:8]	LD[7:0]
0	0	0	0	valid	valid	valid	valid
0	1	1	1	valid	same as LD[31:24]	same as LD[31:24]	same as LD[31:24]
1	0	1	1	same as LD[23:16]	valid	same as LD[23:16]	same as LD[23:16]
1	1	0	0	same as LD[15:0]		valid	
1	1	0	1	same as LD[15:8]	same as LD[15:8]	valid	same as LD[15:8]
1	1	1	0	same as LD[7:0]	same as LD[7:0]	same as LD[7:0]	valid

3. IDE Interface

a. DA[2:0] generation:

LA2	BEN[3:0]	DA[2:0]
0	XX00	000
0	XX01	001
0	X011	010
0	0111	011
1	XXX0	100
1	XX01	101
1	X011	110
1	0111	111

b. Drive select signal operation:

Signal Name	Address Range
CS1FXN	1F0h-1F7h for primary drive.
CS3FXN	3F6h-3F7h for primary drive.
CS17XN	170h-177h for secondary drive.
CS37XN	376h-377h for secondary drive.

J. HT–6560B Register Setting —

1. Active Time and Recovery Time Setting

a. Hardware setting:

There are four kind of cycle times that you can select during power on reset.

CS3FXN	CS37XN	ACTIVE (Cycles)	RECOVERY (Cycles)
0	0	15	15
1	0	10	10
0	1	7	7
1	1	4	4

b. Software setting:

After power on reset, you still can program the configuration register by following procedures:

- Read I/O port 3E6h four times to turn on configuration mode.
- Wrtie 8 bits data to I/O prot 1F6h for primary port or 176h for secondary port.

Recovery time:

Data	bit7	bit6	bit5	bit4	Cycles
	0	0	1	0	2
	0	0	1	1	3
			⇓		
	1	1	1	1	15
	0	0	0	0	16

Active time:

Data	bit3	bit2	bit1	bit0	Cycles
	0	0	1	0	2
	0	0	1	1	3
			⇓		
	1	1	1	1	15

- Read I/O port 1F7h for primary port or 177h for secondary port one time to clear configuration mode.

2. Primary and Secondary I/O Port Setting

   a. Hardware setting:

      During power on reset, this register can be latched from the S0 pin.

S0	I/O Port
0	1F0~7h, 3F6~7h, 3E6h (primary)
1	170~7h, 376~7h, 3E6h (secondary)

   b. Software setting:

      After power on reset, you can program the I/O port register by writing port 3E6h.

bit 0	I/O Port
0	1F0~7h, 3F6~7h, 3E6h (primary)
1	170~7h, 376~7h, 3E6h (secondary)

      This bit also can be read in data bit0 from port 3E6h.

3. Register 3E6h:

   bit 0: PSPORT
   Primary and secondary I/O port setting

   bit 1: reserved

   bit 2: FIFOEN
   This enable FIFO function

   bit 3: reserved

   bit 4: reserved

   bit 5: PFTCH
   This enable pre-fetched data read function

K. Application Circuit —