HITACHI MOS LSI
HD61885, HD61887

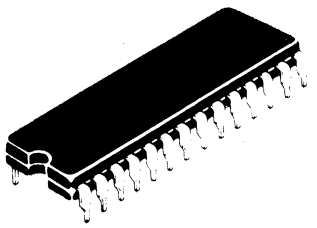
HITACHI

Single-chip CMOS Speech Synthesis LSI

HD61885 is one chip CMOS speech synthesis LSI based on PARCOR method.

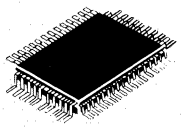
This LSI consists of PARCOR speech synthesizer and ROM (32kbit) which memorizes speech signal information. Besides, D/A converter, keyboard interface, and external ROM interface are included.

HD61885



(DP—28)

HD61887

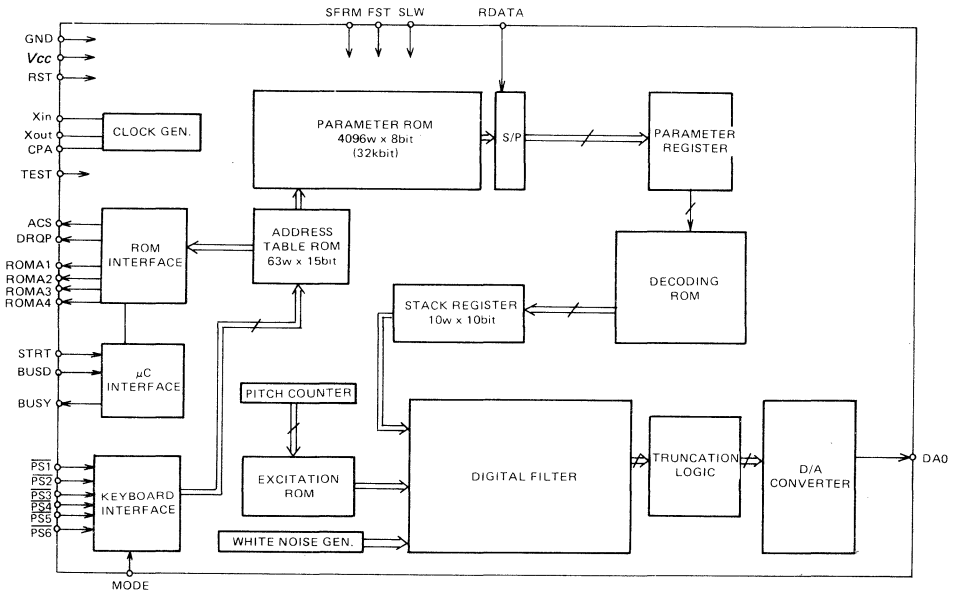


(FP—54)

■ FEATURES

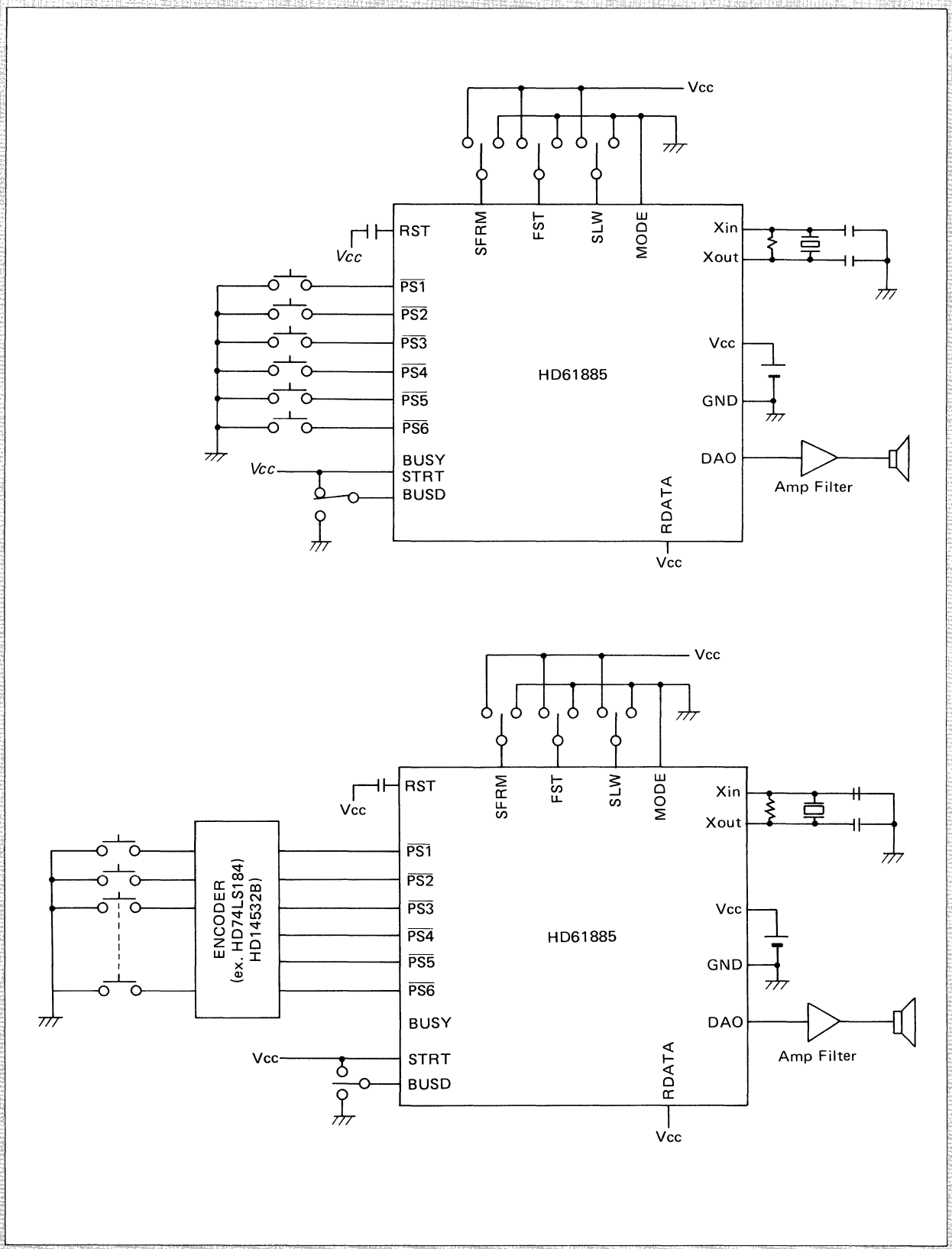
- Selectable bit rates; (1.25 ~ 9.9 kbit/sec.)
- Utterance duration; 26 sec. max.
- Utterance words; 63 words. max.
- Expansion; Utterance duration and words can be expanded easily by the addition of external ROM (HD44881).
  Adding one ROM makes utterance duration 100 second max.
  (Expansion of words is not specified.)
  Max. 16 ROM's can be connected.
- Variable utterance speed; −25%, 0%, +25%.
  Selectable double or half speed mode.
  (This is determined when speech is analyzed.)
- Low power dissipation by using CMOS process.
  Stand-by mode is available.
- Single 5V power supply operation.
  (Operation range is min. 3.6V.)
- Outline
  Plastic DIP – 28 (HD61885)
  Plastic Flat – 54 (HD61887)

■ BLOCK DIAGRAM OF SYNTHESIZER



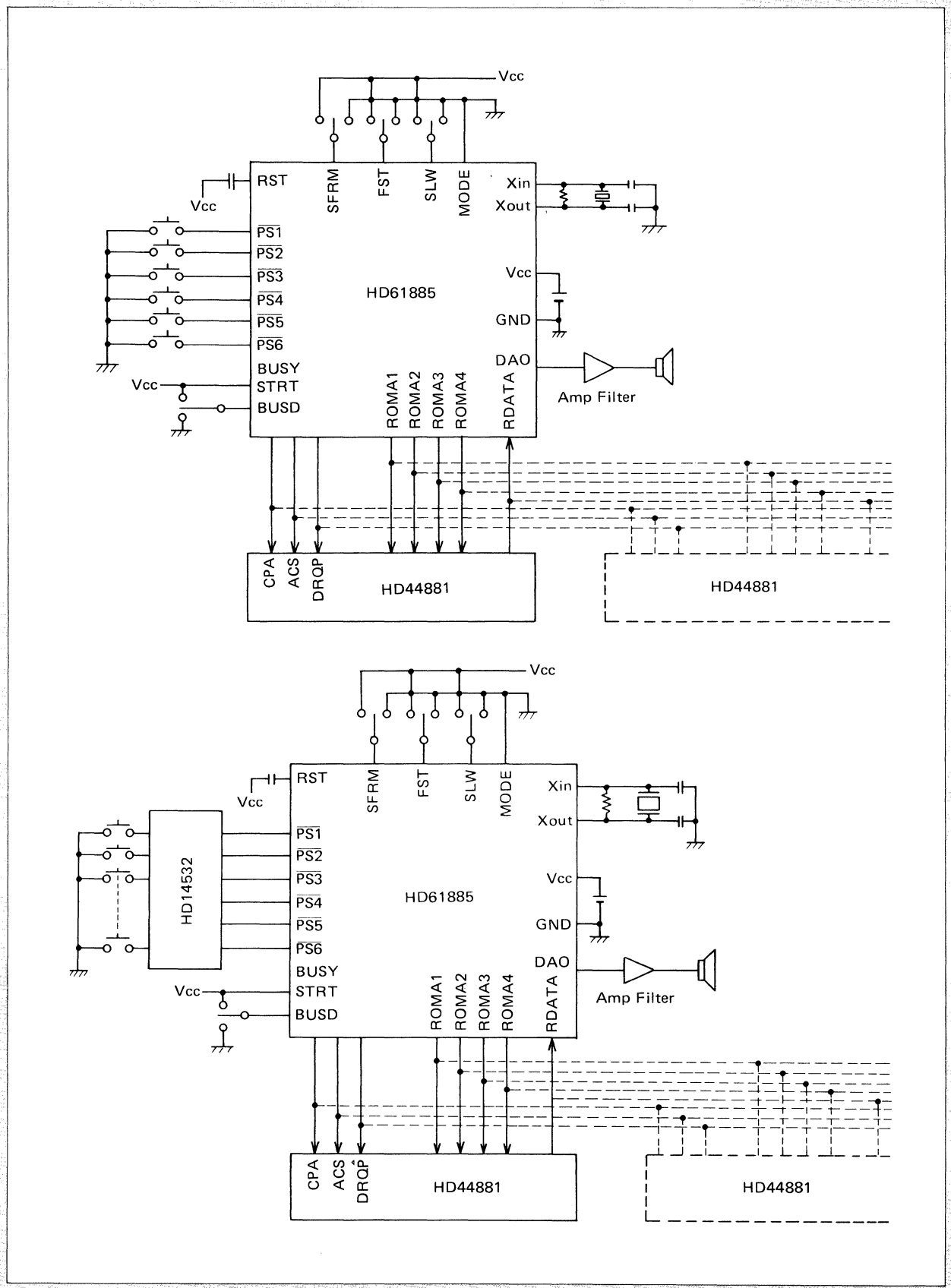
■ SYSTEM BLOCK DIAGRAM

- An Application of The Key Input Type



Note: Terminals not specified are used in open.

- An Application of The Key Input Type (external ROM operation)



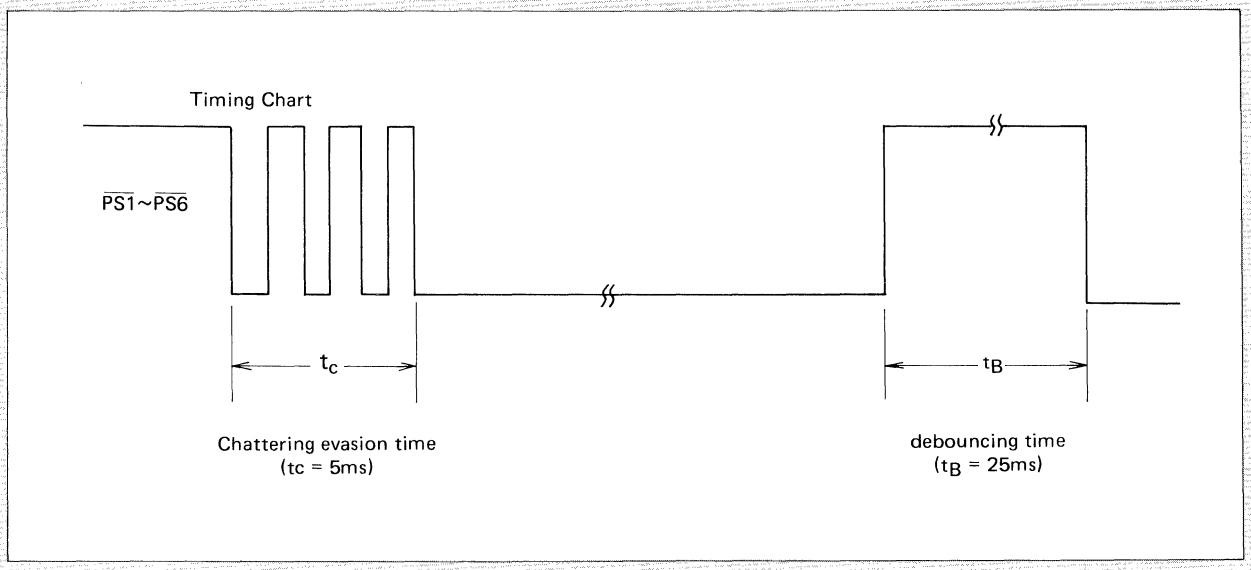
Note: Terminals not specified are used in open.

• An Application of The Key Input Type

Symbol	Function	Remark
MODE	Select Mode	The terminal for selecting key mode operation or MC mode operation. Input "L" level.
$\overline{PS1}$ $\overline{PS2}$ $\overline{PS3}$ $\overline{PS4}$ $\overline{PS5}$ $\overline{PS6}$	Phrase Selection Input Signal	Phrase selection input signal. Internal/external ROM is appointed, and one of 63 phrases can be set up. When "L" is applied to one of these terminals, utterance start signal generates and addressing converter starts. Function of preventing chatter and bounce is included. When input is applied during utterance, utterance stop signal generates and after utterance stop is confirmed, another utterance start signal generates.
STRT BUSD	• Utterance Start • Power Off Control (Stand-by)	Input "H" level for STRT terminal. BUSD terminal is the terminal for selecting power on and off. When input signal "H" for BUSD terminal is applied, internal power supply in the synthesis chip is made to be OFF. When input signal "L" is applied, power supply is ON. In this case the synthesis chip is reset automatically, because the reset terminal is connected to the internal power supply through the internal resistor.

Notes:
1. Pull up MOS to Vcc is added to $\overline{PS1}$~$\overline{PS6}$.
   While the internal power supply is OFF, (stand-by)
   Pull up MOS has high impedance.
2. Pull up MOS of $\overline{PS1}$~$\overline{PS6}$ can be cut off by metal option.

• Key Input



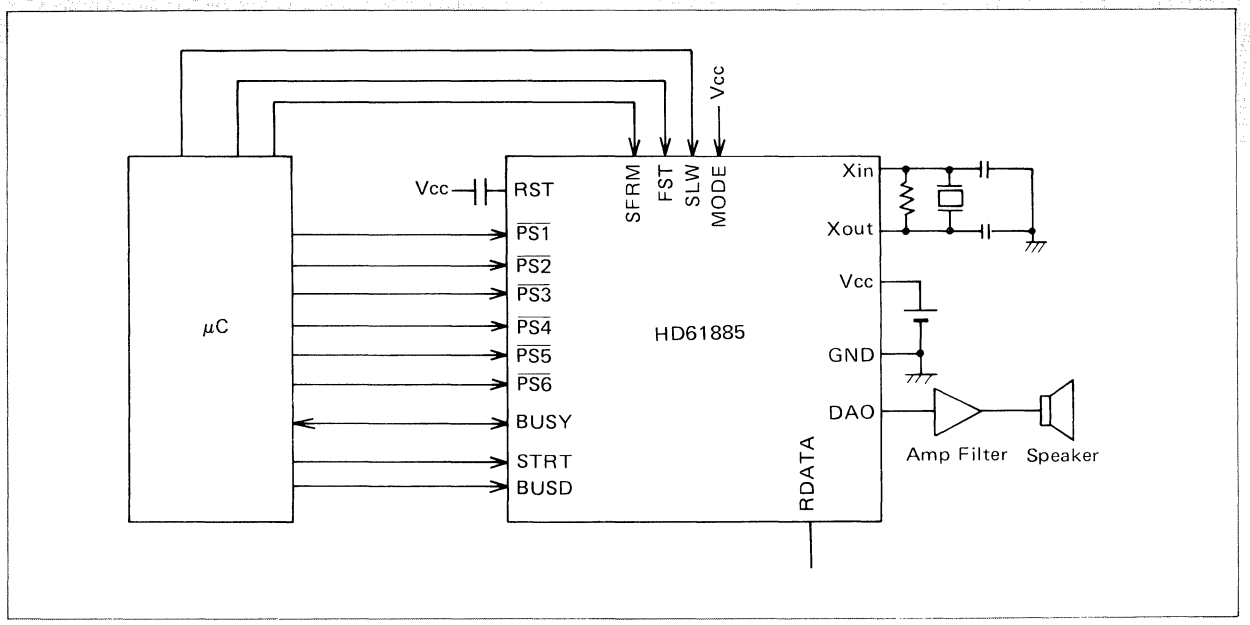
tc . . . . The time from key input to utterance start. The shorter input time than this value is inefective.

t_B . . . The required time to apply the next signal after the key is set free. The shorter key off (bouncing phenomenon) time makes it impossible to apply next input.

Selecting Phrase

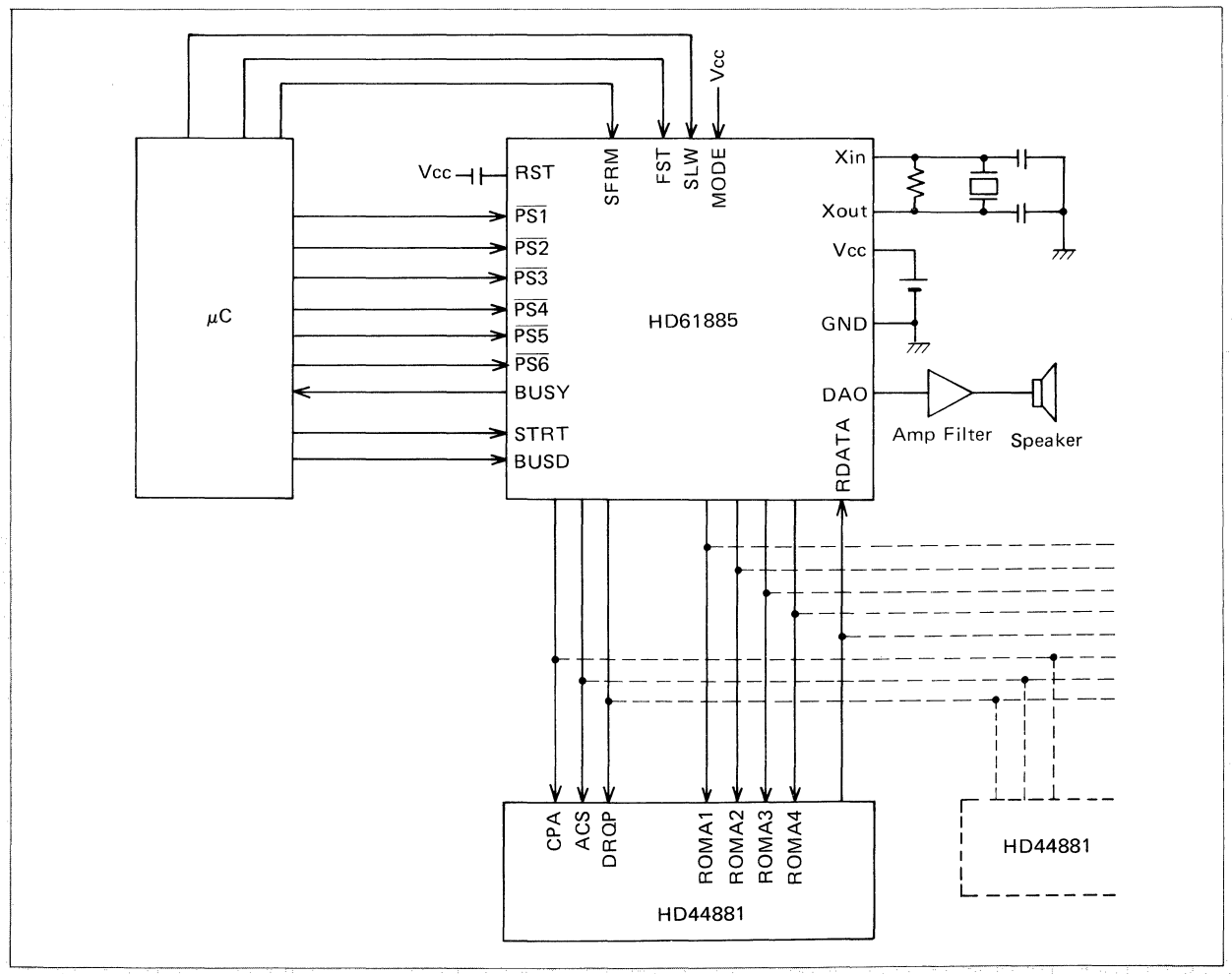
Utterance words, which correspond to the codes specified in $\overline{PS1}$~$\overline{PS6}$, are programmed in the internal PLA in accordance with the user's appointment.
In this case code "0" ($\overline{PS1}$~$\overline{PS6}$ = 1) is inhibited.

● **Microcomputer Control Type**



Note: Terminals not specified are used in open.

● **Microcomputer Control Type (external ROM operation)**



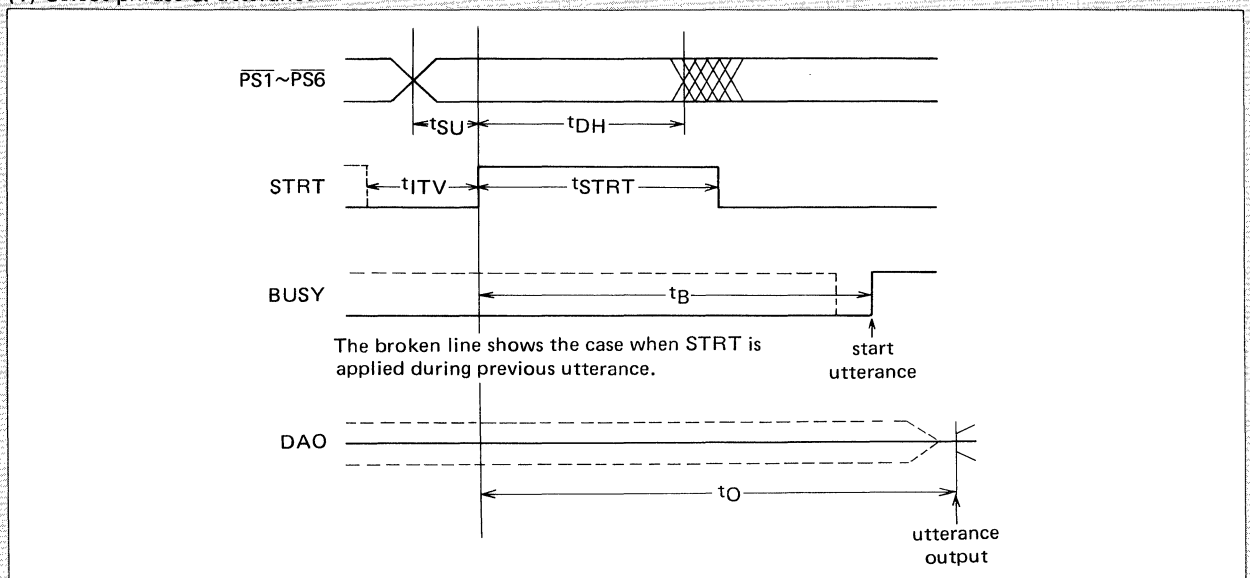
• An Application of the Microcomputer Control Type

Symbol	Function	Remark
MODE	Select Mode	The terminal for selecting key mode operation and microcomputer mode operation. Input "H" level.
$\overline{PS1}$ $\overline{PS2}$ $\overline{PS3}$ $\overline{PS4}$ $\overline{PS5}$ $\overline{PS6}$	Phrase Selection Input Signal	Phrase selection input signal. Internal/external ROM is appointed, and one of 63 phrases can be set up. By applying start input, signals of $\overline{PS1}$~$\overline{PS6}$ are latched and addressing converter starts.
STRT BUSD	Utterance Start Power OFF Control (Stand-by)	STRT instruction The synthesis chip starts operating by applying "H" level to STRT terminal more than 20μs. (This operation is on the leading edge of signal.) Power OFF instruction. When input "H" level signals are applied to both STRT terminal and BUSD terminal, internal power supply in the synthesis chip is made to be OFF. When input signals "L" are applied to BUSD terminal and STRT terminal, power supply is ON. In this case the synthesis chip is reset automatically, because the reset terminal is connected to the internal power supply through the internal resistor.

Notes:
1. Conformable to the note (An Application of The Key Input Type).
2. STRT instruction during utterance makes this utterance stop and new phrase generate.
3. Usually, utterance stops automatically detecting the End Mark programmed in ROM.

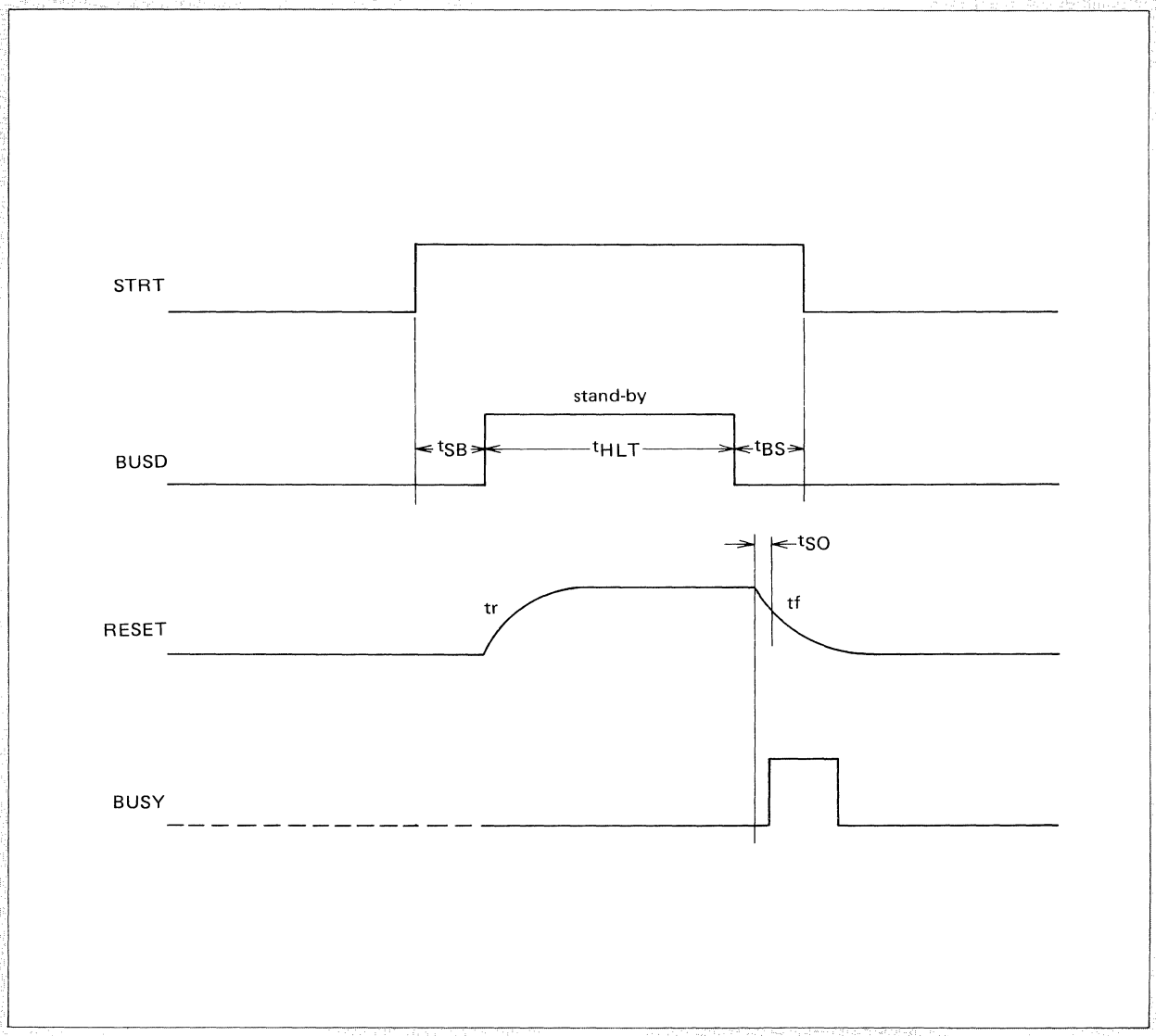
• Microcomputer Control Timing Chart

(1) Select phrase & utterance



Item	Symbol	min.	max.	Unit	Note
Input Data Set Up Time	t_{SU}	10.0	—	μs	
Input Data Hold Time	t_{DH}	20.0	—	μs	
STRT pulse width	t_{STRT}	20.0	—	μs	
STRT pulse interval	t_{INTV}	20.0	—	μs	
BUSY Signal Generation Starting Time	t_B	—	3.5	ms	
Utterance Output Starting Time	t_O	20		ms	depends upon speech data

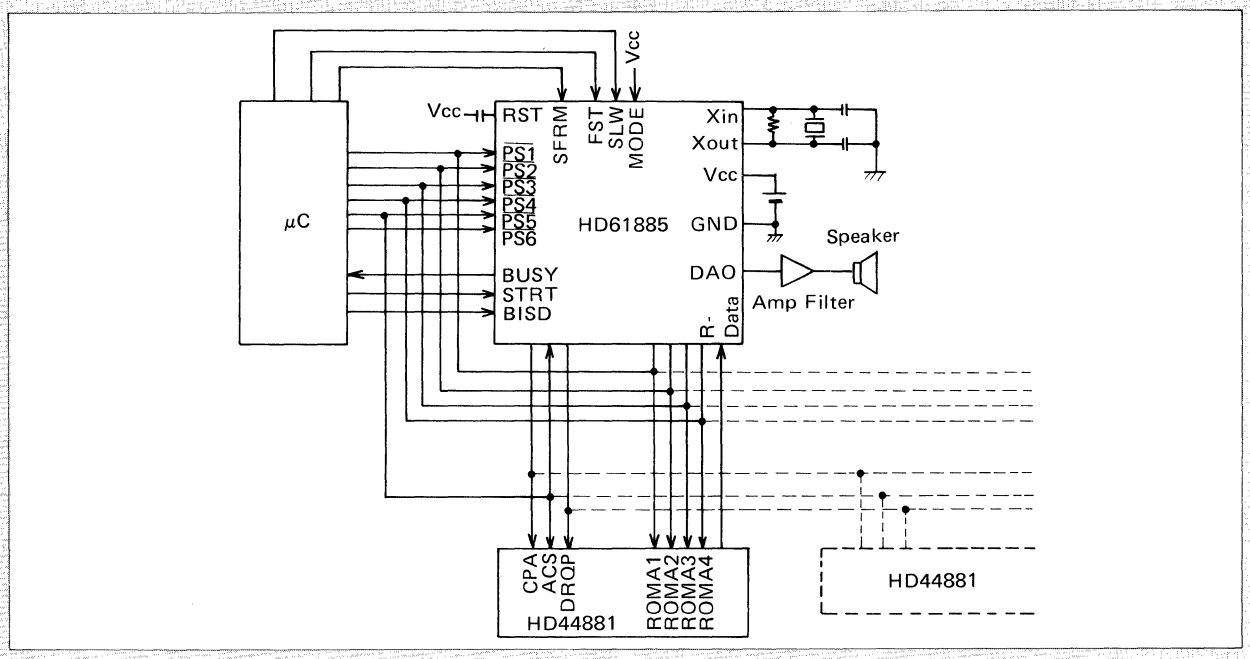
(2) Stand-by control



Item	Symbol	min.	max.	Unit	Remark	Note
STRT-BUSD Pulse Phase Difference	t_{SB}	10.0	(1000)	μs		1
BUSD-STRT Pulse Phase Difference	t_{BS}	10.0	—	μs		
Stand-by Time	t_{HLT}	(100)	—	ms		2
Operation Recovery	t_{SO}	—	—			3

Notes:
1. Specification within parenthesis is to prevent utterance generated by STRT signal. The cases that utterance has already finished and that an unvoiced sounds' phrase is selected are exclusive.
2. The minimum of the stand-by time is determined by C_R time, so that the reset is effective during recovering time from stand-by. So this value depends upon C_R. This C_R components mute D/A output, while transposing time for stand-by mode and recovering time from stand-by mode.
3. Time constant determined by external capacitance (C_R) of the reset terminal.
4. When the system is reset, busy signal is "H". During this time no instructions can be accepted. Instructions are accepted when Busy signal is "L".

• Phrase Edition Type by Microcomputer (More than 63 phrases)



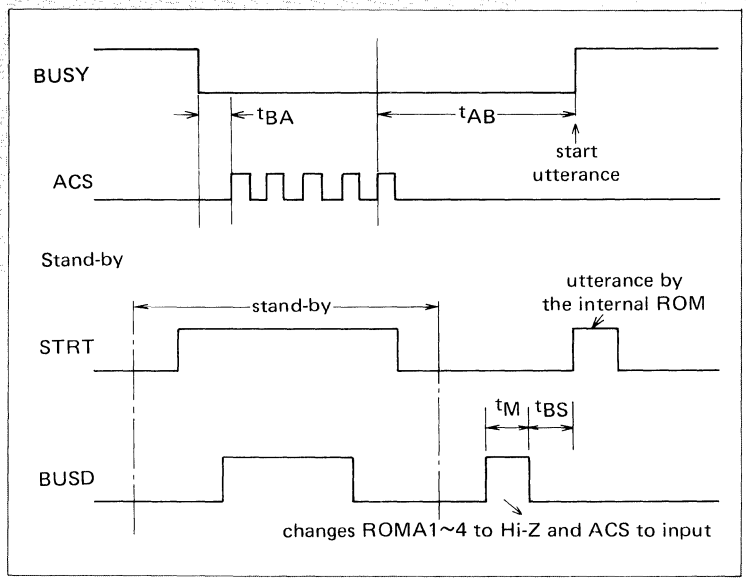
Note: Terminals not specified are used in open.

• The Phrase Edition Type by Microcomputer

Symbol	Function	Remark
MODE	Select Mode	The terminal for selecting key mode and microcom. mode. Input "H" level.
$\overline{PS1}$ $\overline{PS2}$ $\overline{PS3}$ $\overline{PS4}$ $\overline{PS5}$ $\overline{PS6}$	Phrase Selection Input Signal	Phrase selection input signal. The appointment of internal/external ROM and the phrase selection signal of internal ROM. Max. 63 kinds of phrases in the internal ROM and one in the external ROM can be set up. By applying the start signal, signals ($\overline{PS1}$~$\overline{PS6}$) are latched and the addressing converter starts.
STRT	$\overline{PS1}$~$\overline{PS6}$ Strobe Utterance stop	$\overline{PS1}$~$\overline{PS6}$ strobe and the instruction of stopping the utterance.
BUSD	Bus Output Control for ROM	By applying "H" level to the STRT terminal, $\overline{PS1}$~$\overline{PS6}$ are latched, but if the present utterance is continued, it is stopped and a new phrase is uttered.
	Power ON/OFF Control (STRT & BUSD in common)	BUS Hi-Z instruction Make ROM A1~A4 Hi-Z condition, and change ACC to input state. The external ROM direct address mode using the microcomputer is set up by this mode. To make this mode, after the power ON or reset apply BUSD signal before applying the start signal. Power OFF instruction (Stand-by) See the power OFF instruction in the application of the MC control type.
ACS	ROM Address Control	This signal moniters the external ROM address transmission, detects the completion of the address transmission, and generates the utterance start signal automatically. (Utterance starts at ACS 5 pulses.)

Notes:
1. See the footnotes (An Application of The Key Input Type) and (An Application of the Microcomputer Control Type).
2. ACS must generates 5 pulses accurately by MC. If more than 5 pulses are generated at a time, it will lead misoperation. And ACS must generates when BUSY is "L". The generation under "H" level will lead misoperation. See the specification of the speech synthesis CMOSROM (HD44881) for the timing chart of the external ROM address transmission.

• Timing Chart in The Case of the External Direct Addressing Mode



Item	Symbol	Min.	Max.	Unit	Note
BUSY-ACS Pulse Interval	t_{BA}	0.0	—	μs	
ACS-BUSY Pulse Interval	t_{AB}	—	3.5	ms	
BUSD Pulse Width	t_M	10.0	—	μs	Reset shall be released.
BUSD-STRT Pulse Interval	t_{BS}	10.0	—	μs	same as above

The Function of Terminals Used in Each Mode in Common

Symbol	Function	Remark
BUSY	Utterance Signal	The output terminal for showing that the utterance is going on. ("H"). This signal is "H" during reset.
SFRM	Frame Length Set Up	The terminal for changing the frame length. (10ms, 20ms.) "L" ..... 10ms (good speech quality) "H" ..... 20ms Bit rate (speech quality) is determined by combining frame length and bit/Frame.
Xout Xin	Oscillation	The terminal for oscillation. Using the ceramic resonator. (800kHz)
RST	Reset	In the case that the power supply is on. 1. Reset the internal state. 2. Mute DAO output for a time. This reset operation is available as recovering from stand-by mode. Reset time and Mute time are determined by the external capacitor. This capacitor also prevents the generation of pop sound.
DAO	D/A Output	The output terminal of D/A converter. Speech is generated through Filter, Amp, and Speaker.
DRQP	ROM Data Requesting Pulse	The output terminal for requesting the external ROM data.
FST SLW	Utterance Speed Set Up	Changeable to the following conditions by SLW, FST input.
RDATA	ROM Data Input	The input terminal for the external ROM.
ROMA1 ROMA2 ROMA3 ROMA4	ROM Address Output	The output terminal for the external ROM address.
CPA	ROM Clock	The output terminal for the external ROM drive.
Vcc GND	Power Supply +5V 0V	+5V power supply terminal. 0V ground terminal.

SLW	L	H	L	H
FST	L	L	H	H
Bit/Frame	50	50	50	99
Frame Length	Normal	+25%	−25%	Normal
		slow speed	fast speed	

● The List of Terminals (HD61885) . . . DIP-28

Pin No.	Function	Symbol	Power Supply	Clock	In	Out	3-state	Pull Up	Pull Down
1	Utterance Signal	BUSY				○			
2	ROM Data Requesting Pulse	DRQP				○			
3	ROM Address Control	ACS			○	○	○	●	
4	Phrase Selection Input Signal	$\overline{PS1}$			○			○	
5		$\overline{PS2}$			○			○	
6		$\overline{PS3}$			○			○	
7		$\overline{PS4}$			○			○	
8		$\overline{PS5}$			○			○	
9		$\overline{PS6}$			○			○	
10	Select Mode	MODE			○				
11	ROM Data Input	RDATA			○				
12	Utterance Start	STRT			○				
13	ROM Output Control	BUSD			○				
14	Power Supply (+5V)	V_{CC}	○						
15	Utterance Speed Set Up	FST			○				
16		SLW			○				
17	Frame Length Set Up	SFRM			○				
18	Reset	RST			○				
19	Test	TEST			○				
20	Oscillation	X_{IN}		○	○				
21		X_{OUT}		○		○			
22	D/A Output	DAO				○			
23	ROM Clock	CPA		○		○			
24	Power Supply (0V)	GND	○						
25	ROM Address Output	ROMA1				○	○	●	
26		ROMA2				○	○	●	
27		ROMA3				○	○	●	
28		ROMA4				○	○	●	

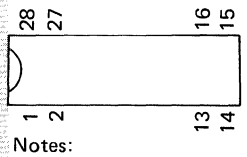
internal minus power supply → ○ ○

Notes:
1. Phrase Selection Input Signal:
   Pull up MOS is selected by metal option.
   While stand-by mode, pull up MOS is Hi-Z.
2. ● Pull up is effective while output Hi-Z or stand-by mode.
   Pull up is Hi-Z while other condition.

● HD61887 (FPP-54) Pin Assignment

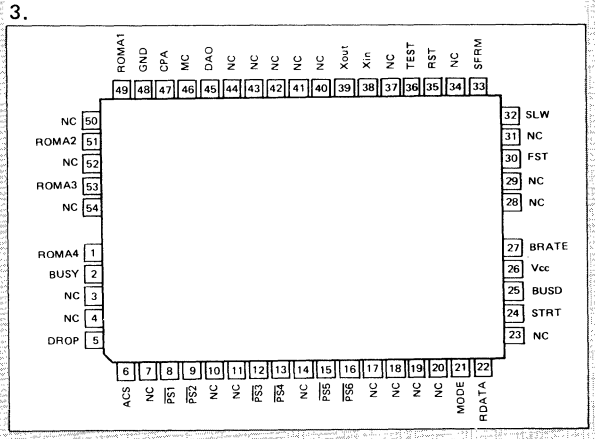
Pin#	Terminal	Pin#	Terminal	Pin#	Terminal	Pin#	Terminal
1	ROMA4	15	$\overline{PS5}$	29	⟨NC⟩	43	⟨NC⟩
2	BUSY	16	$\overline{PS6}$	30	FST	44	⟨NC⟩
3	⟨NC⟩	17	⟨NC⟩	31	⟨NC⟩	45	DAO
4	⟨NC⟩	18	⟨NC⟩	32	SLW	46	⟨NC⟩
5	DRQP	19	⟨NC⟩	33	SFRM	47	CPA
6	ACS	20	⟨NC⟩	34	⟨NC⟩	48	GND
7	⟨NC⟩	21	MODE	35	RST	49	ROMA1
8	$\overline{PS1}$	22	RDATA	36	TEST	50	⟨NC⟩
9	$\overline{PS2}$	23	⟨NC⟩	37	⟨NC⟩	51	ROMA2
10	⟨NC⟩	24	STRT	38	Xin	52	⟨NC⟩
11	⟨NC⟩	25	BUSD	39	Xout	53	ROMA3
12	$\overline{PS3}$	26	Vcc	40	⟨NC⟩	54	⟨NC⟩
13	$\overline{PS4}$	27	BRATE	41	⟨NC⟩		
14	⟨NC⟩	28	⟨NC⟩	42	⟨NC⟩		

3.



(Top View)

Notes:
1. BRATE is the test terminal for flat package type device, and is to be used in open.
2. ⟨NC⟩ indicates NO connection.
3.



■ ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Note
Supply Voltage	Vcc	−0.3 ~ +6.7	V	
Terminal Voltage (1)	V_{T1}	−0.3 ~ Vcc+0.3	V	
Operating Temperature (1)	Topr1	−20 ~ +75	°C	The range of utterance;
Operating Temperature (2)	Topr2	−10 ~ +55	°C	guarantee: CPG ±3%
Storage Temperature	Tstg	−55 ~ +125	°C	

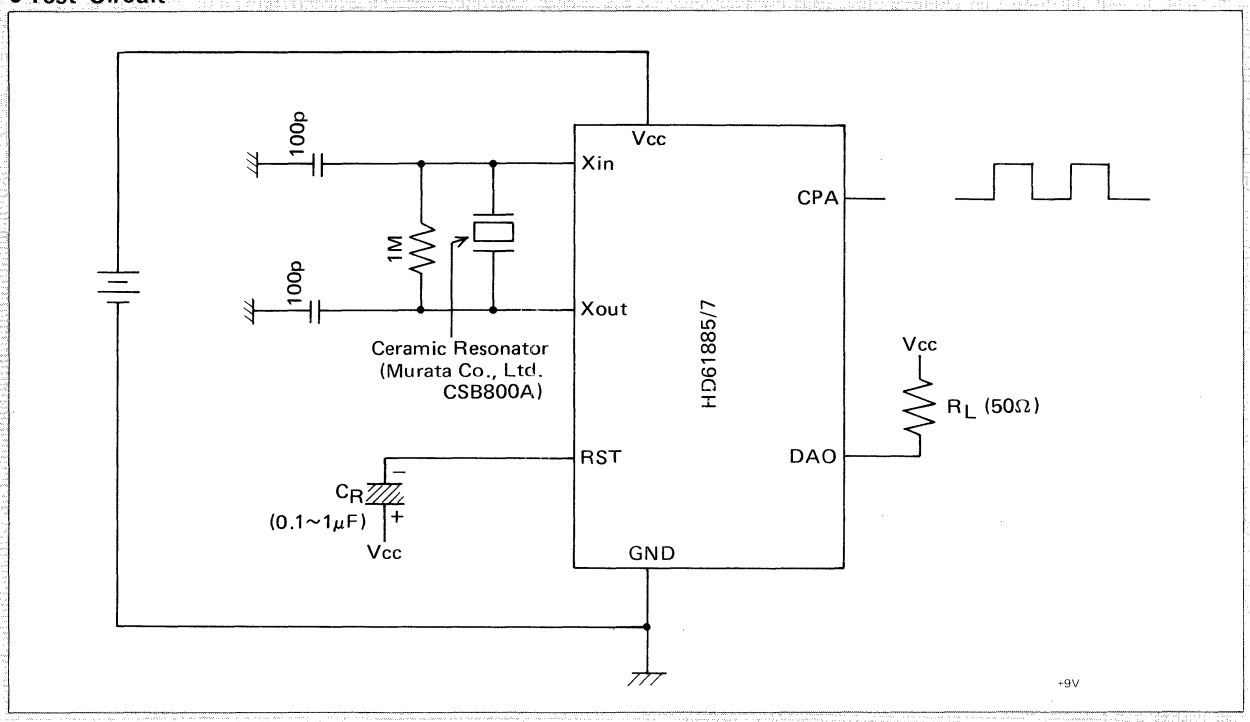
• Electrical Characteristics Vcc = +5V ± 10%, Ta = −20~+75°C (unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Input Voltage	V_{IL1}		—	—	1.0	V	
	V_{IH1}		Vcc −1.0	—	—	V	
	V_{IL2}		—	—	1.0	V	
	V_{IH2}		Vcc −1.0	—	—	V	
Pull Up MOS	I_{PULL}	V_{IN} = Vcc	30	—	240	μA	RST
		VIN = GND	5	—	100	μA	ROMS1~4, ACS
			20	—	100	μA	$\overline{PS1}$~$\overline{PS6}$
Output Voltage	V_{OL}	I_{OL} = 1.6mA	—	—	0.8	V	Output except DAO
	V_{OH1}	I_{OH} = 1.0mA	2.4	—	—	V	
	V_{OH2}	I_{OH} = 0.1mA	Vcc −0.8	—	—	V	
Clock Oscillation Frequency	fcp	CPA terminal	194	200	206	kHz	Ta = −10~+55°C
Input Leakage Current	$\pm I_{IN}$	V_{IN} = 0~Vcc	—	—	1	μA	applied to the terminal without pull up
D/A Output Voltage	V_{OS}	R_L = 50 Ω	0.25	0.5	—	Vp-p	
Power Dissipation	P_T		—	3.5	—	mW	D/A power dissipation is not included.
Stand-by Current	I_{SC}		—	—	10	μA	STRT = BUSD = Vcc−0.2V

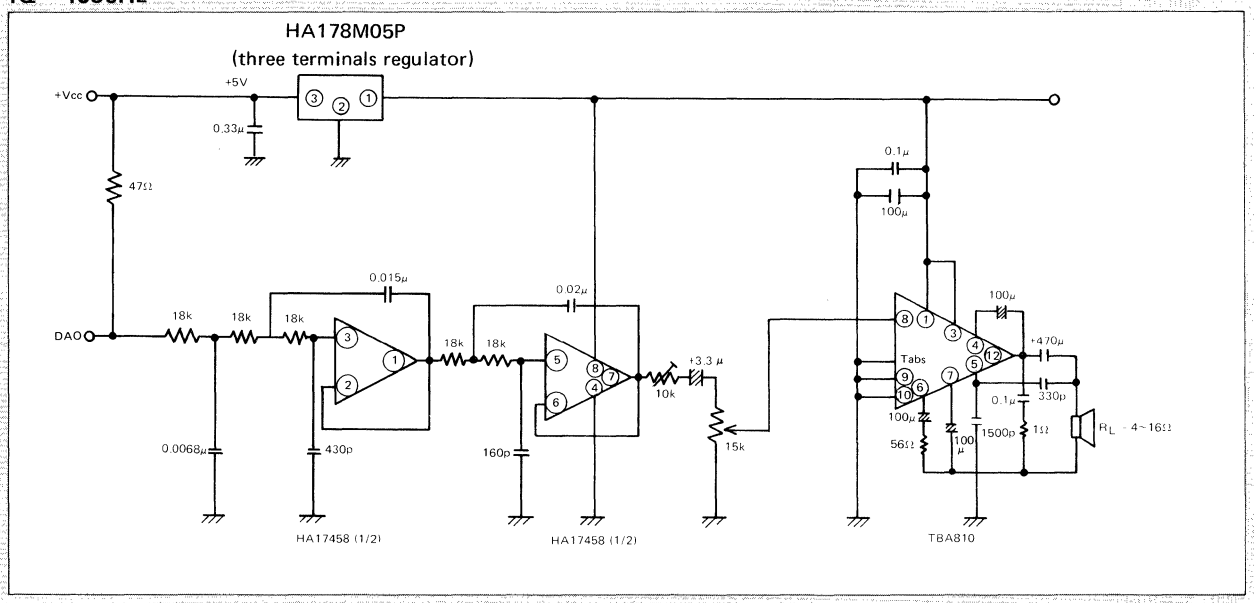
• Electrical Characteristics (Ta = −10 ~ 55°C, Vcc = 3.6 ~ 5.5 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Terminal
Input Voltage	V_{IH1}		Vcc −0.7	—	—	V	
	V_{IL1}		—	—	0.7	V	
	V_{IH2}		Vcc −0.7	—	—	V	
	V_{IL2}		—	—	0.7	V	
Output Voltage	V_{OH}	$-I_{OH}$ = 50μA	Vcc −0.5	—	—	V	
	V_{OL}	I_{OL} = 50 μA	—	—	0.5	V	
Pull Up MOS	$-I_p$	V_{IN} = 0V	10	—	100	μA	$\overline{PS1}$~$\overline{PS6}$
			2	—	100	μA	ACS, ROMA1~4
	I_P	V_{IN} = Vcc	30	—	240	μA	RST
Clock Oscillation Frequency	fcp	measured at the CPA terminal	194	200	206	kHz	
Input Leakage Current	$+I_{IN}$	V_{IN} = 0 ~ Vcc	—	—	1	μA	
D/A Output Voltage		R_L = 50 Ω	0.1	0.5	—	Vp-p	
Power Dissipation	P_T		—	3.5	—	mW	DAO is open
Stand-by Current	I_{SC}		—	—	10	μA	STRT = BUSD = Vcc−0.2V

● **Test Circuit**



● **Fifth Order 1.0 dB Ripple Chebyshev Filter**
fQ = 4950Hz



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