HIGHPOINT TECHNOLOGIES, INC.

HPT370 DATA MANUAL (Rev. 1.02)

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Preface

This manual assumes your some prior knowledge of PCI and ATA/ATAPI Standard.

The data manual is to be organized into the following chapters:

Chapter 1- Overview
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Any advice concerning this manual will be appreciated!

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Chapter 1
Overview

HPT3xx is a family of high-performanced PCI-to-IDE ATA/ATAPI Ultra DMA controller ICs developed by HighPoint Technologies, Inc.. The family bases on the PCI local bus and brings the PCI's high performance to ATA/ATAPI devices.

HPT370 is the new generation of HPT3xx family. Compared to its pre-generation products, HPT370 integrates the latest ATA100 technology and enable users add the fastest ATA/ ATAPI devices onto the system.

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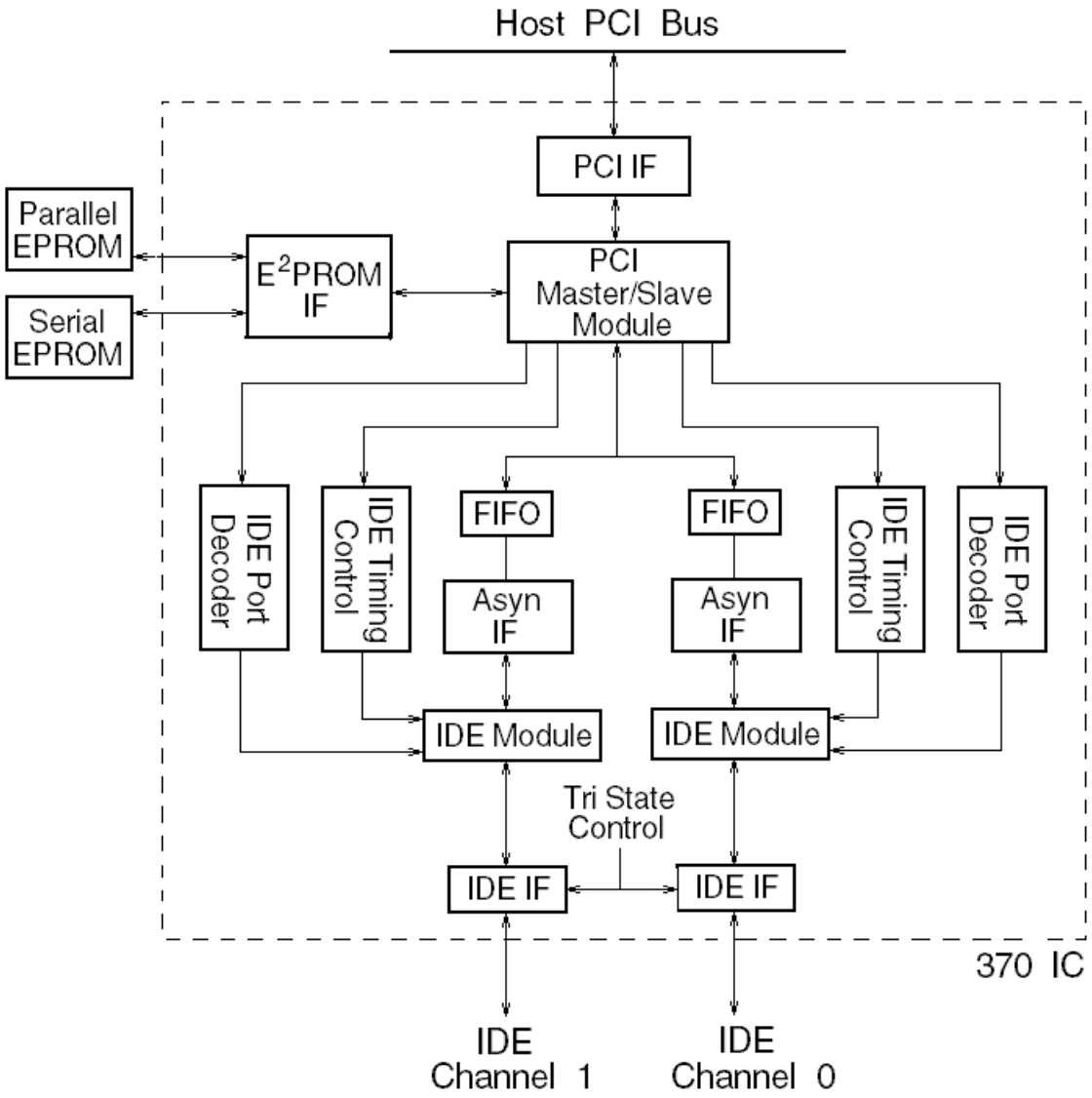
1.1 HPT370 Block Diagram



1.2 Features

- Ultra DMA 100MB/S operation per ATA channel
- Supports up to 66MHz PCI bus Clock
- One PCI function support two independent ATA channels
- Dedicated ATA Bus
- ATA clock independents from PCI bus
- Optional between external 50MHz ATA bus clock or internal PLL
- 256 Bytes FIFO per ATA channel
- Large FIFO concurrent
- Supports all hard disks and ATAPI CD-ROM, DVD-ROM, CD-R, CD-RW, LS-120, MO, Tape and ZIP devices
- Easy Plug-and-Play feature
- Supports up to 8 ATA/ATAPI devices. (Coexist with on-board IDE)
- RAID function supported(RAID 0, 1, 0+1)
- Supports the most popular OS like Windows 95/98, Windows NT 4.0, Windows 2000 and Linux
- Supports booting function with Flash Memory interface
- Automatically fine tune to the best performance for each ATA/ATAPI device
- Concurrent PIO and bus master access (ATA port accessible during DMA transfer)
- Total IDE bus tri-state by software control and supports hotswap (Low signal Current)
- Reloadable PCI configuration using parallel EPROM or 2 wire serial EPROM (Loading address 0 for serial EPROM, loading address 400H for parallel EPROM)
- Small foot print 144-pin LQFP package(Dedicated Parallel EPROM pins)
- Embedded serial resistor on chip for ATA spec.

Chapter 2
Signal Description

This chapter will give an introduction on all 144 pins.
The signals are organized into the following functional groups:

* System Pins
* Power and Ground Pins
* Interface Control Pins
* Arbitration Pins
* PCI Interrupt Pins
* Address/Data Pins
* IDE Interface Pins
* EPROM Interface Pins
* Other Pins

There are three signal type definitions:

I ——— Input, a standard input-only signal
O ——— Totem Pole Output, a standard output driver
I/O ——— Input and Output

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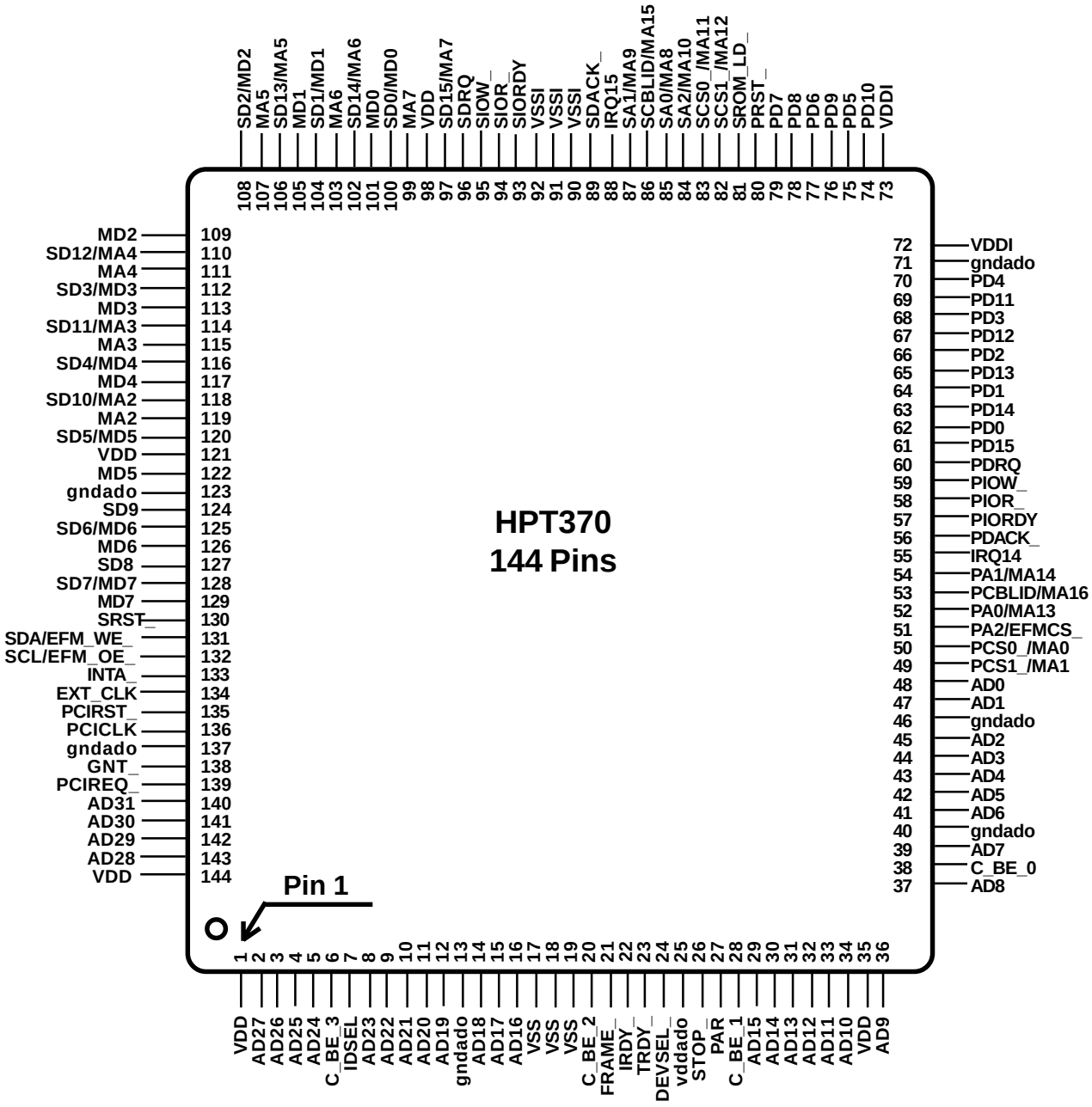
2.1 Pin Configuration



2.2 Pin Signal Description

• System Pins

Pin Number	Pin Name	Type	Description
136	PCICLK	I	**PCI Clock** provides timing for all transactions on the PCI bus and is input to all PCI devices. All other PCI signals are sampled on the rising edge of PCICLK, and other timing parameters are defined with respect to this edge.
135	PCIRST_	I	**Reset PCI Bus**

• Power and Ground Pins

Pin Number	Pin Name	Type	Description
17,18,19	VSS		Ground reference power supply.
90,91,92	VSSI		Ground reference power supply.
1,25,35, 98,121,144	VDD		Positive power supply.
72,73	VDDI		Positive power supply.
13,40,46, 71,123,137	GND		Ground

• Interface Control Pins

Pin Number	Pin Name	Type	Description
7	IDSEL	I	**PCI Initialization Device Select** is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.
21	FRAME_	I/O	**PCI Cycle Frame** is driven by the current master to indicate the beginning and duration of an access. FRAME_ is asserted to indicate that a bus transaction is beginning. While FRAME_ is deasserted, either the transaction is in the final data phase or the bus is idle.
22	IRDY_	I/O	**PCI Initiator Ready** indicates the initiating agent's(bus master's) ability to complete the current data phase of the transaction. IRDY_ is used in conjunction with TRDY_. A data phase is completed on any clock both IRDY_ and TRDY_ are asserted. During a write, IRDY_ indicates that valid data is present on AD(31-0). During a read, it indicates that master is prepared to accept data. Wait cycles are inserted until both IRDY_ and TRDY_ are asserted together.
23	TRDY_	I/O	**PCI Target Ready** indicates the target agent's(selected device's) ability to complete the current data phase of the transaction. TRDY_ is used in conjuction with IRDY_. A data phase is completed on any clock both TRDY_ and IRDY_ are asserted. During a write, TRDY_ indicates that the target is prepared to accept data. During a read,it indicates that valid data is present on AD(31-0). Wait cycles are inserted until both IRDY_ and TRDY_ are asserted together.
24	DEVSEL_	I/O	**PCI Device Select** indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
26	STOP_	I/O	**PCI Stop** indicates that the selected target is requesting the master to stop the current transaction.

• Arbitration Pins

Pin Number	Pin Name	Type	Description
139	PCIREQ_	O	**PCI Request** indicates to the arbiter that this agent desires use of the PCI bus.
138	GNT_	I	**PCI Grant** indicates to the agent that access to the PCI bus has been granted.

• PCI Interrupt Pins

Pin Number	Pin Name	Type	Description
133	INTA_	O	**PCI Interrupt A** is used to request a PCI Bus interrupt.

• Address/Data Pins

Pin Number	Pin Name	Type	Description
140,141,142, 143,2,3,4,5, 8,9,10,11,12, 14,15,16,29, 30,31,32,33, 34,36,37,39, 41,42,43,44, 45,47,48	AD(31-0)	I/O	PCI Physical longword **Address and Data** are multiplexed on the same PCI pins. During the first clock of a transaction, AD(31-0) contain a physical byte address. During subsequent clocks, AD(31-0) contain data. A bus transaction consists of an address phase followed by one or more data phase. PCI supports both read and write bursts. AD(7-0) define the least significant byte, and AD(31-24) define the most significant byte.
6,20,28,38	C/BE_(3-0)	I/O	**PCI Bus command and Byte Enables** are multiplexed on the same PCI pins. During the address phase of a transaction, C/BE_(3-0) define the bus command. During the data phase, C/BE_(3-0) are used as byte enables. The byte enable indicates which byte lanes carry meaningful data. C/BE_0 applies to byte 0, and C/BE_3 to byte 3.
27	PAR	I/O	**PCI Parity** is the even parity bit that protects the AD(31-0) and C/BE_(3-0) lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

● IDE Interface Pins

Pin Number	Pin Name	Type	Description
51,54,52	PA(2-0)/ MEMCS# &MA(14-13)	O	Primary IDE Device Address They are also used as MEMCS# and Parallel EPROM Address Bus signal.
84,87,85	SA(2-0)/ MA(10-8)	O	Secondary IDE Device Address They are also used as Parallel EPROM Address Bus signal.
61,63,65,67, 69,74,76,78, 79,77,75,70, 68,66,64,62	PD(15-0)	I/O	Primary IDE Data
97,102,106, 110,114,118, 124,127,128, 125,120,116, 112,108,104, 100	SD(15-0)/ MA(7-2)& MD(7:0)	I/O	Secondary IDE Data Some of them can be also shared as Data Bus and Address Bus signal of Parallel EPROM.
56	PDACK_	O	Primary IDE Channel DMA Acknowledge
89	SDACK_	O	Secondary IDE Channel DMA Acknowledge
50	PCS0_/MA0	O	Primary IDE Channel Device Chip Select 0. /Parallel EPROM Address.
49	PCS1_/MA1	O	Primary IDE Channel Device Chip Select 1. /Parallel EPROM Address.
83	SCS0_/MA11	O	Secondary IDE Channel Device Chip Select 0. /Parallel EPROM Address.
82	SCS1_/MA12	O	Secondary IDE Channel Device Chip Select 1. /Parallel EPROM Address.
57	PIORDY	I	Primary IDE Channel I/O Ready
93	SIORDY	I	Secondary IDE Channel I/O Ready
60	PDRQ	I	Primary IDE Channel DMA Request
96	SDRQ	I	Secondary IDE Channel DMA Request
88	IRQ15	I	**Interrupt Request 15.** This Pin is used to request an interrupt for secondary IDE Channel.
55	IRQ14	I	**Interrupt Request 14.** This pin is used to request an interrupt for primary IDE Channel.

Pin Number	Pin Name	Type	Description
58	PIOR_	O	Primary IDE Channel I/O Read.
94	SIOR_	O	Secondary IDE Channel I/O Read.
59	PIOW_	O	Primary IDE Channel I/O Write.
95	SIOW_	O	Secondary IDE Channel I/O Write.
53	PCBLID /MA16	I/O	Primary IDE Channel Cable Assembly Type Identifier /Parallel EPROM address.
86	SCBLID /MA15	I/O	Secondary IDE Channel Cable Assembly Type Identifier /Parallel EPROM address.

• EPROM Interface Pins

Pin Number	Pin Name	Type	Description
53,86,54,52, 82,83,84,87, 85,97,99,102, 103,106,107, 110,111,114, 115,118,119, 49,50	MA(16-8)& MA(6-0)	O	**Memory Address Bus.** This bus is used in conjunction with the memory address strobe pins and external address latches to assemble up to a 20-bit address for an external EPROM or flash memory. This bus puts out the least significant byte first and finishes with the most significant bits. It is also used to write data to a flash memory or read data into the chip from external EPROM/flash memory. They are also used as PCBLID, SCBLID, PA(1-0), SCS1_,SCS0_,SA(2-0),SD(15-10), PCS1_ and PCS0_ signal.
99	MA7	I/O	When system reset, the MA7 signal will be latched on rising edge of PCIRST_ signal. If the value is 1, the IC is packaged of 144 Pins. The MA7 pin must have an external pull_up resistor (<5K).
129,126,122, 117,113,109, 105,101,	MD(7-0)/	I/O	**Memory Data Bus.** This is Data Bus for EPROM. It is used to write data to a flash memory or read data from external EPROM/flash memory. All MD pins have internal pull-down resistors.
132	SCL/ MEM_OE_	O	**EPROM Output Enable.** This pin is used as an output enable signal to an external EPROM or flash memory during read operations. It is also used as a SCL signal.
131	SDA/ MEM_WE_	O	**EPROM Write Enable.** This pin is used as a write enable signal to an external flash memory. When system reset, this signal will be latched on rising edge of PCIRST_ signal. If latched values of SDA/EFM_WE_ & SROM_LD_ signals are both high-LEV, the configuration will be loaded from parallel EPROM automatically. It is also used as a SDA signal.
51	MEMCS#/ PA2	O	**EPROM Chip Select.** It is also used as a Primary IDE Device Address signal.

• Other Pins

Pin Number	Pin Name	Type	Description
80	PRST_	O	Primary IDE Channel Reset
130	SRST_	O	Secondary IDE Channel Reset
81	SROM_LD_	I	When system reset, the SROM_LD_ signal will be latched on rising edge of PCIRST_ signal. If the latched value of SROM_LD_ is 0, the configuration will be loaded from serial EPROM automatically.
134	EXT_CLK	O	External Clock input pin. This is the optional external OSC input. If not use, should be tied through a 10K resistor to GND.

Chapter 3
Registers

PCI Configuration Registers and I/O Space Registers of HPT370 are introduced in this chapter.
HPT370 has one PCI function.

3.1 Registers Index

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3.2 PCI Configuration Registers

The PCI Configuration registers are accessed by performing a configuration read/write to the device with its IDSEL pin asserted and the appropriate value in AD(10:8) during the address phase of the transaction. All PCI-compliant devices, must support the Vendor ID, Device ID, Command, and Status Registers. Support of other PCI-compliant registers is optional.

To enable user access PCI configuration registers more conveniently, most PCI configuration registers are mapped to the I/O space. When a PCI configuration register is mapped to the I/O space, its mapped address in I/O space is given after the “I/O Address” .

Vendor ID and Device ID

Address: 00h-03h
I/O Address: 20h-23h
Attribute: Read Only, Power On Loading

BIT	DESCRIPTION
31:16	Device Identification Number: IDE Controller=0004h
15:0	Vender Identification Number=1103h

***Notes:** These fields identify the manufacturer of the device and the device type.

Command Register

Address: 04h-05h
I/O Address: 24h-25h
Attribute: R/W

BIT	DESCRIPTION
15:10	Reserved
9	Fast Back-to-Back Enable(Not Implemented).Hardwired to 0b
8 : 3	Reserved
2	Bus Master Enable.If set 1,Master Mode Enable. Defalt=0b
1	Memory Space Enable.1=Enable.0=Disable. Defalt=0b
0	I/O Space Enable.1=Enable.0=Disable. Default=0b

Status Register

Address: 06h-07h
I/O Address: 26h-27h
Attribute: Read Only

BIT	DESCRIPTION
15:14	Reserved
13	PCI Bus Master Abort
12	PCI Bus Received Target Abort
11	PCI Bus Signaled Target Abort
10:9	DEVSEL_Timing. Hardwared 01-Medium
8	Reserved
7	Fast Back_to_Back Capable. Power on loading, default=0b
6	Reserved
5	66MHz capable. Power on loading
4	Capabilities, Power On Loading
3:0	Reserved

Revision Identification Register

Address: 08h
I/O Address: 28h
Attribute: Read Only, Power On Loading

BIT	DESCRIPTION
7:0	Revision ID Byte=03h.

***Note:** This field specifies device revision identifier.

Class Code Register

Address: 09h-0Bh
I/O Address: 29h-2Bh
Attribute: Read Only/Power On Loading

BIT	DESCRIPTION
23 : 0	If Compatible Mode:Class Code=010180h, If In Native Mode:Class Code=018000h. Default=Native Mode.

***Notes:** This register is used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface.

Cache Line Size Register

Address: 0Ch
I/O Address: 2Ch
Attribute: R/W

BIT	DESCRIPTION
7:0	This register must be implemented by master devices that can generate the Memory Write and Invalidate command.

Latency Timer Register

Address:0Dh
I/O Address:2Dh
Attribute: R/W

BIT	DESCRIPTION
7 : 0	Latency Timer

***Notes:** The Latency Timer Register specifies, in unit of PCI bus clocks, the value of the Latency Timer for the PCI bus master.

Header Type Register

Address: 0Eh
I/O Address: 2Eh
Attribute: Read Only

BIT	DESCRIPTION
7:0	Header Type=00h.

Notes: This register identifies whether or not the device contains multiple functions.

Command Block Register

Primary Channel: 10h-13h
Secondary Channel: 18h-1Bh
Primary Channel I/O Address: 10h-13h
Secondary Channel I/O Address: 18h-1Bh
Attribute: R/W

BIT	DESCRIPTION
31 : 3	Base registers used to map IDE Command Block registers, must ask for 8 bytes of I/O space.

Notes: In mode the registers of the IDE channels are completely relocatable in I/O space. Base Address sters in the PCI IDE controller Configuration Space registers are used to map the IDE register into space.

Control Block Register

Primary Channel: 14h-17h
Secondary Channel: 1Ch-1Fh
Primary Channel I/O Address: 14h-17h
Secondary Channel I/O Address: 1Ch-1Fh
Attribute: R/W

BIT	DESCRIPTION
31 : 2	Base Address registers in the PCI IDE controller's Configuration Space registers are used to map the IDE control block registers into I/O space. Base registers to map Control Block registers must ask for 4 bytes of I/O space. In this four-byte allocation, the byte at offset 02h is where the Alternate Status/Device Control byte is located. Other bytes in the four-byte allocation(bytes at offset 0,1 and 3) are undefined and can be used for device specific purposes.

I/O Space Base Register

Address: 20h-23h
I/O Address: 40h-43h
Attribute: R/W

BIT	DESCRIPTION
31:8	I/O Base Address.
7:1	Reserved.
0	Hardwired to 1.

CardBus CIS Pointer Register

Address: 28h-2Bh
I/O Address: 48h-4Bh
Attribute: Read Only. Power On Loading

BIT	DESCRIPTION
31:0	CardBus CIS Pointer.

Subsystem Vendor ID Register

Address: 2Ch-2Dh
I/O Address: 4Ch-4Dh
Attribute: Read Only, Power On Loading

BIT	DESCRIPTION
15:0	Subsystem Vender ID

Subsystem ID Register

Address: 2Eh-2Fh
I/O Address: 4Eh-4Fh
Attribute: Power On Loading

BIT	DESCRIPTION
31:24	Subsystem ID. Read Only
23:16	Subsystem ID. Software Writable, Default=01h

Expansion ROM Base Register

Address: 30h-33h
I/O Address: 50h-53h
Attribute: R/W

BIT	DESCRIPTION
31:17	ROM Base Address
16:1	Reserved
0	Address decode enable.

***Notes:** This register handles the base address and size information for the expansion ROM. It functions exactly like the Base Address registers, except that the encoding of the bits is different.
The Expansion ROM Enable bit, bit 0, is the only bit defined in this register. This bit controls whether or not the device accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled, and a device is used with or without an expansion ROM depending on the system configuration. To access the external memory interface, also set the Memory Space bit in the Command register.

Cap_Ptr Register

Address: 34h
I/O Address: 54h
Attribute: Read Only

BIT	DESCRIPTION
7:0	Hardwared to 8'h60

Interrupt Line Register

Address: 3Ch
I/O Address: 5Ch
Attribute: R/W

BIT	DESCRIPTION
7:0	Interrupt line Number. After Reset=00h.

***Notes:** This register can communicate interrupt line routing information. POST software writes the routing information into this register as it configures the system. The value of this register tells that to which input of the system interrupt controller(s) the devices interrupt pin is connected. Value of this register is specified by system architecture.

Interrupt Pin Register

Address: 3Dh
Attribute: R/W, Power On Loading

BIT	DESCRIPTION
7:0	Interrupt Pin Number. Hardwared to 1. Connected to INTA_.

***Notes:** This register tells which interrupt pin the device uses. It is defaultly set to 01h at power-up. Other register controls its write.

IDE Timing 0 Register

Address: 40h-43h
I/O Address: 60h-63h
Attribute: R/W

BIT	DESCRIPTION
31	Primary Drive 0 Buffer Enable for PIO Read/Write. 0=disable, 1=enable.
30	Primary Drive 0 PIO_MST Enable. 0=disable, 1=enable. PIO_MST means the chip working in bus master state on PCI side, but devece working in PIO mode.
29	Primary Drive 0 Normal DMA Enable.0=disable, 1=enable.
28	Primary Drive 0 UDMA Enable, 0=disable, 1 =enable.
27:25	Primary Drive 0 cmd_pre_high_time.
24:22	Primary Drive 0 pre_high_time.
21:18	Primary Drive 0 udma_cycle_time.
17:13	Primary Drive 0 cmd_low_time. Cycles=Value+1
12:9	Primary Drive 0 cmd_high_time. Cycles=Value+1
8:4	Primary Drive 0 data_low_ time cycle number. Cycles=Value+1
3:0	Primary Drive 0 data_high_time cycle number. Cycles=Value+1

IDE Timing 1 Register

Address: 44h-47h
I/O Address: 64h-67h
Attribute: R/W

BIT	DESCRIPTION
31	Primary Drive 1 Buffer Enable for PIO Read/Write. 0=disable, 1=enable
30	Primary Drive 1 PIO_MST Enable. 0=disable, 1=enable. PIO_MST means the chip working in bus master state on PCI side, but device working in PIO mode.
29	Primary Drive 1 Normal DMA Enable. 0=disable, 1=enable.
28	Primary Drive 1 UDMA Enable. 0=disable, 1=enable.
27:25	Primary Drive 1 cmd_pre_high_time.
24:22	Primary Drive 1 pre_high_time.
21:18	Primary Drive 1 udma_cycle_time.
17:13	Primary Drive 1 cmd_low_time. Cycles=Value+1
12:9	Primary Drive 1 cmd_high_time. Cycles=Value+1
8:4	Primary Drive 1 data_low_time cycle number. Cycles=Value+1
3:0	Primary Drive 1 data_high_time cycle number. Cycles=Value+1

IDE Timing 2 Register

Address: 48h-4Bh
I/O Address: 68h-6Bh
Attribute: R/W

BIT	DESCRIPTION
31	Secondary Drive 0 Buffer Enable for PIO Read/Write. 0=disable, 1=enable.
30	Secondary Drive 0 PIO_MST Enable.0=disable, 1=enable. PIO_MST means the chip working in bus master state on PCI side, but device working in PIO mode.
29	Secondary Drive 0 Normal DMA Enable. 0=disable, 1=enable.
28	Secondary Drive 0 UDMA Enable. 0=disable, 1=enable.
27:25	Secondary Drive 0 cmd_pre_high_time.
24:22	Secondary Drive 0 pre_high_time.
21:18	Secondary Drive 0 udma_cycle_time.
17:13	Secondary Drive 0 cmd_low_time. Cycles=Value+1
12:9	Secondary Drive 0 cmd_high_time. Cycles=Value+1
8:4	Secondary Drive 0 data_low_time cycle number. Cycles=Value+1
3:0	Secondary Drive 0 data_high_time cycle number. Cycles=Value+1

IDE Timing 3 Register

Address: 4Ch-4Fh
I/O Address: 6Ch-6Fh
Attribute: R/W

BIT	DESCRIPTION
31	Secondary Drive 1 Buffer Enable for PIO Read/Write. 0=disable, 1=enable.
30	Secondary Drive 1 PIO_MST Enable. 0=disable, 1=enable. PIO_MST means the chip working in bus master state on PCI side, but device working in PIO mode.
29	Secondary Drive 1 Normal DMA Enable. 0=disable, 1=enable.
28	Secondary Drive 1 UDMA Enable. 0=disable, 1=enable.
27:25	Secondary Drive 1 cmd_pre_high_time.
24:22	Secondary Drive 1 pre_high_time.
21:18	Secondary Drive 1 udma_cycle_time.
17:13	Secondary Drive 1 cmd_low_time. Cycles=Value+1
12:9	Secondary Drive 1 cmd_high_time. Cycles=Value+1
8:4	Secondary Drive 1 data_low_time cycle number. Cycles=Value+1
3:0	Secondary Drive 1 data_high_time cycle number. Cycles=Value+1

***Notes:** Refer to Chapter 6.1 on how to use IDE Timing X registers.

MISC.Control 1 Register(Primary IDE Channel)

Address: 50h
I/O Address: 70h
Attribute: R/W

BIT	DESCRIPTION
7	Enable clear SG bit. 0=Disable, 1=Enable. When SG Counter is greater than IDE transfer size, if this bit is 1, hardware will automatically clear SG State Machine after Interrupt asserted. This bit is R/W.
6	Channel 0 Read Flush Bit. 0=Not Flush, 1=Flush. Software flush all contents in FIFO by writing a 1 to this bit.
5	Clear All State Machine Bit. 0=Not Clear, 1=Clear. Software clear all State Machine by writing a 1 to this bit. Clear all state machine is one PCI Clock Pulse.
4	Clear SG Counter bit. 0=Not Clear Counter, 1=Clear Counter. Software clear SG Counter by writing a 1 to this bit. Clear SG Counter is one PCI Clock Pulse.
3	Disable channel 0 Block Read/Write Bit. 1=Disable Block Read/Write, 0=Enable Block Read/Write. After reset, this bit is 0. Software can set this bit by writing a 1 to it. It is cleared by writing a 0 to this bit. This bit is R/W.
2	Primary IDE channel enable Bit. 1=Enable, 0=Disable. After reset, this bit is set to 1. Software can disable this bit by writing a 0 to it.
1	Clear ATA data buffer 0 Bit. 1=Clear, 0=not clear. Software clear buffer pointer and counter to 0 by writing this bit to 1. Clear ATA data buffer signal is one PCI clock Pulse only.
0	Allocate Address 1Fx Enable Bit. 1=enable, 0=disable. After reset, this bit is set to 0. If Dis_alc pin=0, then hardware set this bit to 1 automatically. Enable means that all Primary IDE Device Registers are allocated to I/O. BA offset 0X10, 0X14. This bit=0(Disable) means all Primary IDE Registers are at Default IDE Address. This bit is Read Only.

MISC.Control 2 Register(Primary IDE Channel)

Address: 51h
I/O Address: 71h
Attribute: R/W

BIT	DESCRIPTION
15:10	Reserved
9	Fast Interrupt Enable Bit. 1=enable, 0=disable. If enable, Interrupt will be generated before IDE interrupt occur. After reset, this bit is 0. R/W
8	Hold channel 0 Interrupt enable bit. 1=enable, 0 =disable. If enable, when read from IDE interrupt will be gernerated afte the buffer is empty. After reset, this bit is 0. R/W

MISC.Control 3 Register(Primary IDE Channel)

Address: 52h-53h
I/O Address: 72h-73h

BIT	DESCRIPTION
31	Soft tri-state IDE bus enable bit. 0=disable, 1=enable. Software write a 1 to enable. After Reset, this bit is set to 0. R/W
30	Bus Parking AD&CBE output enable. 0=disable, 1=enable. If this bit enable when PCI GNT_Parking on IDE, PCI AD&CBE will be drive by HPT370. After reset this bit=0. R/W
29:27	SG State Machine Number. Read Only.
26:25	Fast Interrupt Byte counter setting Register. If 0 is set, Interrupt will be sent when the SG Counter remain 512 Bytes. If 1 is set, Interrupt will be sent when the SG Counter remain 1K Bytes. If 2 is set, Interrupt will be sent when SG Counter remain 2K Bytes. These Bits are R/W.
24:16	Bytes Number Remained in the channel 0 Buffer. Read Only.

MISC.Control 4 Register(Secondary IDE Channel)

Address: 54h
I/O Address: 74h
Attribute: Read Only

BIT	DESCRIPTION
7	Enable clear SG bit. 0=Disable, 1=Enable. When SG Counter is greater than IDE transfer size, if this bit is 1, hardware will automatically clear SG State Machine after Interrupt asserted. This bit is R/W.
6	Channel 1 Read Flush Bit. 0=Not Flush, 1=Flush. Software flush all contents in FIFO by writing a 1 to this bit.
5	Clear All State Machine Bit. 0=Not Clear, 1=Clear. Software clear all State Machine by writing a 1 to this bit. Clear all state machine is one PCI Clock Pulse.
4	Clear SG Counter bit. 0=Not Clear Counter, 1=Clear Counter. Software clear SG Counter by writing a 1 to this bit. Clear SG Counter is one PCI Clock Pulse.
3	Disable channel 1 Block Read/Write Bit. 1=Disable Block Read/Write, 0=Enable Block Read/Write. After reset, this bit is 0. Software can set this bit by writing a 1 to it. It is cleared by writing a 0 to this bit. This bit is R/W.
2	Secondary IDE channel enable Bit. 1=Enable, 0=Disable. After reset, this bit is set to 1. Software can disable this bit by writing a 0 to it.
1	Clear ATA data buffer 1 Bit. 1=Clear, 0=not clear. Software clear buffer pointer and counter to 0 by writing this bit to 1. Clear ATA data buffer signal is one PCI clock Pulse only.
0	Allocate Address 17x Enable Bit. 1=enable, 0=disable. After reset, this bit is set to 0. If Dis_alc pin=0, then hardware set this bit to 1 automatically. Enable means that all Secondary IDE Device Registers are allocated to I/O. BA offset 0X18, 0X1C. This bit=0(Disable) means all Secondary IDE Registers are at Default IDE Address. This bit is Read Only.

MISC.Control 5 Register(Secondary IDE Channel)

Address: 55h
I/O Address: 75h

BIT	DESCRIPTION
15:10	Reserved
9	Fast Interrupt Enable Bit. 1=enable, 0=disable. If enable, Interrupt will be generated before IDE interrupt occur. After reset, this bit is 0. R/W
8	Hold channel 1 Interrupt enable bit. 1=enable, 0 =disable. If enable, when read from IDE interrupt will be gernerated afte the buffer is empty. After reset, this bit is 0. R/W

MISC.Control 6 Register(Secondary IDE Channel)

Address: 56h-57h
I/O Address: 76h-77h
Attribute: Read Only

BIT	DESCRIPTION
31	Soft tri-state IDE bus enable bit. 0=disable, 1=enable. After reset, this bit is set to 0. R/W
30	Bus Parking AD&CBE output enable. 1=enable, 0=disable. If this bit enable when PCI GNT_Parking on IDE AD&CBE will be drive by HPT370. After reset, this bit=0. R/W
29:27	SG State Machine Number. Read Only.
26:25	Fast Interrupt Byte counter setting Register. If 0 is set. Interrupt will be sent when the SG Counter remain 512 Bytes. If 1 is set, Interrupt will be sent when the SG Counter remain 1K Bytes. If 2 is set, Interrupt will be sent when SG Counter remain 2K Bytes. R/W
24:16	Bytes Number Remained in the channel 1 Buffer. Read Only.

Bus Status 1 Register

Address: 58h
I/O Address: 78h
Attribute: Bit 0-5 is Read Only.

BIT	DESCRIPTION
7	Reserved
6	Reserved
5	Secondary channel DMARQ
4	Secondary channel DMACK_
3	Secondary channel I/O CHRDY
2	Primary channel DMARQ
1	Primary channel DMACK_
0	Primary channel IO CHRDY

Bus Status 2 Register

Address: 59h
I/O Address: 79h

BIT	DESCRIPTION
7	Secondary IDE bus soft reset. R/W
6	Primary IDE bus soft reset. R/W
5	Secondary POLL_EN Reset to 0. R/W
4	Secondary IRQ_DEV1. Read Only
3	Secondary channel IRQ_DEV0. Read Only
2	Primary Auto POLL Function Enable. If this bit is set, HPT370 will start auto poll function after an NOP Auto Poll command is issued by the host. As defined by ATA/ATAPI-4 specification, HPT370 will return ERR bit as "0" regardless the value read from an attached device. The Auto Poll Function is terminated upon any ATA port read or write access by the host Reset to 0. R/W
1	Primary IRQ_DEV1. Read Only
0	Auto Poll Status. "1" indicates a successful poll is found. Read Only

Soft Control 1 Register

Address: 5Ah
I/O Address: 7Ah
Attribute: R/W

BIT	DESCRIPTION
7	Soft_W_SCL, R/W. When soft write 0 or 1 to this bit, it can generate SCL signal of SPROM.
6	Soft_W_SDA, R/W. When soft write 0 or 1 to this bit, it can generate SDA signal of SPROM.
5	Soft_W_SROM_en, R/W. 1=R/W SPROM through soft program Soft_W_SCL and Soft_W_SDA registers; 0=disable soft programming SPROM.
4	Disable interrupt register, 0=enable 1=disable.R/W
3	Disable PCI function, 0=enable 1=disable. R/W
2	Enable write interrupt pin and Subsystem ID register, 0=disable 1=enable. R/W
1	P_CBLID, cable detect signal for Primary IDE channel. Read Only
0	S_CBLID, cable detect signal for Secondary IDE channel. Read Only

Soft Control 2 Register

Address: 5Bh
I/O Address: 7Bh

BIT	DESCRIPTION
7	osc_ok. 1=osc is ready; 0=osc is not ready. Read Only
6	Reserved
5	Enable osc output. 0=enable the osc output to IRQ15 pin. Default=1b. It is used for debug ging only.
4	Ext_CLK_en. 0=disable external clock, 1=enable external clock. Default=0b
3	BLOCK_PIO_16b_ . 0=16bit Block PIO, 1=32bit block PIO. Default=0b
2	No waiting DMARQ when start bus master state machine. 1=no waiting DMARQ, 0=waiting DMARQ. Default=0b
1	Single clock enable bit, Default=1b
0	Enable output MA15, MA16, Default=1b

f_low Register

Address: 5Ch-5Dh
I/O Address: 7Ch-7Dh
Attribute: Read/Write

BIT	DESCRIPTION
8:0	This register is used to adjust the Output Frequency in DPLL.

f_high Register

Address: 5Eh-5Fh
I/O Address: 7Eh-7Fh
Attribute: Read/Write

BIT	DESCRIPTION
24:16	This register is used to adjust the Output Frequency in DPLL.

Capability ID Register

Address: 60h
I/O Address: 80h
Attribute: Read Only

BIT	DESCRIPTION
7:0	Hardwared to 01h.

Next Item Pointer Register

Address: 61h
I/O Address: 81h
Attribute: Read Only

BIT	DESCRIPTION
7:0	Default=00h.

Power Management Capabilities Register

Address: 62h-63h
I/O Address: 82h-83h
Attribute: Read Only

Bit	DESCRIPTION
15:11	PME_Support. This field indicates the power states in which the function may assert PME#. Default=00000b. Read only.
10	D2_Support. 1 means this function supports the D2 Power Management State. Default=0b. Read only.
9	D1_Support. 1 means this function supports the D1 Power Management State. Default=1'b0. Read only.
8:6	Aux_Current. This field reports the 3.3Vaux auxiliary current requirements for the PCI function. Default=0b. Read only.
5	DSI. The Device Specific Initialization bit indicates whether special initialization of this function is required(beyond the standard PCI configuration header) before the generic class device driver is able to use it. Default=1b. Read only.
4	Reserved
3	PME Clock. 1 indicates that the function relies on the presence of the PCI clock for PME# operation. 0 indicates that no PCI clock is required for the function to generate PME#. Default=0b. Read only.
2:0	Version. 010b indicates that this function complies with Revision 1.1 of the PCI Power Management Interface Specification. Default=010b. Ready only.

Power Management Control/Status Register

Address: 64h-65h
I/O Address: 84h-85h
Attribute: Read Only

BIT	DESCRIPTION
15	PME_Status. This bit is set when the function would normally assert the PME# signal independent of the state of the PME_En bit. Default=0b. Read only.
14:13	Data_Scale. This field indicates the scaling factor to be used when interpreting the value of the Data register. Default=00b. Read only.
12:9	Data_Select. This field is used to select which data is to be reported through the Data register and Data_Scale field. Default=0000b. Read only.
8	PME_En. Enable function to assert PME#. Default=0b. Read only.
7:2	Reserved
1:0	PowerState. This field is used both to determine the current power state of a function and to set the function into a new power state. Default=00b. Read only.

PMCSR Bridge Supports Extensions

Address: 66h
I/O Address: 86h
Attribute: Read Only

BIT	DESCRIPTION
7:0	Reserved.

Data Register

Address: 67h
I/O Address: 87h
Attribute: Read Only

BIT	DESCRIPTION
7:0	Data. This bit is used to report the state dependent data requested by the Data_Select field. Default=00h. Read only.

f_CNT

Address: 78h-79h
I/O Address: 98h-99h
Attribute: Read Only

BIT	DESCRIPTION
9:0	This register is used to identify the Intput Frequency in DPLL.

3.3 I/O Space Registers

Bus Master Command Register

Primary Channel: 00h,
Secondary Channel: 08h
Attribute: R/W

BIT	DESCRIPTION
7:4	Reserved
3	Bus Master R/W Control.Bus Master Read (Disk Write)=0,Bus Master Write (DiskRead)=1.
2:1	Reserved
0	Start/Stop Bit.Start=1, Stop=0.When This Bit is set to 1, Bus Master operation will be started. After this Bit is clear to 0,Bus Master operation will be stopped.

Bus Master Status Register

Primary Channel: 02h,
Secondary Channel: 0Ah
Attribute: R/W

BIT	DESCRIPTION
7	Reserved
6	Drive 1 DMA Capable.1=Drive support DMA, 0=Drive does not support DMA. This Bit Softw are use Only.Not affect Hardware operation.
5	Drive 0 DMA Capable.1=Drive support DMA, 0=Drive does not support DMA. This Bit Softw are use Only.Not affect Hardware operation.
4 : 3	Reserved
2	Interrupt Status Bit.1=Device issue an Interrupt, 0=Device does not issue an Interrupt. Software sets this bit to 0 by writing a 1 to it. This Bit perates on both Bus Master Mode and Slave Mode.
1	DMA Error Bit.This bit is set to 1 when target abort or master abort happened. Software set this to 0 by writing 1 to it.
0	Read Only Bit. Bus Master Active Bit. 1=Bus master operation is processing. 0=no bus master operation.

Bus Master Scatter Gather Table Base Register

Primary Channel: 04h-07h
Secondary Channel: 0Ch-0Fh
Attribute: R/W

BIT	DESCRIPTION
31:2	Bus Master Scatter Gather Table Base Address.
1 : 0	Reserved

Chapter 4
Electrical Parameters

This chapter defines the electrical characteristics and constraints of PCI components and systems.

The PCI electrical definition provides for 3.3V signaling environments, and all IOs of HPT370 are 5V tolerant.

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4.1 3.3V Signaling Environment

The 3.3V environment is based on Vcc-relative switching voltages and is an optimized CMOS approach.

DC Specifications

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS	NOTES
Vcc	Supply Voltage		3.0	3.6	V	
Vih	Input High Voltage		0.5Vcc	Vcc+0.5	V	
Vil	Input Low Voltage		-0.5	0.3Vcc	V	
Vipu	Input Pull-up Voltage		0.7Vcc		V	1
Iil	Input Leakage Current	0<Vin<Vcc		+10	uA	2
Voh	Output High Voltage	Iout=-500uA	0.9Vcc		V	
Vol	Output Low Voltage	Iout=1500uA		0.1Vcc	V	
Cin	Input Pin Capacitance			10	pF	3
Cclk	**CLK** Pin Capacitance		5	12	pF	
CIDSEL	**IDSEL** Pin Capacitance			8	pF	4
lpin	Pin Inductance			20	nH	5

***Notes:** 1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.

2. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tri-state outputs.
3. Lower capacitance on this input-only pin allows for non-resistive coupling to **AD[xx].**
4. This is a recommendation, not an absolute requirement. The actual value should be provided with the component data sheet.

AC Specifications

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNITS	NOTE-S
Ioh(AC)	Switching Current High	0<Vout≤0.3Vcc	-12Vcc		mA	1
		0.3Vcc<Vout<0.9Vcc	-17.1(Vcc-Vout)		mA	1
		0.7Vcc<Vout<Vcc		Eqt'nC		1,2
	(Test Point)	Vout=0.7Vcc		-32Vcc	mA	2
Iol(AC)	Switching Current Low	Vcc>Vout>0.6Vcc	16Vcc		mA	1
		0.6Vcc>Vout>0.1Vcc	26.7Vout		mA	1
		0.18Vcc>Vout>0		Eqt'nD		1,2
	(Test Point)	Vout=0.18Vcc		38Vcc	mA	2
Icl	Low Clamp Current	-3<Vin<-1	-25+(Vin+1)/0.015		mA	
Ich	High Clamp Current	Vcc+4>Vin>Vcc+1	25+(Vin-Vcc-1)/0.015		mA	
$slew_r$	Output Rise Slew Rate	0.2Vcc-0.6Vcc load	1	4	V/ns	3
$slew_f$	Output Fall Slew Rate	0.6Vcc-0.2Vcc load	1	4	V/ns	3

Notes:
1. Switching current characteristics for REQ_ and GNT_ are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST_ which are system outputs.
2. Maximum current requirements must be met as drivers pull beyond the first step voltage. The equation defined maxima should be met by design.
3. This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range.

Chapter 5
Key Timing

This chapter is organized into the following sections:

- Timing Parameters
- Clock Timing
- Read Transaction
- Write Transaction
- IDE Timing

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5.1 Timing Parameters

The table below provides the timing parameters for 5V and 3.3V signaling environments.

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
t_{val}	CLK to Signal Valid Delay bused signals	2	11	ns	1,2
$t_{val(ptp)}$	CLK to Signal Valid Delay point to point	2	12	ns	1,2
t_{on}	Float to Active Delay	2		ns	1
t_{off}	Active to Float Delay		28	ns	1
t_{su}	Input Set up Time to CLK-bused signals	7		ns	2,3
$t_{su(ptp)}$	Input Set up Time to CLK-point to point	10,12		ns	2,3
t_{h}	Input Hold Time from CLK	0		ns	3
t_{rst}	Reset Active Time After Power Stable	1		ms	4
$t_{rst-clk}$	Reset Active Time After CLK Stable	100		us	4
$t_{rst-off}$	Reset Active to Output Float delay		40	ns	4

Notes:
1. For parts compliant to the 3.3V signaling environment:
   Maximum times are evaluated with the following load circuits, for high-going and low-going edges respectively.
2. REQ and GNT_ are point-to-point signals, and have different output valid delay and input setup times than do bused signals. GNT_ has a setup of 10; REQ has a setup of 12. All other signals are bused.
3. RST_ is asserted and deasserted asynchronously with respect to CLK.
4. All output drivers must be asynchronously floated when RST_ is active.

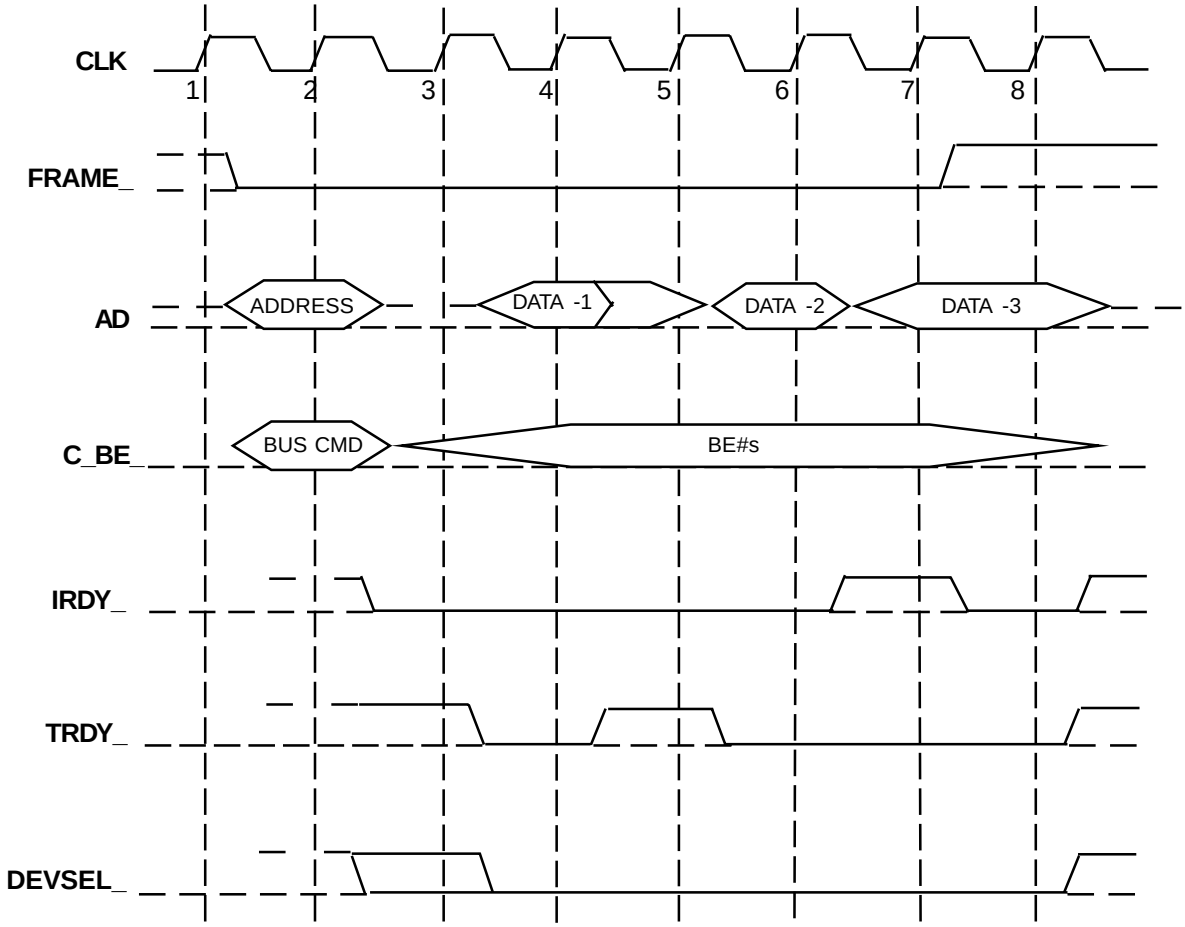
5.2 Clock Timing

Clock Specifications

		66	MHz	33	MHz		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
tcyc	CLK Cycle Time	15	30	30		ns	1
thigh	CLK High Time	6		11		ns	
tlow	CLK Low Time	6		11		ns	
-	CLK Slew Rate	1.5	4	1	4	V/ns	2

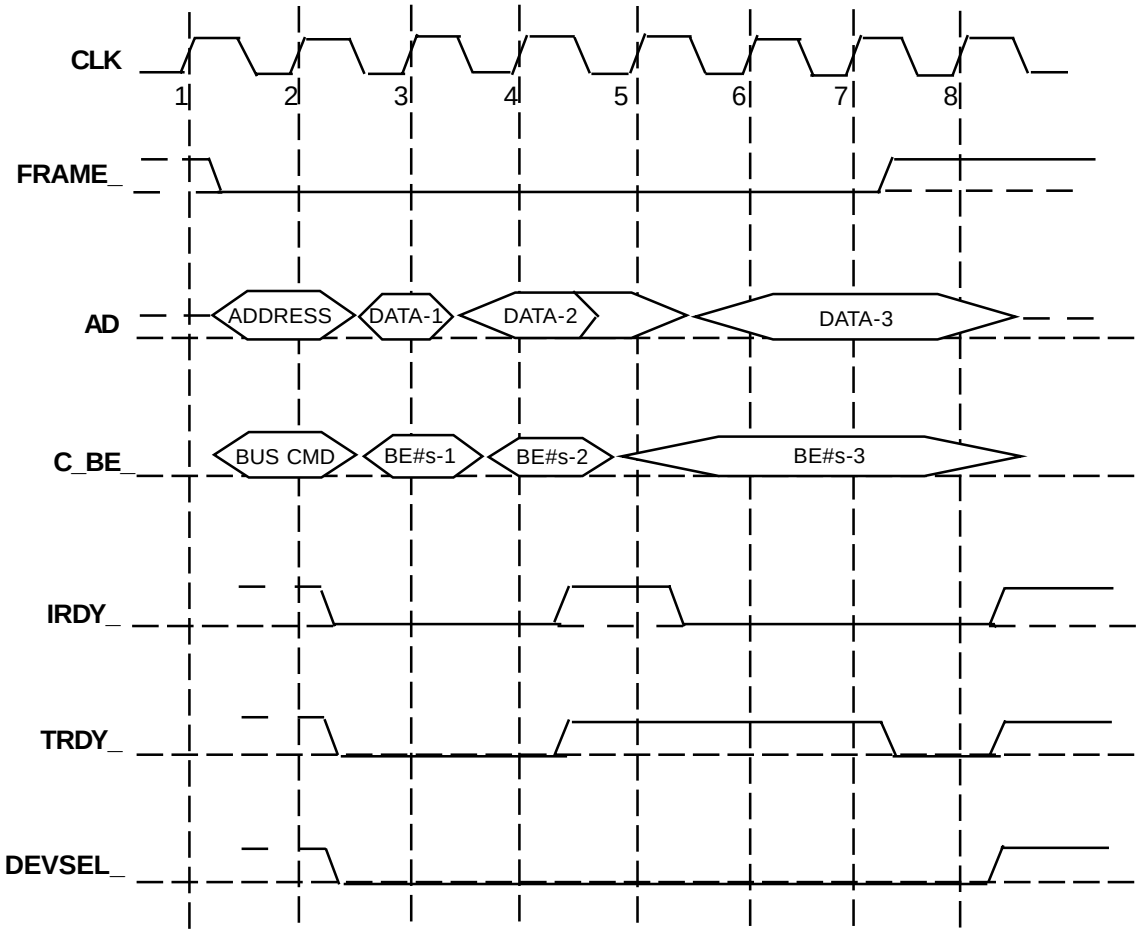
Notes:
1. In general, all 66MHz PCI components must work with any clock frequency up to 66MHz. The clock frequency may be changed at any time during the operation of the system so long as the clock edges remain clean and the minimum cycle and high and low times are not violated. The clock may only be stopped in a low state.
2. The minium clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter.

5.3 Read Transaction



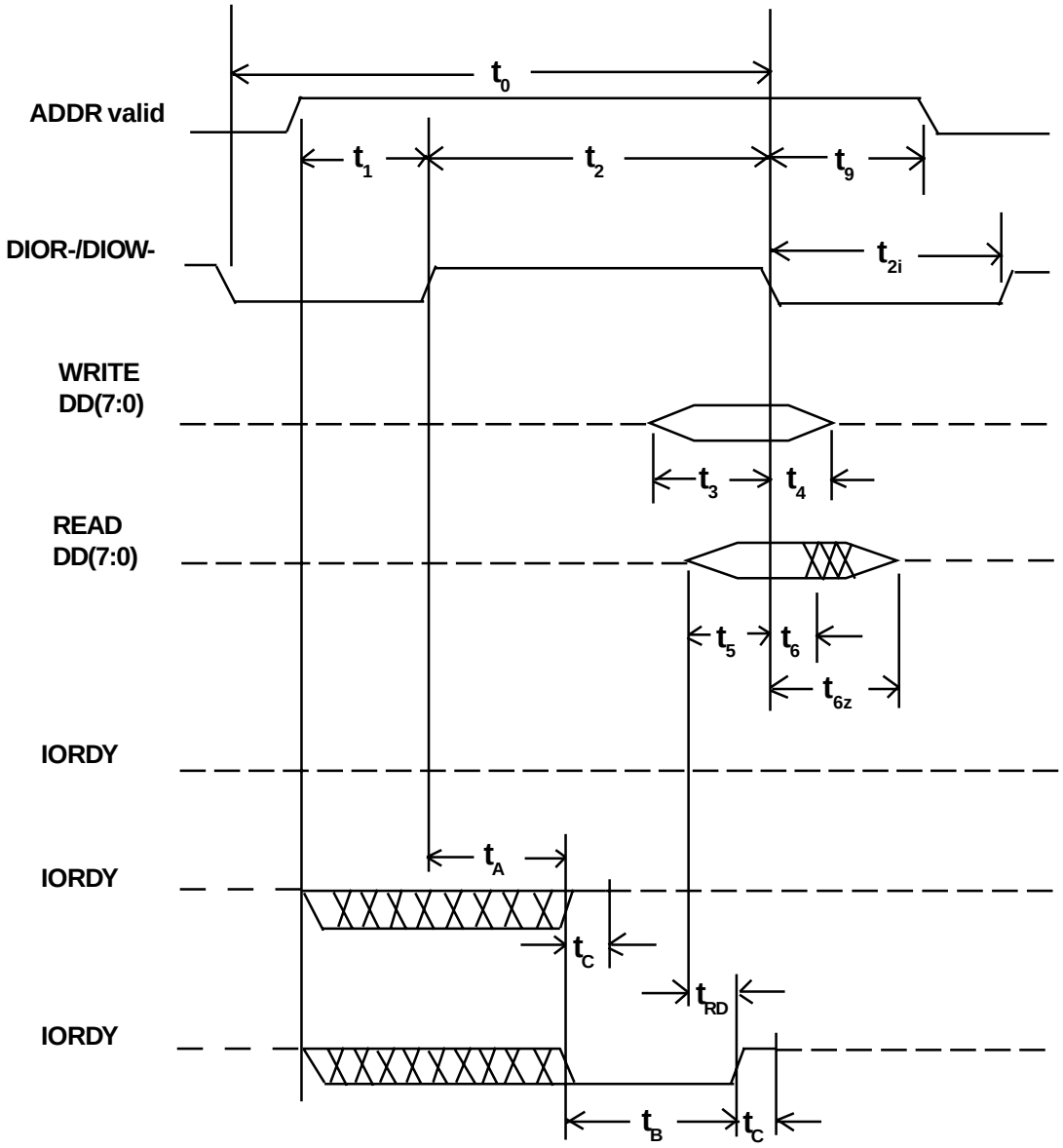
***Notes:** The transaction starts with an address phase which occurs when **FRAME_** is asserted for the first time and occurs on clock 2. During the address phase, **AD[31:0]** contain a valid address and **C/BE_[3:0]** contain a valid bus command.

5.4 Write Transaction



***Notes:** The transaction starts when **FRAME**_ is asserted for the first time which occurs on clock 2. A write transaction is similar to a read transaction except no turnaround cycle is required following the address phase because the master provides both address and data. Data phases work the same for both read and write transactions.

5.5 IDE Timing



Notes:
1. Device address consists of signals CS0_, CS1_ and DA(2:0).
2. Data consists of DD(7:0).
3. The negation of IORDY_ by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the assertion of DIOR-or DIOW-.

PIO Timing Parameters

PIO	Timing Parameters	Mode0 ns	Mode1 ns	Mode2 ns	Mode3 ns	Mode4 ns	Note
t_0	Cycle time (min)	600	383	240	180	120	1
t_1	Address valid to DIOR-/ DIOW-setup (min)	70	50	30	30	25	
t_2	DIO-/DIOW-pulse width 16-bit (min)	105	125	100	80	70	1
t_{2i}	DIOR-/DIOW-recovery time (min)	-	-	-	70	25	1
t_3	DIOW-data setup (min)	60	45	30	30	20	
t_4	DIOW-data hold (min)	30	20	15	10	10	
t_5	DIOR-data setup (min)	50	35	20	20	20	
t_6	DIOR- data hold (min)	5	5	5	5	5	
t_{6Z}	DIOR- data tristate (min)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold (min)	20	15	10	10	10	
t_{RD}	Read data Valid to IORDY active(if IORDY initialy low after t_{Aa}) (min)	0	0	0	0	0	
t_A	IORDY Setup time (min)	35	35	35	35	35	3
t_B	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	
t_C	IORDY assertion to release (max)	5	5	5	5	5	

Notes:
1. t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirement is greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
2. This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device(tri-state).
3. The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY# negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY# negated at the time t_A after the activation of DIOR- or DIOW-, then tRD shall be met and t_5 is not applicable.

Chapter 6
Programming Guide

This chapter will help you to learn the necessary points for programming HPT370.

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6.1 Device Mode Setting

Register	43h, 47h, 4Bh, or 4Fh								42h, 46h, 4Ah, or 4Eh								41h, 45h, 49h, 4Dh								40h, 44h, 48h, or 4Ch								32 Bit Value	Soft Control 2 Register(5Bh) Value
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
	Buffer enable	MST enable	DMA enable	UDMA enable	cmd_pre_high_time				pre_high_ time		udma_cycle_time				cmd_low_time					cmd_high_time					low time cycle number				high time cycle number					
Device Mode	Just for PIO 1=FIFO enable for 16bits or 32bits block PIO (Defaut=16 bits), 0=no FIFO and 16 bits.	For PIO, 1=IC in bus master mode during PIO, must be 0 if bit 29 or 28 is set.	Enable multiword DMA, must be 0 if bit 28 is set.	Enable Ultra DMA, must be 0 if bit 29 is set.	This time to initialize the first PIO cycle for task file register access.				The time to initialize the first cycle for PIO and Multiword DMA data transfer.		Bit21 for CLK frequency, 0=ATA clock, 1=dual ATA clock.	Bits 20-18: Number of clock cycles for Ultra DMA transfer.			Active time of DIOW_ or DIOR_ during task file register access, cycles=val+1					Inactive time of DIOW_ or DIOR_ during task file register access, cycles=val+1					Active time of DIOW_ or DIOR_ during PIO and Multiword DMA data transfers, cycles=val+1				Inactive time of DIOW_ or DIOR_ during PIO and Multiword DMA data transfers, cycles=val+1					
PIO Mode 0	0	0	0	0	3				2		4				A					7					5				7				06 91 4E 8A	22
PIO Mode 1	0	0	0	0	3				2		4				A					7					4				3				06 91 4E 65	22
PIO Mode 2	0	0	0	0	3				1		4				A					7					3				3				06 51 4E 33	22
PIO Mode 3	0	0	0	0	3				1		4				A					7					2				2				06 51 4E 22	22
PIO Mode 4	0	0	0	0	3				1		4				A					7					2				1				06 51 4E 21	22
Multiword DMA Mode 0	0	0	1	0	3				1		4				A					7					9				7				26 51 4E 97	22
Multiword DMA Mode 1	0	0	1	0	3				1		4				A					7					3				3				26 51 4E 33	22
Multiword DMA Mode 2	0	0	1	0	3				1		4				A					7					2				1				26 51 4E 21	22
Ultra DMA Mode 0	0	0	0	1	3				1		4				A					7					3				1				16 51 4E 31	22
Ultra DMA Mode 1	0	0	0	1	3				1		3				A					7					3				1				16 4D 4E 31	22
Ultra DMA Mode 2	0	0	0	1	3				1		2				A					7					3				1				16 49 4E 31	22
Ultra DMA Mode 3	0	0	0	1	3				1		B				A					7					3				1				16 6D 4E 31	22
Ultra DMA Mode 4	0	0	0	1	3				1		1				A					7					3				1				16 45 4E 31	22
Ultra DMA Mode 5 (Read)	0	0	0	1	3				1		1				A					7					3				1				16 45 4E 31	22
Ultra DMA Mode 5 (Write)	0	0	0	1	5				2		1				F					A					4				2				1A 85 F4 42	20

Notes:

1. Bit28, Bit 29 and Bit30 can be either enabled, but only one bit can be enabled at the same time.
2. Dual ATA Clock is to implement ATA100 read and write at different clocks.
3. Registers Match:

	PCI Cfg. Address	Mapped I/O Offset Address
IDE Timing 0 Register (Primary Drive 0)	40h-43h	60h-63h
IDE Timing 1 Register (Primary Drive 1)	44h-47h	64h-67h
IDE Timing 2 Register (Secondary Drive 0)	48h-4Bh	68h-6Bh
IDE Timing 3 Register (Secondary Drive 1)	4Ch-4Fh	6Ch-6Fh
Soft Control 2 Register	5Bh	7Bh

(Refer to Chapter 3 for details on these four Registers.)

4. Here is the way to Set a hard disk's mode through accessing I/O space:
   Step 1: Check the I/O Base Address for the HPT370 controller;
   Step 2: Calculate the registers' address in I/O space(Base Address+Offset);
   Step 3: Write the registers I/O space address with a particular value;
   Step 4: Write the Soft Control 2 register with a particular value;

   Suppose the base address for HPT370 controller is E000, here are some examples:

   (1) To set Ultra DMA Mode 5(Write) for a hard disk connected as Primary Slave
   Step 1. Write the I/O address E064h-E067h(E000+[64h-67h]) with the value 1A85F442h;
   Step 2. Write the I/O address E07Bh(E000+7Bh) with the value 20h.

   (2) To set Ultra DMA Mode 5(Read) for a hard disk connected as Primary Slave
   Step 1. Write the I/O address E064h-E067h(E000+[64h-67h]) with the value 16454E31h;
   Step 2. Write the I/O address E07Bh(E000+7Bh) with the value 22h.

   (3) To set PIO Mode 2 for a hard disk connected as Primary Slave
   Step 1. Write the I/O address E064h-E067h(E000+[64h-67h]) with the value 06514E33h;
   Step 2. Write the I/O address E07Bh(E000+7Bh) with the value 22h.

   (4) To set Multiword DMA mode 2 for a hard disk connected as Secondary Master
   Step 1. Write the I/O address E068h-E06Bh(E000+[68h-6Bh]) with the value 26514E21h;
   Step 2. Write the I/O address E07Bh with the value 22h.

6.2 PRST_ and SRST_ pins control

The Tri-state of PRST_ and SRST_ pins are controlled combiningly by Soft_RST and Soft_TRI bits.

Controlling Bits Index:

	Soft_RST	Soft_TRI
PRST_	Bus Status 2 Register Bit(6)	MISC. Control 3 Register Bit(31)
SRST_	Bus Status 2 Register Bit(7)	MISC. Control 6 Register Bit(31)

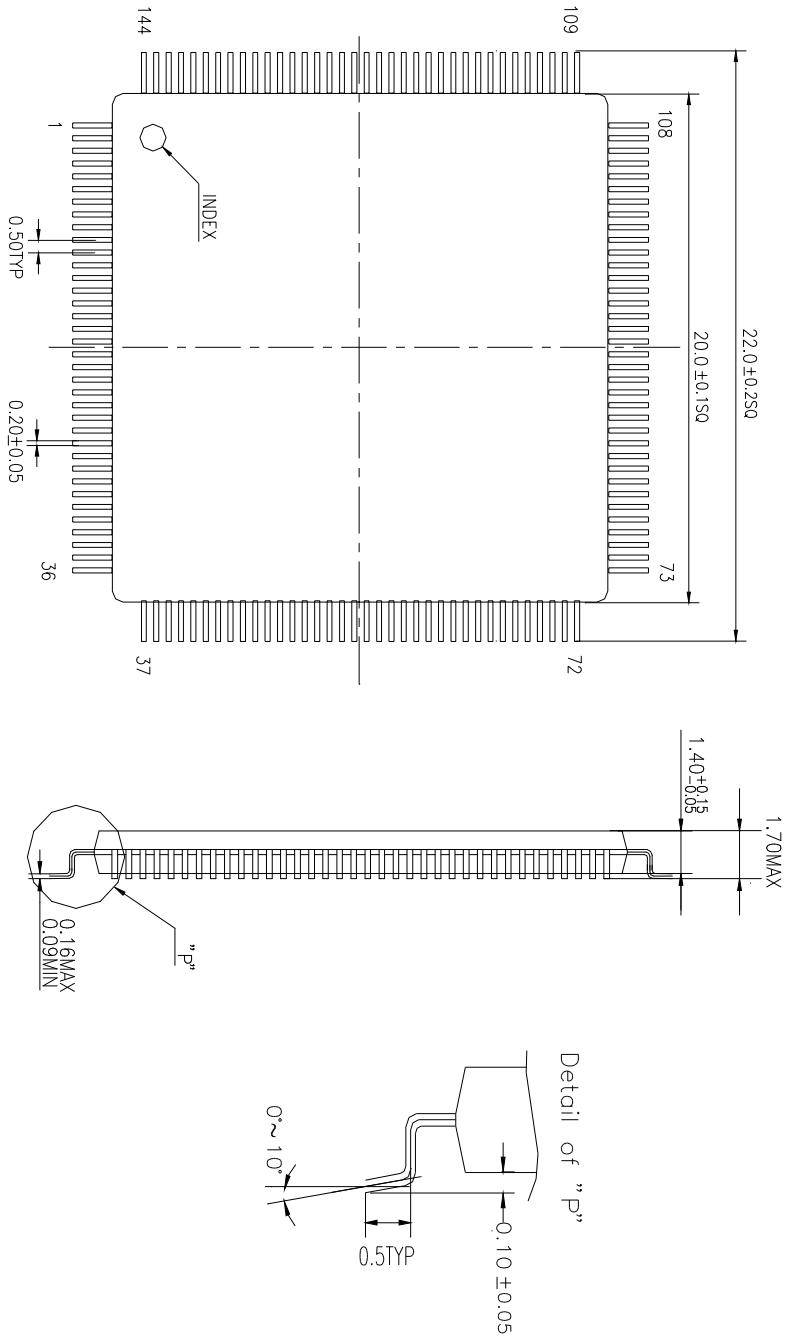
Bits setting:

	Soft_RST	Soft_TRI	PRST_(SRST_)
	1	1	Z
	1	0	0
	0	X	1
Default:	0	0	1

Appendix A
Package Dimensions

This chapter contains the package drawing of HPT370.
HPT370 package is 144-pin LQFP.

A.1 144-pin LQFP



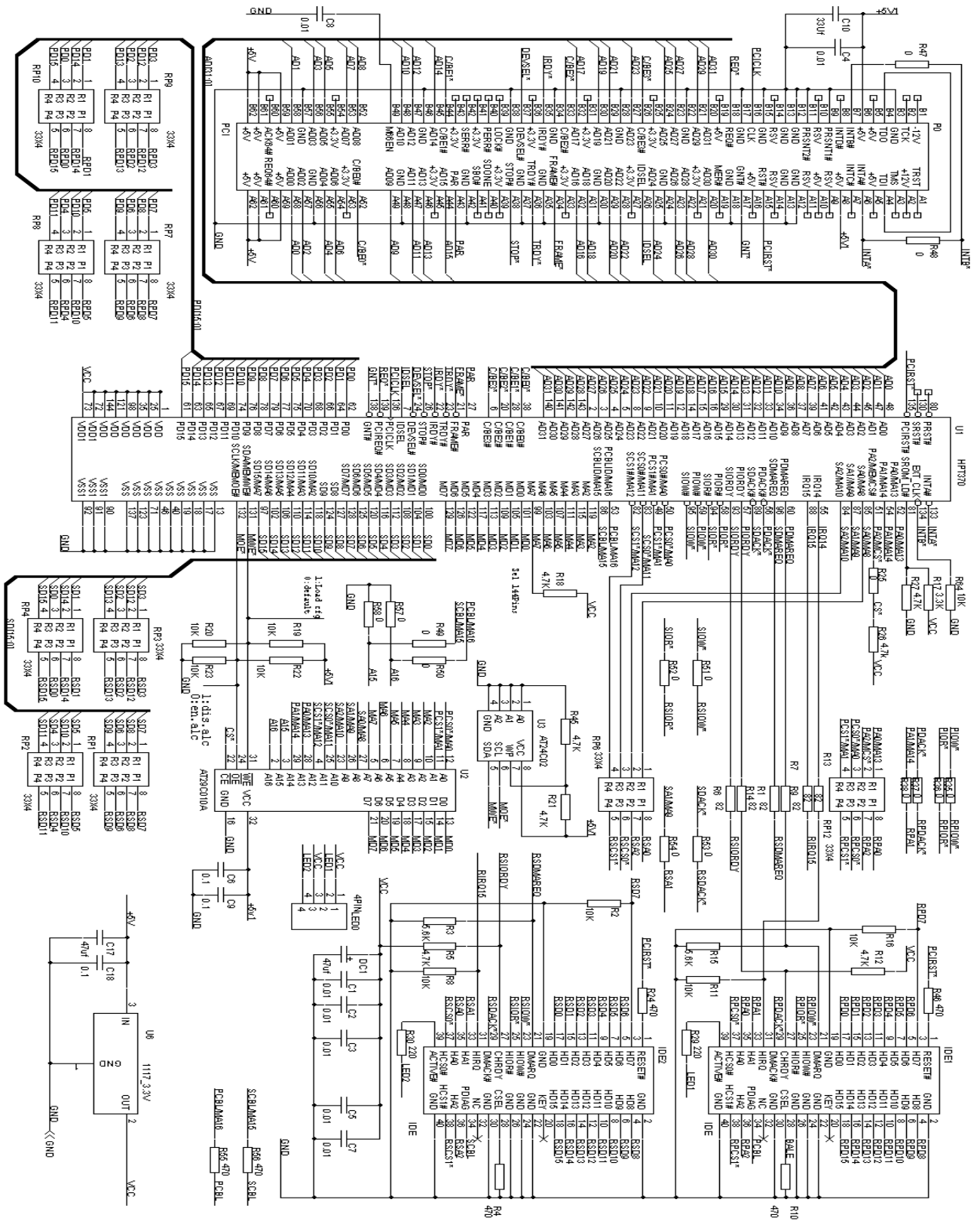
Appendix B
Application Circuits

This appendix contains the following contents:

* Schematic Diagram for Add-On Card
* Schematic Diagram for Mainboard
* Layout for Add-On Card
* Schematic Diagram for Hotswap Function

HighPoint

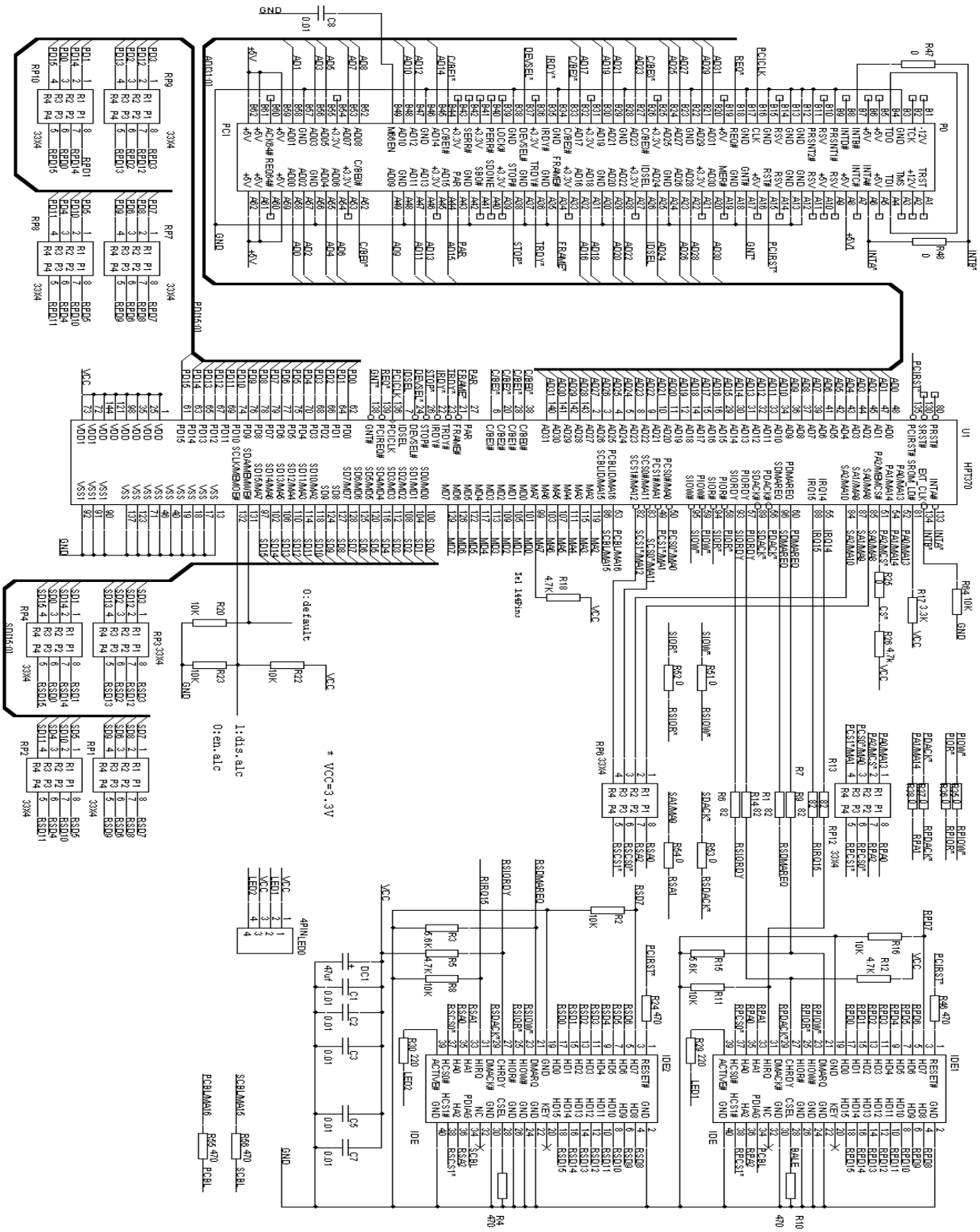
B.1 Schematic Diagram for Add-On Card



Notes:

1. HPT370 power supply(VCC) is 3.3v. The optional box on the lower right corner of the schematic must be used if the system power supply is 5v.
2. IDE address allocation mode is selected by using either R22 or R23 (When using R22 only, HPT370 will decode 1f0-1f7, 3f6 on ATA channel 0, 170-177, 376 on ATA channel 1; when using R23 only, HPT370 will decode operating system assigned addresses as specified by PCI IDE controller specification.).
3. R17 and R27 are alternative. When using R27, HPT370 will try to load configuration from Serial EPROM(U3: AT24C02); when using R17, HPT370 will not load from Serial EPROM.
4. R19 and R20 are alternative. When using R19, HPT370 will try to load configuration from Parallel EPROM(U2: AT29C010A); when using R20 only, HPT370 will use its internal default configuration.
5. R21 and R45 are alternative, and used togather with the Sreial EPROM. When using R21 only, the Serial EPROM is in write-protection mode; when using R45 only, it can be wrote.
6. R57 and R58 must be removed when using HPT370 IC; R49 and R50 must not be used when using HPT368 IC.
7. R47 and R48 must be removed when using HPT370 IC. R47 and R64 must not be used when using HPT368 IC.

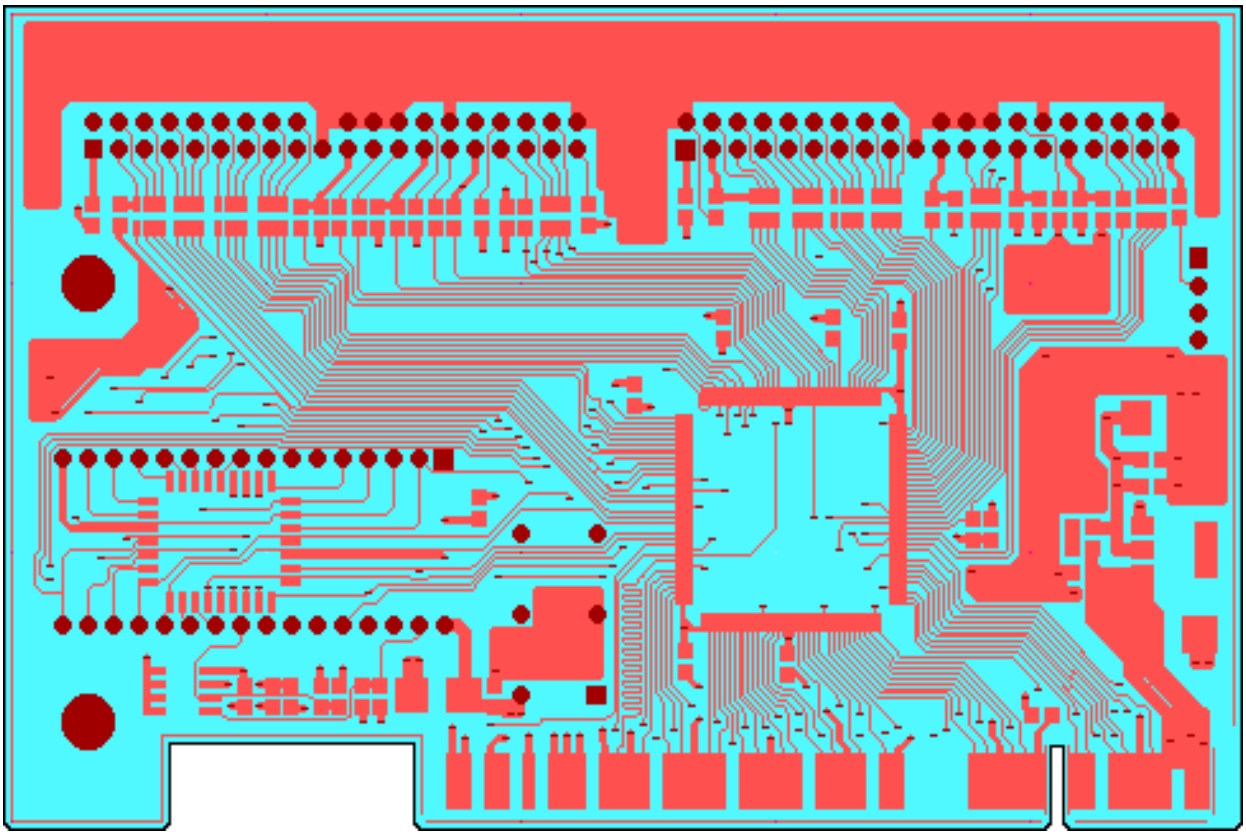
B.2 Schematic Diagram for Mainboard



Notes:

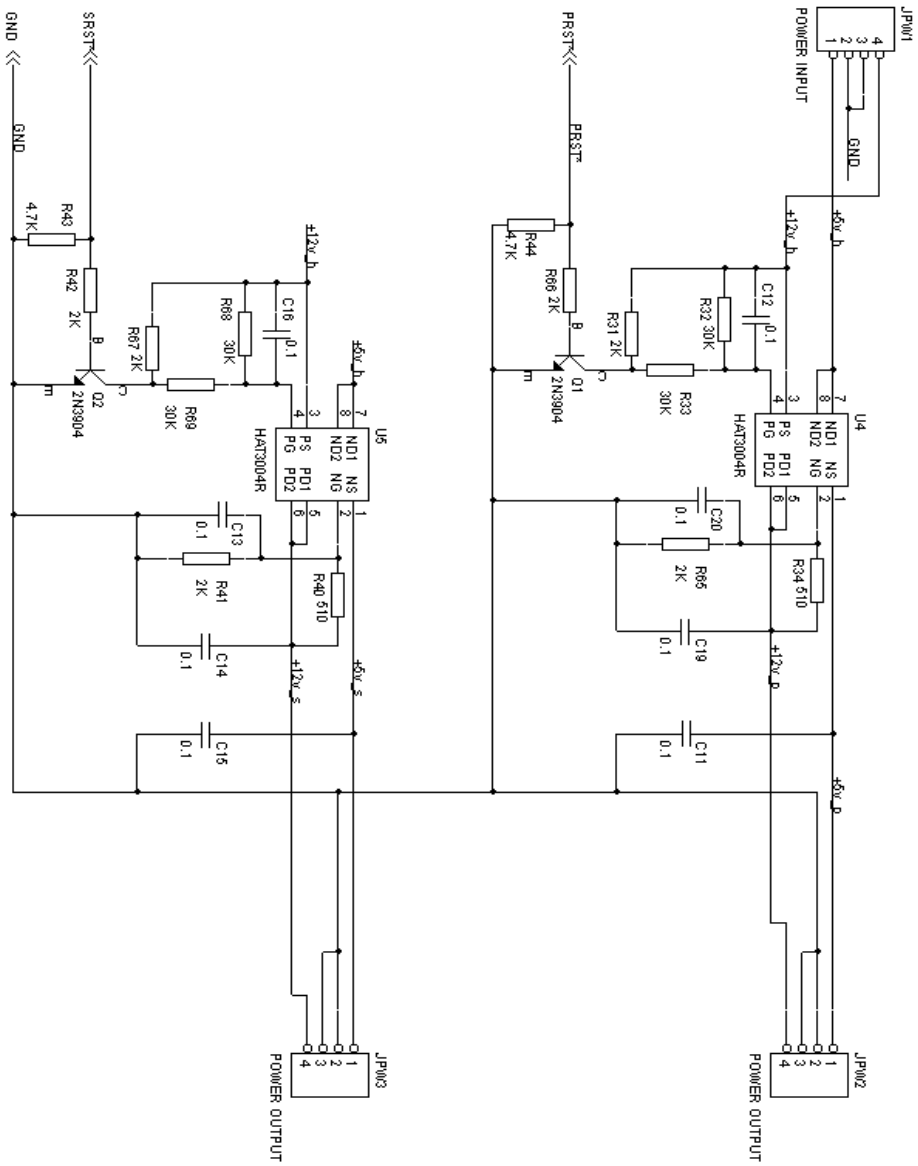
1. HPT370 power supply(VCC) is 3.3v.
2. IDE address allocation mode is selected by using either R22 or R23 (When using R22 only, HPT370 will decode 1f0-1f7, 3f6 on ATA channel 0, 170-177, 376 on ATA channel 1; when using R23 only, HPT370 will decode operating system assigned addresses as specified by PCI IDE controller specification.).
3. R57 and R58 must be removed when using HPT370 IC; R49 and R50 must not be used when using HPT368 IC.
4. R47 and R48 must be removed when using HPT370 IC. R47 and R64 must not be used when using HPT368 IC.

B.3 Layout for Add-On Card



Top Layer

B.4 Schematic Diagram for Hotswap Function



Notes:

1. HPT370 IC and HPT368 IC support hotswap function. The above schematic illustrates the power control circuit, which must be added to the main circuit if hotswap function is wanted.
2. PRST* should be connected to pin80(HPT370 or HPT368 IC);
   SRST* should be connected to pin130(HPT370 or HPT368 IC).

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