

**GENERAL
INSTRUMENT**

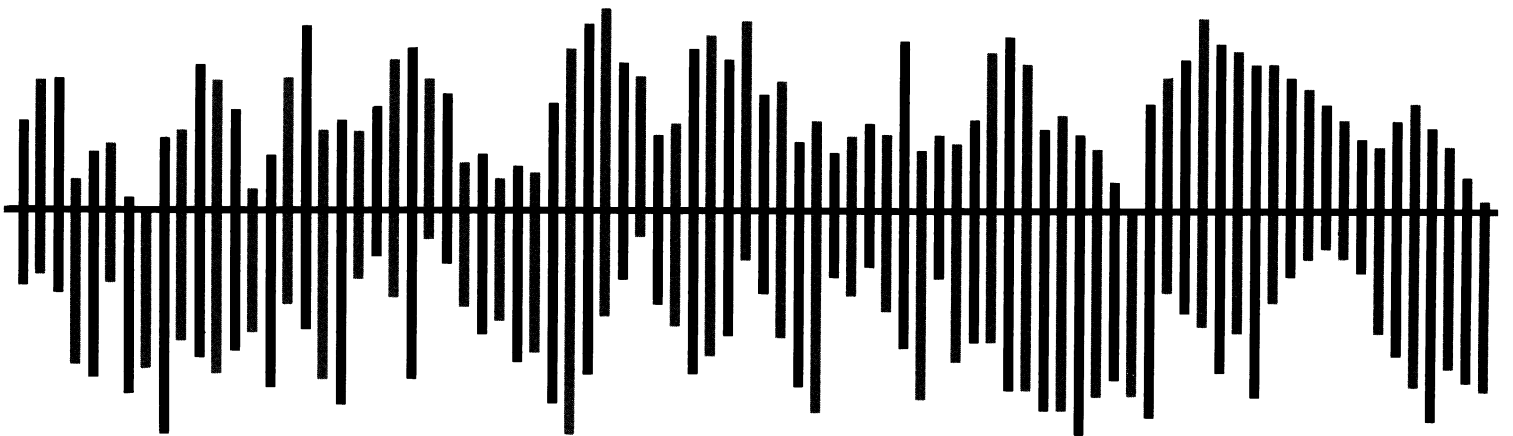
**SP0250
APPLICATIONS
MANUAL**



Microelectronics Division
General Instrument Corporation

GENERAL INSTRUMENT

SP0250 APPLICATIONS MANUAL



**Microelectronics Division
General Instrument Corporation**

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SP0250 Applications Manual

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DESCRIPTION

The SP0250 speech synthesizer is an N-channel MOS LSI device capable of generating high quality speech with the natural inflection and emphasis of the original speaker. Operation requires one or more ROMs to store speech data and a microcomputer/processor such as General Instrument's PIC1650A (Figure 1).

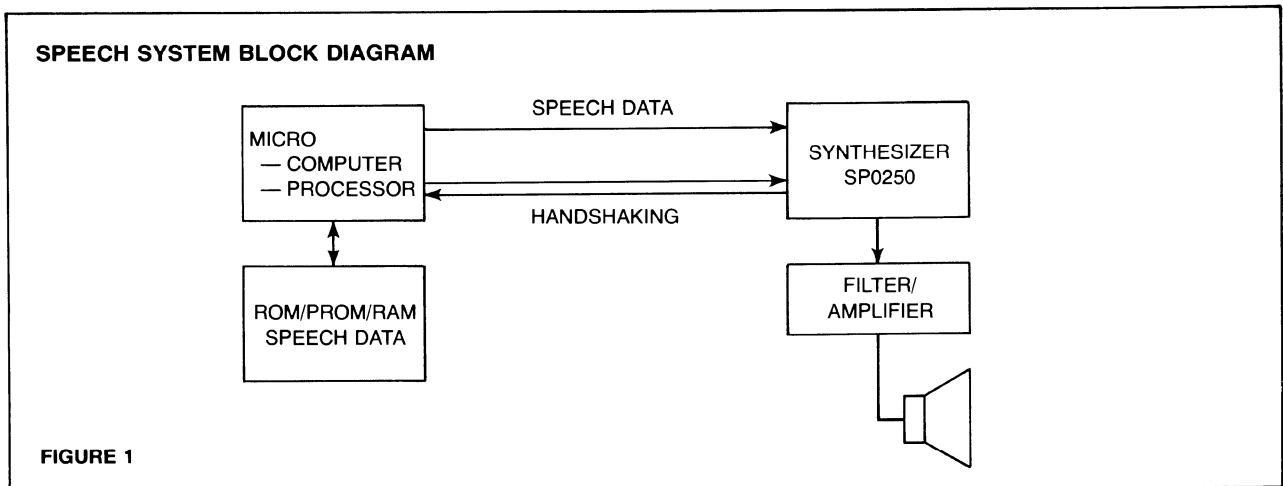
The microcomputer retrieves a data block from the ROM, formats it into a 15 x 8 bit speech data frame and transfers it to the SP0250

8-bit port using two handshaking signals. This speech data frame, which includes such information as pitch period, amplitude, voiced/unvoiced, number of repetitions and filter coefficients "programs" the synthesizer to produce one frame of speech output.

The achievable output has a frequency response of .1-5KHz, a dynamic range of 42dB and a signal to noise ratio of approximately 35 dB.

FEATURES:

- High quality speech synthesizer
- Single +5 volt supply
- Simple interface to a microcomputer or microprocessor based system
- TTL compatible 8 bit bus interface
- Handshaking
- Double Buffered Input



THEORY

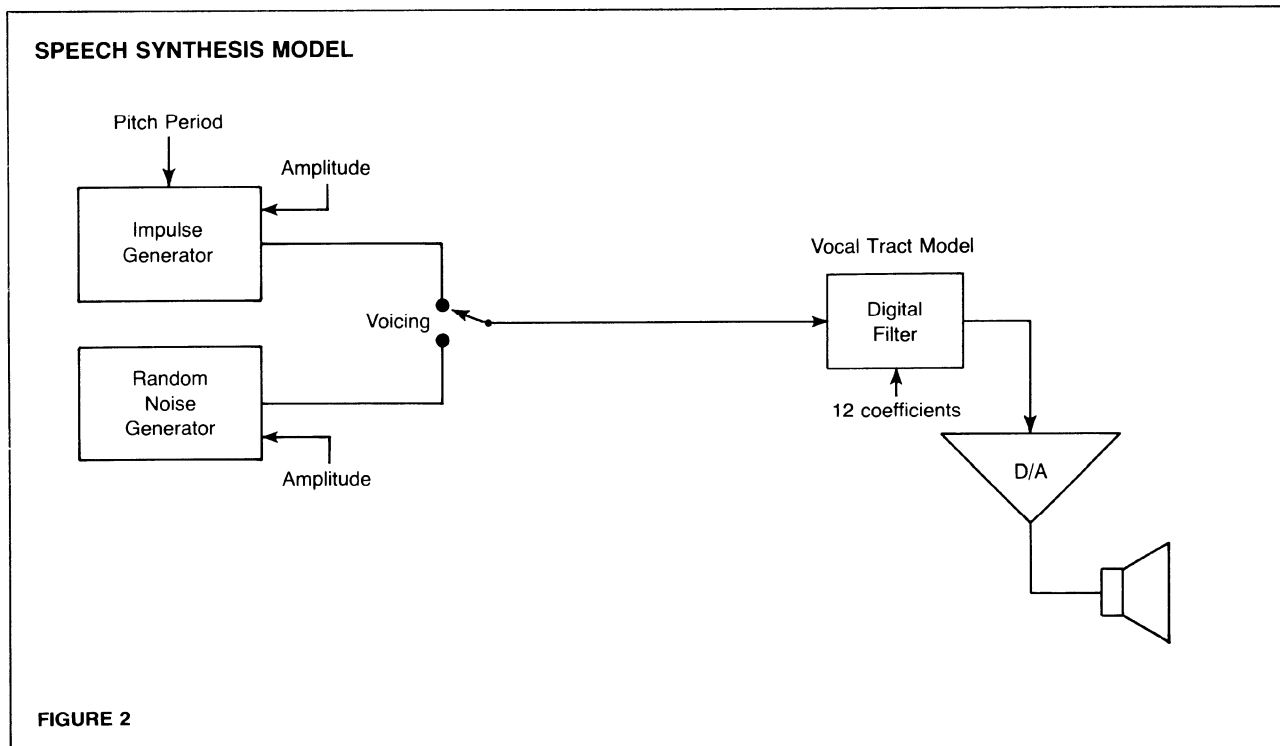
Human speech is characterized as either voiced or unvoiced. When the vocal cords vibrate and the passage of air is not constricted, a "vowel like" sound is produced (voiced). Voiced sounds like *l*, *m* or *ee* have a pitch which is determined by the rate at which the vocal cords vibrate. Unvoiced sounds like *s*, *f* and *sh* have no definite pitch and are produced when air passes through constrictions formed by the teeth, tongue or lips.

The SP0250 is a digital model of this process and is illustrated in Figure 2.

The voiced/unvoiced parameter selects either the impulse generator

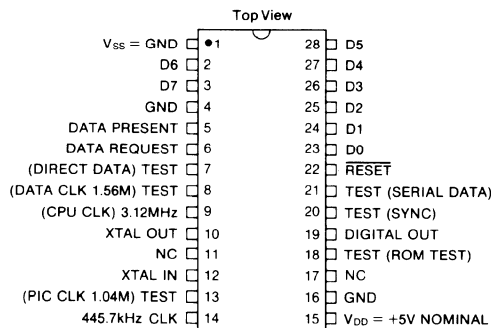
or the random noise generator as the excitation source. The source signal is multiplied by the gain to achieve the correct amplitude and input to the digital filter. The output of the digital filter — which is "programmed" by 12 coefficients to model the human vocal tract — is fed to a pulse width modulator which produces the audio signal.

The coefficients are generated by a speech analysis program incorporating a technique known as Linear Predictive Coding (LPC). LPC is a mathematical technique for generating points of a waveform from a weighted linear combination of previous samples. This form of mathematical comparison, relating the current output to a series of previous outputs, models the characteristic properties of the human speech mechanism.



PIN CONFIGURATION

28 LEAD DUAL IN LINE



PIN FUNCTIONS

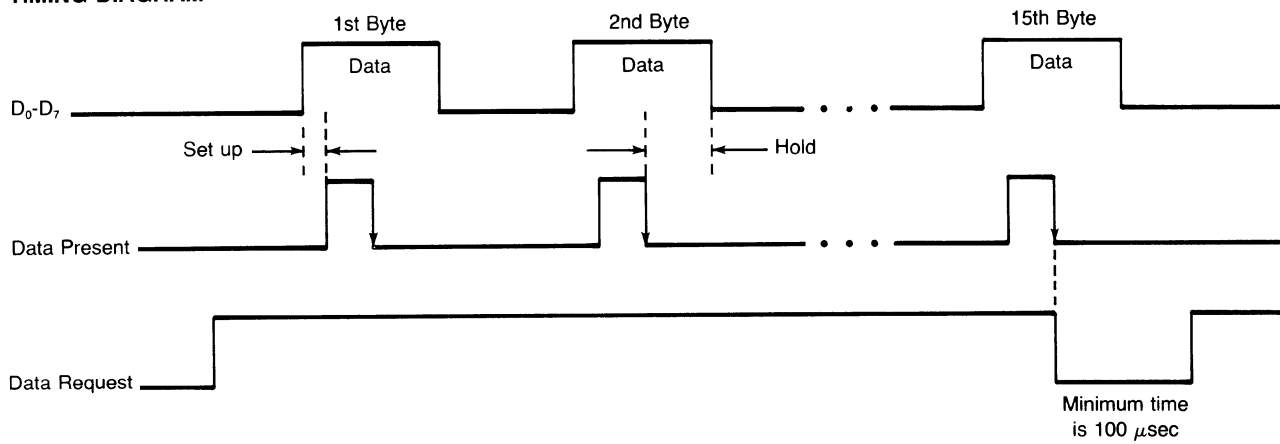
PIN NUMBER	NAME	FUNCTION
15	V_{DD}	Positive power supply
1	V_{SS}	Ground
Clock		
12	XTAL IN	3.12 MHz crystal and associated circuitry.
10	XTAL OUT	
Inputs		
22	Reset	Two high to low transitions; required to reset the chip.
23-28, 2, 3	D ₀ -D ₇ Data Bus	8 bit data bus; used by the microcomputer to transfer speech data to the SP0250.
5	Data Present	The negative edge of the Data Present pulse clocks 8 bits of speech data into the SP0250. Must be low while SP0250 is reset.
4, 16, 7, 18		Must be grounded for proper chip operation.
Outputs		
6	Data Request	The SP0250 drives the Data Request pin high when it is ready to input speech data.
19	Digital Out	Chip output. This output is open collector and requires a pull-up.
9	3.120MHz CPU Clock	Buffered push-pull output.
14	4.5KHz Clock	Buffered push-pull output with a 3:4 high to low ratio.

SP0250

TEST PINS

PIN NUMBER	NAME	FUNCTION
Test Inputs 7	Direct Data Mode	A logic 1 on this input causes the data bus to be loaded directly into the source register in the chip on negative edge of Data Present pulse.
18	ROM Test	A logic 1 on this input causes the contents of the coefficient ROM to appear on the SERIAL DATA pin, Clock rate 1.56 MHz.
Test Outputs 20	SYNC	Buffered push-pull test output; 640ns positive pulse with a duty cycle of 312 clocks.
21	Serial Data	Buffered push-pull test output; monitors a point in the internal data bus.
8	1.56MHz Data Clock	Buffered push-pull square wave output.
13	1.04MHz PIC Clock	Buffered push-pull output with 1:2 high to low ratio.

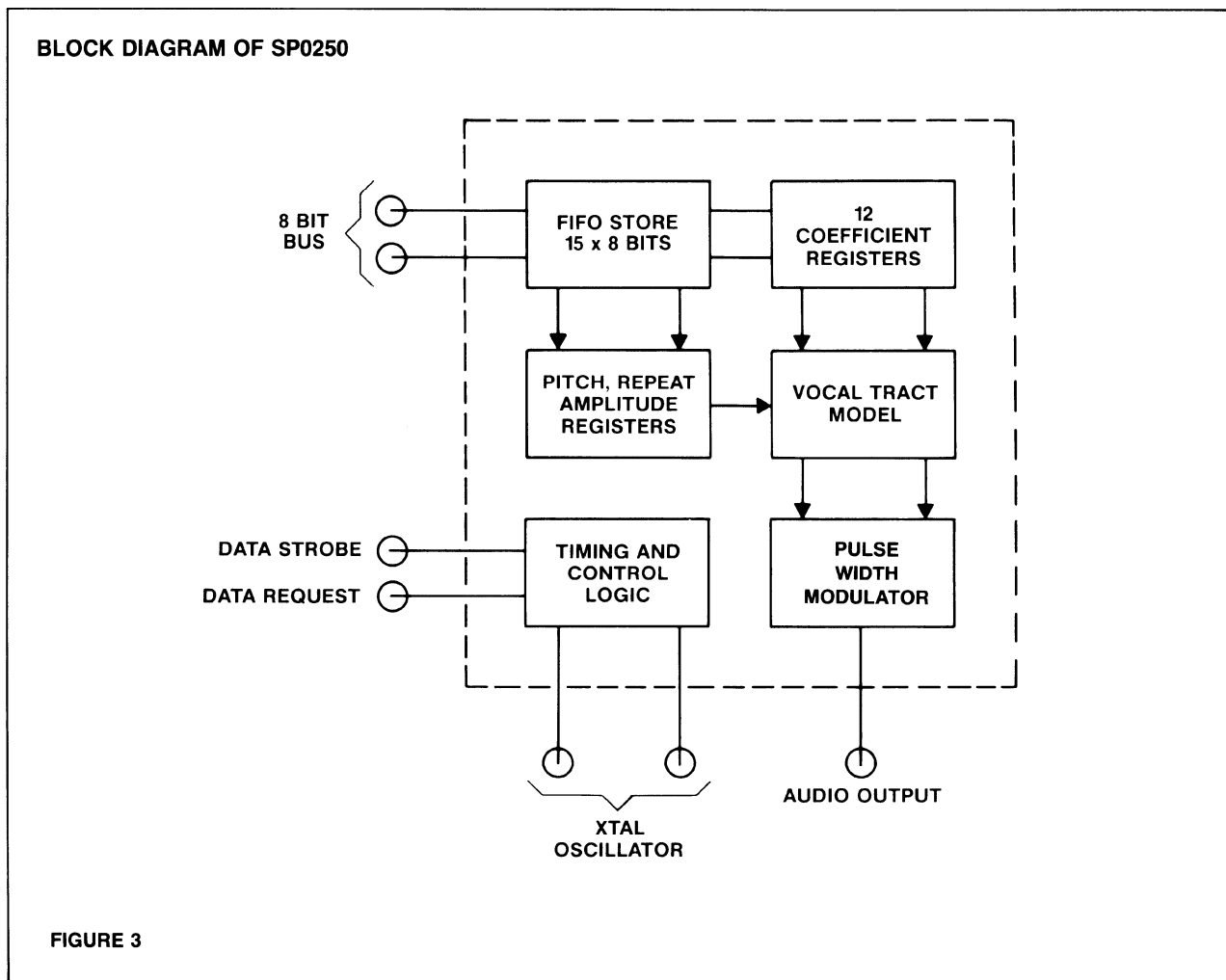
TIMING DIAGRAM



Data Request and Data Present are the handshaking signals used by the SP0250 and the microcomputer to transfer speech data. The SP0250 drives the Data Request line high when it is ready to accept a 15 x 8 bit speech frame (Data Request stays high until the entire frame has been input). When the microcomputer sees a logic 1 on

Data Request, it will begin to send speech data. The microcomputer outputs 8 bits to the SP0250 followed by a Data Present pulse. This procedure is repeated until the entire 15 byte frame has been transferred.

ARCHITECTURE



The SP0250 is controlled by 15 programmable eight bit parameter registers which hold the following information: voiced/unvoiced, pitch period, repeat count, amplitude and 12 digital filter coefficients (Figure 3).

Bit six of the repeat register is used to select either voiced or unvoiced source operation. If voiced mode is selected, the pitch

period register determines the spacing between the scaled unit impulses applied to the digital filter. The repeat register indicates the number of full pitch periods which will be synthesized before the 15 parameter registers are updated. The amplitude register in both voiced and unvoiced mode controls the gain of the source.

SP0250

FIFO

The parameter registers are loaded through an 8 bit port into a 15 x 8 bit (one frame speech data, Figure 4) FIFO store. The FIFO gives the

microcomputer the ability to load the next set of parameters while the present set is controlling the synthesizer.

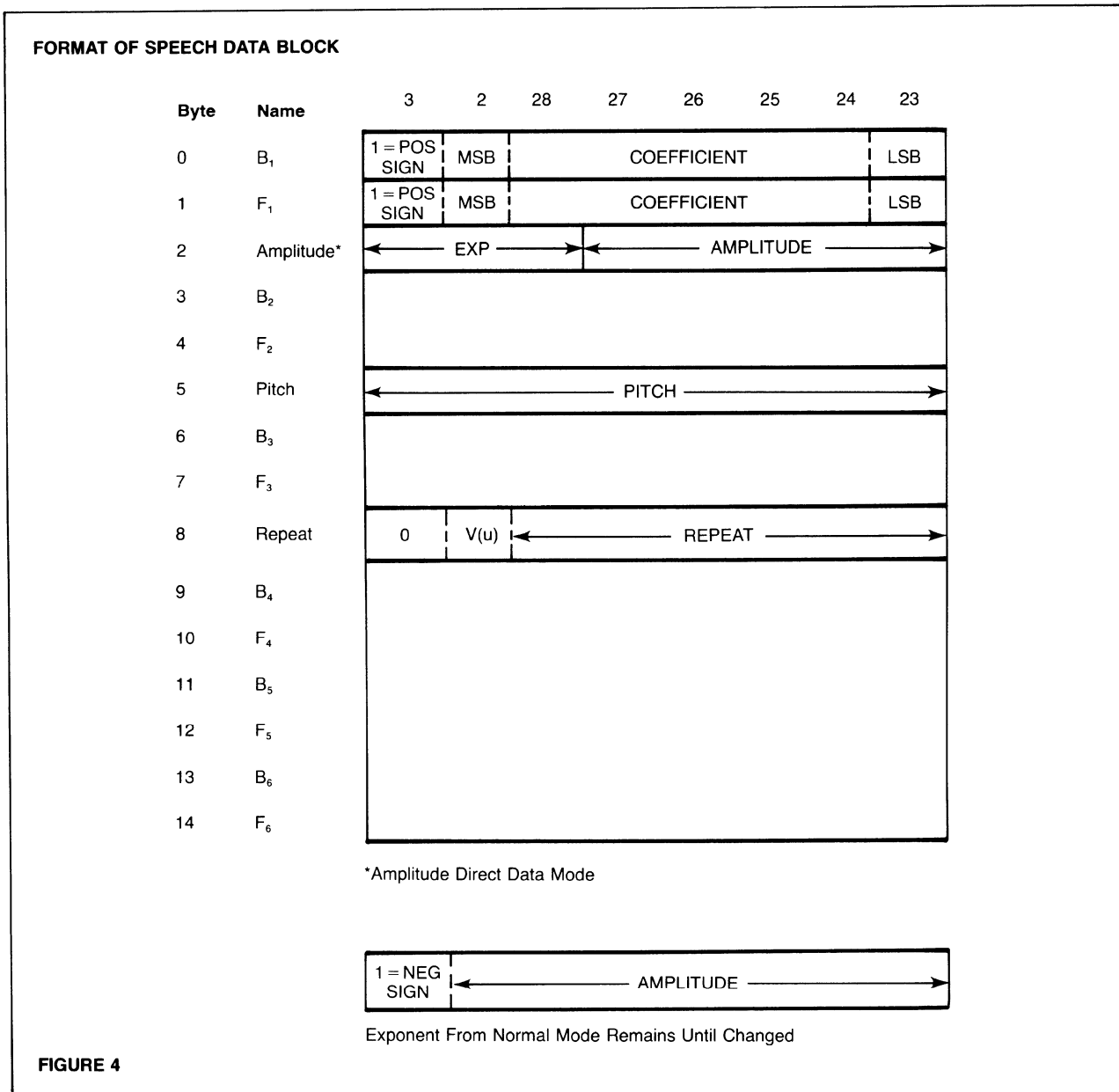


FIGURE 4

DIGITAL FILTER

The filter section is implemented using totally digital techniques. This approach allows one 2nd order section to serve as six sections through the use of multiplexing. The section that is implemented is the 2nd order infinite impulse response (IIR) digital filter shown in Figure 5. This filter stage has the transfer function:

$$H(Z) = \frac{1}{1 - 2F_t Z^{-1} - B_t Z^{-2}}$$

Therefore, it can be shown that the poles of the transfer function occur at:

$$\frac{-2F_t \pm \sqrt{4F_t^2 + 4B_t}}{-2}$$

and when,

$$-1 < B_t \leq 0$$

and,

$$|F_t| \leq \sqrt{-B_t}$$

the poles will be placed in a complex pair, forming a resonator with the bandwidth given by:

$$(1) \quad B.W. = \frac{-F_s \text{LN}(B_t^2)}{\pi}$$

where F_s is the sampling frequency in HZ and the center frequency (F_k) given by:

$$(2) \quad F_k = \frac{F_s \text{COS}^{-1} \frac{2F_t}{\sqrt{-B_t}}}{2\pi}$$

As can be seen from equations (1) and (2), modification of the B coefficient changes both the frequency and bandwidth of the resonator.

Modification of the F coefficient changes only the center frequency, and has no effect on the corresponding bandwidth.

Since speech signals (in particular vowel sounds) convey information through the shifting of resonant peaks in the spectrum, it is desirable to be able to change center frequencies of the 2nd order stages independent of their respective bandwidth settings. In addition it is important that the parameters of the individual stages (corresponding to particular resonances) can be independently modified. The use of cascade 2nd order stages supports these features, giving this configuration a distinct advantage over other filter sections currently in use for speech synthesis, such as the Lattice section, and direct form implementation.

If it is desired to place resonances at a frequency of zero, these real axis poles can be accommodated directly. Each 2nd order stage may be used to place two real axis poles of variable bandwidth. If X_1 is the real axis location of the first pole, and X_2 the second:

$$F_t = \frac{X_1 + X_2}{2}$$

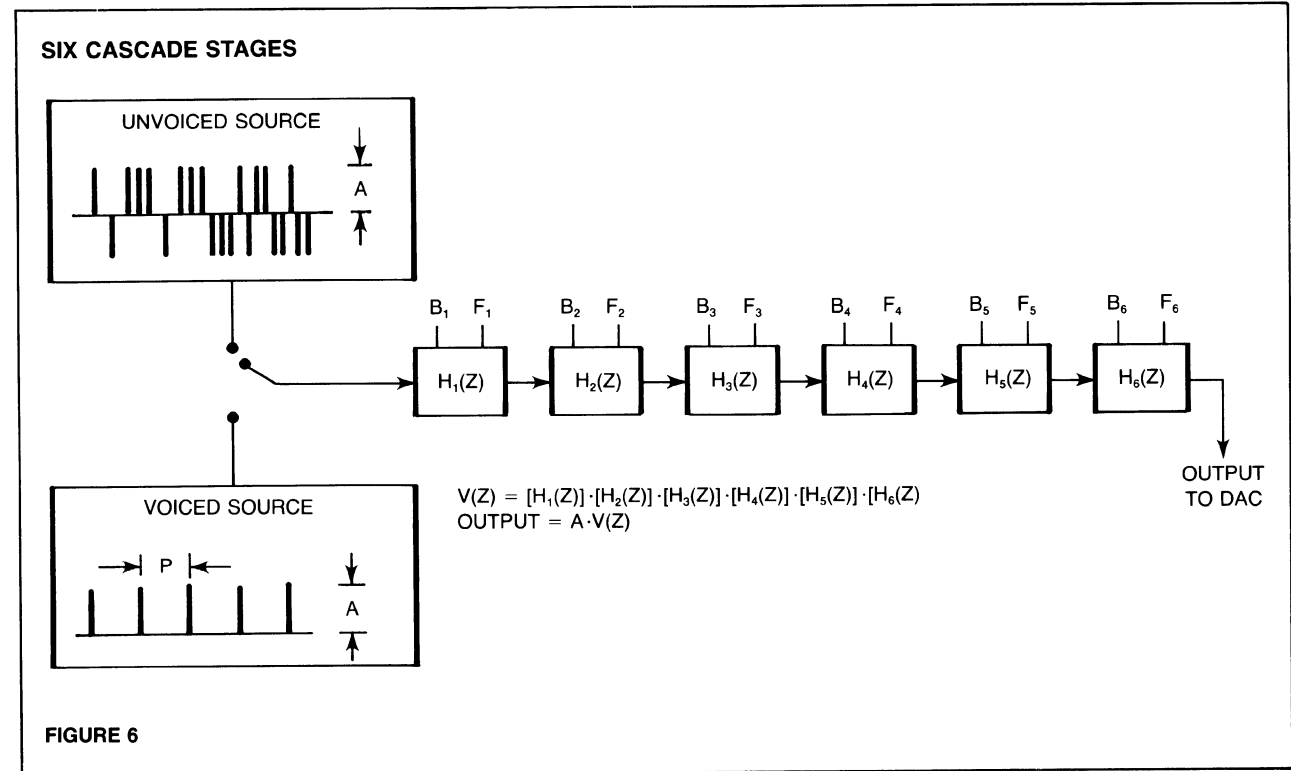
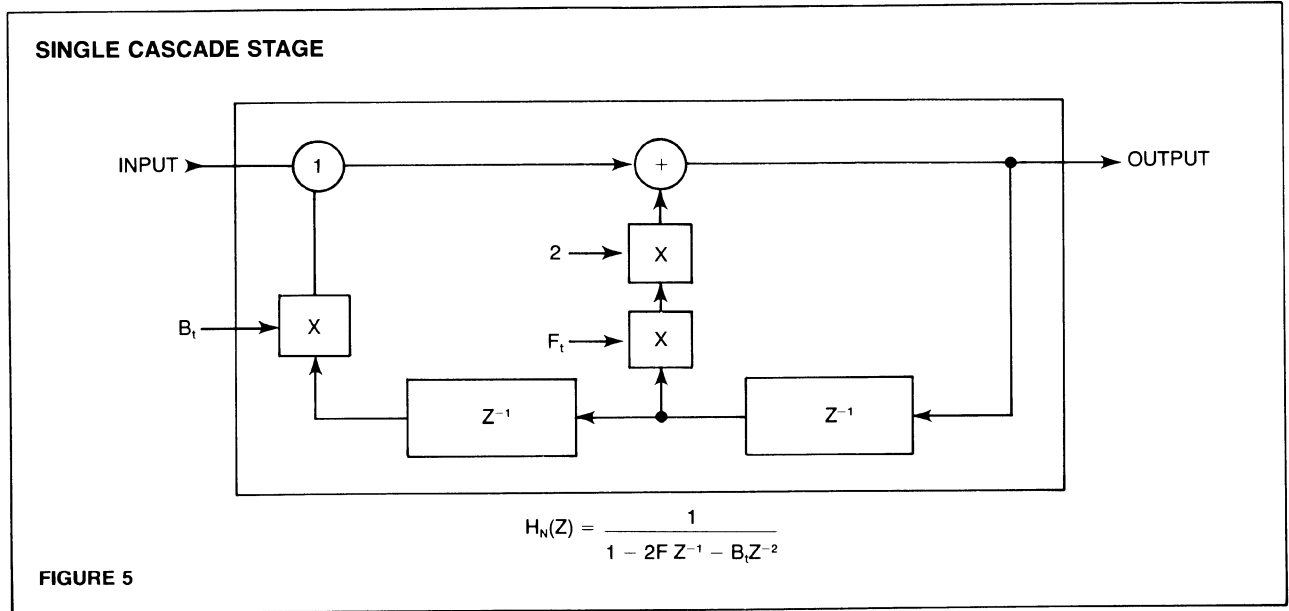
$$\text{and:} \quad B_t = (F - X_1)^2 - F^2$$

with the band widths of each given by:

$$BW_1 = -2F_s \text{LN} X_1$$

$$BW_2 = -2F_s \text{LN} X_2$$

where F_t and B_t represent the coefficients in Figure 6.



FILTER COEFFICIENTS

The coefficients F_t and B_t are non-linearly quantized by a table lookup ROM (internal to SP0250). The low order 7 bits of each filter coefficient addresses a 128 x 9 bit ROM which produces an unsigned 9 bit coefficient with a value between zero and one. The MSB of the original coefficient is the sign bit where 1 is positive and 0 is negative. The ROM contents are listed below:

7 bit coefficient	ROM contents	actual value
0	0	0.000000
1	9	.017578
2	17	.033203
3	25	.048828
4	33	.064453
5	41	.080078
6	49	.095703
7	57	.111328
8	65	.126953
9	73	.142578
10	81	.158203
11	89	.173828
12	97	.189453
13	105	.205078
14	113	.220703
15	121	.236328
16	129	.251953
17	137	.267578
18	145	.283203
19	153	.298828
20	161	.314453
21	169	.330078
22	177	.345703
23	185	.361328
24	193	.376953
25	201	.392578
26	209	.408203
27	217	.423828
28	225	.439453
29	233	.455078
30	241	.470703
31	249	.486328
32	257	.501953
33	265	.517578
34	273	.533203
35	281	.548828
36	289	.564453
37	297	.580078
38	301	.587891
39	305	.595703
40	309	.603516
41	313	.611328
42	317	.619141
43	321	.626953
44	325	.634766
45	329	.642578
46	333	.650391
47	337	.658203
48	341	.666016
49	345	.673828
50	349	.681641
51	353	.689453
52	357	.697266
53	361	.705078
54	365	.712891
55	369	.720703
56	373	.728516
57	377	.736328
58	381	.744141

7 bit coefficient	ROM contents	actual value
59	385	.751953
60	389	.759766
61	393	.767578
62	397	.775391
63	401	.783203
64	405	.791016
65	409	.798828
66	413	.806641
67	417	.814453
68	421	.822266
69	425	.830078
70	427	.833984
71	429	.837891
72	431	.841797
73	433	.845703
74	435	.849609
75	437	.853516
76	439	.857422
77	441	.861328
78	443	.865234
79	445	.869141
80	447	.873047
81	449	.876953
82	451	.880859
83	453	.884766
84	455	.888672
85	457	.892578
86	459	.896484
87	461	.900391
88	463	.904297
89	465	.908203
90	467	.912109
91	469	.916016
92	471	.919922
93	473	.923828
94	475	.927734
95	477	.931641
96	479	.935547
97	481	.939453
98	482	.941406
99	483	.943359
100	484	.945313
101	485	.947266
102	486	.949219
103	487	.951172
104	488	.953125
105	489	.955078
106	490	.957031
107	491	.958984
108	492	.960938
109	493	.962891
110	494	.964844
111	495	.966797
112	496	.968750
113	497	.970703
114	498	.972656
115	499	.974609
116	500	.976563
117	501	.978516
118	502	.980469
119	503	.982422
120	504	.984375
121	505	.986328
122	506	.988281
123	507	.990234
124	508	.992188
125	509	.994141
126	510	.996094
127	511	.998047

DAC OUTPUT

The output of the digital filter drives an internal 7 bit pulse width modulation (PWM) digital to analog converter. The design of the PWM DAC is such that all noise components are at or above 10KHz. The output is low pass filtered to 5KHz, and externally amplified.

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} -0.3V to +12V
 Storage Temperature -25° to +125°C
 Lead Temp (Soldering) 10Sec @ +330°C

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise stated)

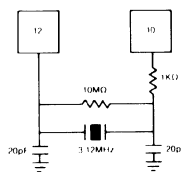
V_{CC} = +4.6V to +6.5V
 Operating Temperature = 0°C to +55°C

DC CHARACTERISTICS

Characteristic	Min	Typ	Max	Units	Conditions
10 Inputs:					
Reset D0-D7, Data Present					
Logic 0	0.0	—	0.6	V	
Logic 1	2.4	—	V _{CC}	V	
Leakage	—	—	10	μA	5.5V
1 Clock Input:					
Logic 0	0.0	—	0.6	V	
Logic 1	4.0	—	V _{CC}	V	
Leakage	—	—	10	μA	5.5V
2 Test Inputs					
Direct Data Mode, ROM Test					
Logic 0	0.0	—	0.6	V	
Logic 1	2.4	—	V _{CC}	V	
Capacitance	—	—	10	pF	
Leakage	—	—	10	μA	5.5V
3 P/P Outputs					
Data Request, CPU Clock, 445.7kHz Clock					
Logic 0	0.0	—	0.6	V	.72mA
Logic 1	3.50	—	V _{CC}	V	-50μA
1 O/C Output					
Digital Out					
Logic 0	0.0	—	0.6	V	2.2K
Logic 1	—	—	10	μA	5.0V Source
Power on V _{DD} = I _{CC}	—	50	75	mA@ 25°C	V _{DD} =5.5 V _{SS} =0.0 No Loads

AC CHARACTERISTICS

Characteristic	Min	Typ	Max	Units	Conditions
Clock Frequency	—	3.12	—	MHz	Square Wave
Clock Period	—	320	—	ns	
Data Present					
Logic 1	1.5	—	—	μs	
Logic 0	10.0	—	—	μs	
Reset D0-D7	1000	—	—	μs	
Set Up	1.5	—	—	μs	
Hold	1.5	—	—	μs	
P/P Test Output					
Serial Data					
Logic 0	0.0	—	0.6	V	No Load
Logic 1	3.50	—	V _{CC}	V	



SPEECH CODE GENERATION

The analog speech signal from a tape recording is applied to a .1-5KHz bandpass filter and sampled at a 10KHz rate. Each sample is converted to a 12 bit digital value. A pitch period estimation and voicing decision is made to obtain the pitch, amplitude, and repeat coefficients. An LPC analysis is then performed on the digital data which produces the digital filter coefficients to best match the spectral characteristics of the samples in a particular speech frame. During this analysis, the number of filter stages and the coefficient precision (low, high, full) information is entered. The coefficients generated by the analysis are then translated into a form which is compatible with the SP0250. If desired, the data may be further compressed by delta coding the coefficients.

APPLICATION:

The SP0250 is easily interfaced to most microcomputers or microprocessor systems. The microcomputer must decide what word or phrase to speak, retrieve speech data, expand data if it was compressed, and transfer the data to the speech chip.

DESCRIPTION:

The VSM2032 speech module includes the SP0250 speech synthesizer, a PIC1650A microcomputer and standard 32K ROM. The module interface consists of seven input lines (S0-S6), a STROBE line, a RESET line and a BUSY line.

OPERATION:

The word or phrase to be spoken is selected by placing its address on lines S0 through S6. The address is clocked into the module by a pulse on the STROBE line. At this time, the module will drive the BUSY line low and start speaking the selected word. When the module has finished speaking it will drive the BUSY line high and wait for new input on S0-S6.

VSM2032 SPEECH MODULE

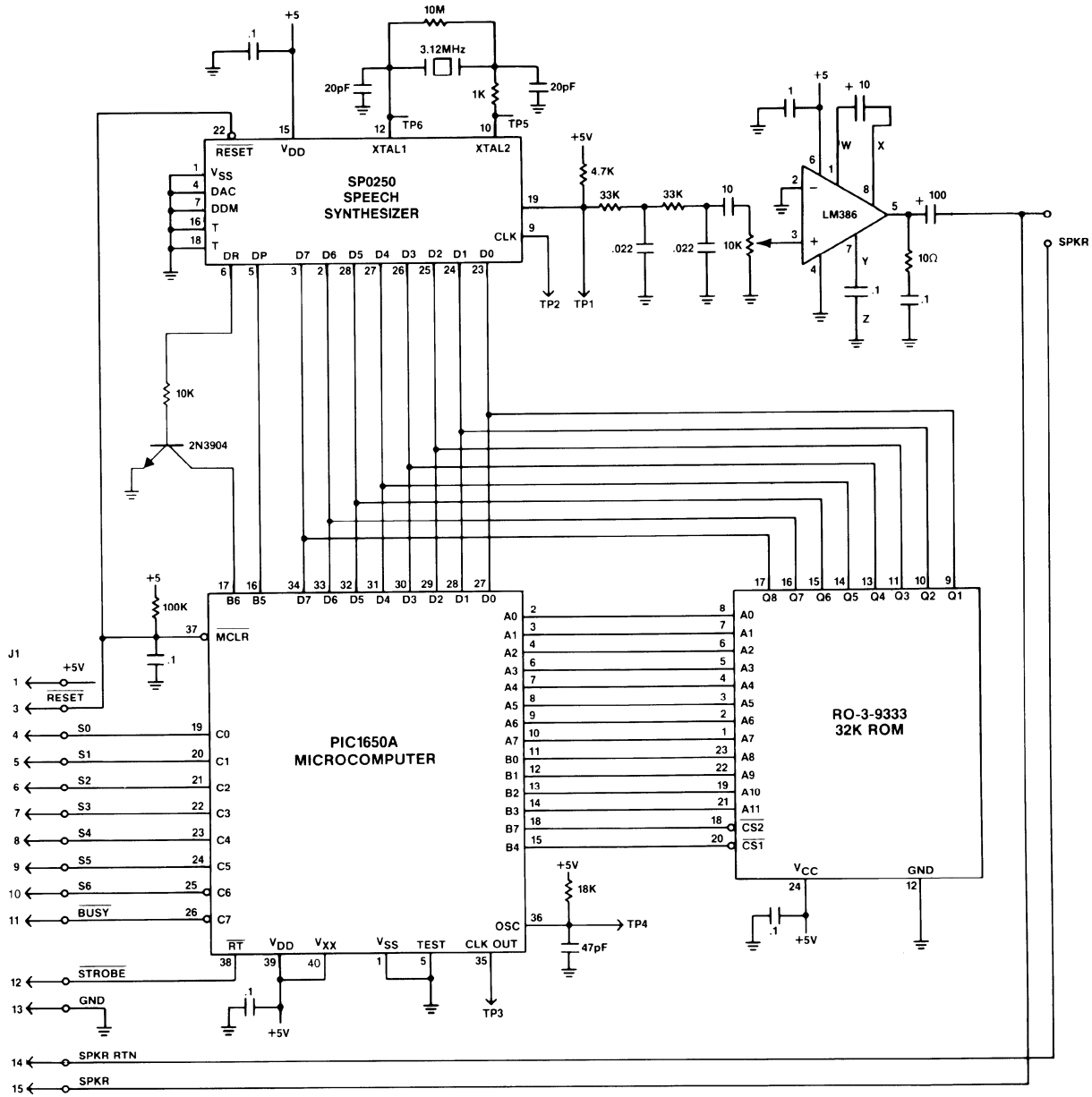


FIGURE 7

PIC MICROCOMPUTER FUNCTIONS

The functions of the PIC microcomputer in the VSM2032 module include the following:

- Input word address
- Retrieve compressed speech data from ROM
- Expand speech data to 15 x 8 bit frame
- Output speech frame to SP0250

Of these four tasks, expanding the speech data is the only one which needs further explanation. The speech data frames are usually stored in a compressed format to yield more speech per ROM. There are three techniques used to compress the data:

REDUCE STAGES:

Often it is unnecessary to implement all six filter stages for adequate speech modeling. In general, voiced speech requires four to six stages while unvoiced speech can be modeled with two to four stages. The unused stages have coefficients of zero.

REDUCE PRECISION:

Storing full 8 bits of precision for all 15 coefficients is unnecessary. It is possible to assign a different bit precision to each of the coefficients.

DELTA CODING:

This technique exploits the relatively smooth and continuous characteristic of the coefficients. The smaller differential between parameters in adjacent frames is stored rather than the absolute magnitude.

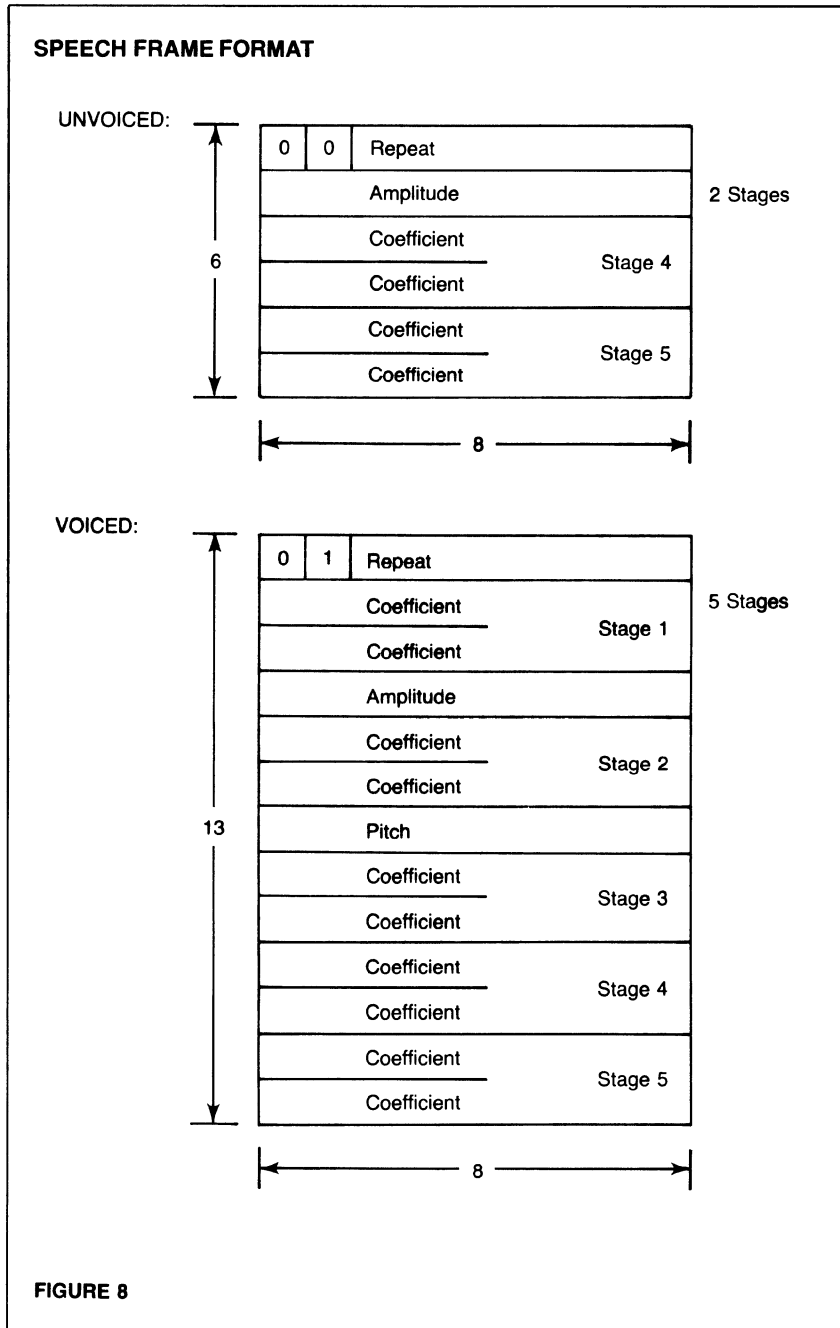
NOTE: Reducing the number of filter stages and reducing the coefficient precision may affect the speech quality. Delta coding does not.

The speech data may be encoded using any, all or none of these techniques. However, there is a tradeoff between data compression and software complexity of the controlling microcomputer (e.g. PIC1650A) — highly compressed speech data will yield more speech per ROM, but will necessitate complex decoding routines in the controlling microcomputer.

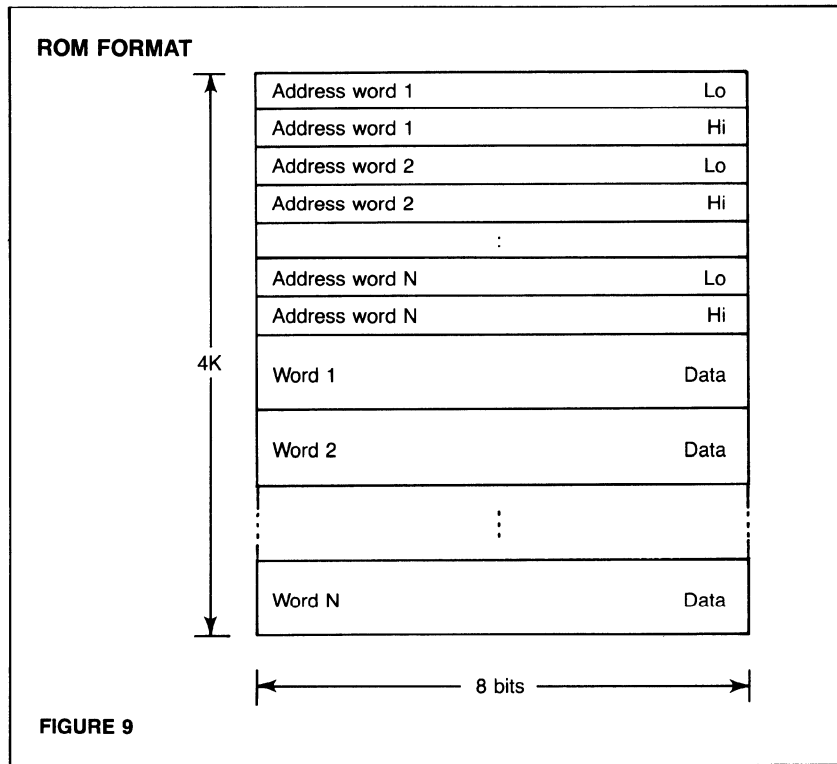
The standard PIC1650A in the VSM2032 module was programmed to handle highly compressed speech data and, therefore, may be overly complex for inclusion in an already burdened microcomputer. The following pages illustrate the use of a simple algorithm to drive the SP0250.

EXAMPLE

The driver routine shown in Figure 10 will retrieve data of the format shown in Figure 8.



The speech data was compressed by technique #1. Five stages are implemented for voiced speech, and two stages for unvoiced speech. The driver routine is easy to implement, yet the ROM stores 30% more speech data than the non-compressed 15 x 8 bit format.



The ROM is divided into two sections — the jump table and the speech data. Each jump table entry points to the starting address of a particular segment of speech data. If there are ten words stored in ROM, then there will be ten two byte entries in the jump table. The speech data for each word will consist of compressed speech frames.

The 32K ROM with data compressed by technique #1 can store approximately 7-10 seconds of speech. If additional compression techniques were performed on the data, the ROM could store up to 30 seconds of speech.

SP0250

SPEECH DATA

Listed below are the speech data for the word "EAT". The first line is the jump table entry which indicates that the speech data starts at octal address 24. The last line marks the end of the speech data block. The remaining lines are the speech data frames — 13 bytes for voiced frames, 6 bytes for unvoiced frames.

```
TEMP    T=00004 IS ON CR A1    USING 00024 BLKS R=0000

0001    S000000,024,000,L,
0002    S000024,
0003    003,065,066,042,034,013,
0004    103,106,040,331,104,064,112,114,020,136,222,141,350,
0005    101,130,040,360,116,054,116,126,020,152,220,127,340,
0006    102,114,040,336,072,044,121,116,020,164,220,144,351,
0007    102,076,034,327,072,060,123,046,010,126,220,153,355,
0008    102,020,024,334,106,044,125,066,014,156,216,134,343,
0009    102,102,034,361,064,044,126,066,014,150,216,131,341,
0010    101,130,040,332,032,040,130,100,020,152,216,137,346,
0011    102,112,040,323,036,040,133,066,020,152,216,147,354,
0012    102,116,040,324,044,050,135,050,014,140,214,140,350,
0013    101,132,040,270,072,074,140,056,014,140,214,161,362,
0014    102,144,044,260,060,070,142,100,010,132,216,142,354,
0015    101,140,044,226,106,100,144,104,010,154,216,163,363,
0016    003,064,062,204,210,201,
0017    003,027,014,020,027,210,
0018    003,011,042,020,230,214,
0019    003,007,026,016,214,003,
0020    003,000,032,014,220,202,
0021    003,000,020,012,205,010,
0022    003,000,036,010,221,014,
0023    003,000,026,040,033,213,
0024    003,072,056,050,050,220,
0025    003,075,120,102,025,005,
0026    003,123,076,102,031,016,
0027    003,163,060,064,033,013,
0028    003,164,076,076,032,202,
0029    003,161,126,102,103,204,
0030    003,135,104,074,041,212,
0031    003,074,100,070,070,224,
0032    003,061,076,056,112,231,
0033    003,026,052,054,115,234,
0034    003,016,040,046,063,232,
0035    003,000,000,000,000,000,
0036    000,L
```

FLOWCHART

NOTE: The drive routine was implemented in a PIC1650A micro-computer.

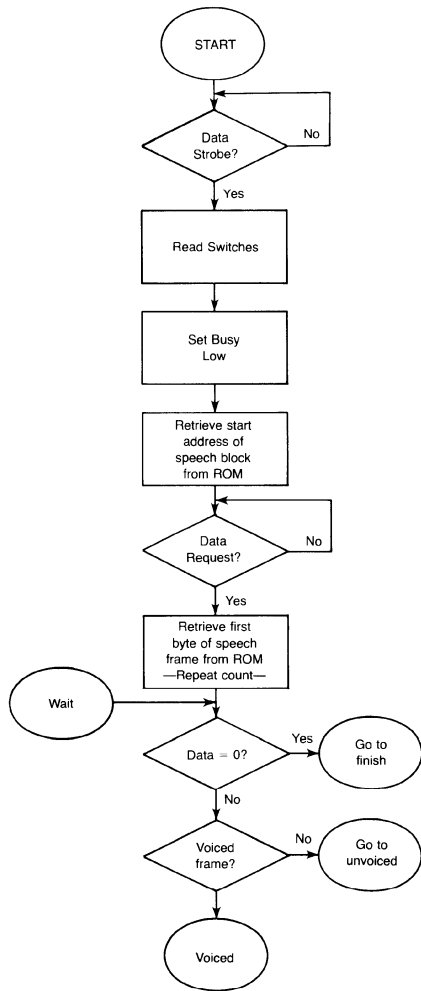


FIGURE 10A

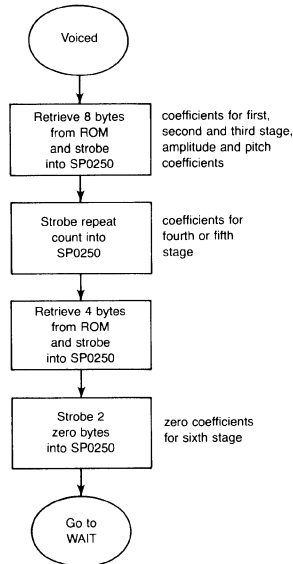


FIGURE 10B

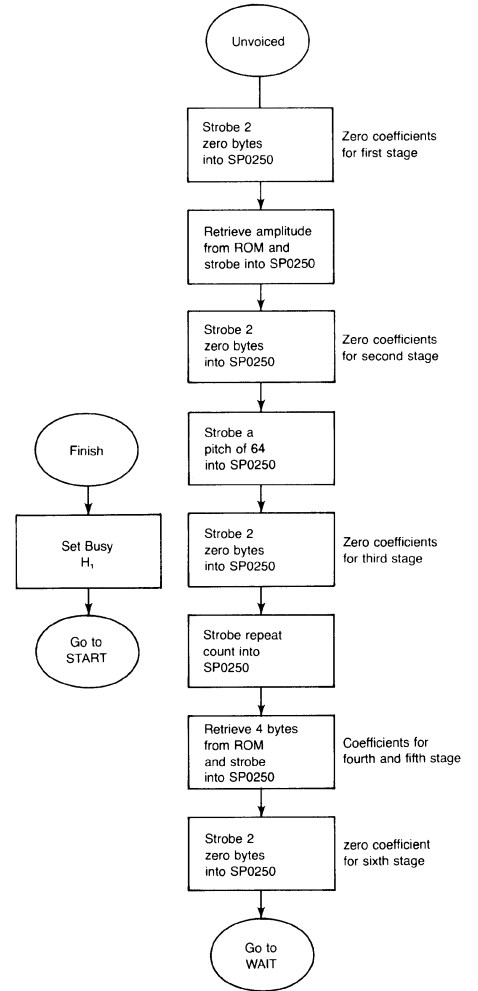


FIGURE 10C

SP0250

LISTING

```

LINE      ADDR      B1      B2
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
;*****
;*
;*          SP 0250 CONTROLLER          *
;*
;*****
LIST      P=1650
ORG       0
;
;
; REGISTER EQUATES
;
RTCC      EQU      1          ;RTCC REGISTER
PC        EQU      2          ;PROGRAM COUNTER
SWR       EQU      3          ;STATUS WORD REGISTER
FSR       EQU      4          ;FILE SELECT REGISTER
IOA       EQU      5          ;ADDRESS LINES TO ROM
IOB       EQU      6          ;ADDRESS/CHIP ENABLE/HANDSHAKING
SWITCH    EQU      7          ;SWITCH INPUT/BUSY LINE
DATA      EQU      10         ;ROM/SP 0250 INTERFACE
LOADD     EQU      11         ;ROM ADDRESS-LO
HIADD     EQU      12         ;ROM ADDRESS-HI
REPEAT    EQU      13         ;REPEAT BYTE -VOICE/UNVOICED
CCOUNT    EQU      14         ;COEFFICIENT COUNT
TEMP      EQU      15         ;TEMP STORE
;
;
; BIT EQUATES
;
C         EQU      0          ;CARRY BIT-SWR
Z         EQU      2          ;ZERO BIT -SWR
DATAP     EQU      5          ;DATA PRESENT -IOB
DATAQ     EQU      6          ;DATA REQUEST -IOB
VOICE     EQU      6          ;VOICED/UNVOICED -REPEAT
;
;
; SUBROUTINES
;
ZEROCO    CLRF     DATA      ;ZERO COEFFICIENT
STROBE    BSF     IOB,DATAP
          BCF     IOB,DATAP   ;STROBE SPO250 -NEG. EDGE
          RETLW  0
;
;INCADD   -INCREMENT ROM ADDRESS
;
INCADD    INCF     LOADD      ;NEXT SEQUENTIAL LOCATION
          BTFSC  SWR,Z
          INCF     HIADD      ;LOW ORDER ROLL-OVER
          RETLW  0
;
;DISABL   -DISABLE ROM
;

```

LINE	ADDR	B1	B2		PAGE	2	
55	000010	06320		DISABL	MOVLW	320	
56	000011	00046			MOVWF	IOB	;DISABLE ROM
57	000012	04000			RETLW	0	
58				:			
59				:			
60				;RESTOR	-RESTORE	DATA BUS	
61				:			
62	000013	06377		RESTOR	MOVLW	377	
63	000014	00050			MOVWF	DATA	;RESTORE FOR SP 0250/ROM COMM.
64	000015	04000			RETLW	0	
65				;READ	-READ	ROM/ADRESSED BY LO/HIADD	
66				:			
67	000016	01011		READ	MOVFW	LOADD	
68	000017	00045			MOVWF	IOA	;PUT OUT LO
69	000020	01012			MOVFW	HIADD	
70	000021	07017			ANDLW	17	;ONLY 4 BITS VALID
71	000022	06720			IORLW	320	;KEEP ROM DISABLED
72	000023	00046			MOVWF	IOB	;PUT OUT HI
73	000024	07157			ANDLW	157	
74	000025	00046			MOVWF	IOB	;ENABLE ROM
75	000026	04000			RETLW	0	;DATA PRESENT ON IOD
76				:			
77				;MAIN PROGRAM			
78				:			
79	000027	00141		START	CLRF	RTCC	;INITIALIZE FOR STROBE INPUT
80	000030	01001		WAIT	MOVFW	RTCC	
81	000031	03103			BTFSC	SWR,Z	
82	000032	05030			GOTO	WAIT	;NO STROBE]]
83	000033	01007			MOVFW	SWITCH	;DATA STROBE]]
84	000034	07177			ANDLW	177	;LOW 7 BITS VALID
85	000035	00051			MOVWF	LOADD	;STORE SWITCH INPUT
86	000036	00152			CLRF	HIADD	;SWITCH INPUT 7 BITS
87	000037	02003			BCF	SWR,C	
88	000040	01551			RLF	LOADD	;JUMP TABLE -2 BYTE ADDRESS
89	000041	06177			MOVLW	177	
90	000042	00047			MOVWF	SWITCH	;BUSY LOW -CHIP "TALKING"
91	000043	04416			CALL	READ	;READ ROM -JUMP TABLE
92	000044	01010			MOVFW	DATA	;GET DATA
93	000045	00055			MOVWF	TEMP	;STORE LO ADDRESS
94	000046	04404			CALL	INCADD	;NEXT ROM LOCATION
95	000047	04410			CALL	DISABL	;DISABLE ROM
96	000050	04416			CALL	READ	;READ ROM -JUMP TABLE
97	000051	01010			MOVFW	DATA	
98	000052	00052			MOVWF	HIADD	;HI ADDRESS FROM JUMP TABLE
99	000053	01015			MOVFW	TEMP	
100	000054	00051			MOVWF	LOADD	;LO ADDRESS FROM JUMP TABLE
101				:			
102				;GET FRAMES OF DATA FROM ROM			
103				;AND SEND TO SP 0250			
104				:			
105	000055	03306		READY	BTFSC	IOB,DATAQ	;LINE INVERTED]]
106	000056	05055			GOTO	READY	;SP 0250 NOT READY
107	000057	04410		FRAME	CALL	DISABL	;DISABLE ROM
108	000060	04416			CALL	READ	;GET VOICE SELECT/REPEAT

LINE	ADDR	B1	B2		PAGE	3
109	000061	01010		MOVFW DATA		
110	000062	03103		BTFSC SWR,Z		
111	000063	05143		GOTO FINISH	:ZERO BYTE -END; "WORD"	
112	000064	00053		MOVWF REPEAT	:STORE VOICE SELECT/REPEAT	
113	000065	03713		BTFSS REPEAT,VOICE		
114	000066	05117		GOTO UNVOIC	:UNVOICED FRAME	
115	000067	06010		MOVLW 10		
116	000070	00054	SHALF	MOVWF CCOUNT	:LOAD COEFFICIENT COUNT	
117	000071	04404	GETDAT	CALL INCADD	:NEXT-LOCATION IN ROM	
118	000072	04410		CALL DISABL	:DISABLE ROM	
119	000073	04416		CALL READ	:GET COEFFICIENT	
120	000074	04401		CALL STROBE	:STROBE DATA INTO SP 0250	
121	000075	01354		DECFSZ CCOUNT		
122	000076	05071		GOTO GETDAT	:MORE COEFFICIENTS	
123	000077	03353		BTFSC REPEAT,7		
124	000100	05111		GOTO ZERO6	:SECOND TIME THROUGH	
125	000101	04410		CALL DISABL		
126	000102	01013		MOVFW REPEAT		
127	000103	00050		MOVWF DATA	:OUTPUT VOICE SELECT/REPEAT	
128	000104	04401		CALL STROBE	:STROBE SP 0250	
129	000105	04413		CALL RESTOR	:RESTORE SP 0250/ROM BUS	
130	000106	02753	REST	BSF REPEAT,7	:SET FLAG	
131	000107	06004		MOVLW 4	:GET STAGES 4 & 5	
132	000110	05070		GOTO SHALF		
133	000111	04410	ZERO6	CALL DISABL	:DISABLE ROM	
134	000112	04400		CALL ZERO6	:ZERO COEFFICIENT FOR	
135	000113	04400		CALL ZERO6	:SIXTH STAGE	
136	000114	04413		CALL RESTOR	:SET IOD FOR INPUT	
137	000115	04404		CALL INCADD		
138	000116	05055		GOTO READY	:GET NEXT SPEECH FRAME	
139				:		
140				:UNVOICED		
141				:		
142	000117	04410	UNVOIC	CALL DISABL	:DISABLE ROM	
143	000120	04400		CALL ZERO6	:ZERO COEFFICIENT FOR	
144	000121	04400		CALL ZERO6	:FIRST STAGE	
145	000122	04413		CALL RESTOR	:RESTORE SP 0250/ROM BUS	
146	000123	04404		CALL INCADD	:NEXT ROM LOCATION	
147	000124	04416		CALL READ	:GET AMPLITUDE	
148	000125	04401		CALL STROBE	:STROBE DATA INTO SP 0250	
149	000126	04410		CALL DISABL	:DISABLE ROM	
150	000127	04400		CALL ZERO6	:ZERO COEFFICIENT FOR	
151	000130	04400		CALL ZERO6	:SECOND STAGE	
152	000131	06100		MOVLW .64		
153	000132	00050		MOVWF DATA	:PITCH PERIOD -> 64	
154	000133	04401		CALL STROBE	:STROBE INTO SP 0250	
155	000134	04400		CALL ZERO6	:ZERO COEFFICIENT FOR	
156	000135	04400		CALL ZERO6	:THIRD STAGE	
157	000136	01013		MOVFW REPEAT		
158	000137	00050		MOVWF DATA	:VOICE SELECT/REPEAT	
159	000140	04401		CALL STROBE	:STROBE INTO SP 0250	
160	000141	04413		CALL RESTOR	:RESTORE SP 0250/ROM BUS	
161	000142	05106		GOTO REST	:GET COEFFICIENTS FOR 4 & 5 STAGE	
162				:		

LINE	ADDR	B1	B2		PAGE	4
163				;FINISH -ONE WORD OR PHRASE HAS		
164				; BEEN SPOKEN		
165				;		
166	000143	06377		FINISH MOVLW 377		
167	000144	00047		MOVWF SWITCH	:BUSY HI -CHIP "NOT TALKING"	
168	000145	04413		CALL RESTOR	:RESTOR IOD FOR INPUT	
169	000146	05027		GOTO START		
170				ORG 777		
171	000777	05027		GOTO START		
172	001000			END		

ASSEMBLER ERRORS = 0

NOTE: On reset all I/O pins are set high and program execution begins at address 777_h.



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