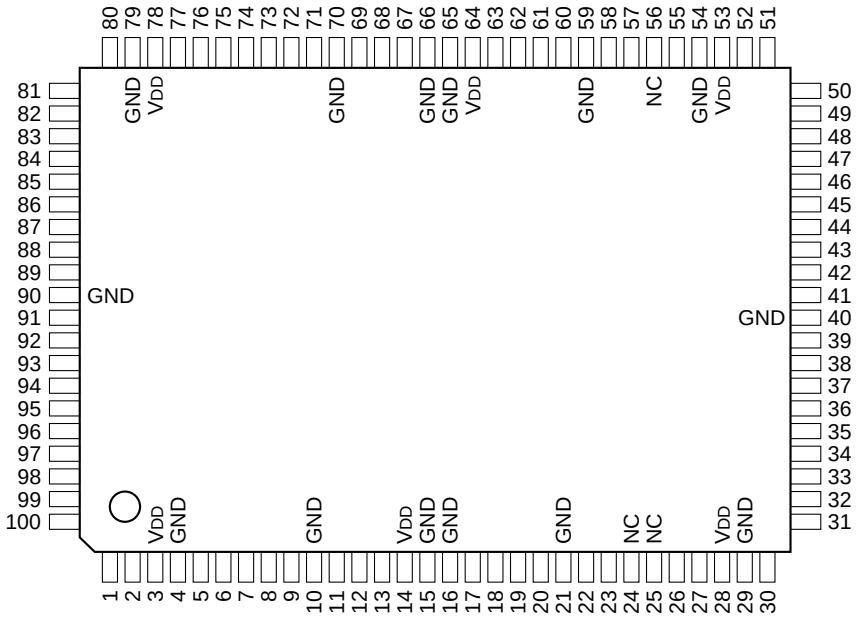
C-MOS SCSI-2 PROTOCOL CONTROLLER

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{WE}$ ($\overline{LDS}$)	26	I	$\overline{IOWR}$ ($\overline{DMLDS}$)	51	I	$\overline{DACK}$	76	I	A4
2	I	$\overline{RD}$ (R/$\overline{W}$)	27	I	$\overline{IORD}$ (DMR/$\overline{W}$)	52	O	DREQ	77	I	$\overline{CS0}$
3	—	VDD	28	—	VDD	53	—	VDD	78	—	VDD
4	—	GND	29	—	GND	54	—	GND	79	—	GND
5	I	CLK	30	I	DMA0	55	I	TP	80	I	$\overline{CS1}$
6	I	$\overline{RESET}$	31	I/O	LDMDP	56	—	—	81	I/O	LDP
7	O	INT ($\overline{INT}$)	32	I/O	DMD0	57	I	TEST2	82	I/O	D0
8	I	MODE	33	I/O	DMD1	58	I/O	$\overline{I/O}$	83	I/O	D1
9	I/O	$\overline{DBP}$	34	I/O	DMD2	59	—	GND	84	I/O	D2
10	—	GND	35	I/O	DMD3	60	I/O	$\overline{REQ}$	85	I/O	D3
11	I/O	DB7	36	I/O	DMD4	61	I/O	$\overline{C/D}$	86	I/O	D4
12	I/O	DB6	37	I/O	DMD5	62	I/O	$\overline{SEL}$	87	I/O	D5
13	I/O	DB5	38	I/O	DMD6	63	I/O	$\overline{MSG}$	88	I/O	D6
14	—	VDD	39	I/O	DMD7	64	—	VDD	89	I/O	D7
15	—	GND	40	—	GND	65	—	GND	90	—	GND
16	—	GND	41	I/O	DMD8	66	—	GND	91	I/O	D8
17	I/O	DB4	42	I/O	DMD9	67	I/O	$\overline{RST}$	92	I/O	D9
18	I/O	DB3	43	I/O	DMD10	68	I/O	$\overline{ACK}$	93	I/O	D10
19	I/O	DB2	44	I/O	DMD11	69	I/O	$\overline{BSY}$	94	I/O	D11
20	I/O	DB1	45	I/O	DMD12	70	—	GND	95	I/O	D12
21	—	GND	46	I/O	DMD13	71	I/O	$\overline{ATN}$	96	I/O	D13
22	I/O	DB0	47	I/O	DMD14	72	I	A0	97	I/O	D14
23	I	TEST1	48	I/O	DMD15	73	I	A1	98	I/O	D15
24	—	—	49	I/O	UDMDP	74	I	A2	99	I/O	UDP
25	—	—	50	I	$\overline{DMBHE}$ ($\overline{DMUDS}$)	75	I	A3	100	I	$\overline{BHE}$ ($\overline{UDS}$)

( ) ; AT LOW LEVEL

SCSI INTERFACE

INPUT/OUTPUT

$\overline{ACK}$	:	ACKNOWLEGE
$\overline{ATN}$	:	ATTENTION
$\overline{BSY}$	:	BUSY
$\overline{C/D}$	:	CONTROL/DATA
$\overline{DB0}$ - $\overline{DB7}$	:	DATA BUS0 - DATA BUS7
$\overline{DBP}$	:	DATA BUS PARITY
$\overline{I/O}$	:	INPUT/OUTPUT
$\overline{MSG}$	:	MESSAGE
$\overline{REQ}$	:	REQUEST
$\overline{RST}$	:	RESET
$\overline{SEL}$	:	SELECT

MPU INTERFACE

INPUT

A0 - A4	:	ADDRESS0 - ADDRESS4
$\overline{BHE}$ ($\overline{UDS}$)	:	BUS HIGH ENABLE (UPPER DATA STOROBE)
$\overline{CS0}$	:	CHIP SELECT 0
$\overline{CS1}$	:	CHIP SELECT 1
MODE	:	MODE
$\overline{RD}$ (R/$\overline{W}$)	:	READ (READ/WRITE)
$\overline{WR}$ ($\overline{LDS}$)	:	WRITE (LOWER DATA STOROBE)

OUTPUT

INT ($\overline{INT}$)	:	INTERRUPT REQUEST

INPUT/OUTPUT

D0 - D15	:	DATA0 - DATA15
LDP	:	LOWER DATA PARITY
UDP	:	UPPER DATA PARITY

DMA INTERFACE

INPUT

DACK	:	DMA ACKNOWLEDGE
DMA0	:	DMA ADDRESS 0
DMBHE (DMUDS)	:	DMA BUS HIGH ENABLE (DMA UPPER DATA STOROBE)
IORD (DMR/W)	:	I/O READ (DMA READ/WRITE)
IOWR(DMLDS)	:	I/O WRITE (DMA LOWER DATA STOROBE)
TP	:	TRANSFER PERMISSION

OUTPUT

DREQ	:	DMA REQUEST

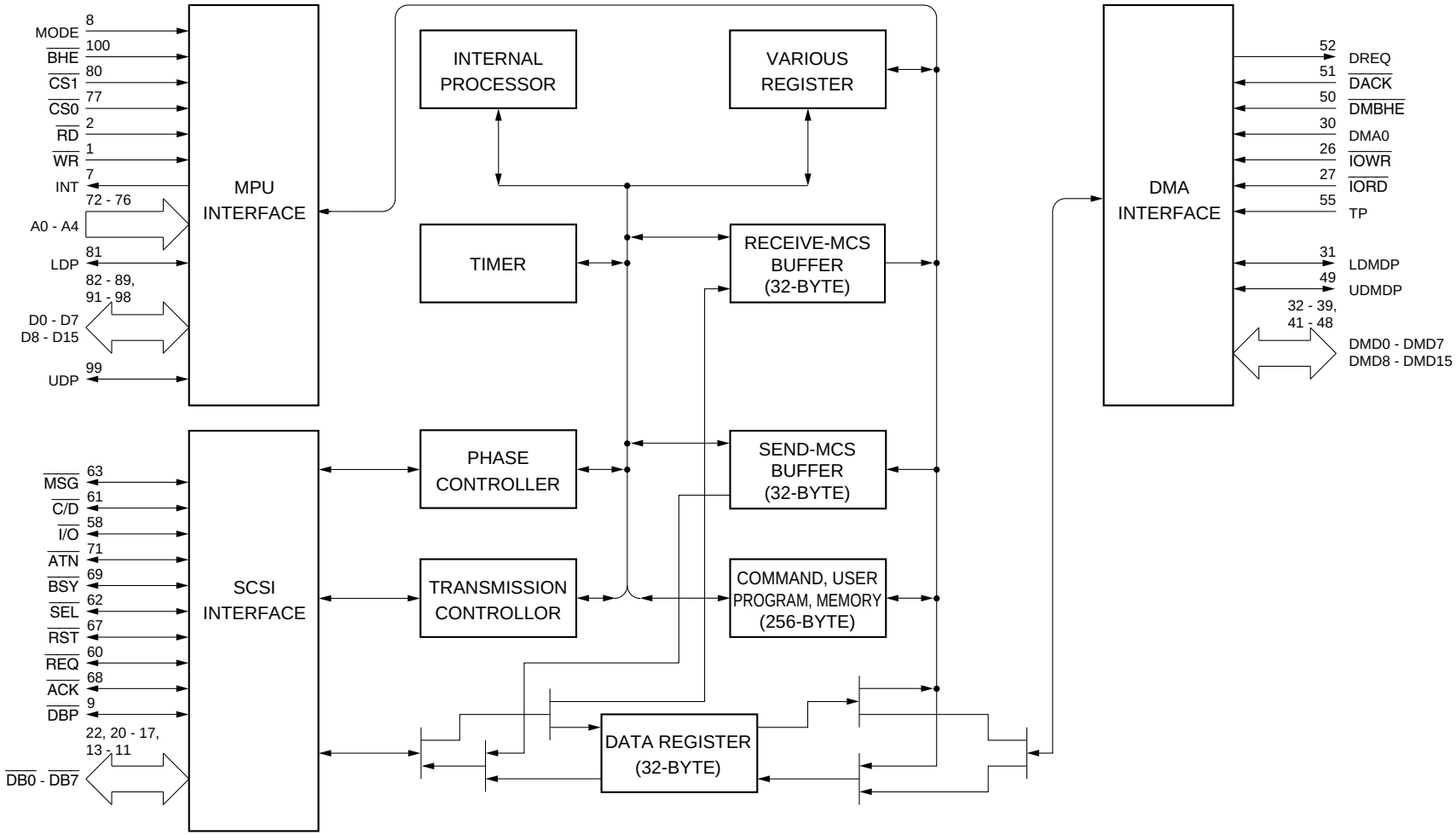
INPUT/OUTPUT

DMD0 - DMD15	:	DMD DATA0 - DMD DATA15
LDMDP	:	LOWER DMA DATA PARITY
UDMDP	:	UPPER DMA DATA PARITY

INPUT

CLK	:	CLOCK
RESET	:	RESET
TEST1, 2	:	TEST

( ) ; WHEN “MODE” (8PIN) IS “L” LEVEL INPUT.


MODE 8
BHE 100
CS1 80
CS0 77
RD 2
WR 1
INT 7
A0 - A4 72 - 76
LDP 81
D0 - D7
D8 - D15 82 - 89, 91 - 98
UDP 99
MPU INTERFACE
INTERNAL PROCESSOR
VARIOUS REGISTER
TIMER
RECEIVE-MCS BUFFER (32-BYTE)
PHASE CONTROLLER
SEND-MCS BUFFER (32-BYTE)
TRANSMISSION CONTROLLOR
COMMAND, USER PROGRAM, MEMORY (256-BYTE)
DATA REGISTER (32-BYTE)
MSG 63
C/D 61
I/O 58
ATN 71
BSY 69
SEL 62
RST 67
REQ 60
ACK 68
DBP 9
DB0 - DB7 22, 20 - 17, 13 - 11
SCSI INTERFACE
DMA INTERFACE
DREQ 52
DACK 51
DMBHE 50
DMA0 30
IOWR 26
IORD 27
TP 55
LDMDP 31
UDMDP 49
DMD0 - DMD7
DMD8 - DMD15 32 - 39, 41 - 48