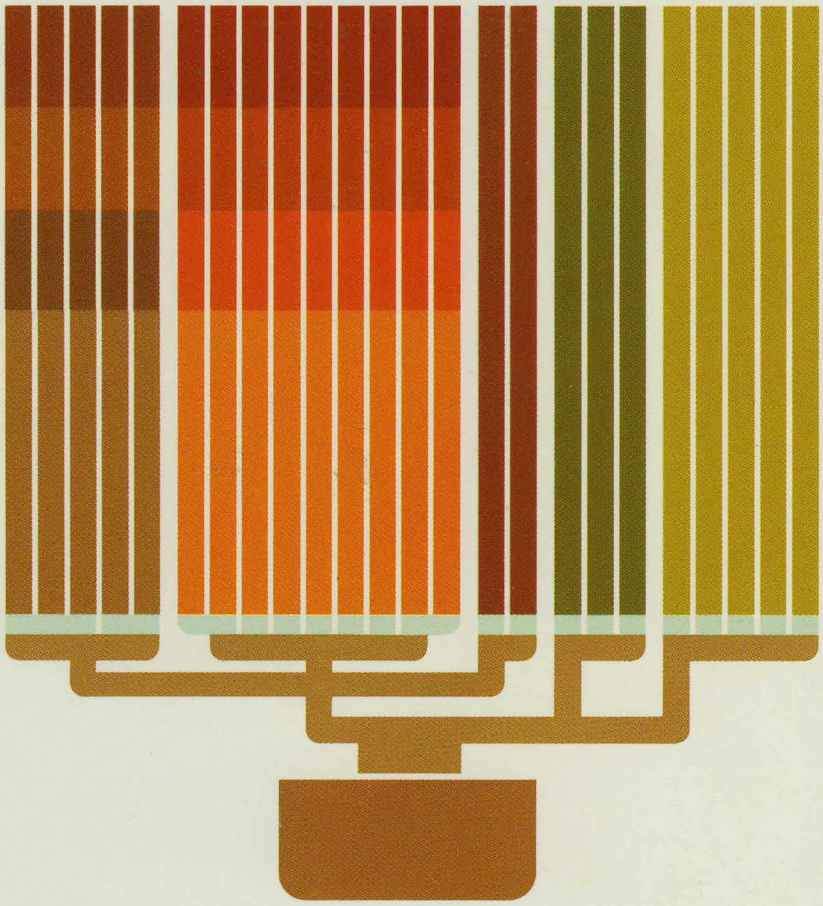
FAIRCHILD SEMICONDUCTOR

Fairchild TTL Family



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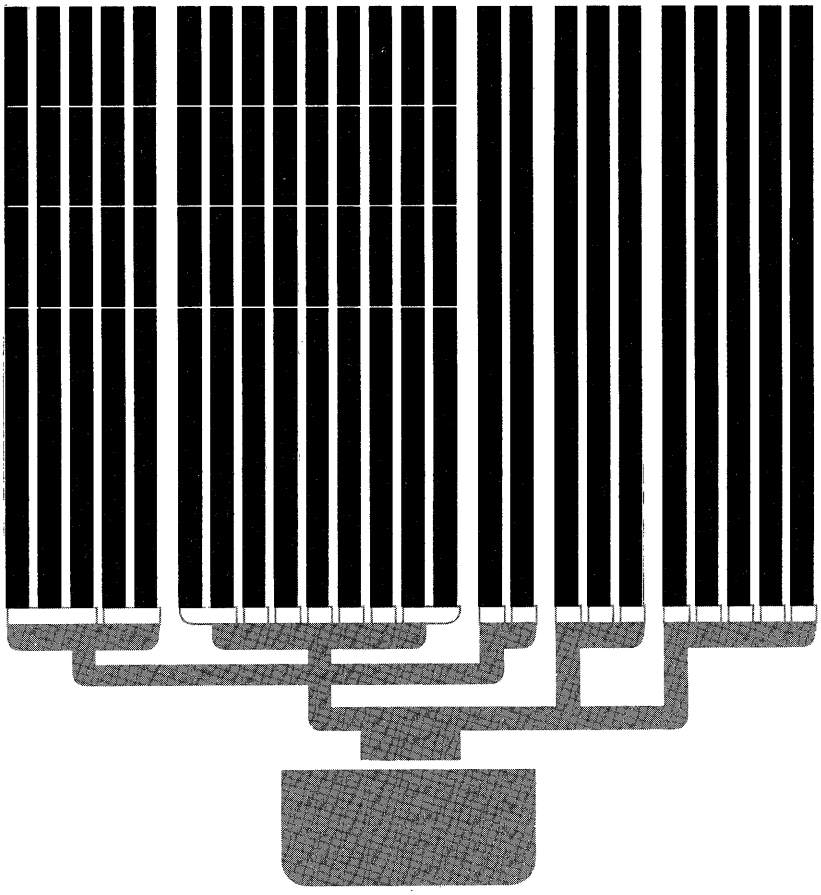


SECTION SELECTOR

- SSI
- MSI
- Memory
- Interface

SPEED/POWER RANGE SELECTOR

- Standard TTL
- Low Power TTL
- High Speed TTL
- Super High Speed TTL (SCHOTTKY)

FUNCTION SELECTOR

- Gates & Flip-Flops
- Registers
- Encoders
- Operators
- Decoders-Demultiplexers
- Multiplexers
- Latches
- Counters
- RAM
- ROM
- CAM
- Pulse Shapers
- Drivers
- Line Drivers/Receivers
- Translators
- Sense Amplifiers

Table of Contents

INTRODUCTION

Fairchild's TTL Family is the most complete line of TTL products available today. There are over 150 circuit functions with more than 75 MSI devices from which to choose. The family consists of logic, memory and interface functions, and is a unique blend of Fairchild proprietary circuits and a large number of second source devices which have achieved wide market acceptance.

Fairchild's family of functions has been designed to provide the system designer with a complete line of standard, off-the-shelf functional building blocks that can be interfaced directly with each other in the same system to provide almost any Speed/ Power combination.

The typical characteristics of the Fairchild TTL Family are as follows. Full loading information is given on pages 81 to 107.

Supply Voltage	5.0 V
Logic "0" Output Voltage	0.2 V
Logic "1" Output Voltage	3.0 V
Noise Immunity	1.0 V
Temperature Ranges	0°C to +70°C
	−55°C to +125°C
Packages	14, 16 and 24 Lead Dip and Flat Pack

NUMERICAL INDEX OF DEVICES

NUMERICAL INDEX OF DEVICES

54/74 SERIES INDEX

The following is a quick-look index to Fairchild second-sourced devices in the popular 5400/7400 series.

SERIES 54 (Standard)

DEVICE	Page No. SPECS	PINS DIP	PINS FP
5400	8	89	100
5401	8	89	100
5402	8	89	100
5403	8	89	
5404	8	89	100
5405	8	89	100
5408	8	89	100
5410	8	89	100
5411	8	89	100
5420	8	89	100
5430	8	89	100
5440	8	89	100
5442	31	94	
5443	31	94	
5444	32	94	
5446	32	94	
5447	32	94	
5448	33	94	
5449	33		104
5450	8	90	100
5451	8	90	101
5453	8	90	101
5454	8	90	101
5460	8	90	101
5470	8	90	101
5472	8	90	101
5473	8	90	101
5474	8	90	101
5475	37	94	
5476	8	90	
5477	37		104
5480	25	95	104
5482	25	95	105
5483	26	95	
5486	8	90	101
5490	45	95	
5491	16	95	105
5492	46	95	
5493	46	95	
5494	17	95	
5495	18	95	105
5496	19	95	105
54104	8	90	101
54105	8	90	101
54107	8	90	
54141	29	95	105
54181	23	94	104
54182	24	94	104
54192	43	94	104
54193	44	94	104

SERIES 54H (High Speed)

DEVICE	Page No. SPECS	PINS DIP	PINS FP
54H00	9	91	102
54H01	9	91	102
54H04	9	91	102
54H05	9	91	102
54H10	9	91	102
54H20	9	91	102
54H22	9	91	102
54H30	9	91	102
54H40	9	91	102
54H50	9		
54H51	9		
54H61	9		
54H72	9		
54H73	9	91	102
54H76	9	91	
54H78	9	91	102

SERIES 74 (Standard)

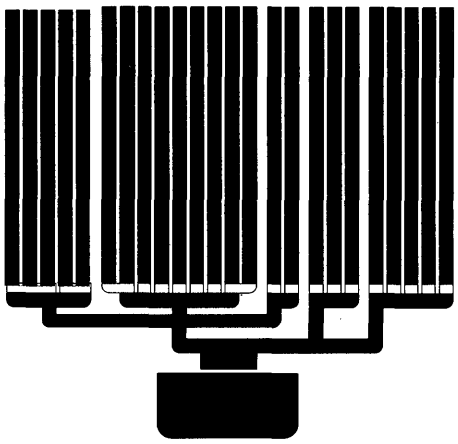
DEVICE	Page No. SPECS	PINS DIP	PINS FP
7400	8	89	100
7401	8	89	100
7402	8	89	100
7403	8	89	
7404	8	89	100
7405	8	89	100
7408	8	89	100
7410	8	89	100
7411	8	89	100
7420	8	89	100
7430	8	89	100
7440	8	89	100
7441	28	93	104
7442	31	94	
7443	31	94	
7444	32	94	
7446	32	94	
7447	32	94	
7448	33	94	
7449	33		104
7450	8	90	100
7451	8	90	101
7453	8	90	101
7454	8	90	101
7460	8	90	101
7470	8	90	101
7472	8	90	101
7473	8	90	101
7474	8	90	101
7475	37	94	
7476	8	90	
7477	37		104
7480	25	95	104
7481	65	97	106
7482	25	95	105
7483	26	95	
7486	8	90	101
7488	70	97	106
7489	66	97	106
7490	45	95	
7491	16	95	105
7492	46	95	
7493	46	95	
7494	17	95	
7495	18	95	105
7496	19	95	105
74104	8	90	101
74105	8	90	101
74107	8	90	
74141	29	93	105
74181	23	94	104
74182	24	94	104
74192	43	94	104
74193	44	94	104
74196	61	96	106
74197	61	96	106

SERIES 74H (High Speed)

DEVICE	Page No. SPECS	PINS DIP	PINS FP
74H00	9	91	102
74H01	9	91	102
74H04	9	91	102
74H05	9	91	102
74H10	9	91	102
74H20	9	91	102
74H22	9	91	102
74H30	9	91	102
74H40	9	91	102
74H50	9		
74H51	9		
74H60	9		
74H61	9		
74H72	9		
74H73	9	91	102
74H76	9	91	
74H78	9	91	102

SERIES 74S
(Super High Speed)

DEVICE	Page No. SPECS	PINS DIP	PINS FP
74S00	9		
74S01	9		
74S04	9		
74S05	9		
74S20	9		
74S22	9		
74S40	9		
74S112	9		
74S113	9		
74S114	9		



TTL/SSI

INTRODUCTION — The Fairchild TTL/SSI line offers the designer a broad selection of gates and flip flops for use with Fairchild MSI, Interface and Memory products in implementing TTL system designs. A total of 56 TTL/SSI functions are available for use in military and industrial temperature range applications. These products are available in the popular Dual In-Line package as well as Flat packages. All Fairchild TTL products are logic and supply voltage compatible so that circuit families may be mixed within a system for optimum speed, power and economy.

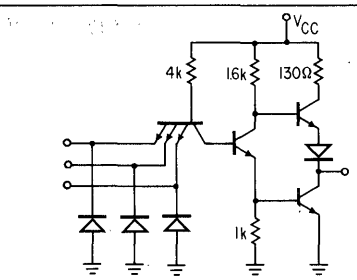
9N/54, 74 SERIES TTL/SSI

FEATURES

- 10 ns Typical Gate Delay
- 10 mW Typical Gate Power Dissipation
- Input Clamp Diodes Minimize Termination Effects
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages
- 26 Functions Available

DESCRIPTION

The 9N/54, 74 Series is a broad family of SSI devices which are pin and function identical with the popular 7400 series. These gates and binaries are available in industrial and military temperature ranges in both DIP and Flat packages. The line includes NAND gates, NOR gates, Exclusive-OR gates, AND gates, open collector gates as well as single and dual flip flops.



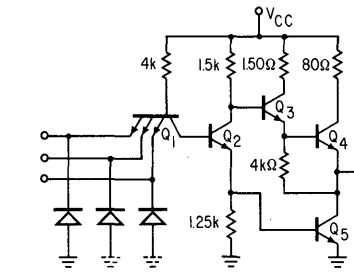
9000 SERIES TTL/SSI

FEATURES

- 8 ns Typical Gate Delay
- 10 mW Typical Gate Power Dissipation
- Input Clamp Diodes Reduce Termination Effects
- Darlington Output Stage Increases Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages
- 18 Functions Available

DESCRIPTION

The 9000 Series of gates and flip flops offers a family of high speed functions with speed and power specifications in between the 9N/54, 74 Series and the 9H/54H, 74H Series. The Darlington output stage provides faster switching times and increased capacitive drive capability over the 9N/54, 74 Series.



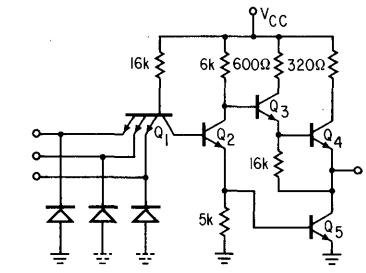
9L SERIES LPTTL/SSI

FEATURES

- 20 ns Typical Gate Delay
- 2 mW Typical Gate Power Dissipation
- Input Clamp Diodes Minimize Termination Effects
- Darlington Output Stage Increases Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages

DESCRIPTION

The 9L Series of low power TTL gates and flip flops offers a speed/power trade-off well suited to both industrial and military applications. The power is one fourth that of a standard TTL gate and typical system speeds of up to 10 MHz are possible. The 9L Series TTL/SSI functions are used with the 93L low power TTL/MSI devices to implement low power, moderate speed systems.



9H/54H, 74H SERIES HSTTL/SSI

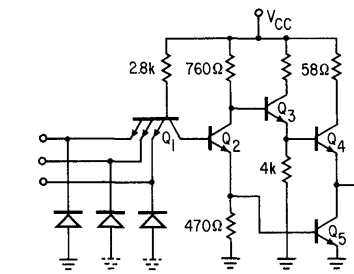
FEATURES

- 6 ns Typical Gate Delay
- 22 mW Typical Gate Power Dissipation
- Input Clamp Diodes to Minimize Termination Effects
- Darlington Output Stage to Increase Circuit Speed
- Military and Industrial Temperature Range
- Available in DIP and Flat Packages
- 11 Functions Available

DESCRIPTION

The 9H/54H, 74H Series is a line of high speed gates and flip flops which are pin and function identical with the popular 74H00 Series.

These devices are used with the 9300 and 93H Series of TTL/MSI devices to implement high speed logic functions in digital systems.

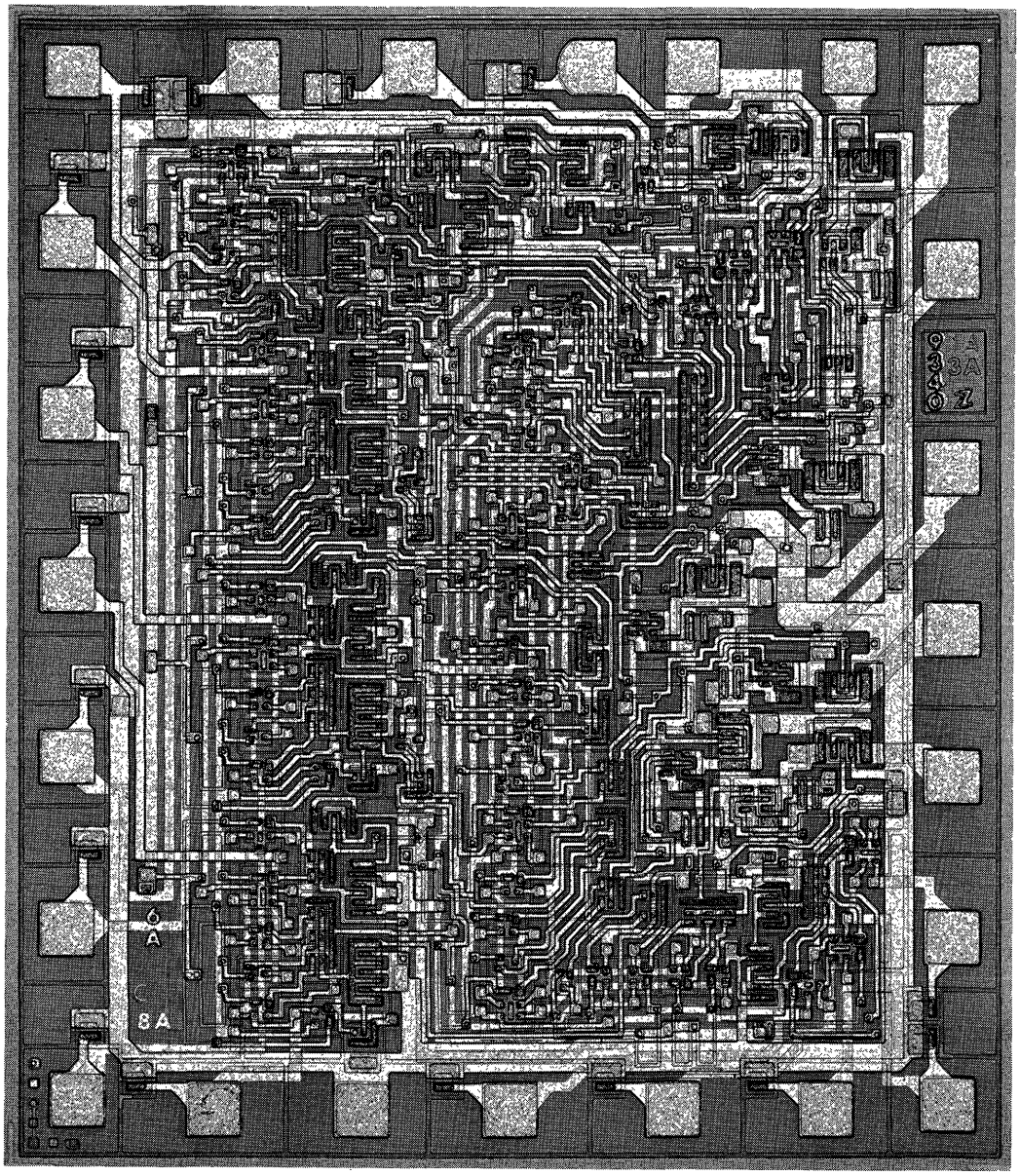


	STANDARD		
	t_{pd} = 10 ns P_d = 10 mW per Gate		
NAND GATES	0° to +70°C	−55° to +125°C	
Quad 2-Input Positive NAND Gate	9N00/7400	9N00/5400	
Quad 2-Input Positive NAND Gate	9N01/7401	9N01/5401	
with Open-Collector Output	9N03/7403	9N03/5403	
Triple 3-Input Positive NAND Gate	9N10/7410	9N10/5410	
Dual 4-Input Positive NAND Gate	9N20/7420	9N20/5420	
8-Input Positive NAND Gate	9N30/7430	9N30/5430	
NOR GATES			
Quad 2-Input Positive NOR Gate	9N02/7402	9N02/5402	
Quad 2-2-2-4-Input Positive NOR Gate			
AND GATES			
Quad 2-Input Positive AND Gate	9N08/7408	9N08/5408	
Quad 2-Input Positive AND Gate (Open Collector)	9N09/7409	9N09/5409	
Triple 3-Input Positive AND Gate	9N11/7411	9N11/5411	
EXCLUSIVE-OR GATES			
Quad Exclusive-OR Gate	9N86/7486	9N86/5486	
Quad Exclusive-OR Gate with Inverted Outputs			
AND-OR-INVERT GATES AND EXPANDERS			
Dual 2-Wide 2-Input AND-OR-INVERT Gate	9N51/7451	9N51/5451	
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	9N50/7450	9N50/5450	
4-Wide 2-Input AND-OR-INVERT Gate	9N54/7454	9N54/5454	
Expandable 4-Wide 2-Input AND-OR-INVERT Gate	9N53/7453	9N53/5453	
Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate			
Dual 4-Input Expander	9N60/7460	9N60/5460	
INVERTERS AND BUFFERS			
Hex Inverter	9N04/7404	9N04/5404	
Hex Inverter with Open-Collector Output	9N05/7405	9N05/5405	
Dual 4-Input Positive NAND Buffer	9N40/7440	9N40/5440	
FLIP-FLOPS			
J-K Flip-Flop	9N70/7470	9N70/5470	
	9N105/74105	9N105/54105	
J-K Master Slave Flip-Flop	9N72/7472	9N72/5472	
	9N104/74104	9N104/54104	
Dual J-K Flip-Flop			
Dual J-K Master Slave Flip-Flop	9N73/7473	9N73/5473	
	9N107/74107	9N107/54107	
Dual J-K Master Slave Flip-Flop with Separate Preset and Clear	9N76/7476	9N76/5476	
Dual D-Type Edge-Triggered Flip-Flop	9N74/7474	9N74/5474	

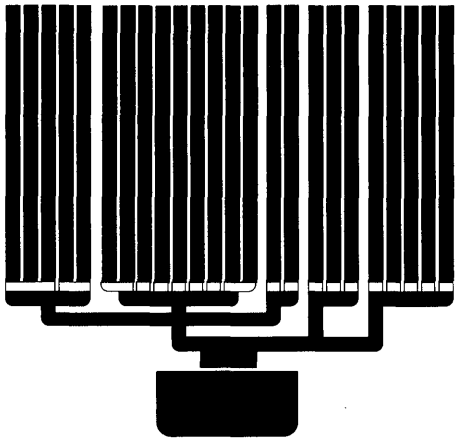
	LOW POWER	HIGH SPEED		SUPER HIGH SPEED
t_{pd} = 8 ns P_d = 10 mW per Gate	t_{pd} = 20 ns P_d = 2 mW per Gate	t_{pd} = 6 ns P_d = 22 mW per Gate		t_{pd} = 3 ns P_d = 19 mW per Gate
0°C to +70°C and −55° to +125°C	0°C to +70°C and −55° to +125°C	0° to +70°C	−55° to +125°C	0° to +70°C
9002	9L00	9H00/74H00	9H00/54H00	9S00/74S00
		9H01/74H01	9H01/54H01	9S01/74S01
9012				
9003		9H10/74H10	9H10/54H10	
9004		9H20,22/74H20,22	9H20,22/54H20,22	9S20,22/74S20,22
9007		9H30/74H30	9H30/54H30	
9015				
		9H08/74H08	9H08/54H08	
		9H11/74H11	9H11/54H11	
	9L86			
9014				
		9H51/74H51	9H51/54H51	
9005		9H50/74H50	9H50/54H50	
	9L54	9H54/74H54	9H54/54H54	
		9H53/74H53	9H53/54H53	
9008				
9006		9H60/74H60	9H60/54H60*	
9016	9L04	9H04/74H04	9H04/54H04	9S04/74S04
9017		9H05/74H05	9H05/54H05	9S05/74S05
9009		9H40/74H40	9H40/54H40	9S40/74S40
		9H71/74H71	9H71/54H71	
9001				
		9H72/74H72	9H72/54H72	
9000				
9020				
9022				
9024	9L24			
		9H73/74H73	9H73/54H73	9S113/74S113
		9H78/74H78	9H78/54H78	9S114/74S114
		9H76/74H76	9H76/54H76	9S112/74S112
		9H74/74H74	9H74/54H74	

IN DEVELOPMENT

* TO BE ANNOUNCED



Photomicrograph of the TTL/MSI 9340 Arithmetic Logic Unit Showing Dual Layer Metal Technology



TTL/MSI

INTRODUCTION — The Fairchild TTL/MSI product line includes 75 complex digital logic functions, including standard, high speed, and low power circuits. The use of complex TTL functions in the design of new digital systems can significantly reduce package count and systems cost while providing smaller size, increased reliability, and greater overall system speed. The Fairchild TTL/MSI product line is divided into 7 functional categories and contains standard, high speed and low power complex circuits.
The table below summarizes the Fairchild TTL/MSI product line.

	STANDARD TTL	LOW POWER TTL	HIGH SPEED TTL	SUPER HIGH SPEED TTL
REGISTERS				
4-Bit Shift Register	9300 9394/7494	93L00	93H00*	
4-Bit Shift Register With Clock Enable			93H72	
4-Bit Right/Left Shift Register	9395/7495			
5-Bit Shift Register	9396/7496			
8-Bit Shift Register	9391/7491			
Dual 8-Bit Shift Register	9328	93L28		
8-Bit Multiple Port Register	9338			
ENCODERS				
8-Input Priority Encoder	9318	93L18		
OPERATORS				
Dual Full Adder	9304			
Full Adder	9380/7480			
2-Bit Full Adder	9382/7482			
4-Bit Full Adder	9383/7483			
5-Bit Comparator	9324	93L24		
4-Bit Arithmetic Logic Units	9340 9341/74181	93L40		
Carry Lookahead	9342/74182			
12-Input Parity Checker/Generator	9348			
DECODERS/DEMULTIPLEXERS				
One of Ten Decoder	9301	93L01		
BCD To Decimal Decoder	9352/7442			
Excess - 3 To Decimal Decoder	9353/7443			
Excess - 3 Gray To Decimal Decoder	9354/7444			
One of Sixteen Decoder	9311	93L11		
Dual One of Four Decoder	9321	93L21		
One of Ten Decoder/Driver	9315/7441			
BCD To Decimal Decoder/Driver	9325/74141			
Seven Segment Decoder	9307			
Seven Segment Decoder/Driver	9317 9327 9337			
BCD To Seven Segment Decoder/Driver	9357A/7446 9357B/7447			
BCD To Seven Segment Decoder	9358/7448 9359/7449			

IN DEVELOPMENT

* TO BE ANNOUNCED

TTL/MSI • MULTIPLEXERS • LATCHES • COUNTERS

MULTIPLEXERS	STANDARD TTL	LOW POWER TTL	HIGH SPEED TTL	SUPER HIGH SPEED TTL
Quad Two Input Multiplexer	9322	93L22		
Dual Four Input Multiplexer	9309	93L09		
Eight Input Multiplexer	9312	93L12		
LATCHES				
Four Bit Latch	9314 9375/7475 9377/5477	93L14		
Dual Four Bit Latch	9308	93L08		
Eight Bit Addressable Latch	9334			
COUNTERS				
Decade Counter	9350 9390/7490		93H70*	
Decade Counter	9310	93L10		
Up/Down Decade Counter (Dual Clock)	9360/74192			
Up/Down BCD Counter	9306			
Binary Counter	9356 9393/7493		93H76*	
4-Bit Binary Counter	9316	93L16		
Up/Down Binary Counter (Dual Clock)	9366/74193			
Divide By Twelve Counter	9392/7492			
Variable Modulo Counter	9305			

IN DEVELOPMENT

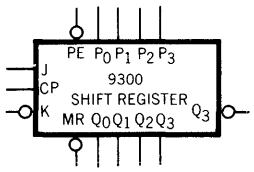
* TO BE ANNOUNCED

9300
4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION The 9300 is a synchronous 4-bit shift register designed to perform functions such as storage, shifting, counting and serial code conversion. It has assertion outputs on each stage and a negation output on the last stage, an overriding asynchronous master reset, J$\overline{K}$ input configuration, and a synchronous parallel load facility.

Data entry is synchronous with the registers changing state after each low to high transition of the clock. With the parallel enable low the parallel inputs determine the next condition of the shift register. When the parallel enable input is high the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through J$\overline{K}$ inputs. By tying the two inputs together D type entry is obtained.

The asynchronous active low master reset when activated overrides all other input conditions and clears the register.



PIN NAMES

		LOADING
$\overline{PE}$	Parallel Enable (Active Low) Input	2.3 UL
P_0, P_1, P_2, P_3	Parallel Inputs	1 UL
J	First Stage J (Active High) Input	1 UL
$\overline{K}$	First Stage K (Active Low) Input	1 UL
CP	Clock(Active High Going Edge)Input	2 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	6 UL
$\overline{Q_3}$	Complementary Last Stage Output	6 UL

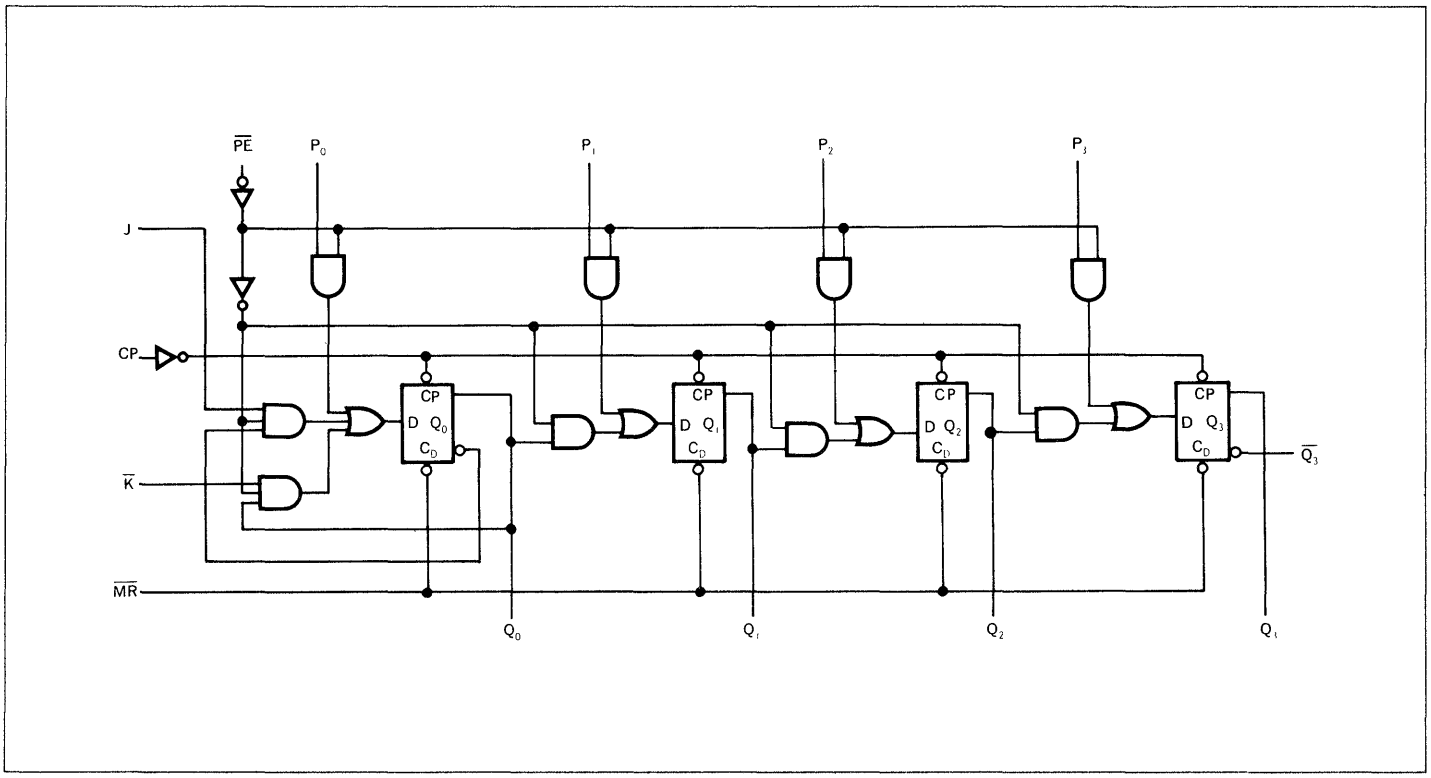
TRUTH TABLE FOR SERIAL ENTRY

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

$\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH, (n + 1) indicates state after next clock

CHARACTERISTICS

TYPICAL SPEED	25 MHz Shifting Frequency
TYPICAL DELAY	CP to Q 23 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	300 mW

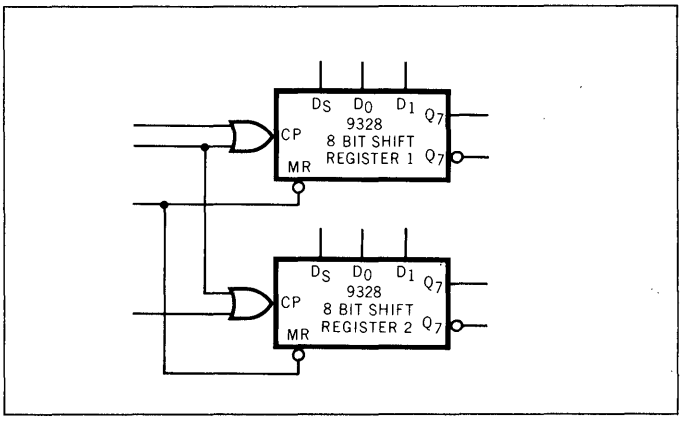


9328
DUAL 8-BIT SHIFT REGISTER

DESCRIPTION The 9328 is a Dual 8-bit synchronous shift register which can be used in high speed serial storage applications. Each register has a true and complemented output from the last stage, 2-input multiplexer with data select control at the input, and a two input clock OR gate input. A common clock, obtained by internally tying one input of each clock OR gate together, and overriding asynchronous master reset are common to both registers.

Data entry is synchronous with the registers changing state after each low to high transition of the clock. Serial data enters through D_0 when the data select line is low and through D_1, when the data select line is high. The clocking scheme employed allows the three clock inputs to be used in the following ways: one clock common with two separate clocks; one clock common with a separate active low clock enable input for each 8 bit shift register, and two separate clocks and one common active low clock enable input.

The asynchronous active low master reset when activated overrides all other input conditions and clears the register.



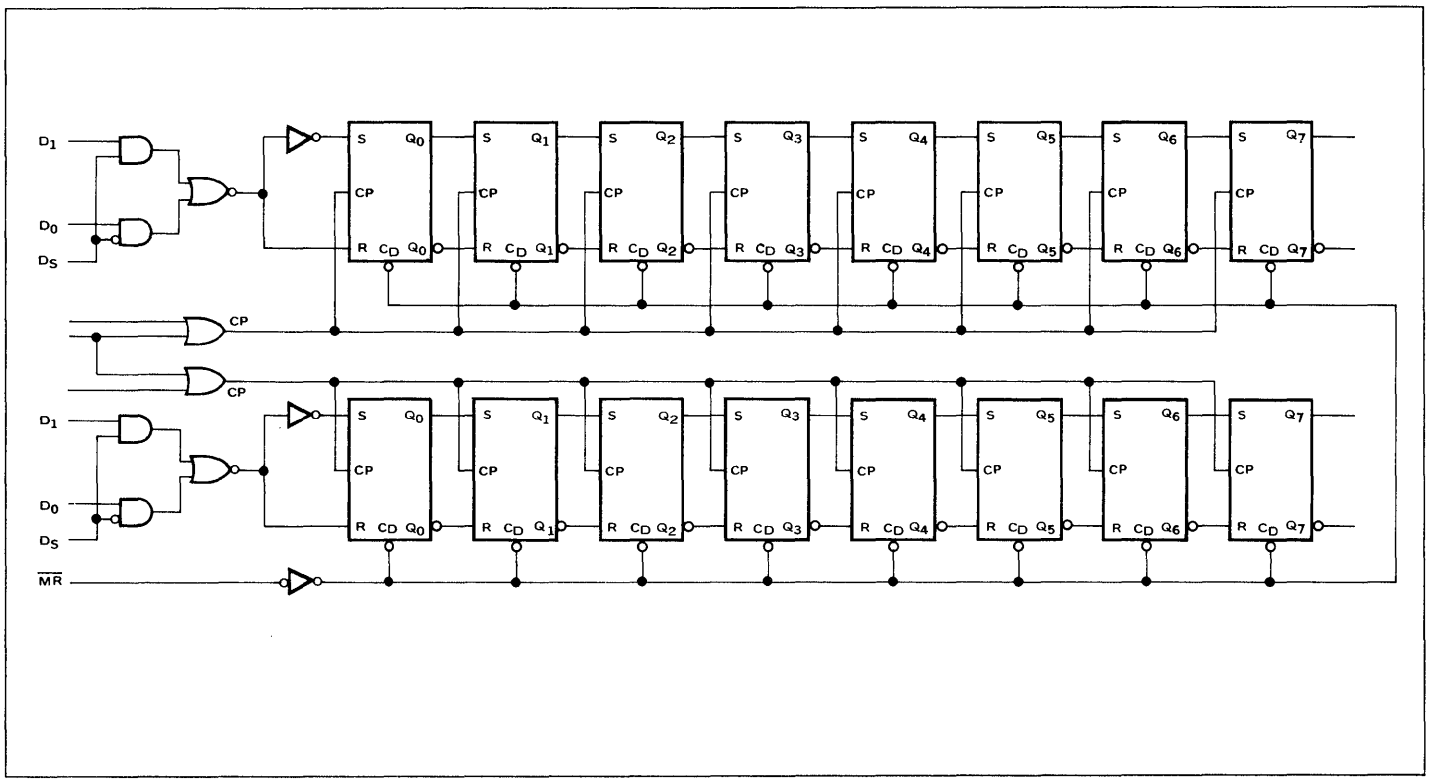
PIN NAMES		LOADING
D_S	Data Select Input	2 UL
D_0, D_1	Data Inputs	1 UL
CP	OR Clock Active High Going Edge Inputs	Common 3.0 UL Separate 1.5 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_7	Last Stage Output	6 UL
$\overline{Q_7}$	Complementary Output	6 UL

LOGIC EQUATION FOR DATA ENTRY

$$S_D = \overline{D_S} \cdot D_0 + D_S \cdot D_1$$

CHARACTERISTICS

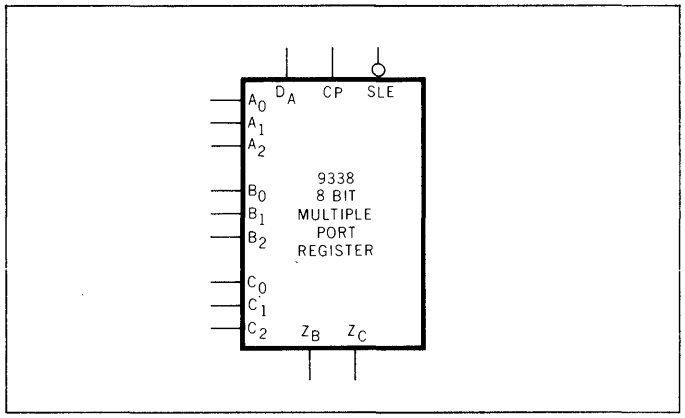
TYPICAL DELAY	CP to Q 17 ns
TYPICAL SPEED	30 MHz Shifting Frequency
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	300 mW



9338
8-BIT MULTIPLE PORT REGISTER

DESCRIPTION The 9338 is a multiple port register designed for high speed random access memory applications where the ability to simultaneously read and write is desirable. A common use would be as a register bank in a three address computer. Data can be written into any one of 8 bits, and read from any two of the 8 bits simultaneously.

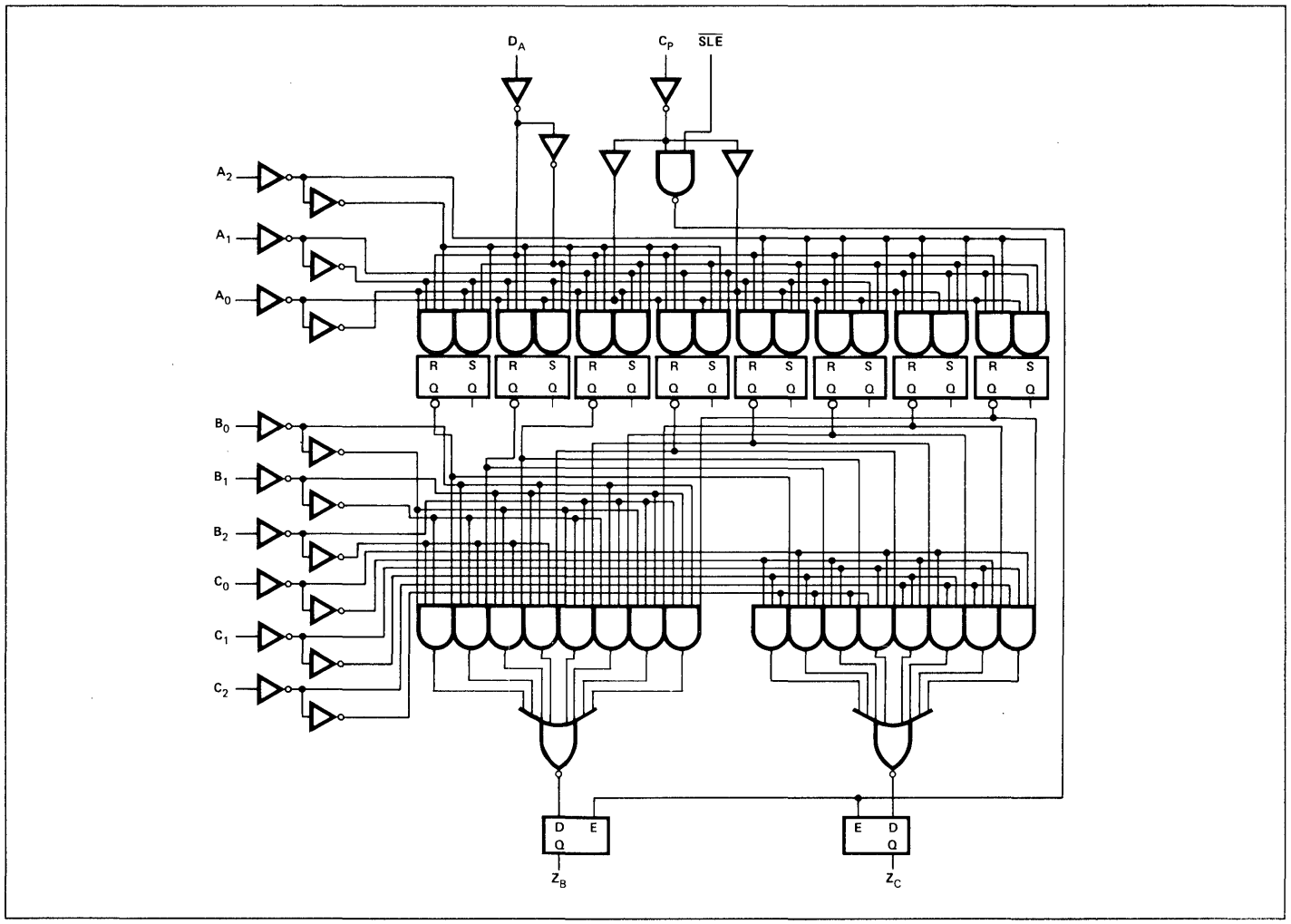
It is organized as a master slave register that has eight masters and two slaves. Data on the D_A input is stored in the master selected by the write address inputs synchronously with the clock pulse (CP). Data from the eight masters is selected by the two independent read address fields and applied to the two slave flip flops. The slaves are controlled by the slave enable input, such that when the slave enable is held high, the masters store on the rising clock and the slaves store on a falling clock thus producing normal master slave operation. If the slave enable is held low the slave flip flops are continuously enabled allowing immediate transfer of information from the master flip flops to the output.



CHARACTERISTICS

TYPICAL DELAY	CP to Z 35 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	265 mW

PIN NAMES		LOADING
A_0, A_1, A_2	Write Address Inputs	2/3 UL
D_A	Data Input	2/3 UL
B_0, B_1, B_2	B Read Address Inputs	2/3 UL
Z_B	B Output	10 UL
C_0, C_1, C_2	C Read Address Inputs	2/3 UL
Z_C	C Output	10 UL
CP	Clock Active High Going Edge Input	2/3 UL
$\overline{SLE}$	Slave Enable (Active Low) Input	2/3 UL

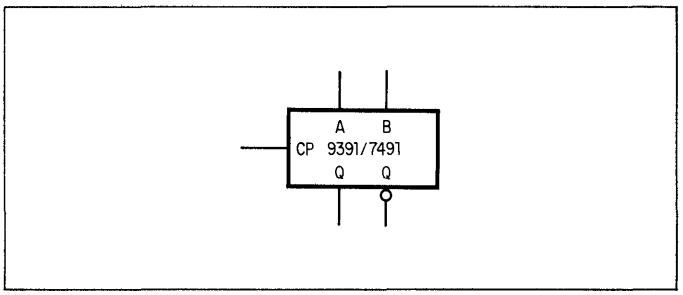


9391/5491,7491
8-BIT SHIFT REGISTER

DESCRIPTION The 9391/5491, 7491 is a serial-in, serial-out, 8-bit shift register utilizing transistor-transistor logic (TTL) circuits, and is composed of eight R-S master-slave flip-flops, input gating, and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and a full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B, and CP) appear as only one TTL input load.

The clock pulse inverter/driver causes these circuits to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with other edge-triggered synchronous functions.



TRUTH TABLE

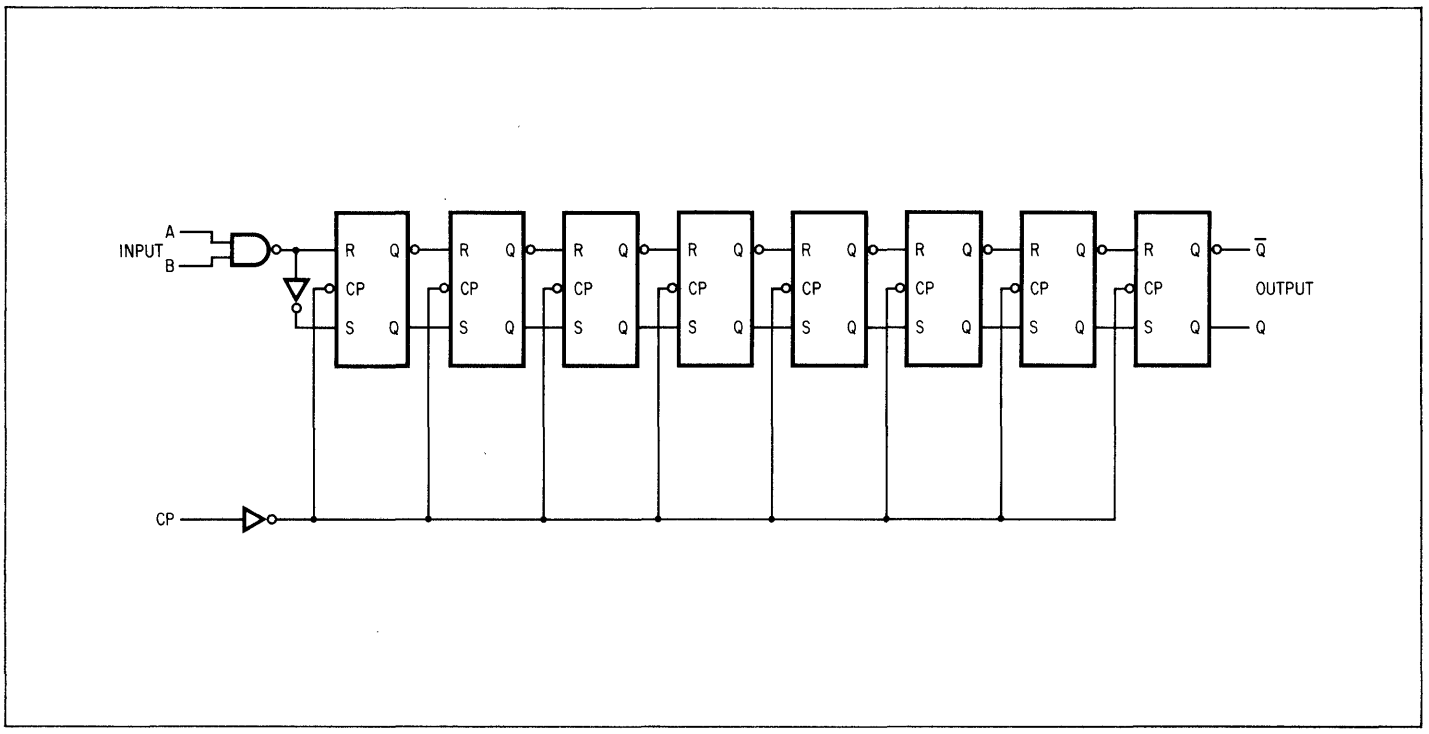
t_n		$t_n + 8$
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES:
1. t_n = bit time before clock.
2. tn + 8 = bit time after 8 clock pulses

PIN NAMES		LOADING
A, B	Data Inputs	1 UL
C_P	Clock Input	1 UL
$\overline{Q}$	Complementary Data Output	10 UL
Q	Data Output	10 UL

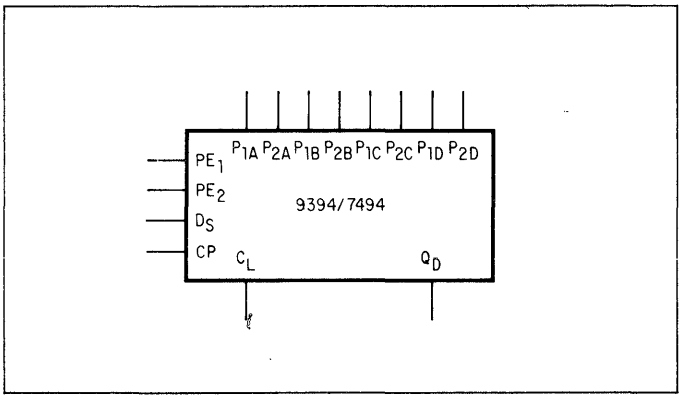
CHARACTERISTICS

SHIFT FREQUENCY	18 MHz
POWER DISSIPATION	175 mW
PACKAGE	14 Pin DIP (6A) and Flat Pack (3I)



9394/5494,7494
4-BIT SHIFT REGISTER

DESCRIPTION The 9394/5494, 7494 shift register is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.



All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

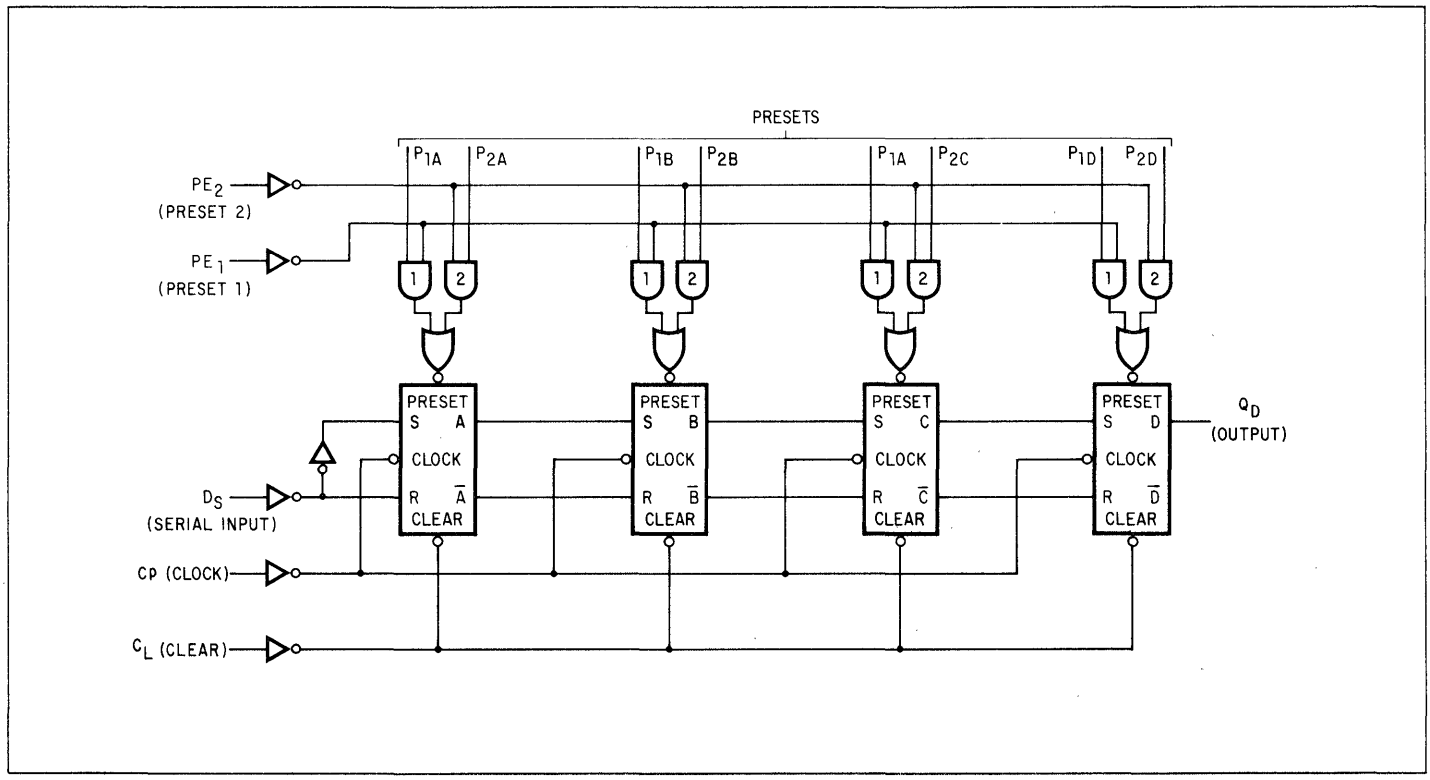
The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs P_{1A} through P_{1D} are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs P_{2A} through P_{2D} are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input and either preset 1 or preset 2 must be at a logical 0 when clocking occurs.

PIN NAMES		LOADING
P_{1A} - P_{2D}	Preset Inputs	1 UL
PE_1	Preset 1 Input	4 UL
PE_2	Preset 2 Input	4 UL
D_S	Serial Data Inputs	1 UL
CP	Clock Input	1 UL
C_L	Clear Input	1 UL
Q_D	Serial Data Output	10 UL

CHARACTERISTICS

CLOCK FREQUENCY	15 MHz
PROPAGATION DELAY (CP to Q_D)	25 ns
POWER DISSIPATION	175 mW
PACKAGE	16 Pin DIP (6B)



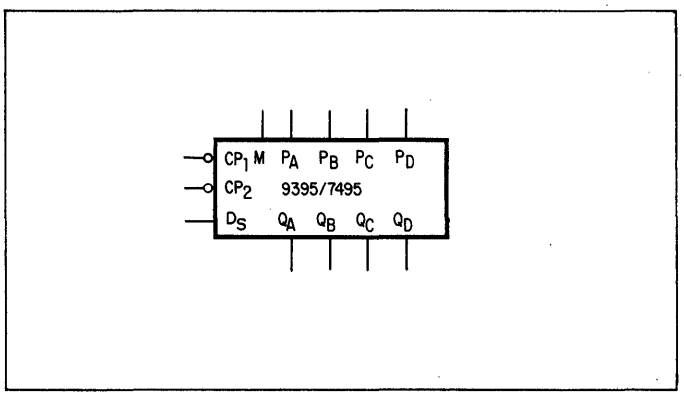
9395/5495,7495
4-BIT(RIGHT/LEFT)SHIFT REGISTER

DESCRIPTION This monolithic shift register is composed of four R-S master-slave flip-flops. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs P_A through P_D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs P_A through P_D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input P_C and etc.), and serial data is entered at input P_D

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

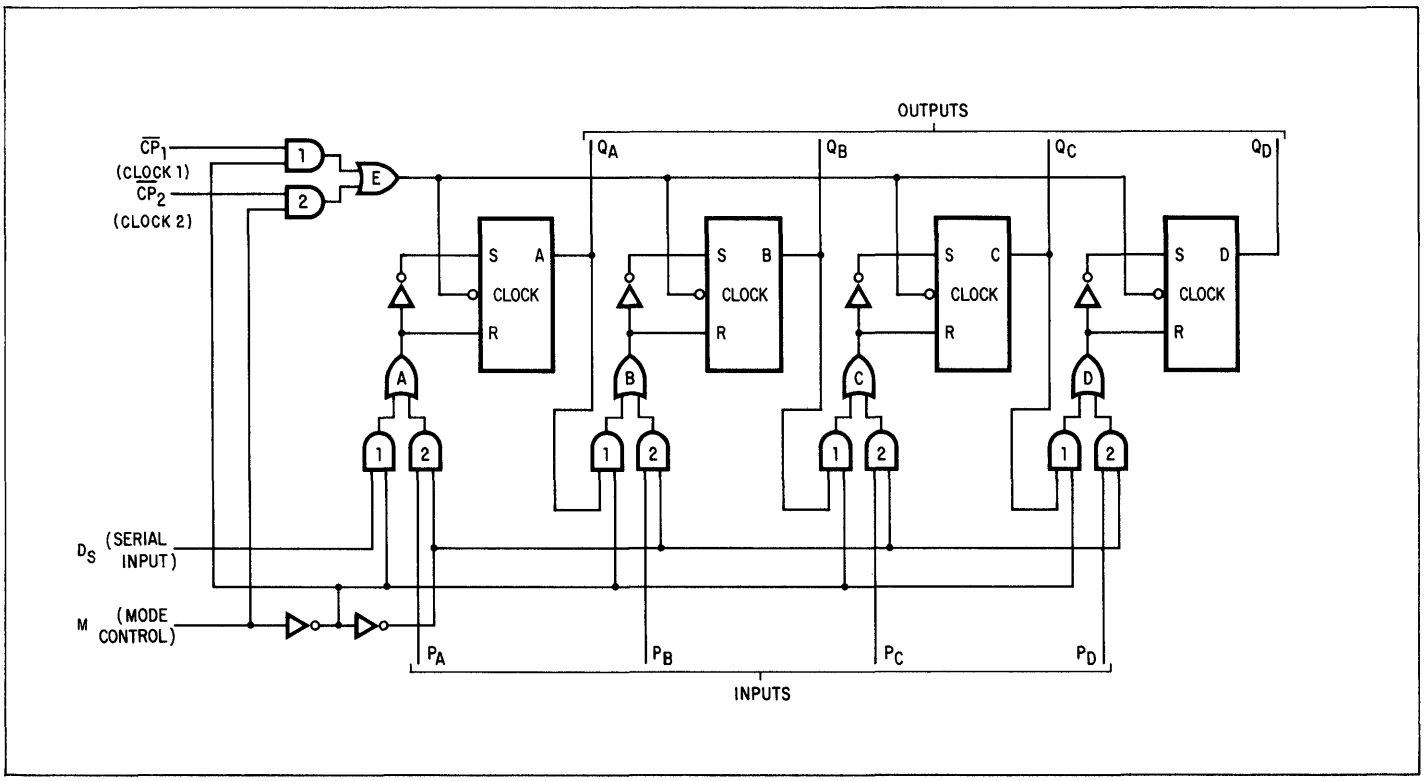


PIN NAMES **LOADING**

$\overline{CP}_1$	Clock 1 Input	1 UL
$\overline{CP}_2$	Clock 2 Input	1 UL
M	Mode Control Input	2 UL
P_A,P_B, P_C, P_D	Parallel Data Inputs	1 UL
Q_A, Q_B, Q_C, Q_D	Parallel Data Outputs	10 UL
D_S	Serial Data Input	1 UL

CHARACTERISTICS

CLOCK FREQUENCY	31 MHz
PROPAGATION DELAY ($\overline{CP}$ to Q)	25 ns
POWER DISSIPATION	250 mW
PACKAGE	14 Pin DIP (6A)



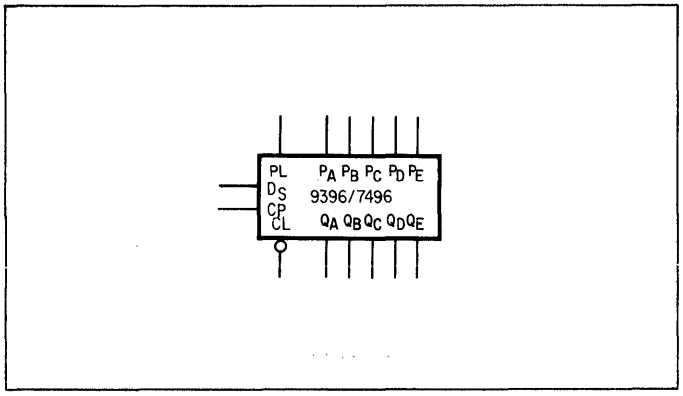
9396/5496,7496
5-BIT SHIFT REGISTER

DESCRIPTION The 9396/5496, 7496 consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common parallel load input. The common parallel load input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Parallel load is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

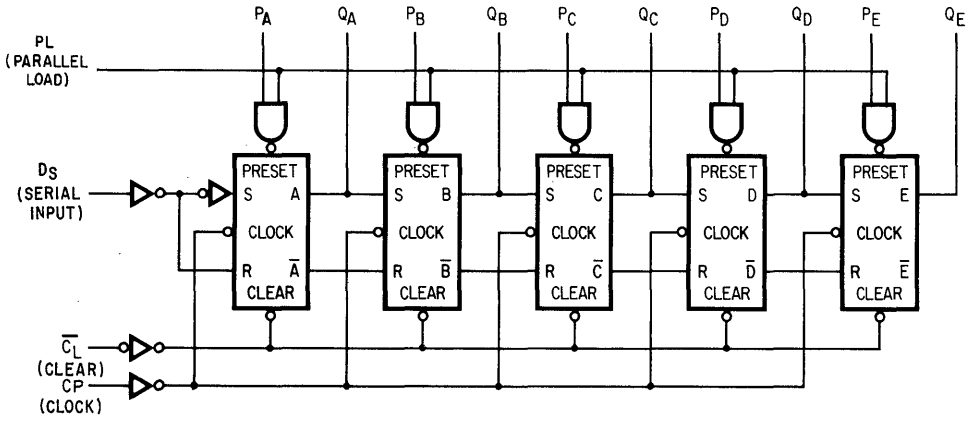


PIN NAMES

		LOADING
PL	Parallel Load Input	5 UL
P_A, P_B, P_C, P_D, P_E	Parallel Data Inputs	1 UL
D_S	Serial Data Input	1 UL
CP	Clock Input	1 UL
$\overline{C}_L$	Clear Input	1 UL
Q_A, Q_B, Q_C, Q_D, Q_E	Parallel Data Outputs	10 UL

CHARACTERISTICS

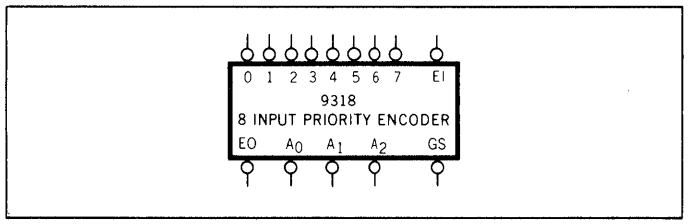
CLOCK FREQUENCY	15 MHz
PROPAGATION DELAY (CP to Q)	25 ns
POWER DISSIPATION	240 mW
PACKAGE	16 Pin DIP (7B)



9318 8-INPUT PRIORITY ENCODER

DESCRIPTION The 9318 is a multipurpose encoder designed to accept 8 active low inputs and produce a binary weighted output code of the highest order input. A priority is assigned to each active low input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input 7 having the highest priority.

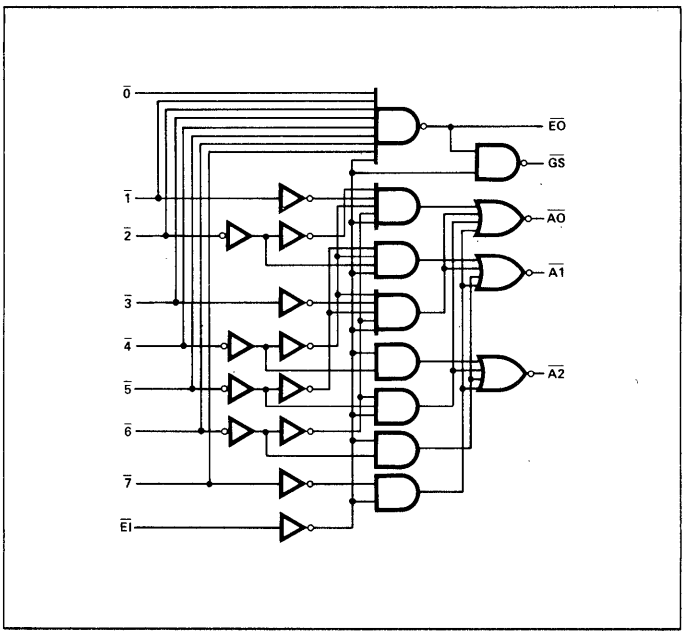
An active low enable input ($\overline{EI}$) and active low enable output ($\overline{EO}$) are provided to expand priority encoding to more inputs. This is accomplished by connecting the more significant encoders enable output ($\overline{EO}$) to the next less significant encoder enable input ($\overline{EI}$). In addition a group signal is provided which is active if any input is active and $\overline{EI}$ is low.



PIN NAMES		LOADING
$\overline{0}$	Priority (Active Low) Input	1 UL
$\overline{1}$ to $\overline{7}$	Priority (Active Low) Inputs	2 UL
$\overline{EI}$	Enable (Active Low) Input	2 UL
$\overline{EO}$	Enable (Active Low) Output	5 UL
$\overline{GS}$	Group Select (Active Low) Output	6 UL
$\overline{A_0}$, $\overline{A_1}$, $\overline{A_2}$	Address (Active Low) Outputs	10 UL

CHARACTERISTICS

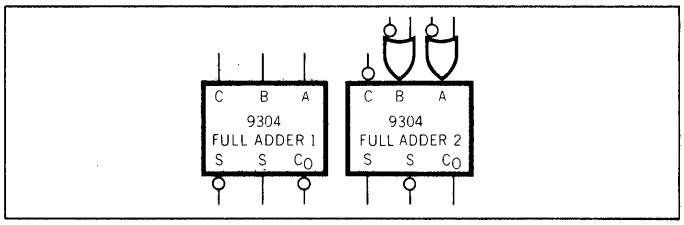
TYPICAL DELAY	$\overline{1}$ to $\overline{A}$ 25 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	250 mW



9304 DUAL FULL ADDER

DESCRIPTION The 9304 consists of two separate high speed binary full adders. The adders are useful in a wide variety of applications including multiple bit parallel add ripple carry addition, parity generation and checking, code conversion, and majority gating. Each adder has the sum and its complement and carry as outputs. Single inversion circuitry is used in the carry logic to provide very low carry through delay (typically 8 ns). The second adder has provisions for either active high or active low inputs at the A and B Operand Inputs.

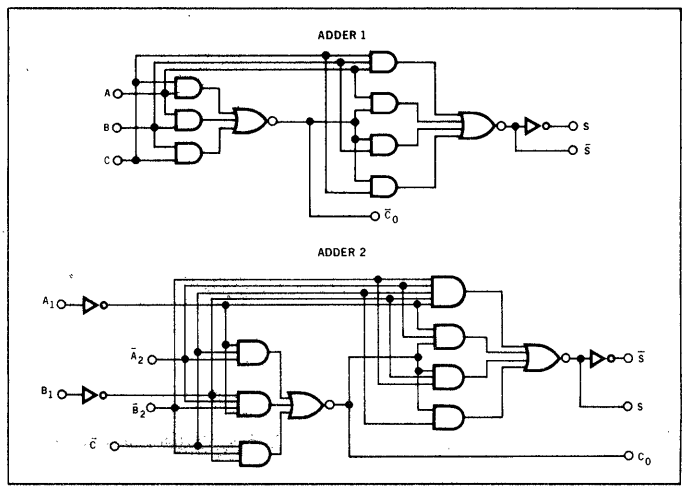
The adders produce a low carry and both low and high sum with active high inputs, or active high carry and both high and low sum when active low inputs are used. This allows two representations of the logic function which are shown below.



PIN NAMES		LOADING
FULL ADDER 1		
A, B	Operand Inputs	4 UL
C	Carry Input	4 UL
S	Sum Output	10 UL
$\overline{S}$	Complementary Sum Output	9 UL
$\overline{C}_O$	Carry (Active Low) Output	7 UL
FULL ADDER 2		
A_I	OR Operand (Active High) Input	1 UL
$\overline{A_2}$	OR Operand (Active Low) Input	4 UL
B_I	OR Operand (Active High) Input	1 UL
$\overline{B_2}$	OR Operand (Active Low) Input	4 UL
$\overline{C}$	Carry (Active Low) Input	4 UL
S	Sum Output	9 UL
$\overline{S}$	Complementary Sum Output	10 UL
C_O	Carry (Active High) Output	7 UL

CHARACTERISTICS

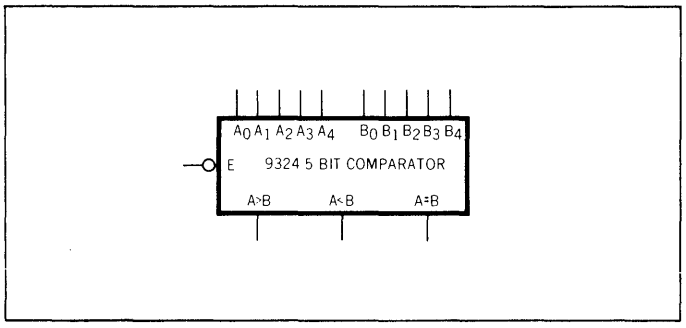
TYPICAL DELAYS	A to $\overline{S}$	26 ns
	A to $\overline{C}_O$	8 ns
PACKAGE	16 Pin Dip (6B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	150 mW	



9324
5-BIT COMPARATOR

DESCRIPTION The 9324 is a high speed expandable comparator which provides comparison between two 5-bit words and gives three outputs, "less than," "greater than," and "equal to." A high level on the active low enable input forces all three outputs low.

Words of more than 5 bits may be compared by either connecting 9324 comparators in series; this is done by connecting the A>B and A<B outputs to the A_0, B_0 inputs respectively of the next stage, or by connecting comparators in parallel, and comparing the outputs with another 9324.



TRUTH TABLE

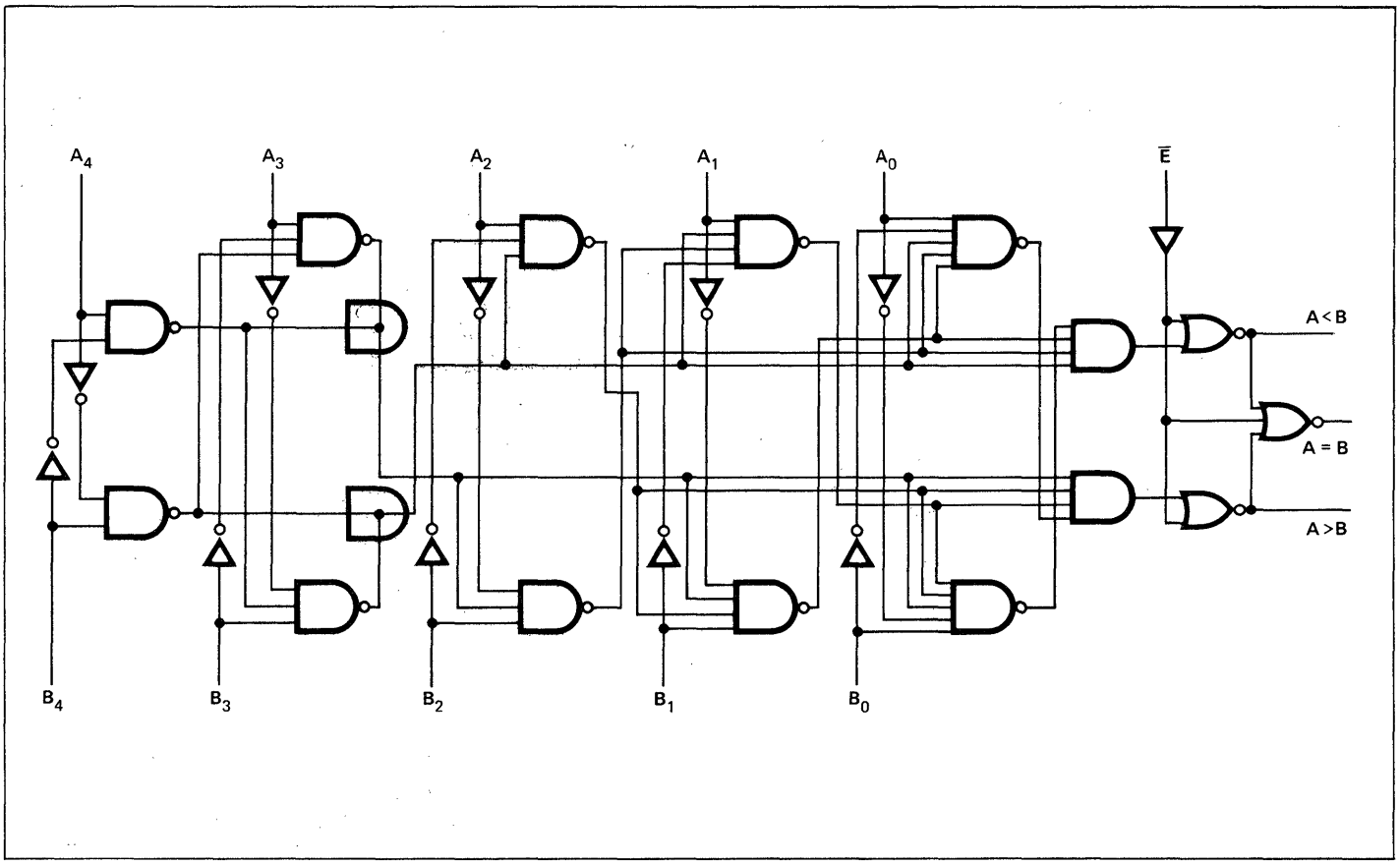
$\bar{E}$	A B	A < B	A > B	A = B
H	X X	L	L	L
L	Word A = Word B	L	L	H
L	Word A > Word B	L	H	L
L	Word B > Word A	H	L	L

L = Low voltage level
H = High voltage level
X = Either high or low voltage level

PIN NAMES		LOADING
$\bar{E}$	Enable (Active Low) Input	2 UL
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	2 UL
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	2 UL
A < B	A Less than B Output	9 UL
A > B	A Greater Than B Output	9 UL
A = B	A Equal to B Output	10 UL

CHARACTERISTICS

TYPICAL DELAY	Data to A > B 20 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	210 mW

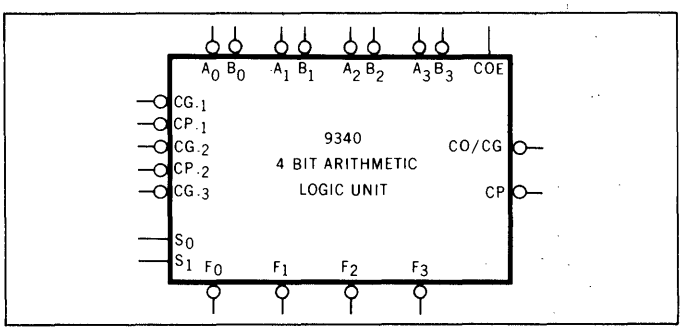


9340
4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION The 9340 is a high-speed arithmetic logic unit which can perform the arithmetic operations add and subtract on two 4-bit parallel binary words which are represented in 1's, 2's complement or sign magnitude notation. The unit can also perform two logic functions, the actual functions depending upon the polarity of the input operands. These functions, which are controlled by two select inputs, S_0, S_1, are shown for active low input operands below.

The 9340 incorporates full carry lookahead internally for the 4 bits and provision for external lookahead by using the carry lookahead functions $\overline{CP}$ (carry propagate) and $\overline{CG/CO}$ (carry generate/carry out). The input carry network enables full external carry lookahead over 16 bits and provides for rippling between additional blocks of 12 bits, without additional gates or special carry lookahead IC's. This ripple block method is operated under control of a COE (carry out enable) input which changes the carry generate into a carry out signal. The delay for various word lengths using the built-in carry lookahead circuitry is given below. If a faster arithmetic unit is required, the 9342 carry lookahead circuit can be used together with the internal circuitry to provide lookahead over blocks.

The $\overline{CP}$ (carry propagate) and $\overline{CG}$ (carry generate) functions can also be used with appropriate gating to give all 0's and all 1's detection, and generate functions A > B, A ≥ B, and overflow indication.



PIN NAMES

		LOADING
$\overline{A}_0$, to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand (Active Low) Inputs	3 UL
S_0, S_1	Mode Select Inputs	1 UL
$\overline{CG}_{-1}$	First Stage Carry Generate (Active Low) Input	3 UL
$\overline{CP}_{-1}$	First Stage Carry Propagate (Active Low) Input	1 UL
$\overline{CG}_{-2}$	Second Stage Carry Generate (Active Low) Input	2 UL
$\overline{CP}_{-2}$	Second Stage Carry Propagate (Active Low) Input	1 UL
$\overline{CG}_{-3}$	Third Stage Carry Generate (Active Low) Input	1 UL
COE	Carry Out Enable Input	1.5 UL
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$	Function (Active Low) Outputs	10 UL
$\overline{CO/CG}$	Carry Out/Carry Generate (Active Low) Output	10 UL
$\overline{CP}$	Carry Propagate (Active Low) Output	10 UL

FUNCTION TABLE ACTIVE LOW OPERANDS

S_0	S_1	FUNCTION	
L	L	A SUBTRACT	B
H	L	A ADD	B
L	H	A EX OR	B
H	H	A AND	B

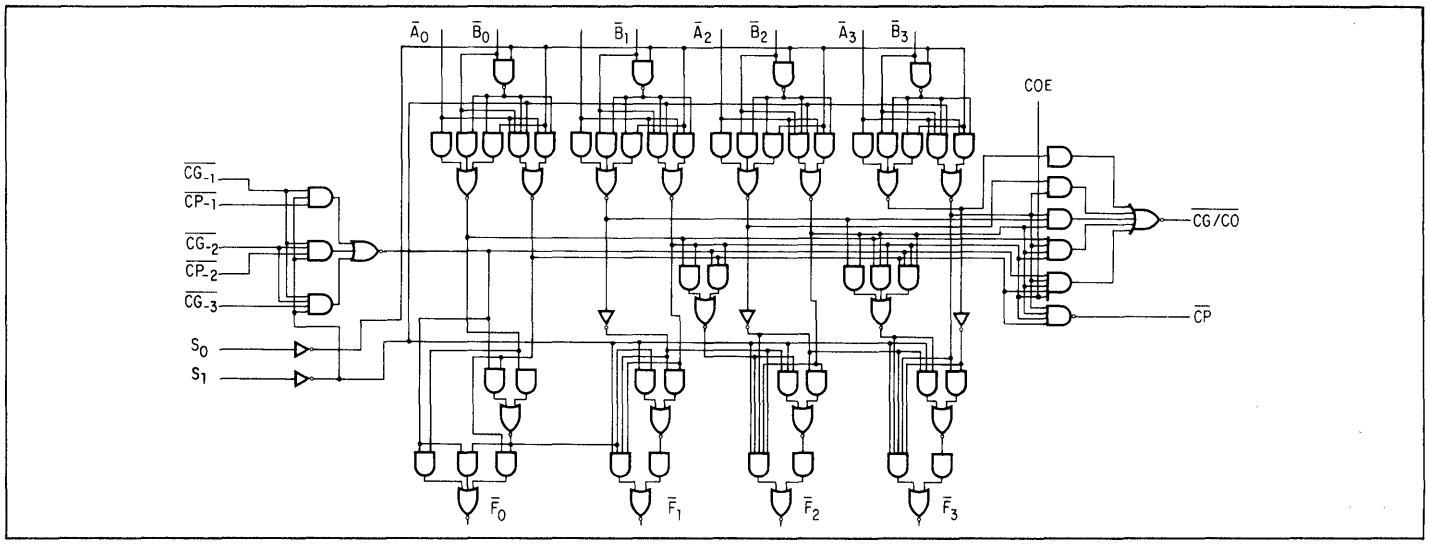
H = High Voltage Level
L = Low Voltage Level

DELAY TABLE

WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1–4	28	35
5–16	42	49
17–28	56	63
29–40	70	77
41–52	84	91
53–64	98	105
65–76	112	119
77–88	126	133
89–100	140	147

CHARACTERISTICS

TYPICAL DELAYS Addition Over 4 Bits 28 ns
Addition Over 16 Bits 42 ns
PACKAGE 24 Pin Dip (6N) or Flat Pack (4M)
TYPICAL POWER DISSIPATION 400 mW



9341/54181,74181
4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION The 9341 is a 4-bit high-speed arithmetic logic unit which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations; the most important being add and subtract.

Logic and arithmetic operations can be performed for both active low and active high operands. The function table shows all possible logic operations for active low and active high operands and shows arithmetic operations without a carry in for active low and active high operands. When a carry in is supplied, a one is added to all arithmetic terms. For example, A minus B minus 1 without a carry in becomes A minus B (2's complement subtraction) with a carry in.

Operation selection is under control of four select lines, S_0–S_3, and an active low carry enable line. When the internal carries are enabled, the device performs arithmetic operations; when the carries are inhibited, logic operations results. Thus arithmetic operations are on a word basis while logic operations are on a bit basis.

The 9341 incorporates full carry lookahead internal to the 4 bits and provision is made for carry lookahead by generation of the signals $\overline{P}$ (carry propagate) and $\overline{G}$ (carry generate). When speed requirements are not stringent, the 9341 can be used in a simple ripple carry mode by connecting the carry out signal to the carry input of the next 4-bit unit. For high-speed operation the 9341 is used in conjunction with the 9342 carry lookahead circuit. One carry lookahead package is required for each group of four 9341 devices. Carry lookahead can be provided at various levels thus providing high-speed capability at extremely long word lengths.

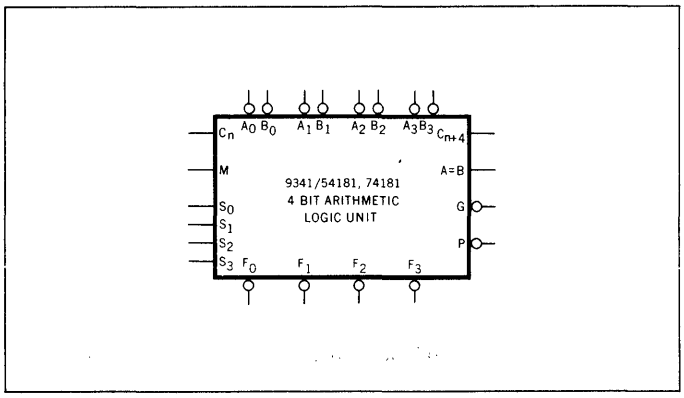
A signal is provided from the 9341 which indicates logic equivalence over 4 bits when the unit is in the subtract mode. This signal can be used together with the carry out signal to indicate A > B, A = B.

FUNCTION TABLE

MODE SELECT INPUTS S_3 S_2 S_1 S_0	ACTIVE LOW INPUTS & OUTPUTS LOGIC (M = H)	ACTIVE LOW INPUTS & OUTPUTS ARITHMETIC (M = L) (C_n = H)	ACTIVE HIGH INPUTS & OUTPUTS LOGIC (M = H)	ACTIVE HIGH INPUTS & OUTPUTS ARITHMETIC (M = L) (C_n = L)
L L L L	$\overline{A}$	A minus 1	$\overline{A}$	A
L L L H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L L H L	$\overline{A}+B$	$A\overline{B}$ minus 1	AB	$A+\overline{B}$
L L H H	Logical 1	minus 1 (2's complement)	Logical 0	minus 1 (2's complement)
L H L L	$\overline{A+B}$	A plus $[A+\overline{B}]$	$\overline{AB}$	A plus $A\overline{B}$
L H L H	B	AB plus $[A+\overline{B}]$	$\overline{B}$	$[A+B]$ plus $A\overline{B}$
L H H L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L H H H	$A+B$	$A+\overline{B}$	$A\overline{B}$	AB minus 1
H L L L	$\overline{A}B$	A plus $[A+B]$	$\overline{A+B}$	A plus AB
H L L H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H L H L	B	$A\overline{B}$ plus $[A+B]$	B	$[A+B]$ plus AB
H L H H	$A+B$	$A+B$	AB	AB minus 1
H H L L	Logical 0	A plus A*	Logical 1	A plus A*
H H L H	$A\overline{B}$	AB plus A	$A+\overline{B}$	$[A+B]$ plus A
H H H L	AB	$A\overline{B}$ plus A	$A+B$	$[A+B]$ plus A
H H H H	A	A	A	A minus 1

*Each bit is shifted to the next more significant position

H = High Voltage Level
L = Low Voltage Level

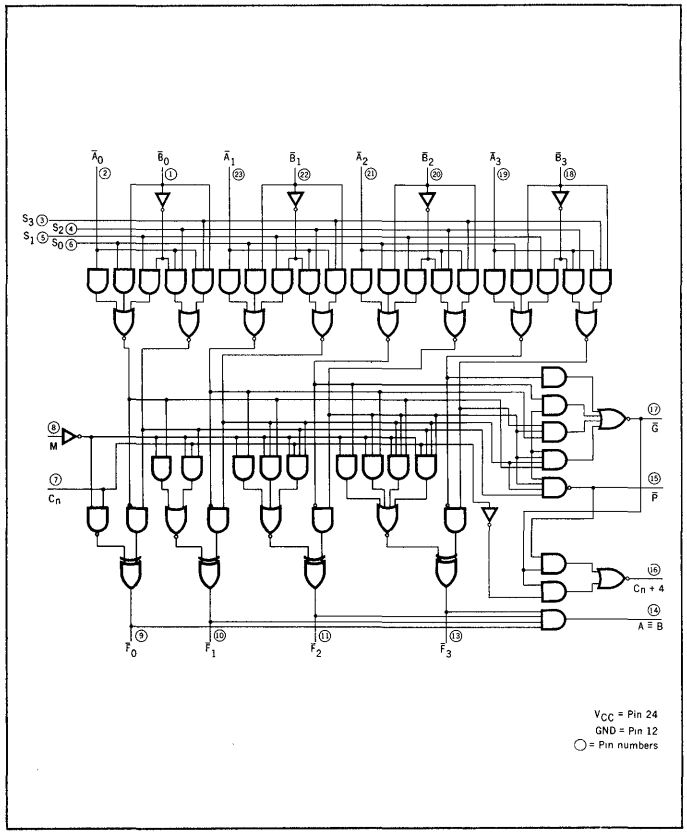


PIN NAMES		LOADING
$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$	Operand (Active Low) Inputs	3 UL
S_0, S_1, S_2, S_3	Function Select Inputs	4 UL
C_n	Carry Input	5 UL
M	Mode Control Input	1 UL
C_{n+4}	Carry Output	10 UL
$\overline{G}$	Carry Generate (Active Low) Output	10 UL
$\overline{P}$	Carry Propagate (Active Low) Output	10 UL
A = B	Comparator Output	O.C.
$\overline{F}_0$, $\overline{F}_1$, $\overline{F}_2$, $\overline{F}_3$	Function (Active Low) Outputs	10 UL

O.C. = Open Collector Output.

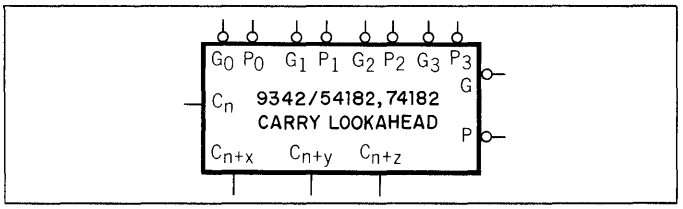
CHARACTERISTICS

TYPICAL DELAYS	Addition Over 4 Bits 24 ns Addition Over 16 Bits 36 ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)
TYPICAL POWER DISSIPATION	450 mW



9342/54182,74182 CARRY LOOKAHEAD

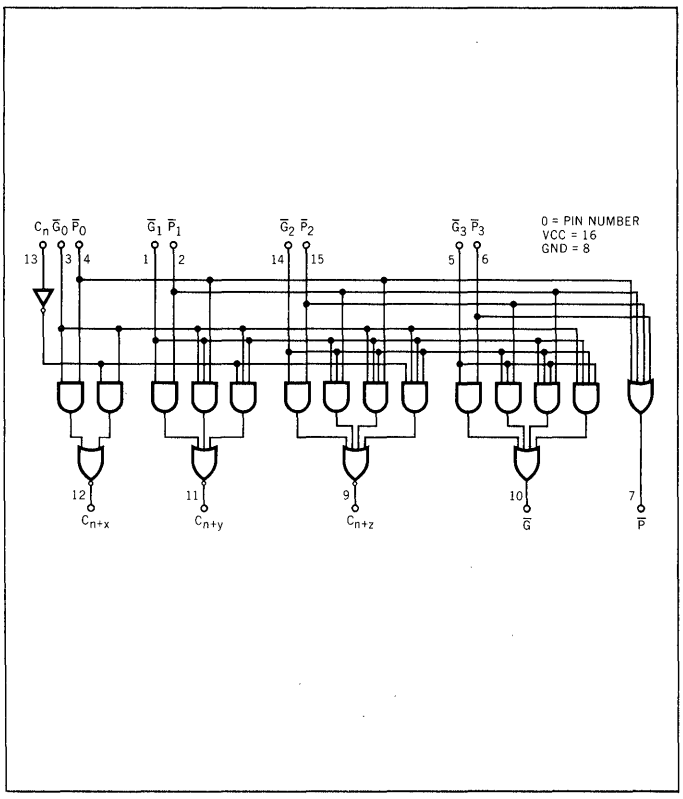
DESCRIPTION The 9342/54182, 74182 is a carry lookahead circuit for use with the 9340 or 9341 arithmetic logic units. The device accepts an active high carry in, active low carry propagate, and an active low carry generate signals from four arithmetic logic units. The outputs from the circuit are the three carry out signals required for arithmetic lookahead operation and the next level carry generate and carry propagate signals. The 9342 allows extremely high-speed arithmetic operations to be performed on long word lengths.



PIN NAMES		LOADING
C_N	Carry Input	2 UL
$\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$	Carry Generate (Active Low) Inputs	9, 10, 9, 5 UL
$\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$	Carry Propagate (Active Low) Inputs	5, 5, 4, 3 UL
$C_{n+x}, C_{n+y}, C_{n+z}$	Carry Outputs	10 UL
$\overline{G}$	Carry Generate (Active Low) Output	10 UL
$\overline{P}$	Carry Propagate (Active Low) Output	10 UL

CHARACTERISTICS

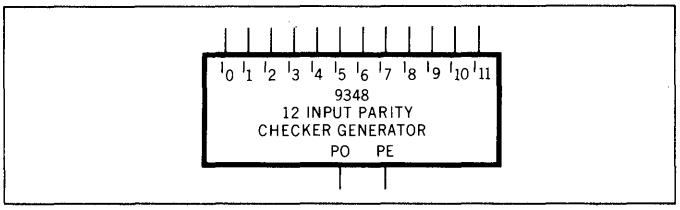
TYPICAL DELAYS	C_n to C_{n+x}	12 ns
	$\overline{P}_0$ to C_{n+x}	8 ns
PACKAGE	16 Pin Dip (6B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	180 mW	



9348 12-INPUT PARITY CHECKER/GENERATOR

DESCRIPTION The 9348 is a 12 input parity checker/generator generating odd and even parity outputs. It can be used in high speed error detection applications.

The even parity output will be high if an even number of logic ones are present on the inputs. The odd parity output will be high if an odd number of logic ones are present on the inputs.



PIN NAMES		LOADING
I_0 to I_{11}	Parity Inputs	2 UL
P_O	Odd Parity Output	10 UL
P_E	Even Parity Output	10 UL

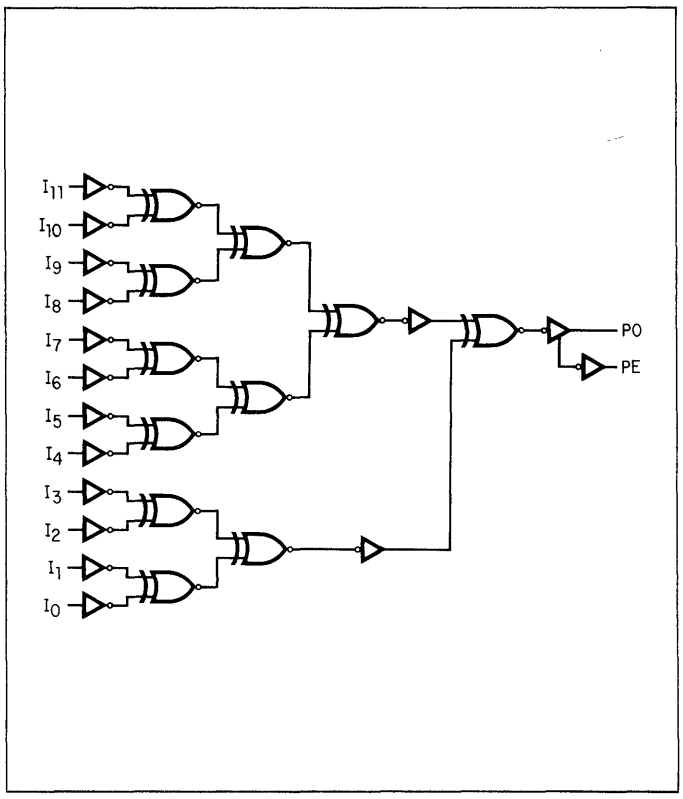
CHARACTERISTICS

TYPICAL DELAYS	I to P_E	44 ns
	I to P_O	38 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	270 mW	

LOGIC EQUATIONS

$$P_O = I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}$$

$$P_E = \overline{I_0 \oplus I_1 \oplus I_2 \oplus I_3 \oplus I_4 \oplus I_5 \oplus I_6 \oplus I_7 \oplus I_8 \oplus I_9 \oplus I_{10} \oplus I_{11}}$$

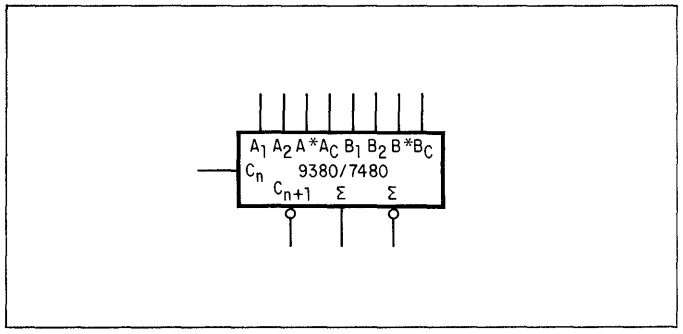


9380/5480,7480
GATED FULL ADDER

DESCRIPTION The 9380/7480 is a high-speed, single-bit, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs, and inverted carry output.

Designed for medium- to high-speed, multiple-bit parallel-add/serial-carry applications, the circuit utilizes diode transistor logic for the gated inputs and high speed, high fan-out transistor-transistor logic for the sum and carry outputs.

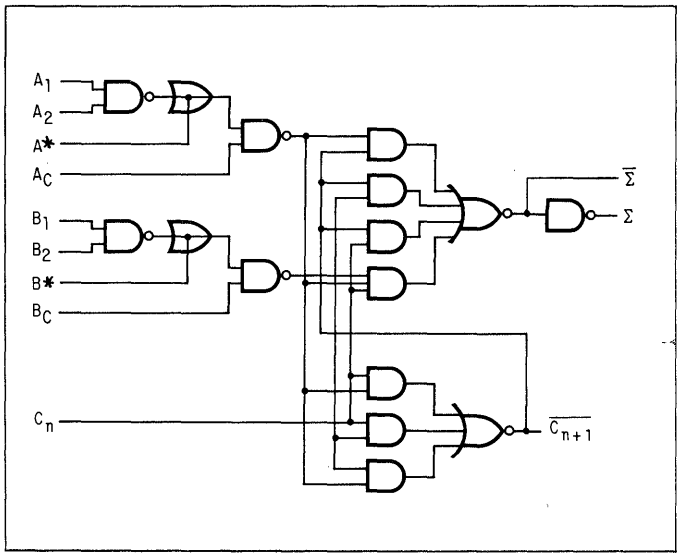
A single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuitry.



PIN NAMES		LOADING
A_1, A_2, B_1, B_2	Non Inverting Data Inputs	1 UL
A*, B*	Inverting Data Inputs	1.65 UL
A_C, B_C	Control Inputs	1 UL
C_n	Carry Input	5 UL
$\overline{C_{n+1}}$	Carry Output	5 UL
Σ, $\overline{\Sigma}$	Sum Outputs	10 UL
A*, B*	When Used as Outputs	3 UL

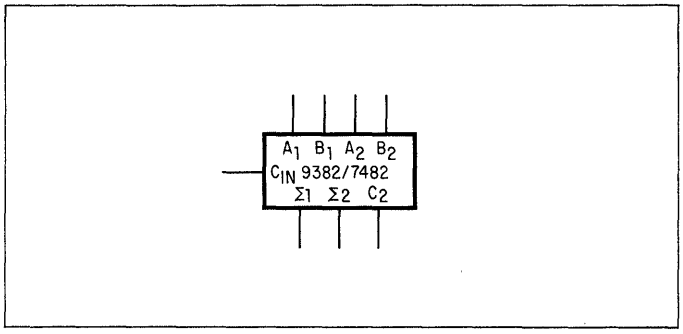
CHARACTERISTICS

PROPAGATION DELAY (B_C to Σ)	47 ns
POWER DISSIPATION	105 mW
PACKAGE	14 Pin DIP (6A) and Flat Pack (3I)



9382/5482,7482
2-BIT FULL ADDER

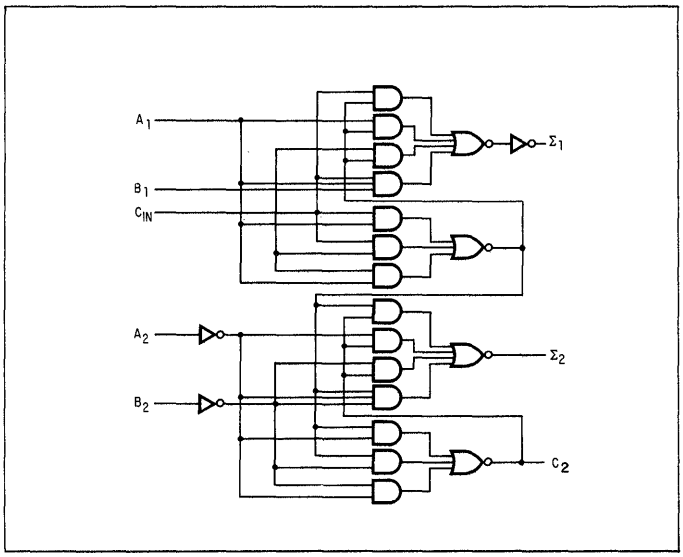
DESCRIPTION This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.



PIN NAMES		LOADING
A_1, B_1	Data Inputs	4 UL
A_2, B_2	Data Inputs	1 UL
C_{IN}	Carry Input	4 UL
Σ_1	Sum Output Bit 1	10 UL
Σ_2	Sum Output Bit 2	10 UL
C_2	Carry Output Bit 2	5 UL

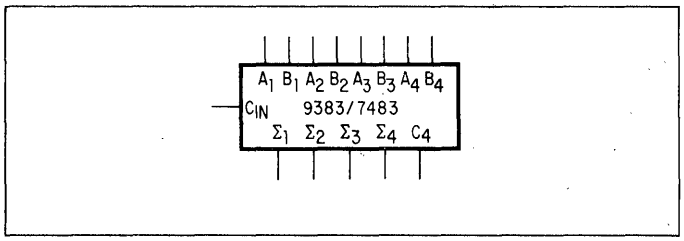
CHARACTERISTICS

PROPAGATION DELAY (B_2 to Σ_2)	38 ns
POWER DISSIPATION	176 mW
PACKAGE	14 Pin DIP (6A) and Flat Pack (3I)



9383/5483,7483
4-BIT FULL ADDER

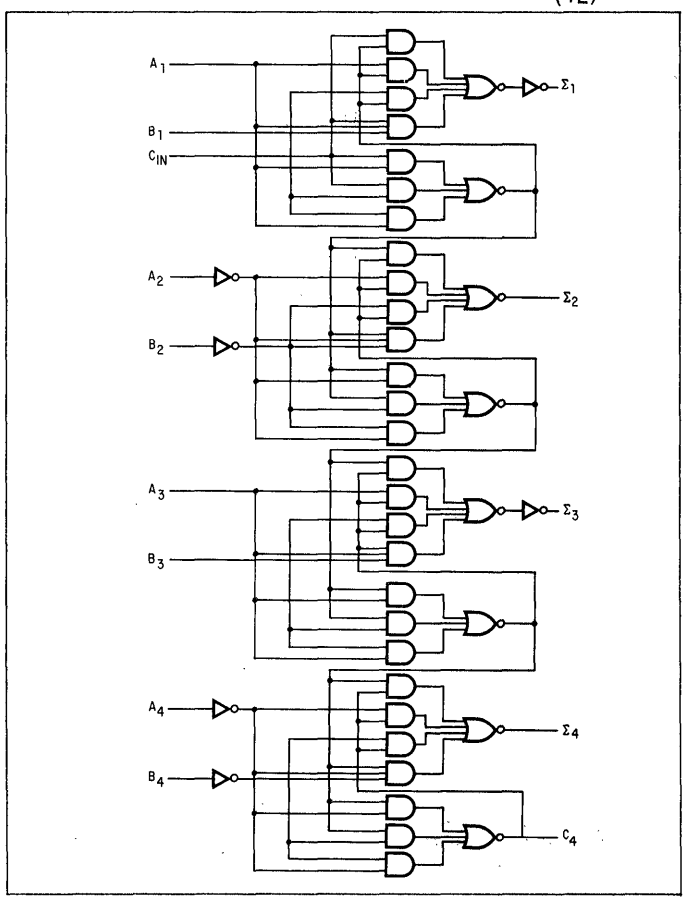
DESCRIPTION The 9383/5483, 7483 full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed high fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.



PIN NAMES		LOADING
A_1, B_1, A_3, B_3	Data Inputs	4 UL
A_2, B_2, A_4, B_4	Data Inputs	1 UL
C_{IN}	Carry Input	4 UL
Σ_1, Σ_2, Σ_3, Σ_4	Sum Outputs	10 UL
C_4	Carry Out Bit 4	5 UL

CHARACTERISTICS

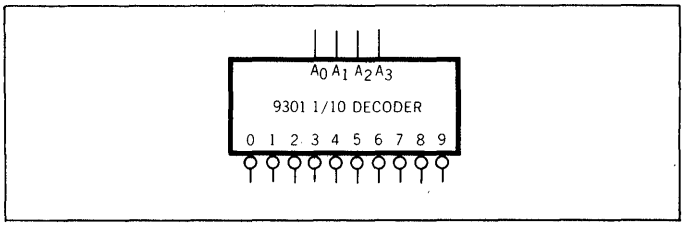
PROPAGATION DELAY (A_2 to Σ_3)	37 ns
POWER DISSIPATION	390 mW
PACKAGE	16 Pin DIP (6B) Flat Pack (4L)



9301
ONE OF TEN DECODER

DESCRIPTION The 9301 accepts four binary weighted inputs and provides one of ten mutually exclusive active low outputs. When a binary code greater than nine is applied, all outputs are high. This facilitates BCD to decimal conversions and eight channel demultiplexing and decoding. The active low decoder outputs are compatible with the low enables of other MSI elements making the 9301 useful in logic selection schemes.

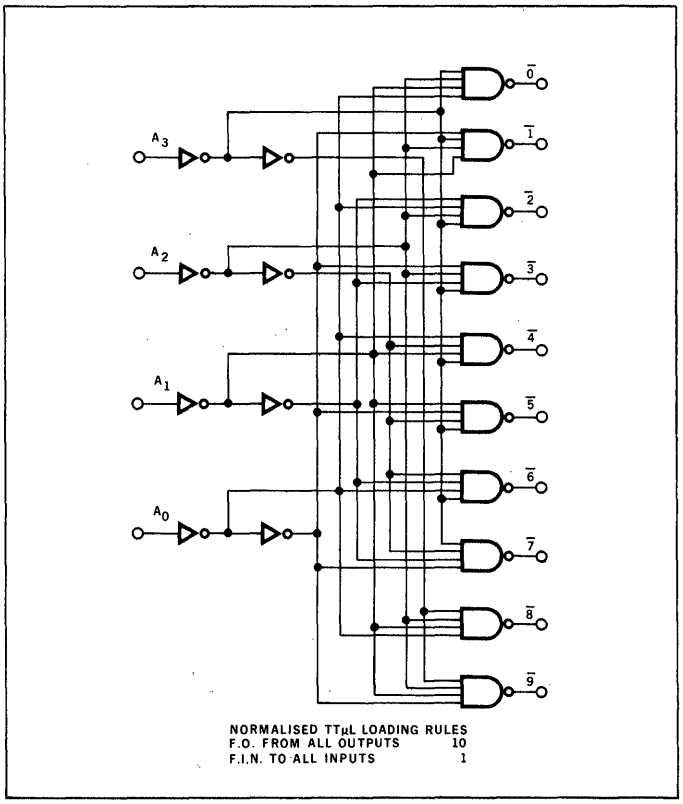
The 9301 can serve as a one of eight decoder with an active low enable, the A_3 input acting as the active low enable. Eight channel demultiplexing results when data is applied to the A_3 input and the desired output is addressed by A_0, A_1, A_2.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{0}$ to $\overline{9}$	Outputs (Active Low)	10 UL

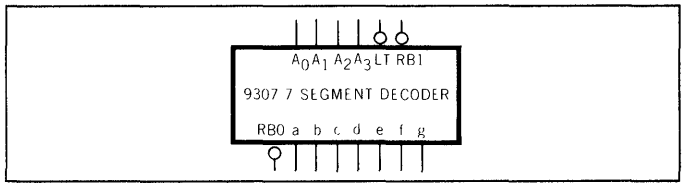
CHARACTERISTICS

TYPICAL DELAY	A to Output 22 ns
PACKAGE	16 Pin Dip (7B) and Flat Pack (4L)
TYPICAL POWER DISSIPATION	145 mW



9307
SEVEN-SEGMENT DECODER

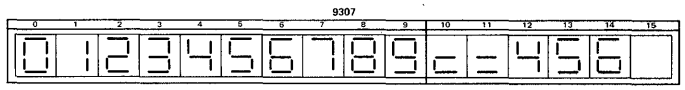
DESCRIPTION The 9307 is a seven segment decoder designed to accept a 4 bit BCD 8421 code input and provide the appropriate outputs for a seven segment numerical display. The decoder can be used with seven segment incandescent lamp, neon, electro-luminescent, or crt displays. The segments and numeric designations chosen to represent the decimal numbers are shown below, together with the resulting displays for input code configuration in excess of binary nine. The decoder outputs are active high so that a buffer transistor may be used directly to provide the high current required for incandescent displays.

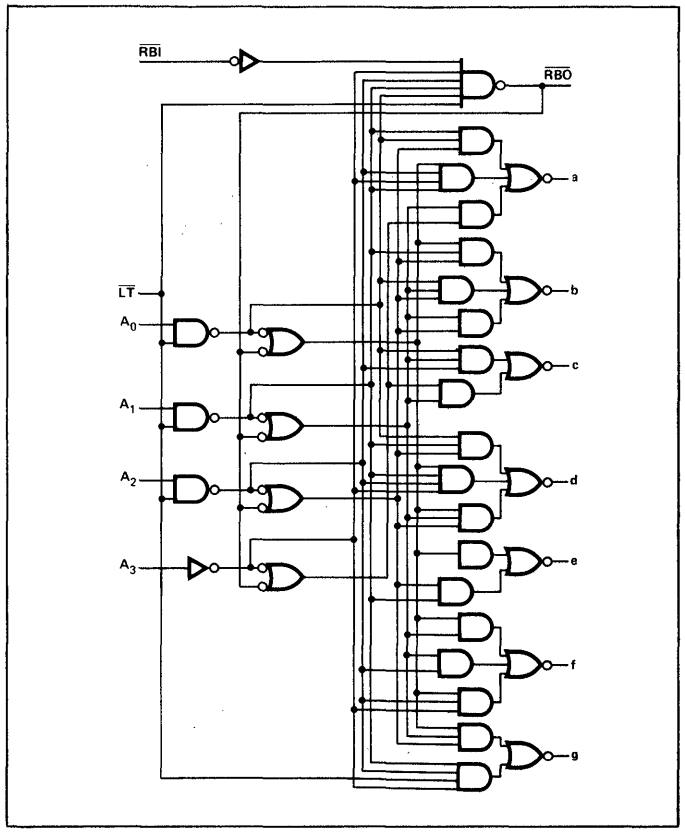


PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{LT}$	Lamp Test (Active Low) Input	4 UL
$\overline{RBI}$	Ripple Blanking (Active Low) Input	0.5 UL
$\overline{RBO}$	Ripple Blanking (Active Low) Output	1.5 UL
a, b, c, d, e, f, g	(Active High) Outputs	7 UL

CHARACTERISTICS

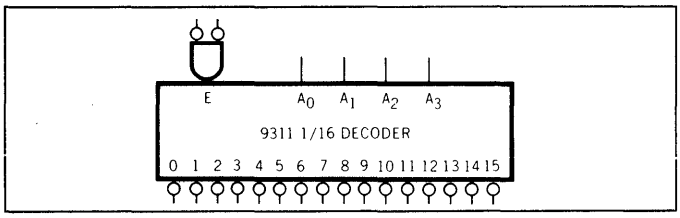
TYPICAL DELAY	A to Output 250 ns
PACKAGE	16 Pin Dip (6B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	165 mW





9311
ONE OF SIXTEEN DECODER

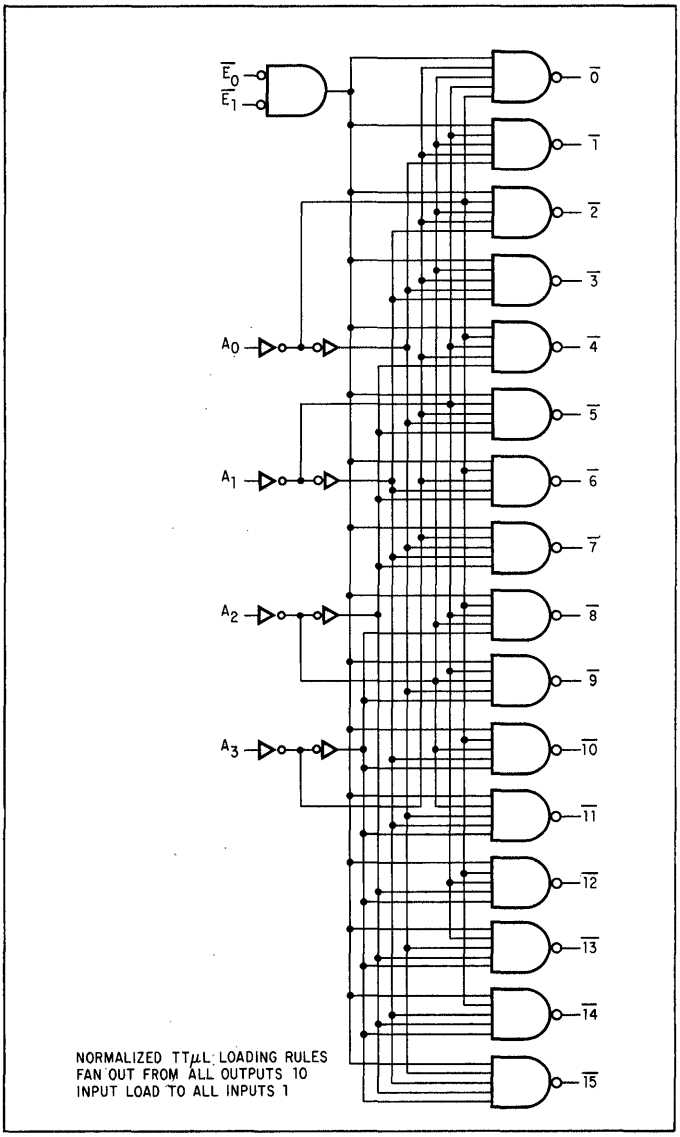
DESCRIPTION The 9311 one of sixteen decoder accepts four binary weighted inputs and provides one low output corresponding to the input code.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{E_0}$, $\overline{E_1}$	AND Enable (Active Low) Inputs	1 UL
$\overline{0}$ to $\overline{15}$	(Active Low) Outputs	10 UL

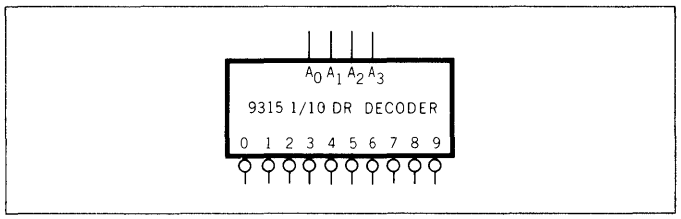
CHARACTERISTICS

TYPICAL DELAYS	A to Output 21 ns $\overline{E}$ to Output 17 ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)
TYPICAL POWER DISSIPATION	175 mW



9315/7441 ONE OF TEN DECODER/DRIVER

DESCRIPTION The 9315 is a one of ten decoder driver which is capable of driving all available cold cathode indicator tubes having 7 mA or less cathode current. It accepts BCD 8421 code inputs and produces the correct output selection to directly drive the tubes. Binary input codes 12 and 13 cause all outputs to remain high thereby blanking the indicator tube. However, using this feature may cause a slight glow to appear in the tube.

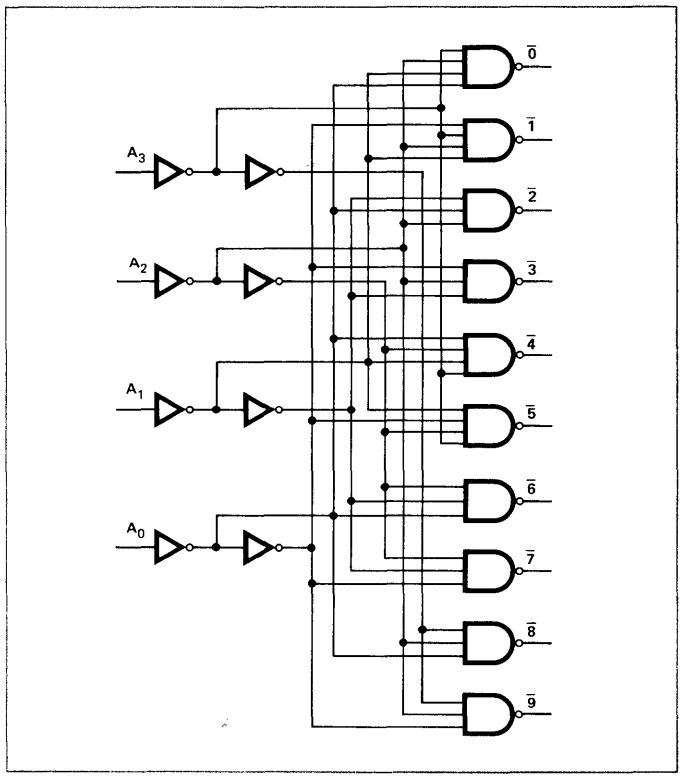


PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{0}$ to $\overline{9}$	(Active Low) Outputs	
	*See Output Characteristics	

CHARACTERISTICS

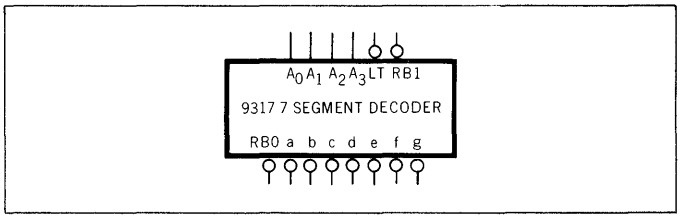
OUTPUT CHARACTERISTICS

Max Current into output when output is low	7 mA
Max Leakage Current at 50 Volts	50 μA
PACKAGE	16 Pin Dip (6B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	100 mW



9317 7-SEGMENT DECODER/DRIVER

DESCRIPTION The 9317 is a seven segment decoder driver designed to accept a 4 bit 8421 code input and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to drive seven segment incandescent lamp displays and light emitting diode indicators directly. The segments and numeric designations chosen to represent the decimal numbers are shown below.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{LT}$	Lamp Test (Active Low) Input	4.0 UL
$\overline{RBI}$	Ripple Blanking (Active Low) Input	0.5 UL
$\overline{RBO}$	Ripple Blanking (Active Low) Output	1.5 UL
$\overline{a}$, $\overline{b}$, $\overline{c}$, $\overline{d}$, $\overline{e}$, $\overline{f}$, $\overline{g}$	(Active Low) Outputs	
	*See Output Characteristics	

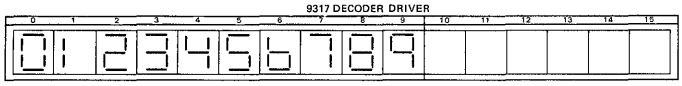
CHARACTERISTICS

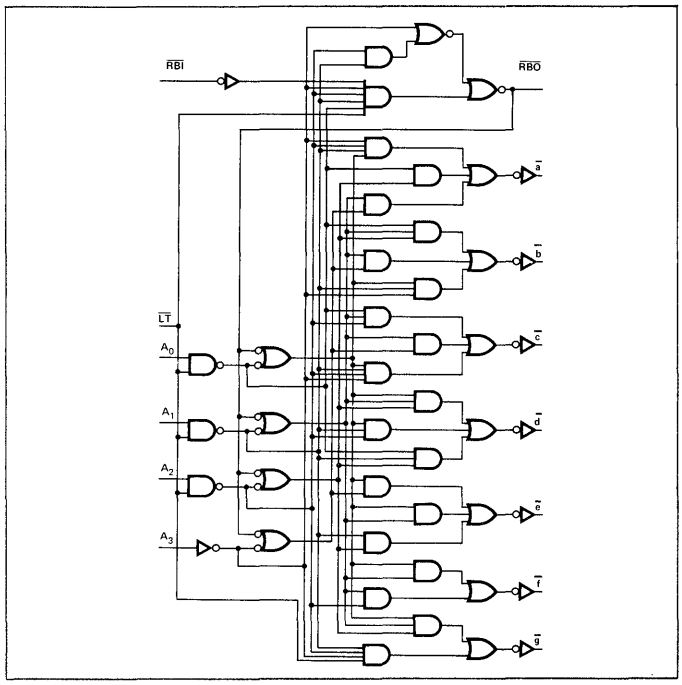
TYPICAL DELAY	A to Outputs 250 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)

OUTPUT CHARACTERISTICS

There are four versions of the 9317 available which differ only in their output characteristics tabulated below.

	A	B	C	D	Units
Max Sinking Current in Low State	40	40	20	20	mA
Max Voltage Applied to Outputs in High State	30	20	30	20	V
Max Power Dissipation Per Output	50	50	30	30	mW

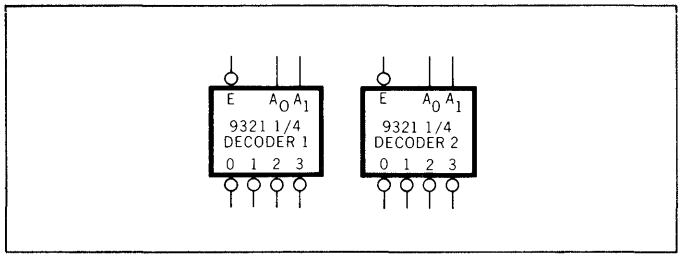




9321
DUAL ONE OF FOUR DECODER

DESCRIPTION The 9321 consists of two independent one of four decoders, each with an active low enable. Each decoder accepts two inputs and provides one of four mutually exclusive active low outputs. An active low enable is provided on each decoder which must be low for any output to be low.

Each decoder can be used as a 4 output demultiplexer by using the enable line as a data input.



PIN NAMES		LOADING
Decoder 1 and 2		
$\overline{E}$	Enable (Active Low) Input	1 UL
A_0, A_1	Address Inputs	1 UL
$\overline{0}$, $\overline{1}$, $\overline{2}$, $\overline{3}$	(Active Low) Outputs	10 UL

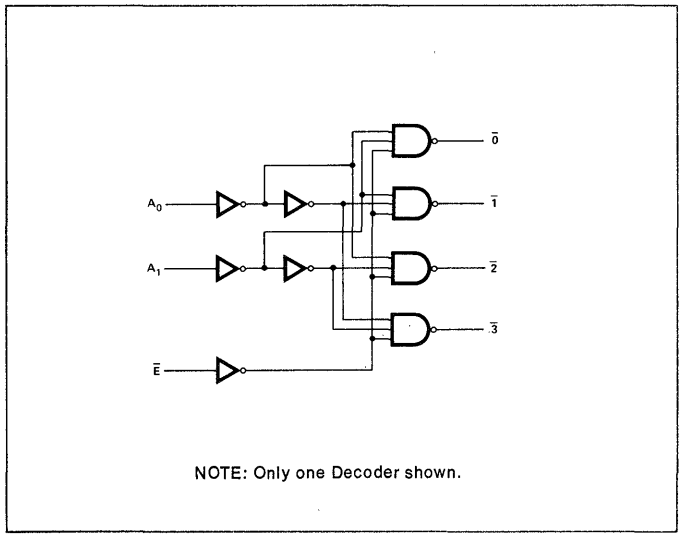
CHARACTERISTICS

TYPICAL DELAY	$\overline{A}$ to Output	22 ns
	$\overline{E}$ to Output	17 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	150 mW	

TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

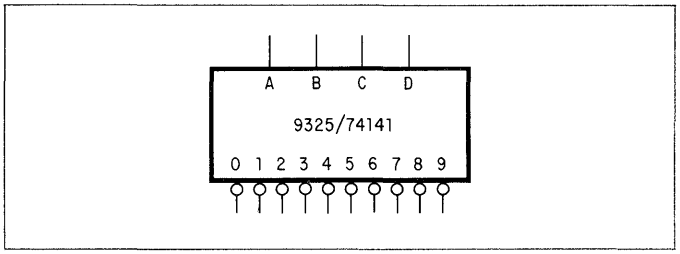


NOTE: Only one Decoder shown.

9325/54141,74141 BCD
TO DECIMAL DECODER/DRIVER

DESCRIPTION The 9325/54141, 74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the 9325/54141, 74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance, N-P-N output transistors have a maximum reverse current of 50 microamperes at 70 volts.

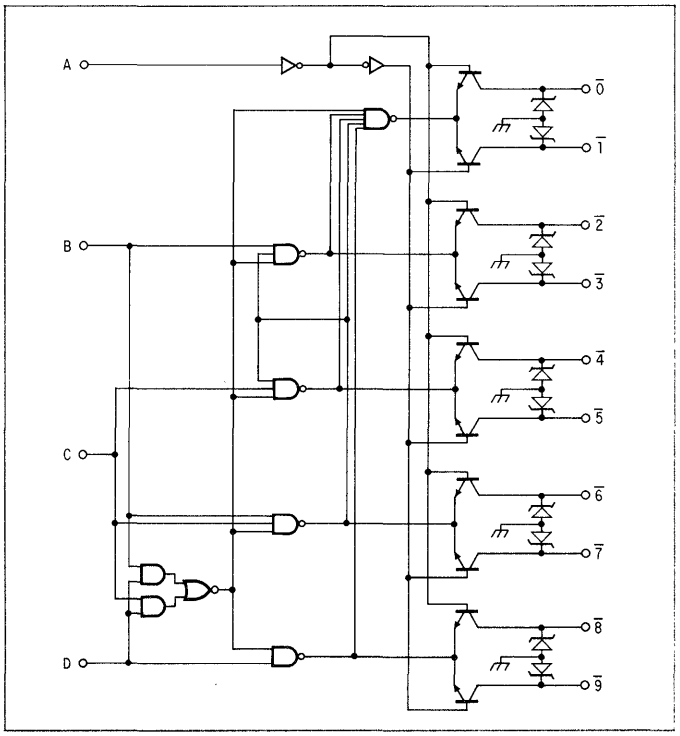


PIN NAMES		LOADING
A	Address Inputs	2 UL
B, C, D	Address Inputs	1 UL
$\overline{0}$ to $\overline{9}$	Outputs	*

*See output characteristics

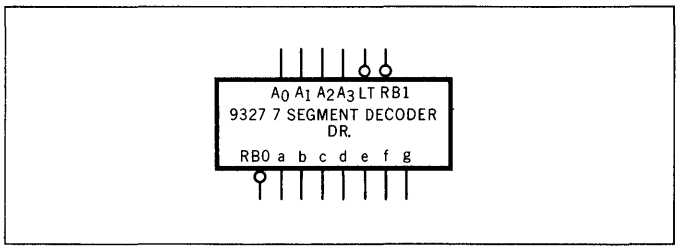
CHARACTERISTICS

MAX. CURRENT INTO OUTPUT DURING "ON" STATE	7 mA
OUTPUT LEAKAGE AT 65 V	50 μA
POWER DISSIPATION	55 mW
PACKAGE	16 Pin DIP (6B) Flat Pak (4L)



9327 7-SEGMENT DECODER/DRIVER

DESCRIPTION The 9327 is a seven segment decoder driver designed to accept a 4-bit 8421 code input and provide the appropriate outputs to drive a seven segment fluorescent numerical display. The segments and numeric designations chosen to represent the decimal numbers are shown below.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{LT}$	Lamp Test (Active Low) Input	4 UL
$\overline{RBI}$	Ripple Blanking (Active Low) Input	0.5 UL
$\overline{RBO}$	Ripple Blanking (Active Low) Output	1.5 UL
a, b, c, d, e, f, g	Active High Outputs	

*See Output Characteristics

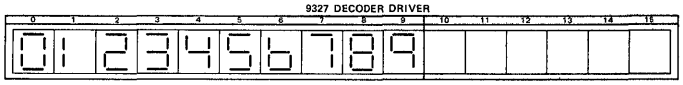
CHARACTERISTICS

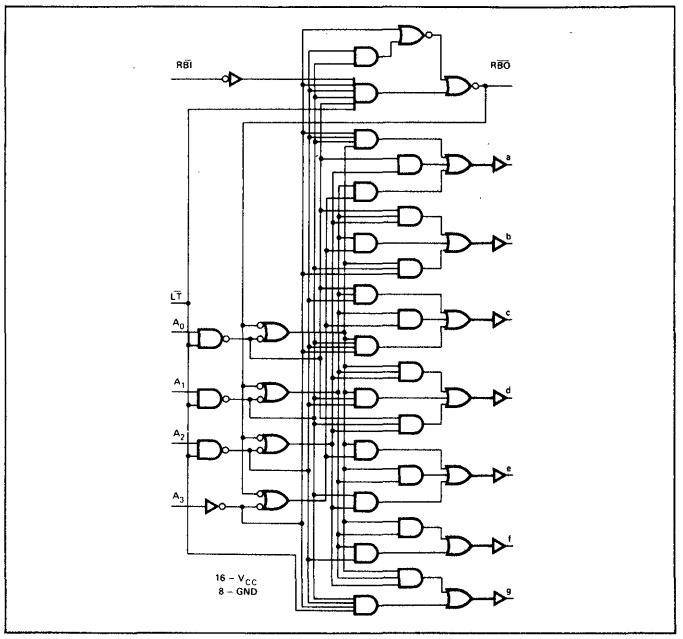
TYPICAL DELAY A to Outputs 250 ns
PACKAGE 16 Pin Dip (7B) or Flat Pack (4L)

OUTPUT CHARACTERISTICS

There are two versions of the 9327 which differ only in their output characteristics tabulated below.

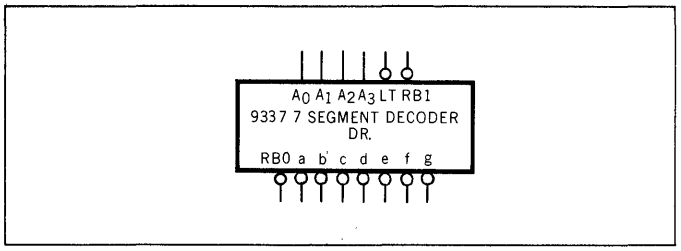
	A	B
MAX. SINKING CURRENT IN LOW STATE	7mA	5mA
MIN. HIGH VOLTAGE BREAKDOWN	55V @ 50μA	25V @ 35μA





9337 7-SEGMENT DECODER/DRIVER

DESCRIPTION The 9337 is a seven segment decoder driver designed to accept a 4-bit 8421 code input and provide the appropriate outputs to drive a seven segment numerical display. The decoder can be used to drive seven segment gas filled cold cathode indicator tubes directly. The device also has high current capabilities which allows the time sharing of display tubes.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	1 UL
$\overline{LT}$	Lamp Test (Active Low) Input	4.0 UL
$\overline{RBI}$	Ripple Blanking (Active Low) Input	0.5 UL
$\overline{RBO}$	Ripple Blanking (Active Low) Output	1.5 UL
$\bar{a}$, $\bar{b}$, $\bar{c}$, $\bar{d}$, $\bar{e}$, $\bar{f}$, $\bar{g}$	(Active Low) Outputs	

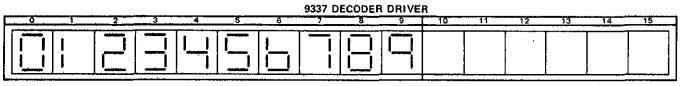
*See Output Characteristics

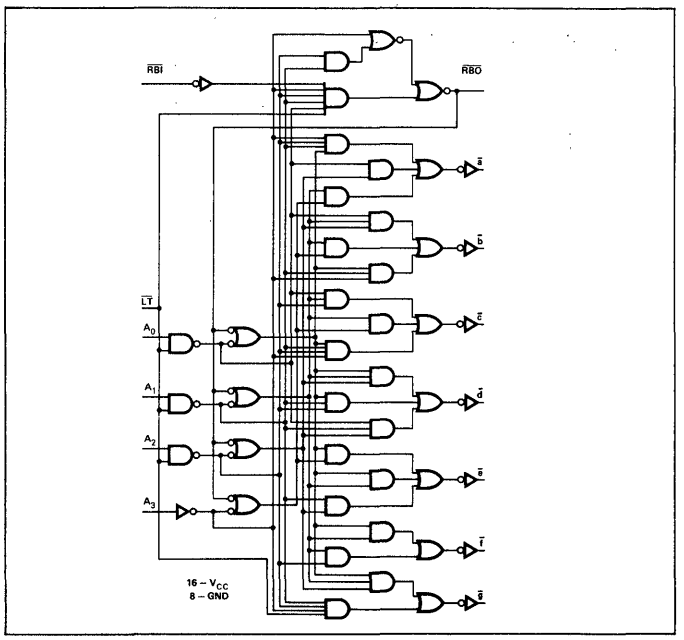
CHARACTERISTICS

TYPICAL DELAY A to Outputs 250 ns
PACKAGE 16 Pin Dip (7B) or Flat Pack (4L)

MAX. SINKING CURRENT IN LOW STATE 10 mA

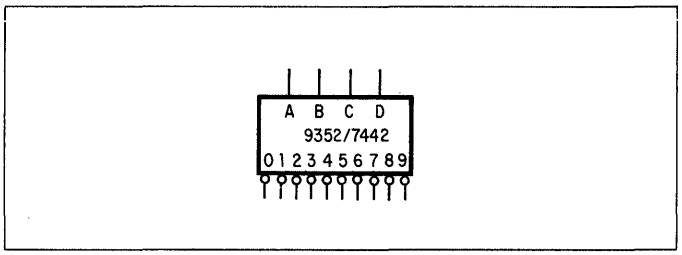
MIN. HIGH VOLTAGE BREAKDOWN 55V @ 6μA 25°C
10 μA 75°C





9352/5442,7442 BCD TO DECIMAL DECODER

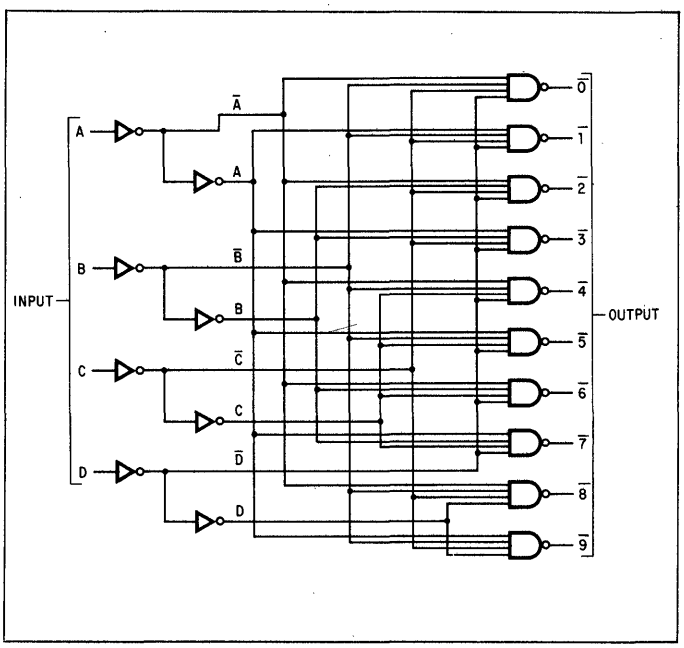
DESCRIPTION The 9352/5442, 7442 accepts binary coded decimal input data and decodes to one of ten output lines. Full fan-out of 10 TTL loads is available at all outputs. This monolithic decimal decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.



PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 UL
$\overline{0}$ to $\overline{9}$	Decimal Output	10 UL

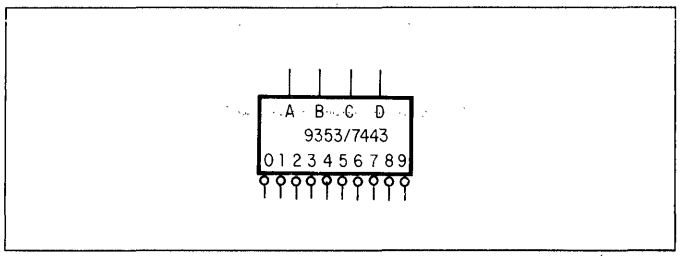
CHARACTERISTICS

PROPAGATION DELAY	22 ns
POWER DISSIPATION	140 mW
PACKAGE	16 Pin DIP (6B)



9353/5443,7443 EXCESS-3 TO DECIMAL DECODER

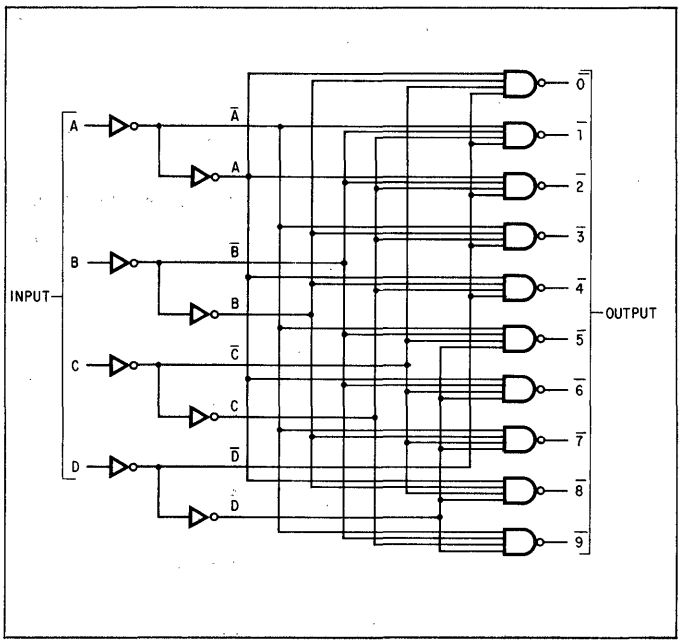
DESCRIPTION The 9353/5443, 7443 accepts excess-3 coded input data and decodes to one of ten output lines. Full fan-out of 10 TTL loads is available at all outputs. This monolithic decimal decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.



PIN NAMES		LOADING
A, B, C, D	Excess 3 Inputs	1 UL
$\overline{0}$ to $\overline{9}$	Decimal Output	10 UL

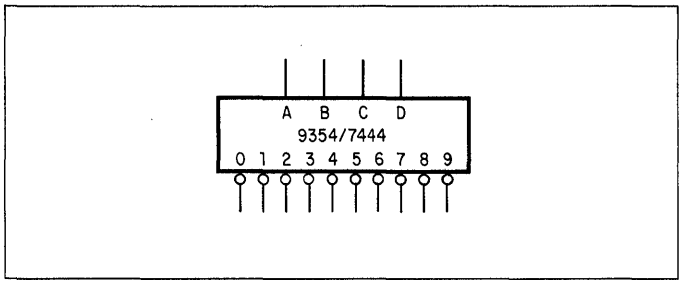
CHARACTERISTICS

PROPAGATION DELAY	22 ns
POWER DISSIPATION	140 mW
PACKAGE	16 Pin DIP (6B)



9354/5444,7444 EXCESS-3 GRAY TO DECIMAL DECODER

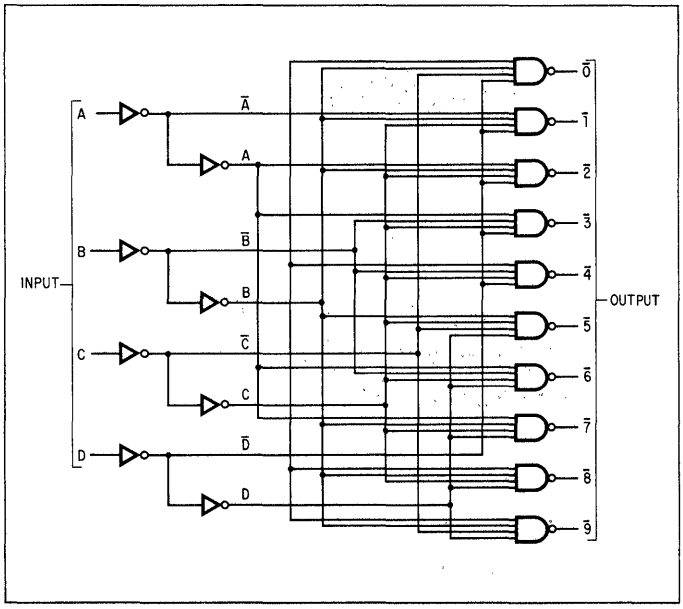
DESCRIPTION The 9354/5444, 7444 accepts excess-3 gray code input data and decodes to one of ten output lines. Full fan-out of ten TTL loads is available at all outputs. This monolithic decimal decoder consists of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.



PIN NAMES		LOADING
A, B, C, D	Excess 3 Gray Inputs	1 UL
$\overline{0}$ to $\overline{9}$	Decimal Output	10 UL

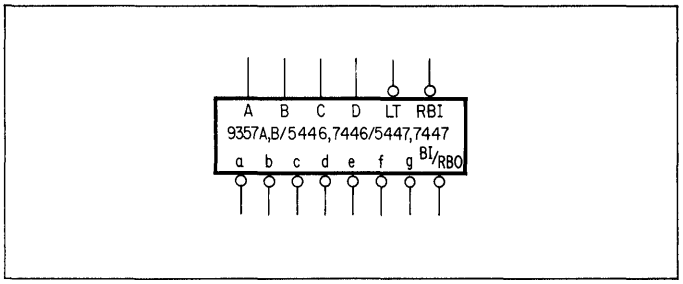
CHARACTERISTICS

PROPAGATION DELAY	22 ns
POWER DISSIPATION	140 mW
PACKAGE	16 Pin DIP (7B)



9357A/5446,7446 • 9357B/5447, 7447 BCD-TO-7-SEG. DECODER

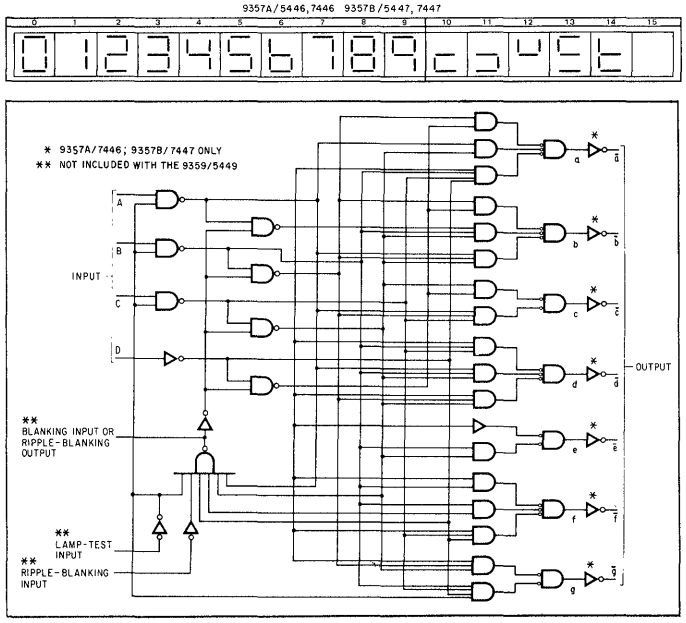
DESCRIPTION The 9357A, B accepts 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a seven-segment display indicator. The relatve positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the 9357A, B are designed to withstand the relatively high voltages required for seven segment indicators. The 9357A outputs will withstand 30 volts, and the 9357B will withstand 15 volts, with a maximum reverse current of 250 microamperes. Indicator segments requiring up to 20 milliamperes of current may be driven directly from the high-performance output transistors. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.



PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 UL
$\overline{RBI}$	Ripple Blanking Input	1 UL
$\overline{LT}$	Lamp Test Input	1 UL
$\overline{BI/RBO}$	Blanking Input or	2.6 UL
	Ripple Blanking Output	5 UL
$\overline{a}, \ldots \overline{g}$	Outputs	12.5 UL

CHARACTERISTICS

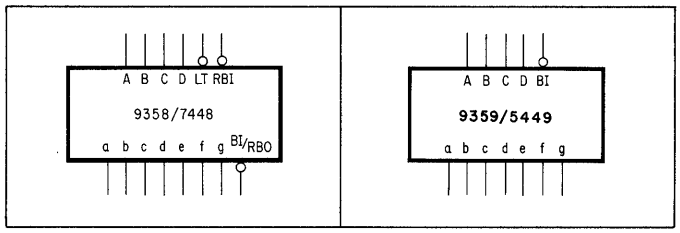
OUTPUT VOLTAGE (9357A/7446)	30 V Min.
OUTPUT VOLTAGE (9357B/7447)	15 V Min.
OUTPUT CURRENT	20 mA Min.
POWER DISSIPATION	265 mW
PACKAGE	16 Pin DIP (7B)



9358/5448,7448 • 9359/5449,7449 BCD-TO-7-SEGMENT DECODER

DESCRIPTION The 9358/5448, 7448 is a BCD to 7 segment decoder designed for driving discrete active devices or other logic circuits. The outputs are active HIGH with a passive 2KΩ pull-up. Features such as leading edge and/or trailing edge zero blanking control, lamp test and lamp intensity control have been incorporated in the 9358/7448.

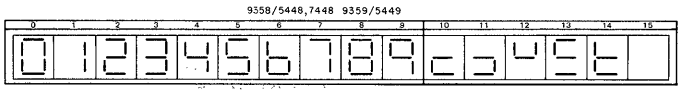
The 9359/5449 is an open collector version of the 9358/7448 which is available in a 14 pin Flatpack.

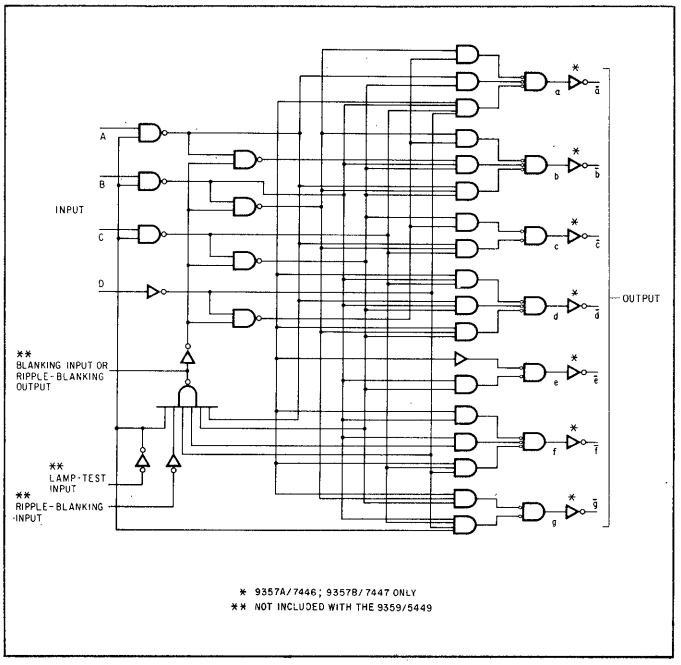


PIN NAMES		LOADING
A, B, C, D	BCD Inputs	1 UL
$\overline{RBI}$	Ripple Blanking Input	1 UL
$\overline{LT}$	Lamp Test Input	1 UL
$\overline{BI/RBO}$	Blanking Input or Ripple Blanking Output	2.6 UL 5 UL
$\overline{BI}$	Blanking Input	1 UL
a to g	Outputs	6 UL

CHARACTERISTICS

POWER DISSIPATION	(9358)	265 mW
	(9359)	167 mW
PACKAGE	(9358/7448)	16 Pin DIP (6B)
	(9359/5449)	14 Pin Flat Pack (3B)

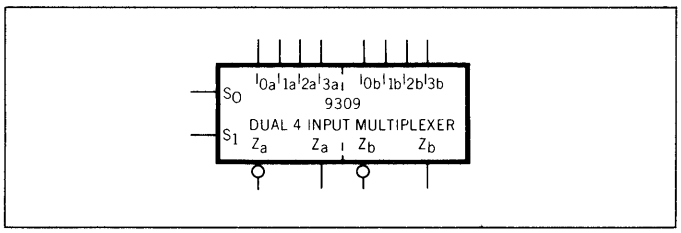




9309 DUAL FOUR-INPUT MULTIPLEXER

DESCRIPTION The 9309 consists of two 4 input multiplexers with common input select logic. It allows two bits of data to be switched in parallel to the appropriate outputs from two 4 bit data sources. Both polarities of outputs are available.

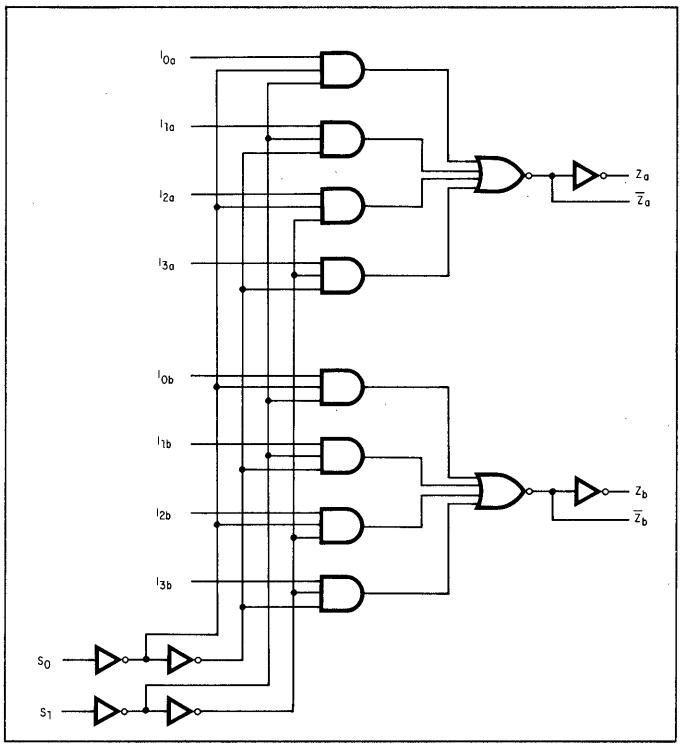
An obvious use of the 9309 is the moving of data from a group of registers to a common output buss. The particular register from which the data comes is determined by the state of the select inputs. A less obvious use is as a function generator. The 9309 can generate two functions of three variables. This is useful for implementing random gating functions.



PIN NAMES		LOADING
S_0, S_1	Common Select Inputs	1 UL
Multiplexer A		
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs	1 UL
Z_a	Multiplexer Output	10 UL
$\overline{Z}_a$	Complementary Multiplexer Output	9 UL
Multiplexer B		
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs	1 UL
Z_b	Multiplexer Output	10 UL
$\overline{Z}_b$	Complementary Multiplexer Output	9 UL

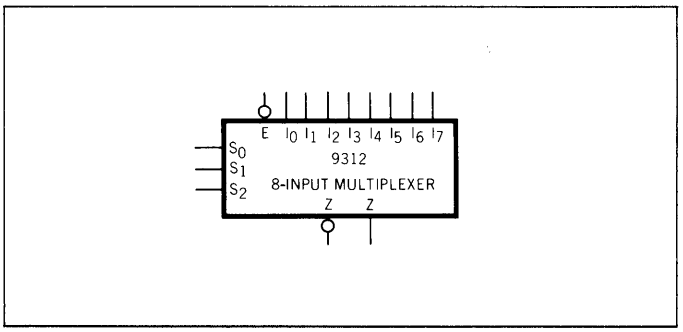
CHARACTERISTICS

TYPICAL DELAYS	S to $\overline{Z}$	24 ns
	I to $\overline{Z}$	9 ns
PACKAGE	16 Pin Dip (6B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	150 mW	



9312
EIGHT-INPUT MULTIPLEXER

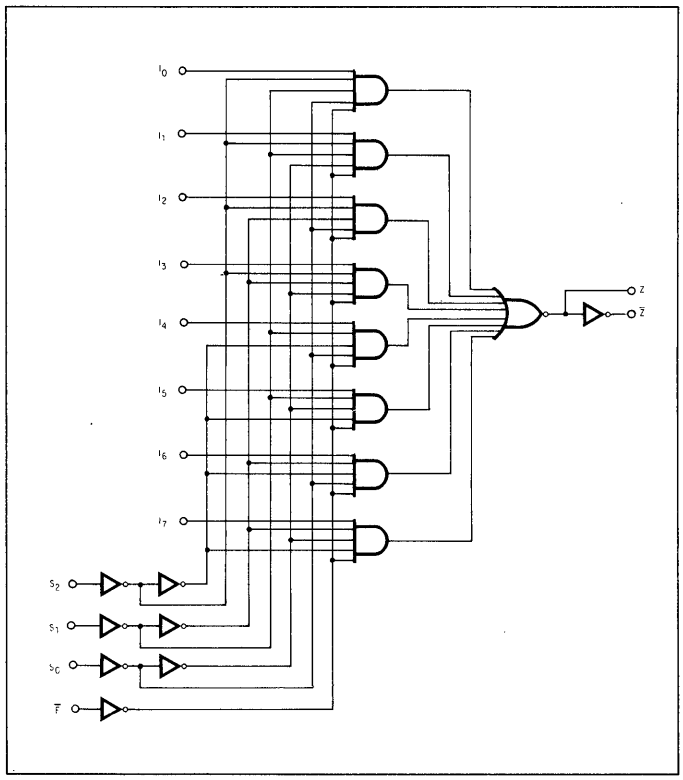
DESCRIPTION The 9312 is an 8-input multiplexer which can select one bit of data from up to eight sources. It has complementary outputs, active low enable, and internal select decoding. With the enable inactive, the multiplexer output is low and the complementary multiplexer output high regardless of all input conditions. Data is routed from a particular multiplexer input to the outputs according to the three input binary code applied to the select inputs.



PIN NAMES		LOADING
S_0, S_1, S_2	Select Inputs	1 UL
$\overline{E}$	Enable (Active Low) Input	1 UL
I_0 to I_7	Multiplexer Inputs	1 UL
Z	Multiplexer Output	10 UL
$\overline{Z}$	Complementary Multiplexer Output	9 UL

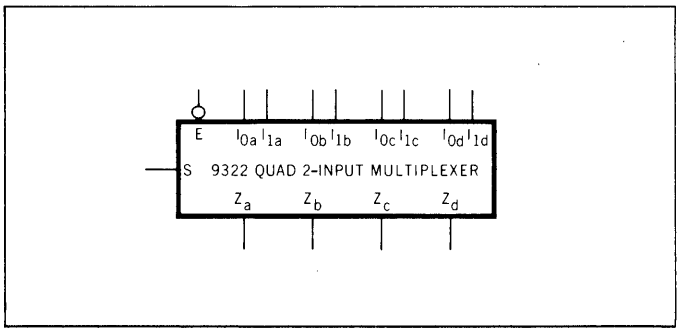
CHARACTERISTICS

TYPICAL DELAYS	S to Z	24 ns
	$\overline{E}$ to $\overline{Z}$	14 ns
	I to $\overline{Z}$	9 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	135 mW	



9322
QUAD 2-INPUT MULTIPLEXER

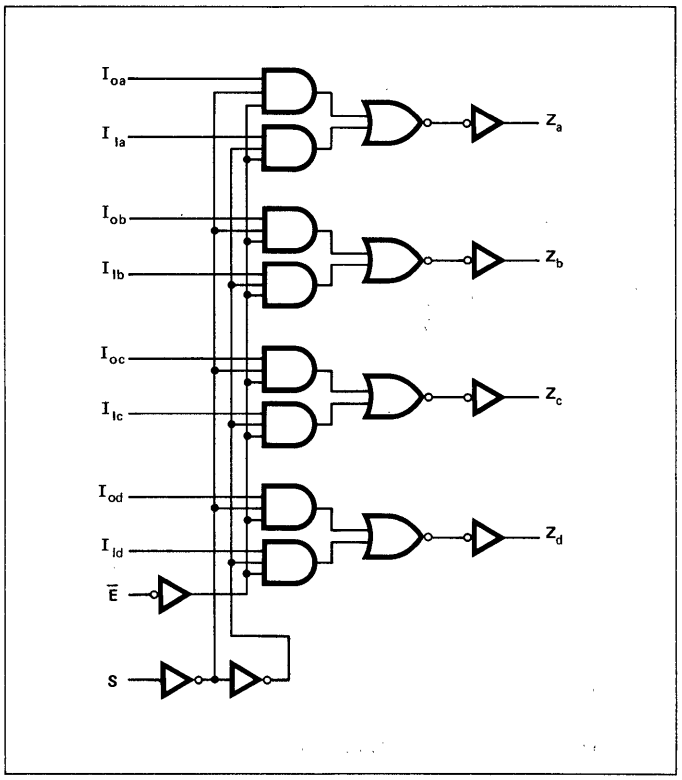
DESCRIPTION The 9322 consists of four 2-input multiplexers with common input select logic, common active low enable and active high outputs. It allows four bits of data to be switched in parallel to the appropriate outputs from four 2 bit data sources. When the enable is not active, all the outputs are held low.



PIN NAMES		LOADING
S	Common Select Input	1 UL
$\overline{E}$	Enable (Active Low) Input	1 UL
Multiplexers A, B, C, D		
I_0, I_1	Multiplexer Inputs	1 UL
Z	Multiplexer Output	10 UL

CHARACTERISTICS

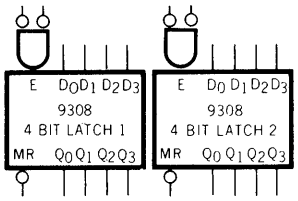
TYPICAL DELAYS	I_0 to Z	10 ns
	$\overline{E}$ to Z	15 ns
	S to Z	19 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	125 mW	



9308
DUAL 4-BIT LATCH

DESCRIPTION The 9308 consists of two separate 4-bit latch sections which provide high speed parallel gated data storage. Each 4-bit latch section has four assertion outputs, overriding master reset, and a two-input active low AND enable.

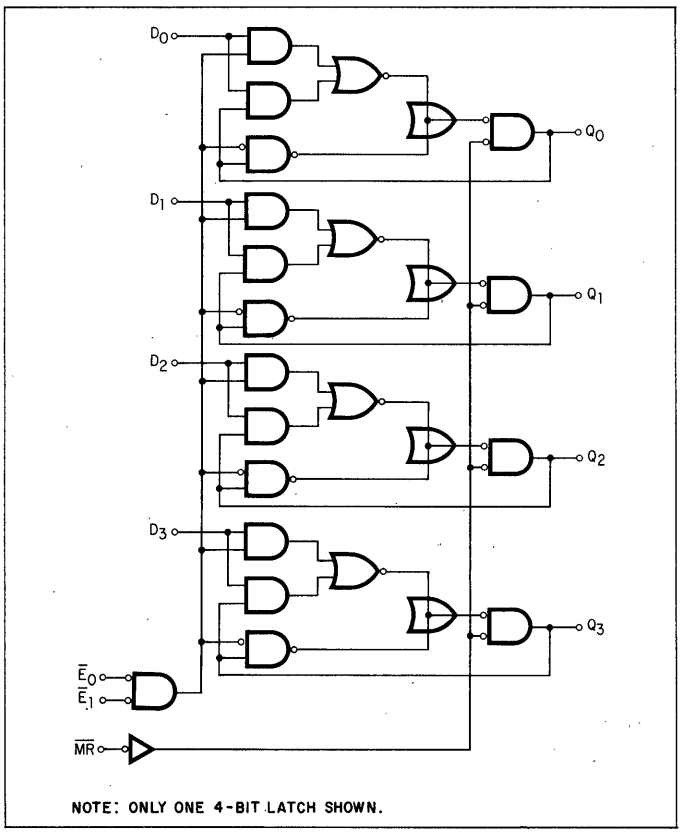
Data enters a latch when both enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs go high, the data present in the latch at that time is held in the latch and is no longer affected by the data input. Active low master reset overrides all other input conditions and when activated forces the outputs of all the latches low.



PIN NAMES		LOADING
D_0, D_1, D_2, D_3	Parallel Latch Inputs	1.5 UL
$\overline{E}_0$, $\overline{E}_1$	AND Enable (Active Low) Inputs	1 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs	9 UL

CHARACTERISTICS

TYPICAL DELAYS	$\overline{E}$ to Output	18 ns
	D to Output	15 ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)	
TYPICAL POWER DISSIPATION	340 mW	



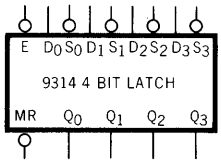
NOTE: ONLY ONE 4-BIT LATCH SHOWN.

9314
4-BIT LATCH

DESCRIPTION The 9314 is a 4-bit latch which can be used in applications where D type latches or set/reset latches are required. The latches have assertion outputs, a common active low enable and overriding active low master reset.

When the common enable goes high data present in the latches is stored and the state of the latches is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs low.

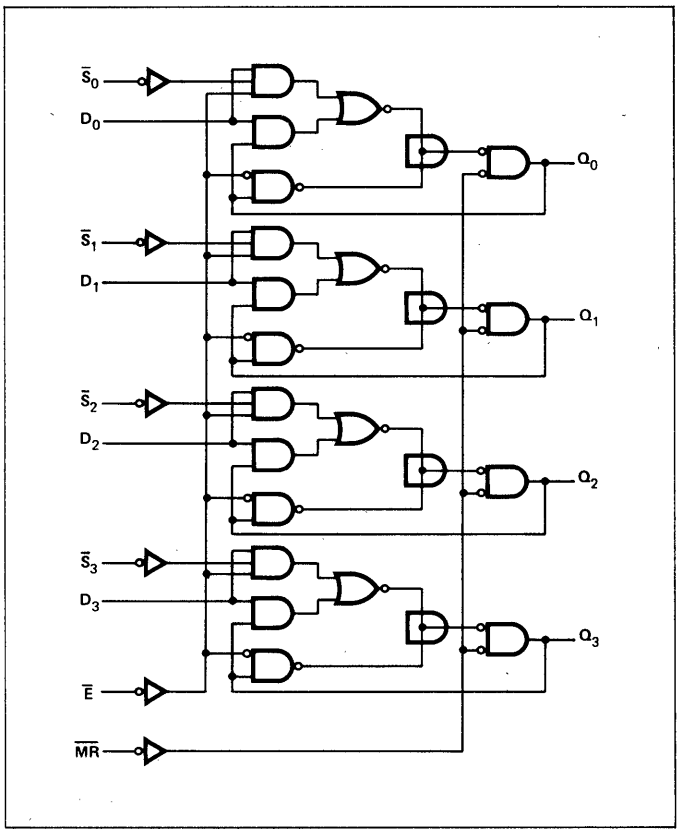
Each of the four latches can be operated either as an active low set/reset latch with reset override or, with $\overline{S}$ low, as D type storage latch.



PIN NAMES		LOADING
$\overline{E}$	(Active Low) Enable Input	1 UL
D_0, D_1, D_2, D_3	Parallel Data Inputs	1.5 UL
$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$	Set (Active Low) Inputs	1 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	9 UL

CHARACTERISTICS

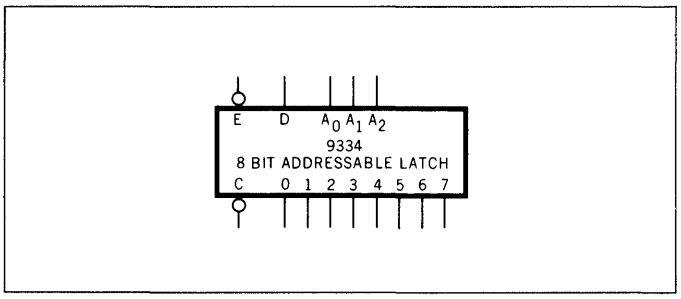
TYPICAL DELAYS	$\overline{E}$ to Q	20 ns
	D to Q	15 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	175 mW	



9334
8-BIT ADDRESSABLE LATCH

DESCRIPTION The 9334 is an 8-bit addressable latch which stores single line data in the addressed latch. It also can be used as a demultiplexer or a one of eight decoder with active high outputs. The device has an active low enable and common clear.

The 9334 has four modes of operation which are shown below. When in the addressable latch mode, the addressed latch will follow the data input with all non-addressed latches remaining in their previous state. In the memory mode, all latches remain in their previous state and are unaffected by the inputs. While in the demultiplexing mode, the addressed output will follow the state of the D input, with all other outputs in the logical zero state. In the clear mode all outputs are held in the logical zero state and are unaffected by the inputs.



PIN NAMES **LOADING**

A_0, A_1, A_2	Address Inputs	1 UL
D	Data Input	1 UL
$\overline{E}$	Enable (Active Low) Input	1.5 UL
$\overline{C}$	Clear (Active Low) Input	1 UL
0 to 7	Parallel Latch Outputs	6 UL

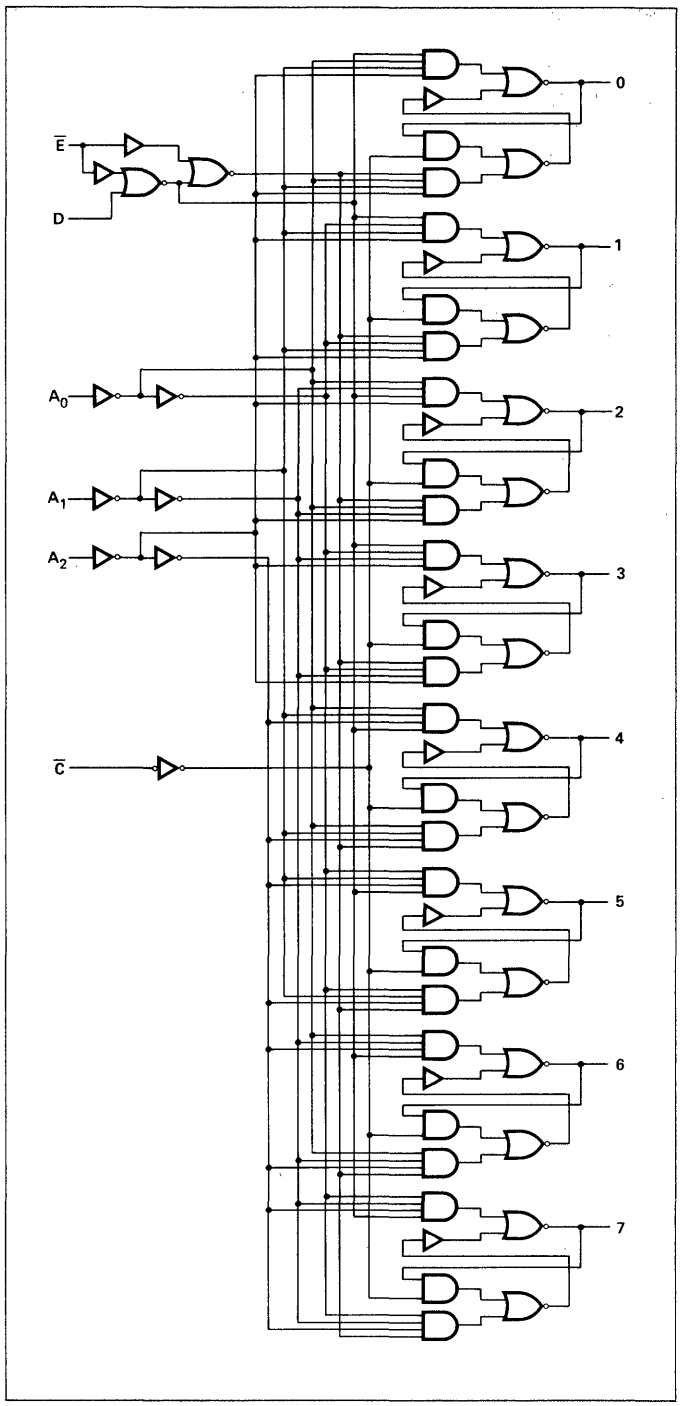
CHARACTERISTICS

TYPICAL DELAY	D to Q 17 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	250 mW

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active High 8 Channel Demultiplexer
H	L	Clear

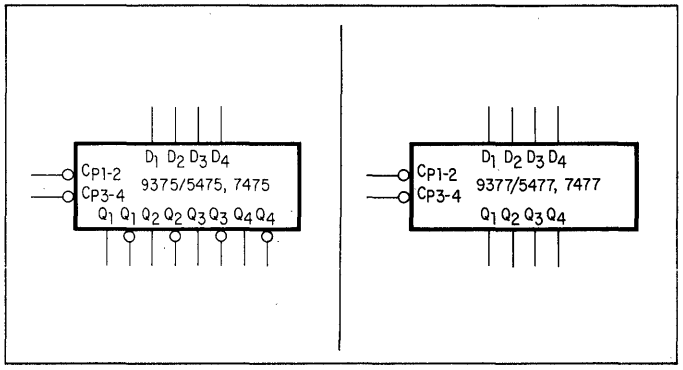
H = High Voltage Level
L = Low Voltage Level



9375/5475,7475 • 9377/5477, 7477
4-BIT LATCH

DESCRIPTION The 9375 and 9377 are suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output.

The 9375 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin dual-in-line packages. For higher component density applications the 9377 4-bit latch is available in the 14-pin flat package.



PIN NAMES

		LOADING
D_1, D_2, D_3, D_4	Data Inputs	2 UL
$\overline{CP}_{1-2}$	Clock Input Latches 1 & 2	4 UL
$\overline{CP}_{3-4}$	Clock Input Latches 3 & 4	4 UL
Q_1, Q_2, Q_3, Q_4	Latch Outputs	10 UL
$\overline{Q}_1$, $\overline{Q}_2$, $\overline{Q}_3$, $\overline{Q}_4$	Complementary Latch Outputs	10 UL

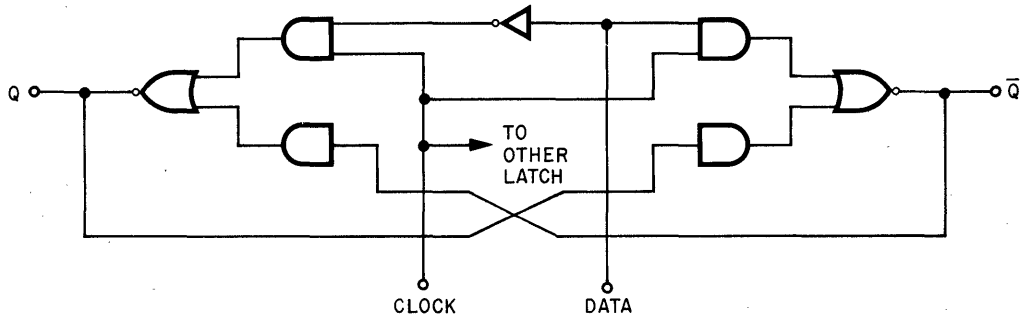
CHARACTERISTICS

PROPAGATION DELAY	15 ns	
POWER DISSIPATION	40 mW/Latch	
PACKAGES	16 Pin DIP (6B)	9375/5475, 7475
	14 Pin Flat Pak (3I)	9377/5477, 7477

TRUTH TABLE (Each Latch)

t_n	$t_n + 1$
D	Q
1	1
0	0

NOTES: 1. t_n = bit time before clock pulse transition.
2. $t_n + 1$ = bit time after clock pulse transition.



NOTE: ONLY 1/4 (ONE BIT) OF LATCH IS SHOWN.

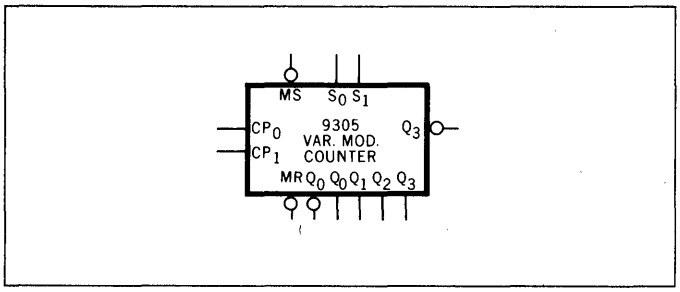
9305
VARIABLE MODULO COUNTER

DESCRIPTION The 9305 is a semi-synchronous counter which can be programmed to provide division or counting by 2, 4, 5, 6, 7, 8, 10, 12, 14, 16. It can count in binary code and also divide by 10, 12, 14, 16 with a 50% duty cycle output. The device has asynchronous overriding master reset and set inputs and an active low $\overline{Q}_3$ output which allows the cascading of stages.

The counter is split into two parts, a divide by two stage and three synchronous stages which can be programmed to divide by 5, 6, 7, 8. Binary counting or division is obtained by feeding the output of the single stage to the input of the three stage synchronous counter. To divide by 10, 12, 14, 16 with 50% duty cycle the single stage is fed by the three stage synchronous counter.

When the active low master reset is active it will clear the counter overriding all other input conditions and forcing outputs Q_{0-3}, low. When the active low master set is active outputs Q_{0-3} are forced high regardless of input conditions. The master set can be used as a synchronous clear since the counters will go to zero on the next clock pulse, after ones have been set into the counter.

No extra logic is needed for asynchronous multistage counting, the $\overline{Q}_3$ output is fed to the following counter's clock input.



PIN NAMES

		LOADING
S_0, S_1	Select Inputs	2 UL
CP_0	First Stage Clock Active High Going Edge Input	1 UL
CP_1	Second Stage Clock Active High Going Edge Input	1 UL
$\overline{MS}$	Master Set (Active Low) Input	1 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_0	First Stage Output	8 UL
$\overline{Q}_0$	Complementary First Stage Output	8 UL
Q_1, Q_2, Q_3	Parallel Last Three Stage Outputs	8 UL
$\overline{Q}_3$	Complementary Last Stage Output	8 UL

CHARACTERISTICS

TYPICAL SPEED	15 MHz Counting Frequency
PACKAGE	14 Pin Dip (7A) or Flat Pack (3B)
TYPICAL POWER DISSIPATION	195 mW

PROGRAMMING CONNECTIONS FOR LAST THREE STAGES

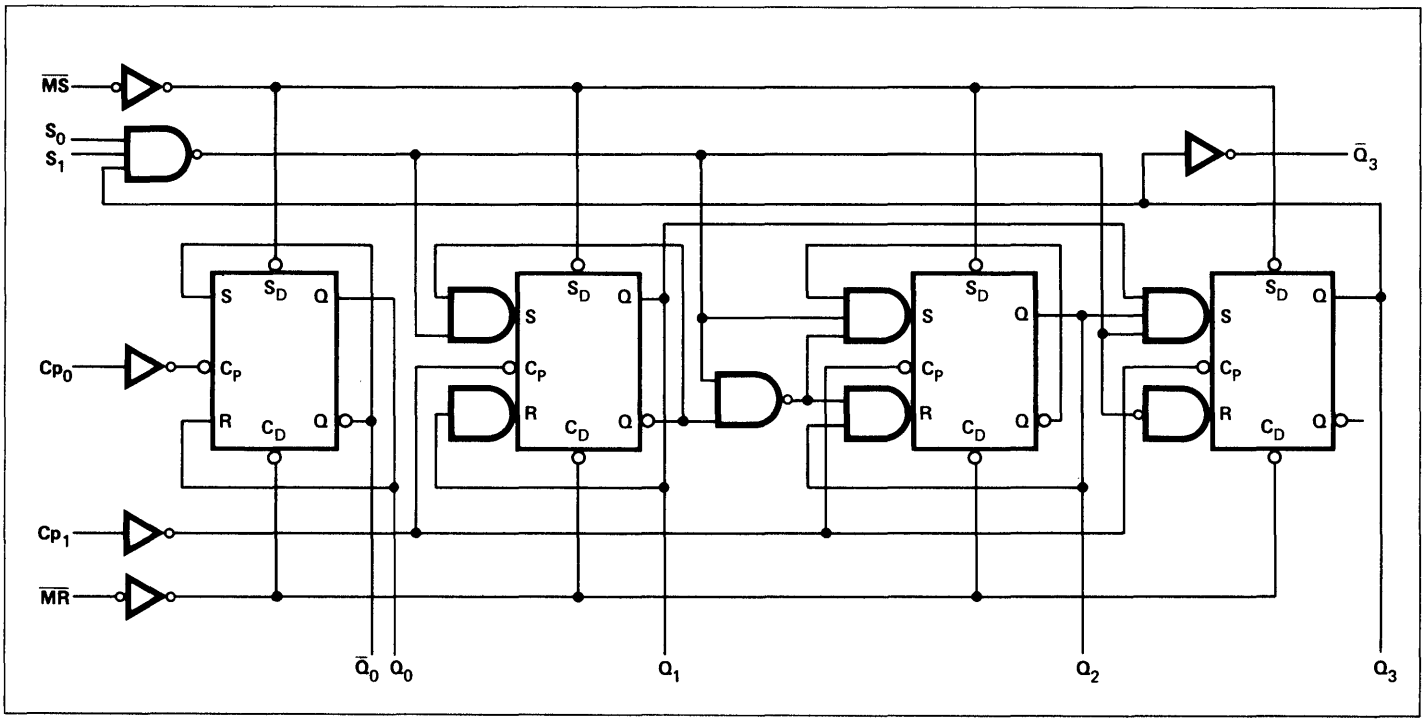
S_0	S_1	MODULO
NC	NC	5
Q_1	NC	6
NC	Q_1	6
Q_2	NC	7
NC	Q_2	7
Q_1	Q_2	8

NC = No Connection

CONNECTIONS FOR BINARY COUNTING AND 50% DUTY CYCLE DIVISION

For Binary Counting
- $\overline{Q}_0$ connected to CP_1
- Incoming clock to CP_0

For 50% Duty Cycle Output
- $\overline{Q}_3$ connected to CP_0
- Incoming clock to CP_1



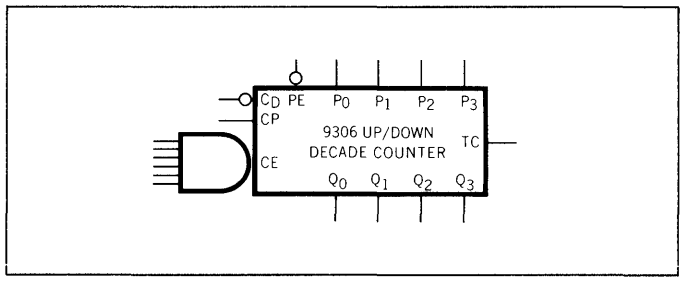
9306
UP/DOWN BCD COUNTER

DESCRIPTION The 9306 is a synchronous up/down BCD decade counter with synchronous parallel load facility, single line up/down control, and carry lookahead logic for multi-decade operation.

Counting is synchronous with the outputs changing state after the low to high transition of the clock. When the conditions are satisfied for counting, a clock pulse will change the counter to the next state of the count sequence shown below, in a forward or reverse direction, depending on the count mode selection. Whenever the parallel enable input is low, the parallel inputs determine the next condition of the counter synchronously with the clock. The state diagram also shows the count sequence if a state not in the normal BCD sequence is loaded into the counter by the parallel inputs.

Mode selection is accomplished as shown in the table below. However, several restrictions are placed on the manner of selection. First, the transition of CE from high to low or of $\overline{PE}$ from low to high may only be done when CP is high. Second, if CE is high, any change of $\overline{CD}$ must be done only when CP is high.

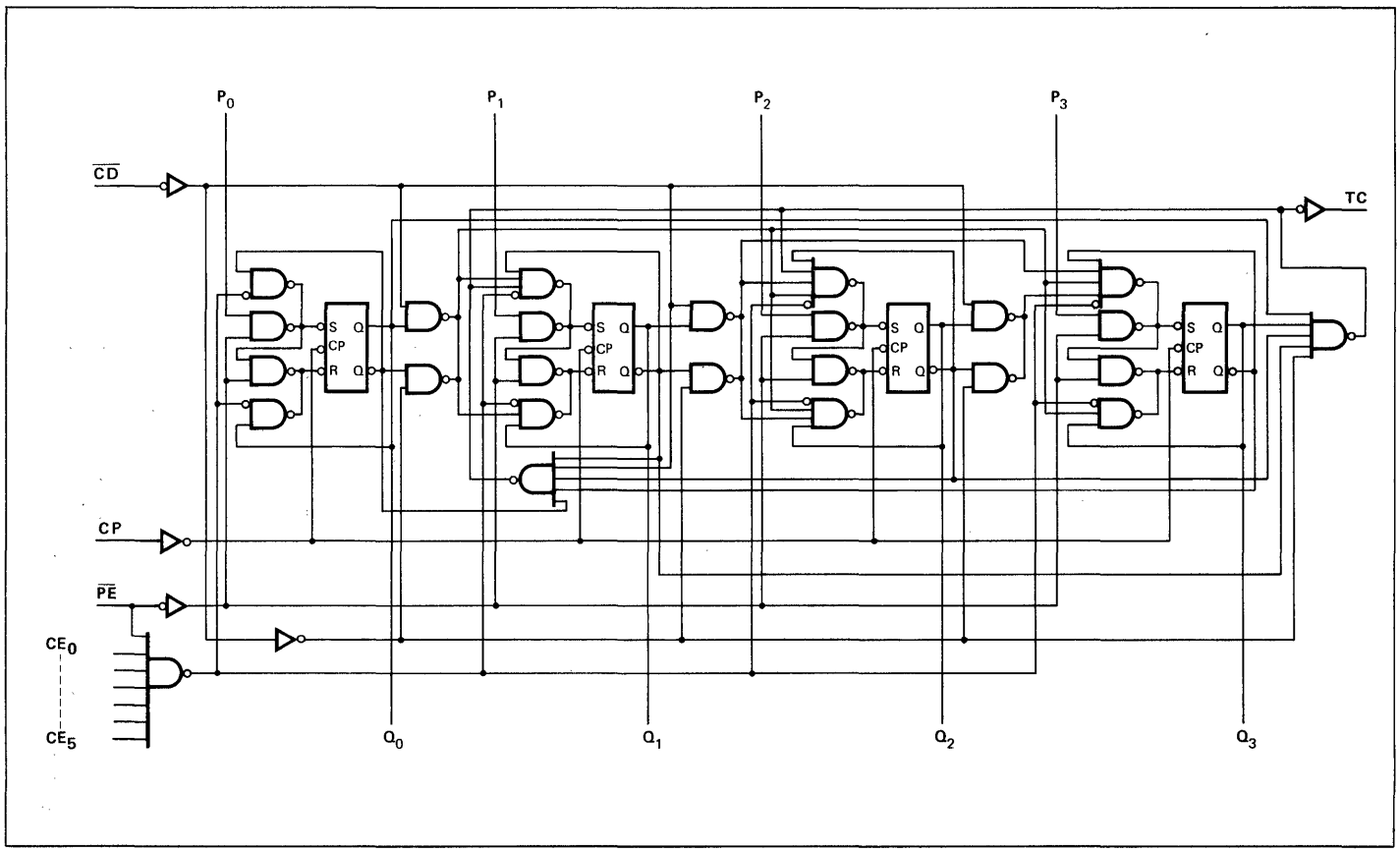
The multi-input count enable inputs and terminal count logic allow high speed multi-decade (7 stages) up/down counting, without extra logic. Terminal counts from less significant stages are applied to the count enable inputs of more significant stages. Then when all less significant stages are either in a borrow or carry condition the counter stage will change state according to its mode.



PIN NAMES		LOADING
P_0, P_1, P_2, P_3	Parallel Inputs	2/3 UL
$\overline{PE}$	Parallel Enable (Active Low) Input	2 UL
CE_0 to CE_5	Count Enable AND Inputs	1 UL
CP	Clock Active High Going Edge Input	2 UL
$\overline{CD}$	Count Down Enable (Active Low) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	6 UL
TC	Terminal Count Output	6 UL

CHARACTERISTICS

TYPICAL SPEED	18 MHz Counting Frequency
TYPICAL DELAY	CP to Q 20 ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)
TYPICAL POWER DISSIPATION	350 mW



9310
UP DECADE COUNTER

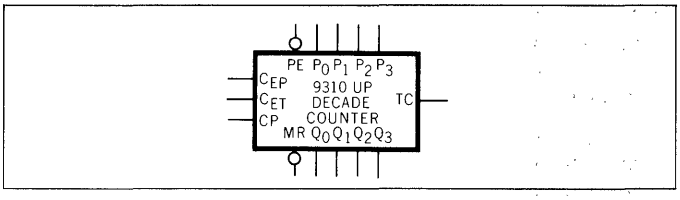
DESCRIPTION The 9310 is a synchronous up decade counter. It has synchronous parallel load facility, overridng asynchronous master reset, terminal count and carry lookahead logic for high speed multidecade operation.

The counter is synchronous, with the counter outputs changing state after the low to high transition of the clock. When conditions are satisfied for counting, a clock pulse will change the counter to the next state of the count sequence shown below. Whenever the parallel enable input is low the parallel inputs determine the next state of the counter synchronously with the clock.

Mode selection is accomplished as shown below. However, a restriction is placed on the manner of selection. The transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high.

By utilizing the two count enable inputs and terminal count outputs multi-stage synchronous counting is obtained, with operating speed equivalent to that of a single stage.

When the asynchronous master reset is active outputs Q_{0-3} will be forced low regardless of all other input conditions.



PIN NAMES		LOADING
$\overline{PE}$	Parallel Enable (Active Low) Input	2 UL
P_0, P_1, P_2, P_3	Parallel Inputs	2/3 UL
CEP	Count Enable Parallel Input	1 UL
CET	Count Enable Trickle Input	2 UL
CP	Clock Active High Going Edge Input	2 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	6 UL
TC	Terminal Count Output	6 UL

CHARACTERISTICS

TYPICAL SPEED	25 MHz Counting Frequency
TYPICAL DELAY	CP to Q 18 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	300 mW

MODE SELECTION

$\overline{PE}$	CE (Count Enable)	MODE
H	H	Count Up
H	L	No Change
L	X	Presetting

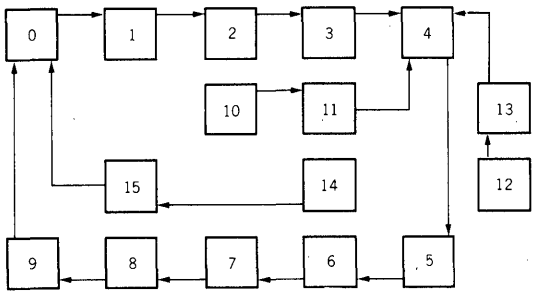
Where CE (Count Enable) = CEP · CET

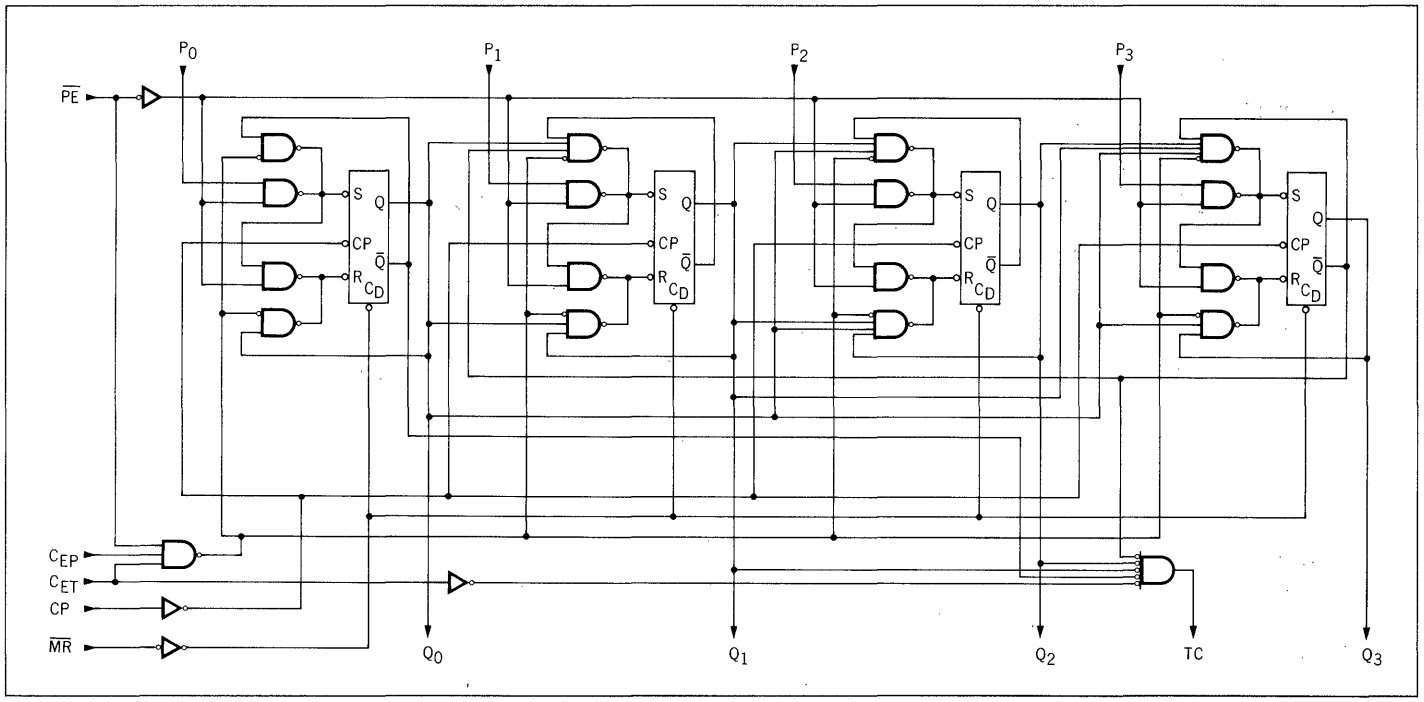
H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

LOGIC EQUATION FOR TERMINAL COUNT

$TC = CET \cdot Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$

STATE DIAGRAM





9316 4-BIT UP BINARY COUNTER

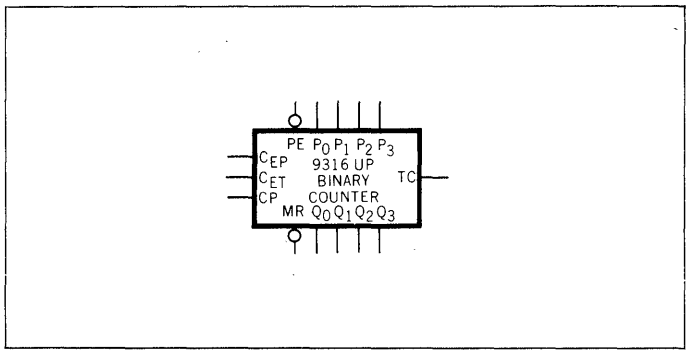
DESCRIPTION The 9316 is a 4–bit synchronous binary up counter. It has synchronous parallel load facility, overriding asynchronous master reset, and carry lookahead logic for high speed multistage operation.

The counter is synchronous, with the counter outputs changing state after the low to high transition of the clock. When conditions are satisfied for counting, a clock pulse will change the counter to the next state of a binary sequence. When the parallel enable is low the parallel inputs determine the next state of the counter synchronously with the clock.

Mode selection is accomplished as shown below. However a restriction is placed on the manner of selection. The transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high.

By utilizing the two count enable inputs and terminal count output, multi-stage synchronous counting is obtained, with operating speeds equivalent to that of a single stage.

When the asynchronous master reset is active outputs Q_{0-3} will be forced low regardless of all other input conditions.



MODE SELECTION

$\overline{PE}$	CE (Count Enable)	MODE
H	H	Count Up
H	L	No Change
L	X	Presetting

Where CE (Count Enable) = CEP · CET

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

LOGIC EQUATION FOR TERMINAL COUNT

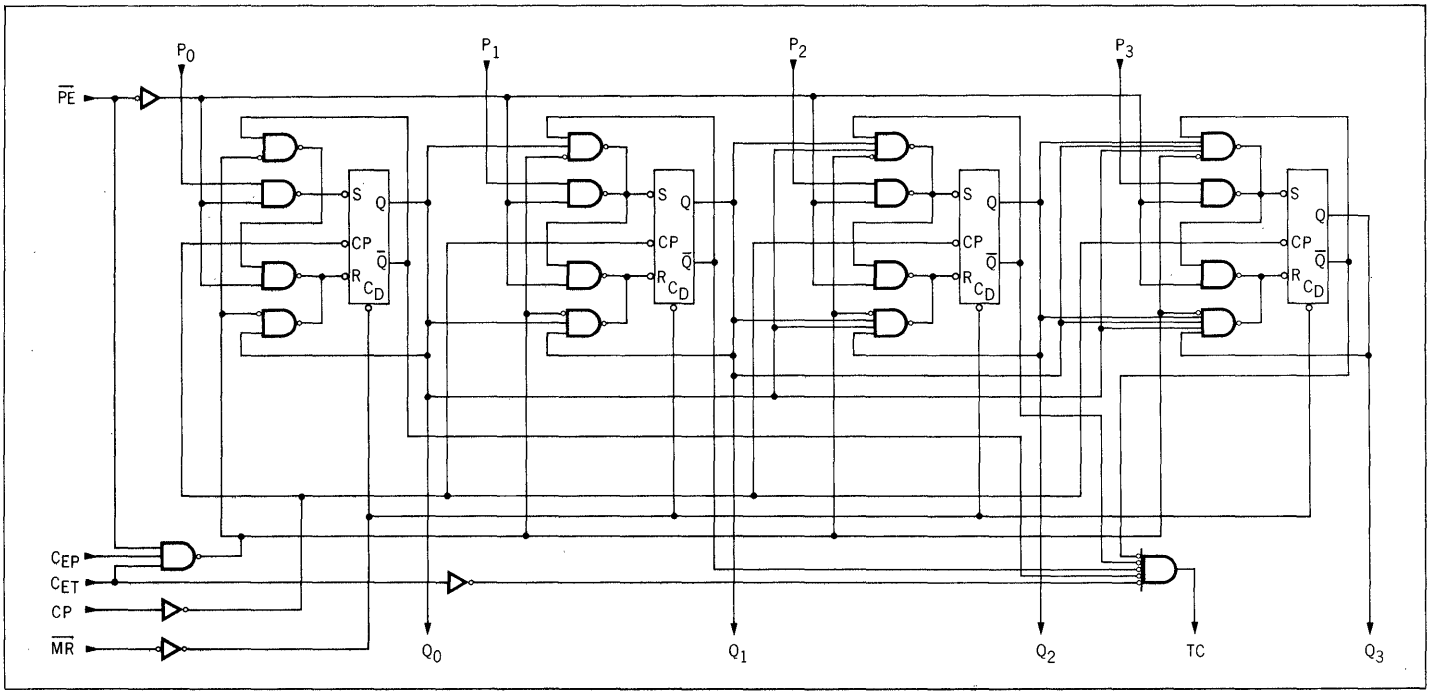
$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

PIN NAMES

		LOADING
$\overline{PE}$	Parallel Enable (Active Low) Input	2 UL
P_0, P_1, P_2, P_3	Parallel Inputs	2/3 UL
CEP	Count Enable Parallel Input	1 UL
CET	Count Enable Trickle Input	2 UL
CP	Clock Active High Going Edge Input	2 UL
$\overline{MR}$	Master Reset (Active Low) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	6 UL
TC	Terminal Count Output	6 UL

CHARACTERISTICS

TYPICAL SPEED	25 MHz Counting Frequency
TYPICAL DELAY	CP to Q 18 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	300 mW



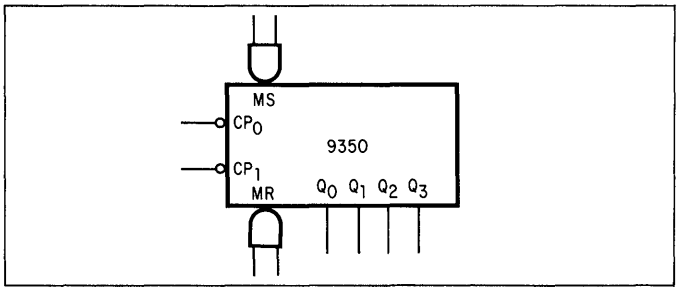
9350
DECADE COUNTER

DESCRIPTION The 9350 is an up decade counter. It consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. A gated "AND" master reset and "AND" master set are provided to inhibit count inputs and return all outputs to the low state and to a binary coded terminal count of nine, respectively. Since the output from the first flip-flop is not internally connected to the succeeding stages, the device may be operated in three independent count modes:

A. BCD Decade Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

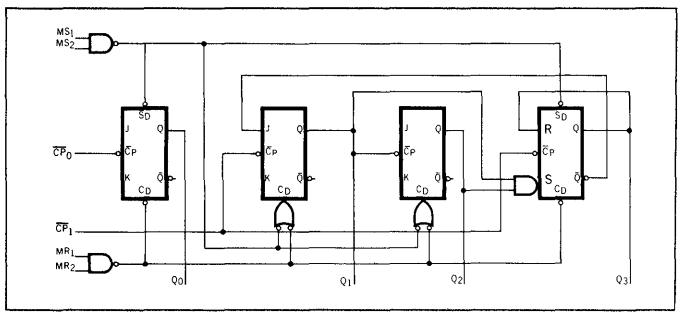
C. Divide-By-Two & Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. ($\overline{CP}_0$ as the input and Q_0 as the output.) The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_1, Q_2 and Q_3 outputs.



PIN NAMES		LOADING
$\overline{CP}_0$	Clock First Stage Negative Going Edge Input	2 UL
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input	4 UL
MR	"AND" Master Reset to Binary Zero (Asynchronous) Input	1 UL
MS	"AND" Master Set to Binary Nine (Asynchronous) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Counter Outputs	10 UL

CHARACTERISTICS

TYPICAL SPEED	18 MHz Counting Frequency
TYPICAL DELAY	$\overline{CP}_0$ to Q_2 60 ns
PACKAGE	14 Pin DIP (7A) Flat Pak (3B)
TYPICAL POWER DISSIPATION	160 mW

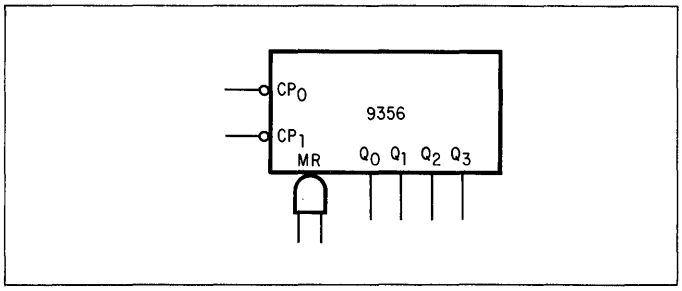


9356
BINARY COUNTER

DESCRIPTION The MSI 9356 is an up 4-bit binary counter. It consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated "AND" master reset is provided to inhibit the counting and return all outputs to a low state. Since the output from the first flop is not internally connected to the succeeding flip-flops, the device may be operated in two independent modes:

A. Four-Bit Ripple-Through Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

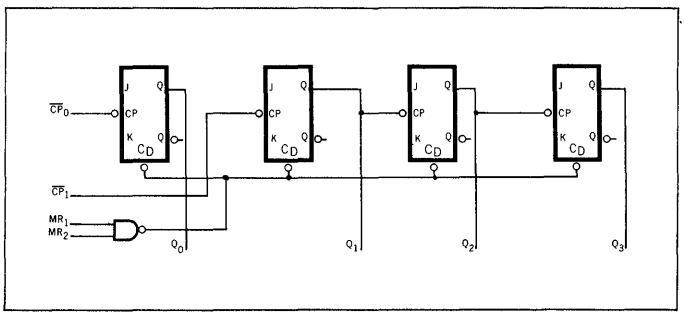
B. Three-Bit Ripple-Through Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.



PIN NAMES		LOADING
$\overline{CP}_0$	Clock First Stage Negative Going Edge Input	2 UL
$\overline{CP}_1$	Clock Second, Third, and Fourth Stage Negative Edge Input	4 UL
MR	"AND"Master Reset to Binary Zero (Asynchronous) Input	1 UL
Q_0, Q_1, Q_2, Q_3	Counter Outputs	10 UL

CHARACTERISTICS

TYPICAL SPEED	18 MHz Counting Frequency
TYPICAL DELAY	$\overline{CP}_0$ to Q_2 60 ns
PACKAGE	14 Pin DIP (7A) Flat Pak (3B)
TYPICAL POWER DISSIPATION	160 mW



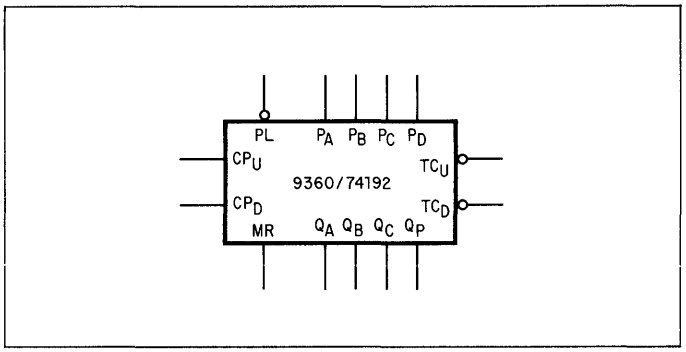
9360/54192, 74192
UP/DOWN DECADE COUNTER (DUAL CLOCK)

DESCRIPTION The MSI 9360/54192, 74192 is a synchronous up/down decade counter with separate up/down clocks, parallel load (asynchronous) facility, two terminal count outputs for multi-decade operation, and an asynchronous overriding master reset.

Counting is synchronous, with the outputs changing state after the low to high transition of either the count-up clock (CP_U) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is high. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are pulsed simultaneously.) The counter will respond to a clock pulse on either input by changing to the next state of the count sequence

The 9360 has a parallel load (asynchronous) facility which permits the counter to be preset. Whenever the parallel load ($\overline{PL}$) input is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D) will be loaded into the counter and appear on the outputs independent of the conditions of the clock inputs. When the parallel load input goes high this information is stored in the counter and when the counter is clocked it changes to the next appropriate state in the count sequence. The data inputs are inhibited when the parallel load is high and have no effect on the counter.

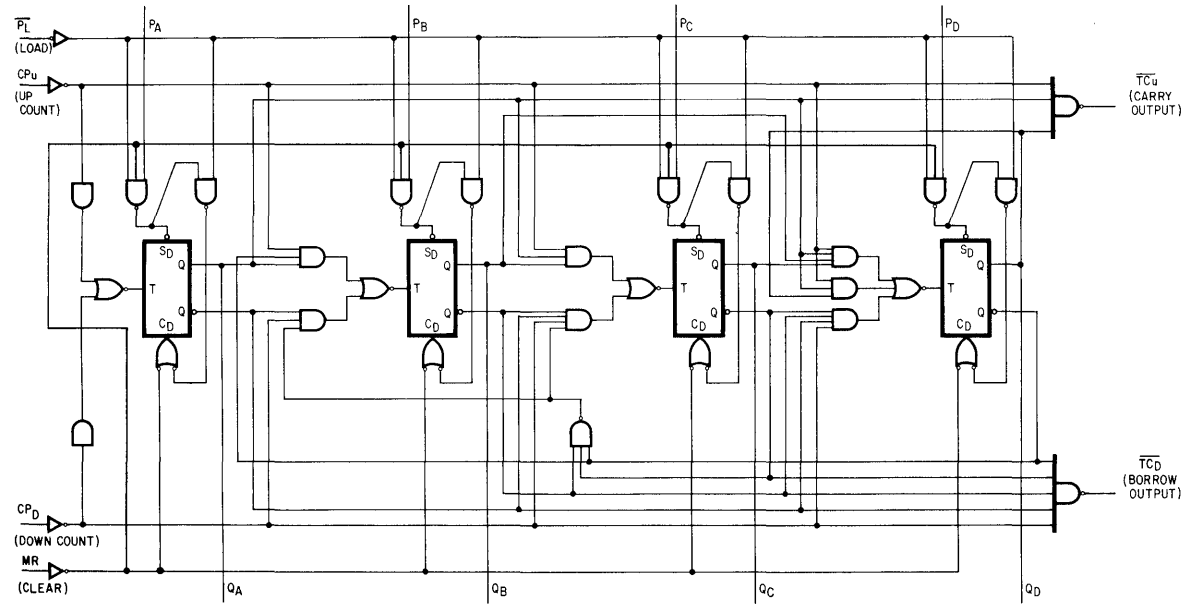
The terminal count-up ($\overline{TC}_U$) and terminal count-down ($\overline{TC}_D$) outputs (carry and borrow respectively) allow multidecade counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and terminal count-down output to the count-down clock input of the following counter.



PIN NAMES		LOADING
$\overline{PL}$	Parallel Load (Active Low) Input	1 UL
P_A, P_B, P_C, P_D	Parallel Data Inputs	1 UL
CP_U	Count Up Clock Pulse Input	1 UL
CP_D	Count Down Clock Pulse Input	1 UL
MR	Master Reset (Clear) Input (Asynchronous)	1 UL
Q_A, Q_B, Q_C, Q_D	Counter Outputs	10 UL
$\overline{TC}_U$	Terminal Count Up (Carry) Output	10 UL
$\overline{TC}_D$	Terminal Count Down (Borrow) Output	10 UL

CHARACTERISTICS

TYPICAL SPEED	30 MHz Counting Frequency
TYPICAL DELAY	CP to Q 30 ns
PACKAGE	16 Pin DIP (7B) and Flat Pack (4L)
TYPICAL POWER DISSIPATION	300 mW



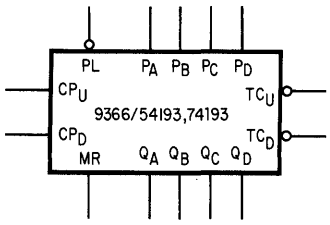
9366/54193, 74193
UP/DOWN 4-BIT BINARY COUNTER (DUAL CLOCK)

DESCRIPTION The 9366/54193, 74193 is a synchronous up/down 4-bit binary counter with separate up/down clocks, parallel load (asynchronous) facility, terminal count outputs for multidecade operation, and an asynchronous overriding master reset.

Counting is synchronous, with the outputs changing state after the low to high transition of either the count-up clock (CP_U) or count-down clock (CP_D). The direction of counting is determined by which clock input is pulsed while the other clock input is high. (Incorrect counting will occur if both the count-up clock and count-down clock inputs are pulsed simultaneously.) The counter will respond to a clock pulse on either input by changing to the next appropriate state of a binary sequence.

The 9366 has a parallel load (asynchronous) facility which permits the counter to be preset. Whenever the parallel load ($\overline{PL}$) input is low, the information present on the parallel data inputs (P_A, P_B, P_C, P_D) will be loaded into the counter and appear on the outputs independent of the conditions of the clock inputs. When the parallel load input goes high, this information is stored in the counter and when the counter is clocked it changes to the next appropriate state in the count sequence. The data inputs are inhibited when the parallel load is high and have no effect on the counter.

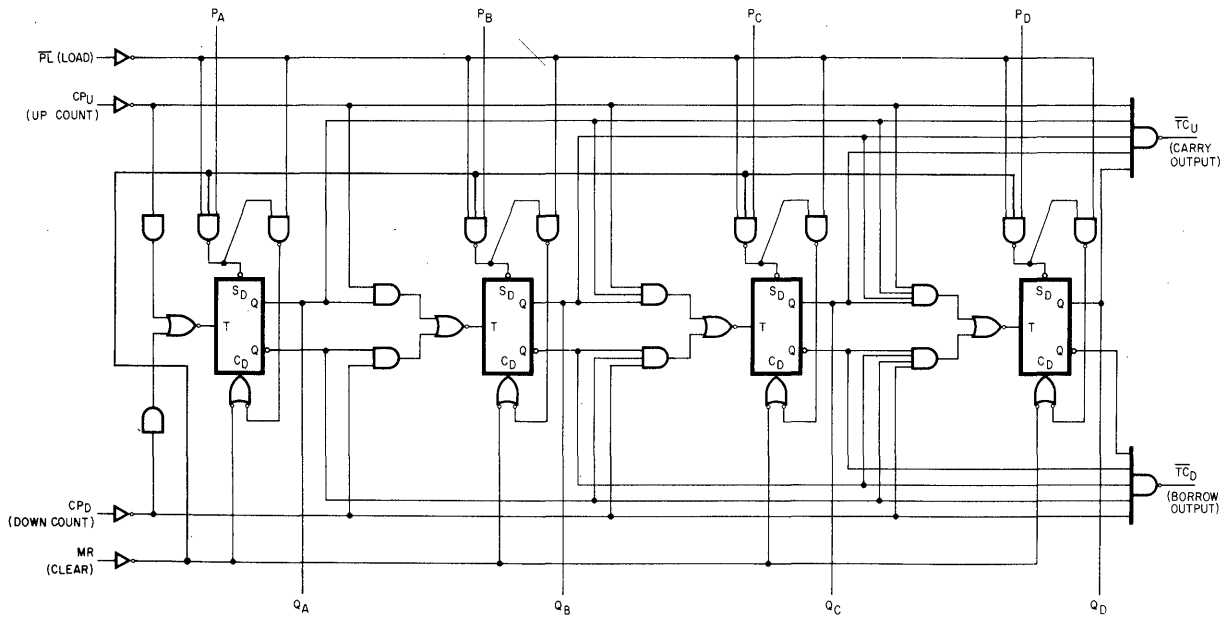
The terminal count-up ($\overline{TC}_U$) and terminal count-down ($\overline{TC}_D$) outputs (Carry and Borrow respectively) allow multistage binary counter operations without additional logic. The counters are cascaded by feeding the terminal count-up output to the count-up clock input and the terminal count-down output to the count-down clock input of the following counter.



PIN NAMES		LOADING
$\overline{PL}$	Parallel Load (Active Low) Input	1 UL
P_A, P_B, P_C, P_D	Parallel Data Inputs	1 UL
CP_U	Count Up Clock Pulse Input	1 UL
CP_D	Count Down Clock Pulse Input	1 UL
MR	Master Reset (Clear) Input (Asynchronous)	1 UL
Q_A, Q_B, Q_C, Q_D	Counter Outputs	10 UL
$\overline{TC}_U$	Terminal Count-Up (Carry) Output	10 UL
$\overline{TC}_D$	Terminal Count-Down (Borrow) Output	10 UL

CHARACTERISTICS

TYPICAL SPEED	30 MHz Counting Frequency
TYPICAL DELAY	CP to Q 30 ns
PACKAGE	16 Pin DIP (7B) or Flat Pak (4L)
TYPICAL POWER DISSIPATION	300 mW



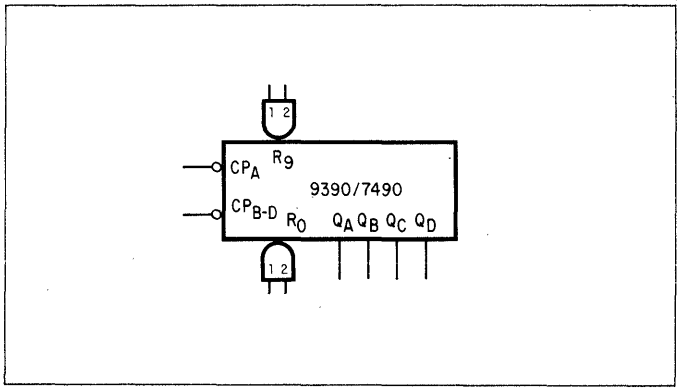
9390/5490, 7490
DECADE COUNTER

DESCRIPTION The 9390/5490, 7490 is a high speed, monolithic decade counter which consists of four dual rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Count inputs are inhibited, and all outputs are returned to logical zero or a binary coded decimal (BCD) count of 9 through gated direct reset lines. The output from flip-flop A is not internally connected to the succeeding stages, therefore, the count may be separated in these independent count modes:

A. If used as a binary coded decimal decade counter, the $\overline{CP}_{B-D}$ input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count for nine's complement decimal applications.

B. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the $\overline{CP}_{B-D}$ input and a divide-by-ten square wave is obtained at output A.

C. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The $\overline{CP}_{B-D}$ input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.



PIN NAMES

		LOADING
R_0	Reset-Zero Inputs	1 UL
R_9	Reset-Nine Inputs	1 UL
$\overline{CP}_A$	Clock Input	2 UL
$\overline{CP}_{B-D}$	Clock Input	4 UL
Q_A, Q_B, Q_C, Q_D	Outputs	10 UL

CHARACTERISTICS

CLOCK FREQUENCY	18 MHz
POWER DISSIPATION	160 mW
PACKAGE	14 Pin DIP (6A) or Flat Pak (3B)

TRUTH TABLES

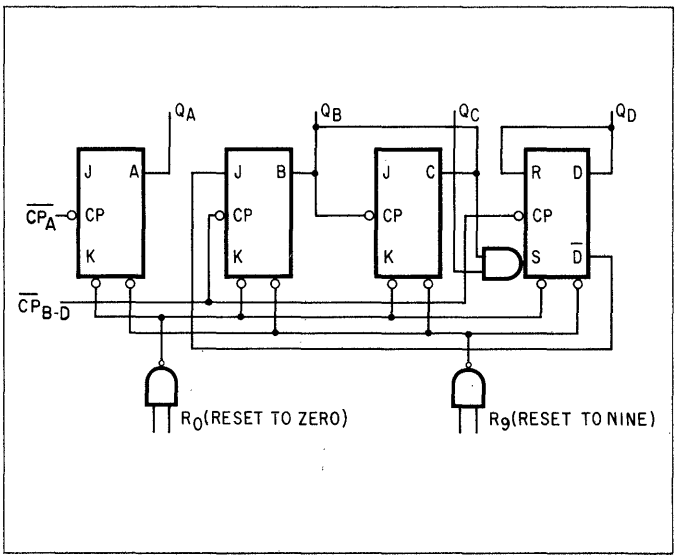
BCD COUNT SEQUENCE (See Note 1)

Count	Output			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

Reset Inputs				Output
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	Count
0	X	0	X	Count
0	X	X	0	Count
X	0	0	X	Count

NOTES: 1. Output A connected to input $\overline{CP}_{B-D}$ for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

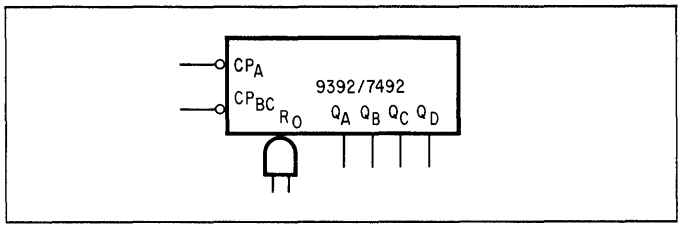


9392/5492,7492
DIVIDE BY TWELVE COUNTER

DESCRIPTION The 9392/5492, 7492 is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

A. When used as a divide-by-twelve counter, output Q_A must be externally connected to input $\overline{CP}_{BC}$. The input count pulses are applied to input $\overline{CP}_A$. Simultaneous divisions of 2, 6, and 12 are performed at the Q_A, Q_C, and Q_D outputs as shown in the truth table above.

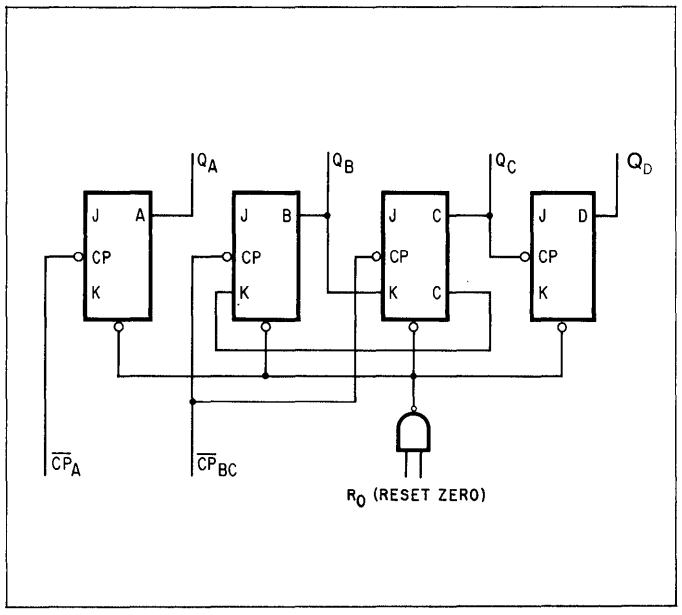
B. When used as a divide-by-six counter, the input count pulses are applied to input $\overline{CP}_{BC}$. Simultaneously, frequency divisions of 3 and 6 are available at the Q_C and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.



PIN NAMES		LOADING
R_0	Reset-Zero Inputs	1 UL
$\overline{CP}_A$	Clock Input	2 UL
$\overline{CP}_{BC}$	Clock Input	4 UL
Q_A, Q_B, Q_C, Q_D	Count Outputs	10 UL

CHARACTERISTICS

CLOCK FREQUENCY	18 MHz
POWER DISSIPATION	160 mW
PACKAGE	14 Pin DIP (6A) or Flat Pak (3B)

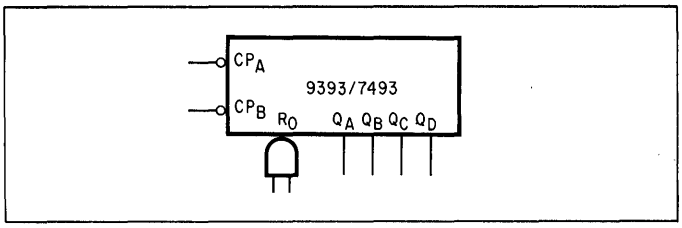


9393/5493,7493
BINARY COUNTER

DESCRIPTION The 9390/5493, 7493 is a high speed, monolithic 4-bit binary counter, consisting of four master-slave flip-flops interconnected internally to provide a divide-by-two counter and a divide-by-eight counter. Count inputs may be inhibited through the use of a gated direct reset line which simultaneously returns the four flip-flop outputs to a logical zero. The output from flip-flop A is not internally connected to the succeeding flip-flops, therefore it may be operated in two independent modes:

A. When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input CP_B. Input count pulses are applied to input CP_A. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs.

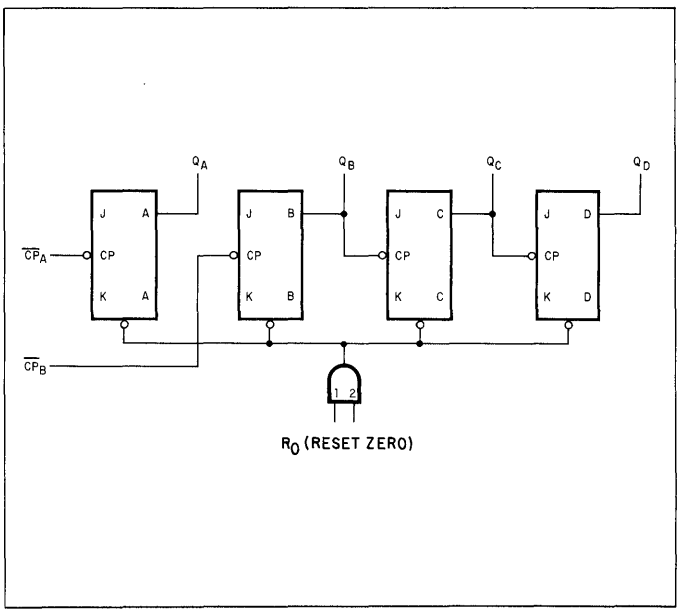
B. When used as a 3-bit ripple-through counter, the input count pulses are applied to input CP_B. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Flip-flop A may be used independently if the reset function coincides with the reset of the 3-bit ripple-through counter.



PIN NAMES		LOADING
R_0	Reset-Zero Input	1 UL
$\overline{CP}_A$	Clock Input	2 UL
$\overline{CP}_B$	Clock Input	2 UL
Q_A, Q_B, Q_C, Q_D	Output	10 UL

CHARACTERISTICS

CLOCK FREQUENCY	18 MHz
POWER DISSIPATION	160 mW
PACKAGE	14 Pin DIP (6A) or Flat Pak (3B)

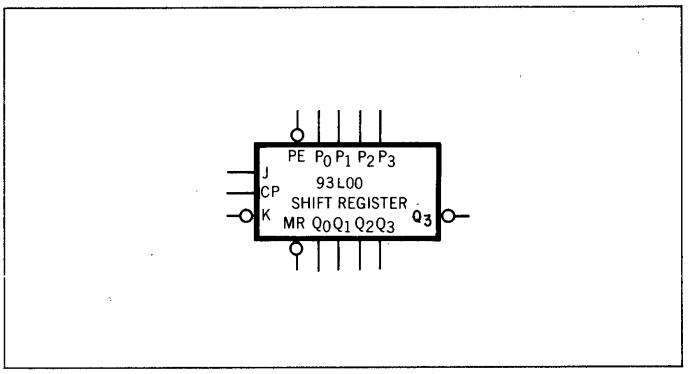


93L00
4-BIT UNIVERSAL SHIFT REGISTER

DESCRIPTION The 93L00 is a synchronous 4 bit shift register designed to perform functions such as storage, shifting, counting and serial code conversion. It has assertion outputs on each stage and a negation output on the last stage, an overriding asynchronous master reset, $J\overline{K}$ input configuration, and a synchronous parallel load facility.

Data entry is synchronous with the registers changing state after each low to high transition of the clock. With the parallel enable low the parallel inputs determine the next condition of the shift register. When the parallel enable input is high the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through $J\overline{K}$ inputs. By tying the two inputs together D type entry is obtained.

The asynchronous active low master reset when activated overrides all other input conditions and clears the register.



PIN NAMES		LOADING
$\overline{PE}$	Parallel Enable (Active Low) Input	.57 UL
P_0, P_1, P_2, P_3	Parallel Inputs	.25 UL
J	First Stage J (Active High) Input	.25 UL
$\overline{K}$	First Stage K (Active Low) Input	.25 UL
CP	Clock Active High Going Edge Input	.5 UL
$\overline{MR}$	Master Reset (Active Low) Input	.25 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	2.0 UL
$\overline{Q_3}$	Complementary Last Stage Output	2.0 UL

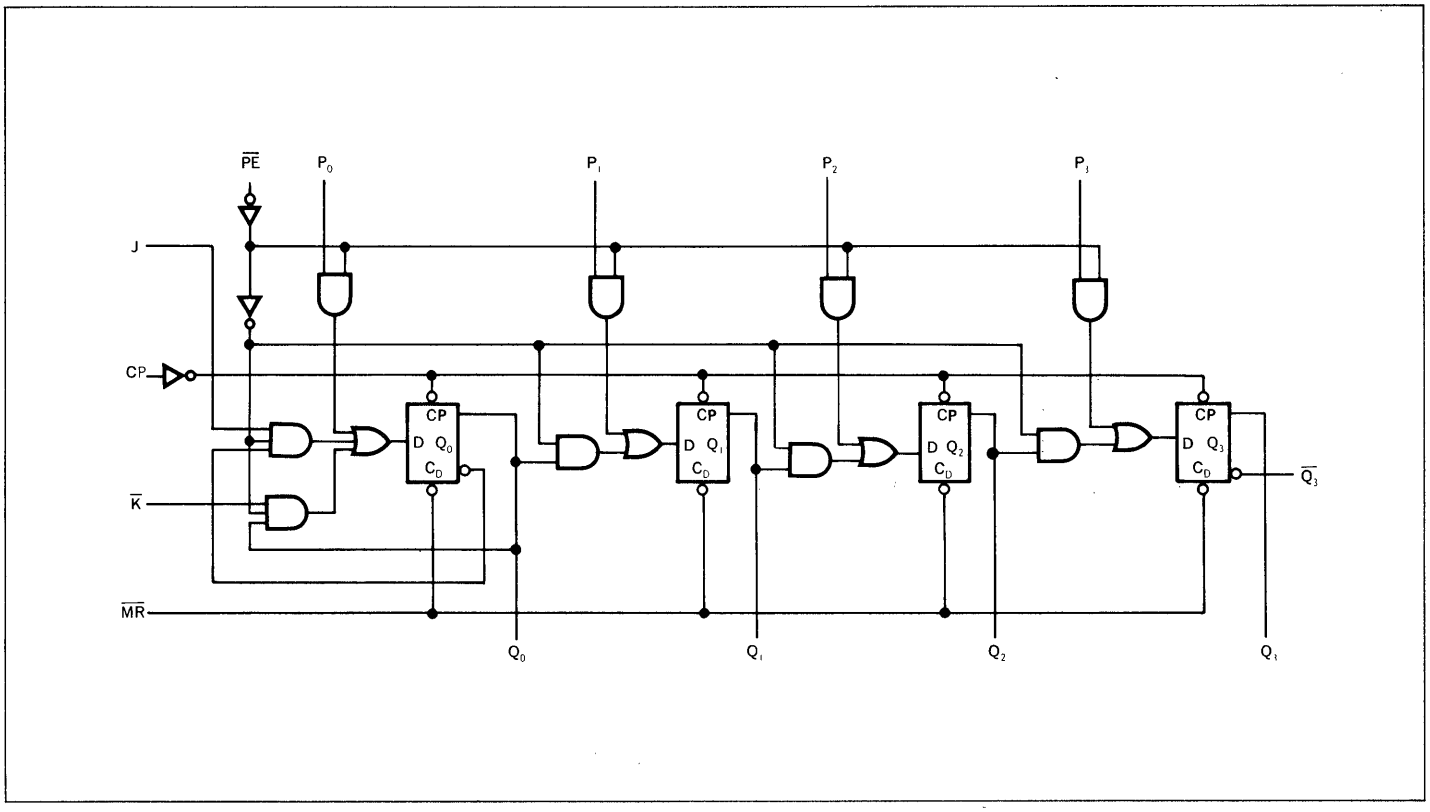
TRUTH TABLE FOR SERIAL ENTRY

J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	$\overline{Q}_0$ at t_n (toggles)
H	H	H

$\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH, (n + 1) indicates state after next clock

CHARACTERISTICS

TYPICAL SPEED	10 MHz Shifting Frequency
TYPICAL DELAY	CP to Q 60 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	75 mW

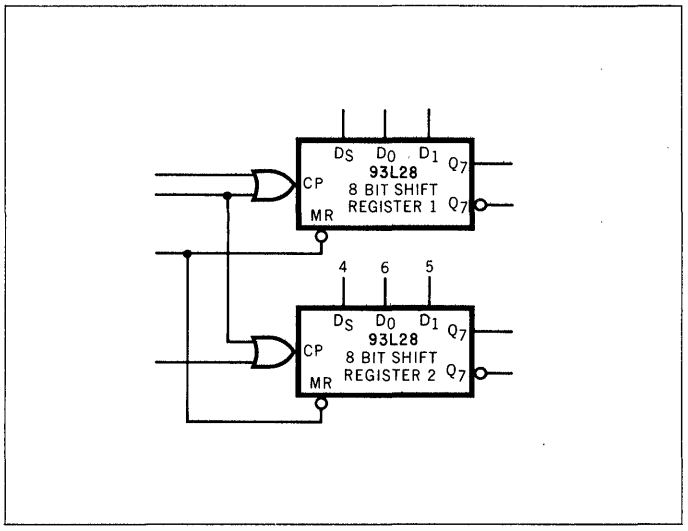


93L28 DUAL 8-BIT SHIFT REGISTER

DESCRIPTION The 93L28 is a Dual 8-bit synchronous shift register which can be used in high speed serial storage applications. Each register has a true and complemented output from the last stage, 2-input multiplexer with data select control at the input, and a two input clock OR gate input. A common clock, obtained by internally tying one input of each clock OR gate together, and overriding asynchronous master reset are common to both registers.

Data entry is synchronous with the registers changing state after each low to high transition of the clock. Serial data enters through D_0 when the data select line is low and through D_1, when the data select line is high. The clocking scheme employed allows the three clock inputs to be used in the following ways: one clock common with two separate clocks; one clock common with a separate active low clock enable input for each 8 bit shift register, and two separate clocks and one common active low clock enable input.

The asynchronous active low master reset when activated overrides all other input conditions and clears the register.



LOGIC EQUATION FOR DATA ENTRY

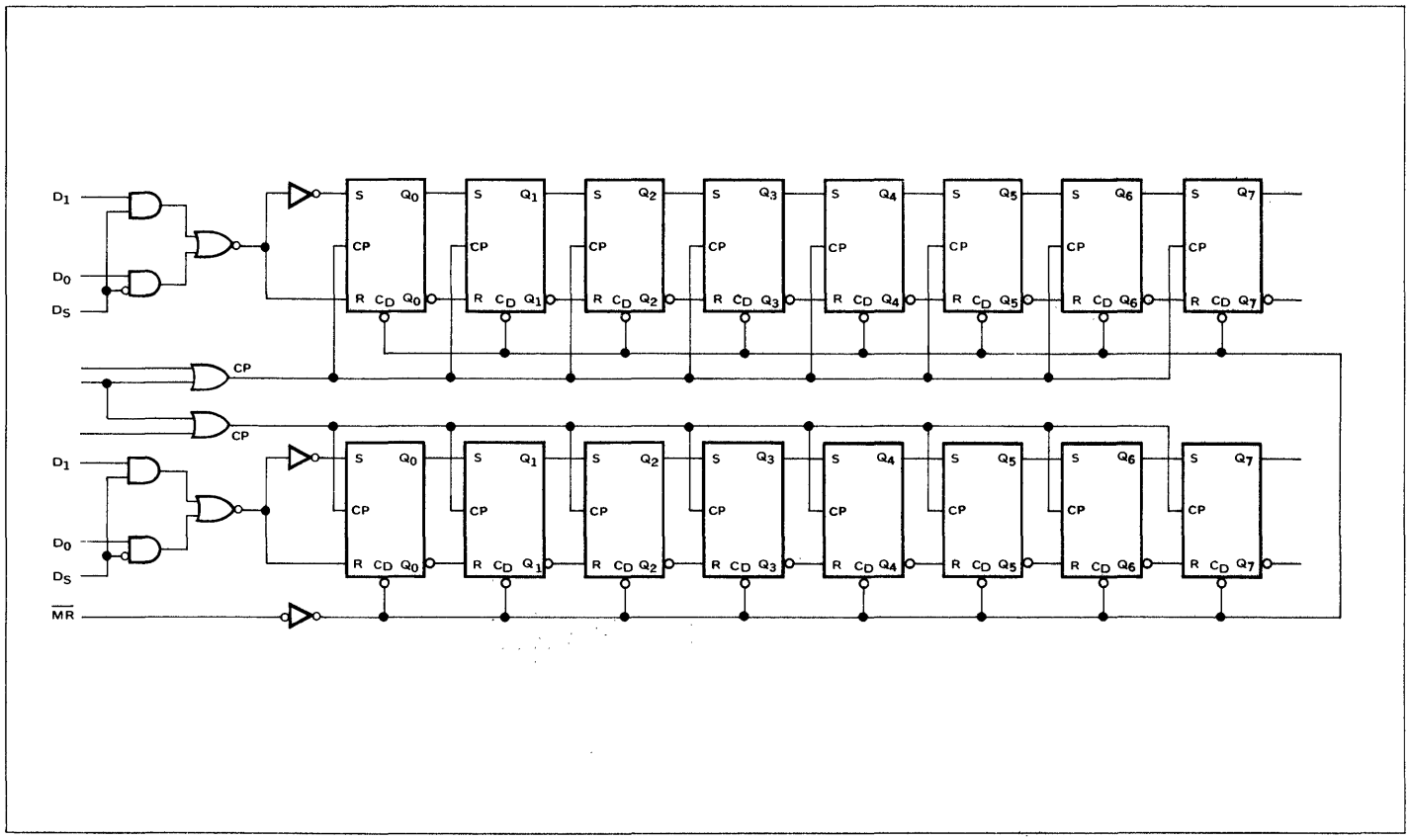
$$S_D = \overline{D_S} \cdot D_0 + D_S \cdot D_1$$

CHARACTERISTICS

TYPICAL DELAY	CP to Q	56 ns
TYPICAL SPEED	10MHz	Shifting Frequency
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	75 mW	

PIN NAMES

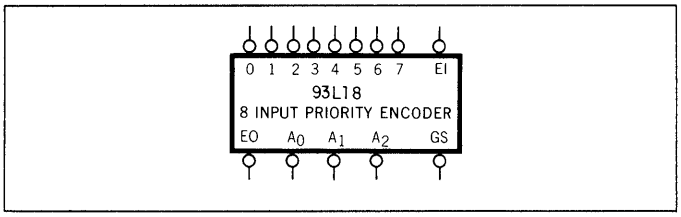
		LOADING
D_S	Data Select Input	.50 UL
D_0, D_1	Data Inputs	.25 UL
CP	OR Clock Active High Going Edge Inputs	
	Common	.75 UL
	Separate	.37 UL
$\overline{MR}$	Master Reset (Active Low) Input	.25 UL
Q_7	Last Stage Output	2.0 UL
$\overline{Q_7}$	Complementary Output	2.0 UL

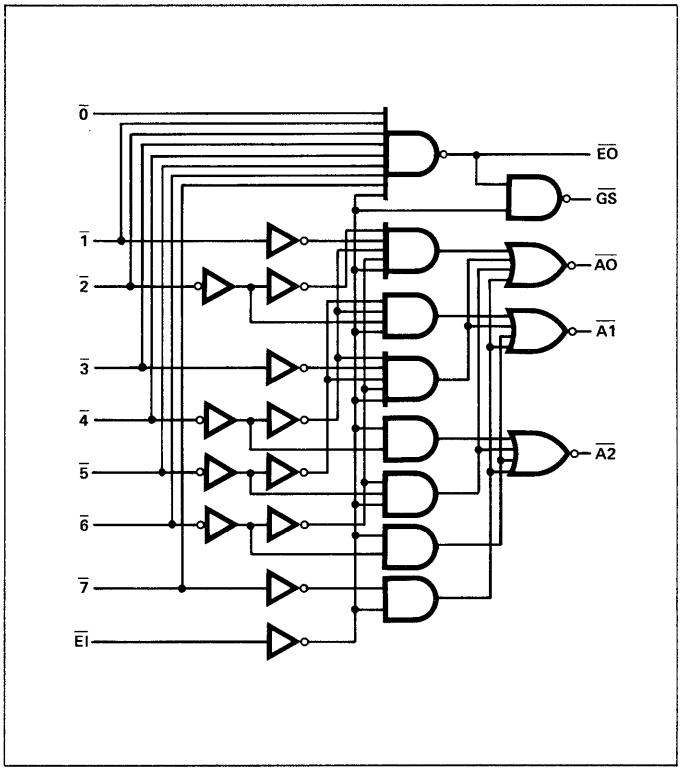


93L18 8-INPUT PRIORITY ENCODER

DESCRIPTION The 93L18 is a multipurpose encoder designed to accept 8 active low inputs and produce a binary weighted output code of the highest order input. A priority is assigned to each active low input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input $\overline{7}$ having the highest priority.

An active low enable input ($\overline{EI}$) and active low enable output ($\overline{EO}$) are provided to expand priority encoding to more inputs. This is accomplished by connecting the more significant encoders enable output ($\overline{EO}$) to the next less significant encoder enable input ($\overline{EI}$). In addition a group signal is provided which is active if any input is active and $\overline{EI}$ is low.





PIN NAMES		LOADING
$\overline{0}$	Priority (Active Low) Input	.25 UL
$\overline{1}$ to $\overline{7}$	Priority (Active Low) Inputs	.5 UL
$\overline{EI}$	Enable (Active Low) Input	.5 UL
$\overline{EO}$	Enable (Active Low) Output	1.25 UL
$\overline{GS}$	Group Select (Active Low) Output	1.5 UL
$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$	Address (Active Low) Outputs	2.5 UL

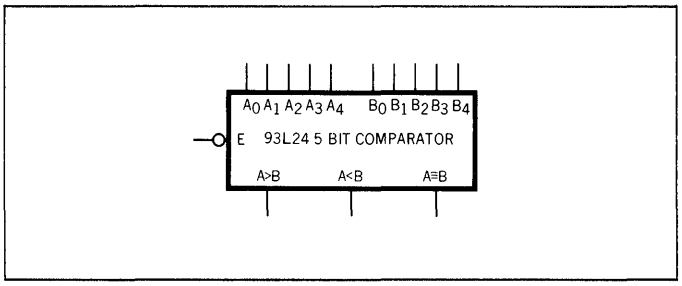
CHARACTERISTICS

TYPICAL DELAY	$\overline{1}$ to $\overline{A}$ 55 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	70 mW

93L24
5-BIT COMPARATOR

DESCRIPTION The 93L24 is a low power expandable comparator which provides comparison between two 5-bit words and gives three outputs, "less than," "greater than," and "equal to." A high level on the active low enable input forces all three outputs low.

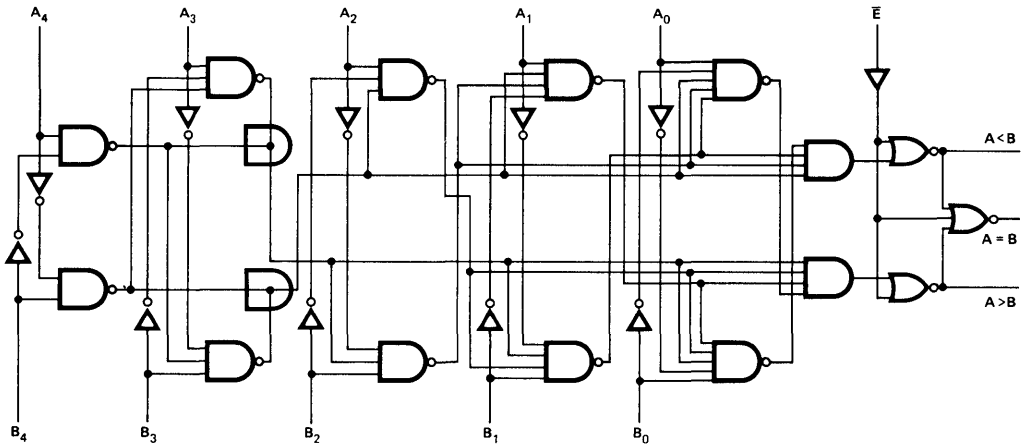
Words of more than 5 bits may be compared by either connecting 93L24 comparators in series; this is done by connecting the A>B and A<B outputs to the A_0, B_0 inputs respectively of the next stage, or by connecting comparators in parallel, and comparing the outputs with another 93L24.



PIN NAMES		LOADING
$\overline{E}$	Enable (Active Low) Input	.5 UL
A_0, A_1, A_2, A_3, A_4	Word A Parallel Inputs	.5 UL
B_0, B_1, B_2, B_3, B_4	Word B Parallel Inputs	.5 UL
A < B	A Less than B Output	2.25 UL
A > B	A Greater Than B Output	2.25 UL
A = B	A Equal to B Output	2.5 UL

CHARACTERISTICS

TYPICAL DELAY	Data to A > B 55 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION	55 mW

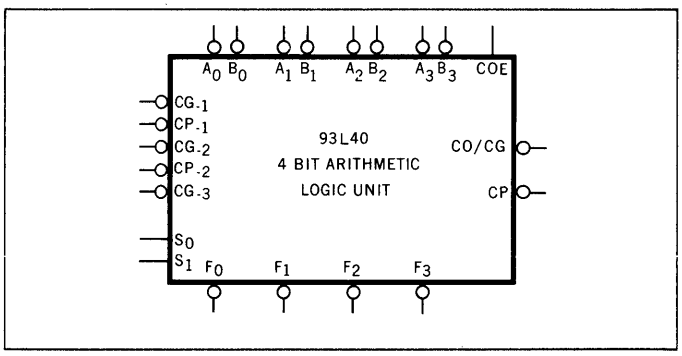


93L40 4-BIT ARITHMETIC LOGIC UNIT

DESCRIPTION The 93L40 is a low power arithmetic logic unit which can perform the arithmetic operations add and subtract on two 4-bit parallel binary words which are represented in 1's, 2's complement or sign magnitude notation. The unit can also perform two logic functions, the actual functions depending upon the polarity of the input operands. These functions, which are controlled by two select inputs, S_0, S_1, are shown for active low input operands below.

The 93L40 incorporates full carry lookahead internally for the 4 bits and provision for external lookahead by using the carry lookahead functions CP (carry propagate) and CG/CO (carry generate/carry out). The input carry network enables full external carry lookahead over 16 bits and provides for rippling between additional blocks of 12 bits, without additional gates or special carry lookahead IC's. This ripple block method is operated under control of a COE (carry out enable) input which changes the carry generate into a carry out signal. The delay for various word lengths using the built-in carry lookahead circuitry is given below.

The CP (carry propagate) and CG (carry generate) functions can also be used with appropriate gating to give all 0's and all 1's detection, and generate functions A > B, A ≥ B, and overflow indication.



CHARACTERISTICS

TYPICAL DELAYS	Addition Over 4 Bits 85ns Addition Over 16 Bits 135ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)
TYPICAL POWER DISSIPATION	110 mW

PIN NAMES

		LOADING
$\bar{A}_0$, to $\bar{A}_3$, $\bar{B}_0$ to $\bar{B}_3$	Operand (Active Low) Inputs	.75 UL
S_0, S_1	Mode Select Inputs	.25 UL
$\overline{CG}_{-1}$	First Stage Carry Generate (Active Low) Input	.75 UL
$\overline{CP}_{-1}$	First Stage Carry Propagate (Active Low) Input	.25 UL
$\overline{CG}_{-2}$	Second Stage Carry Generate (Active Low) Input	.5 UL
$\overline{CP}_{-2}$	Second Stage Carry Propagate (Active Low) Input	.25 UL
$\overline{CG}_{-3}$	Third Stage Carry Generate (Active Low) Input	.25 UL
COE	Carry Out Enable Input	.375 UL
$\bar{F}_0$, $\bar{F}_1$, $\bar{F}_2$, $\bar{F}_3$	Function (Active Low) Outputs	.25 UL
$\overline{CO/CG}$	Carry Out/Carry Generate (Active Low) Output	.25 UL
$\overline{CP}$	Carry Propagate (Active Low) Output	.25 UL

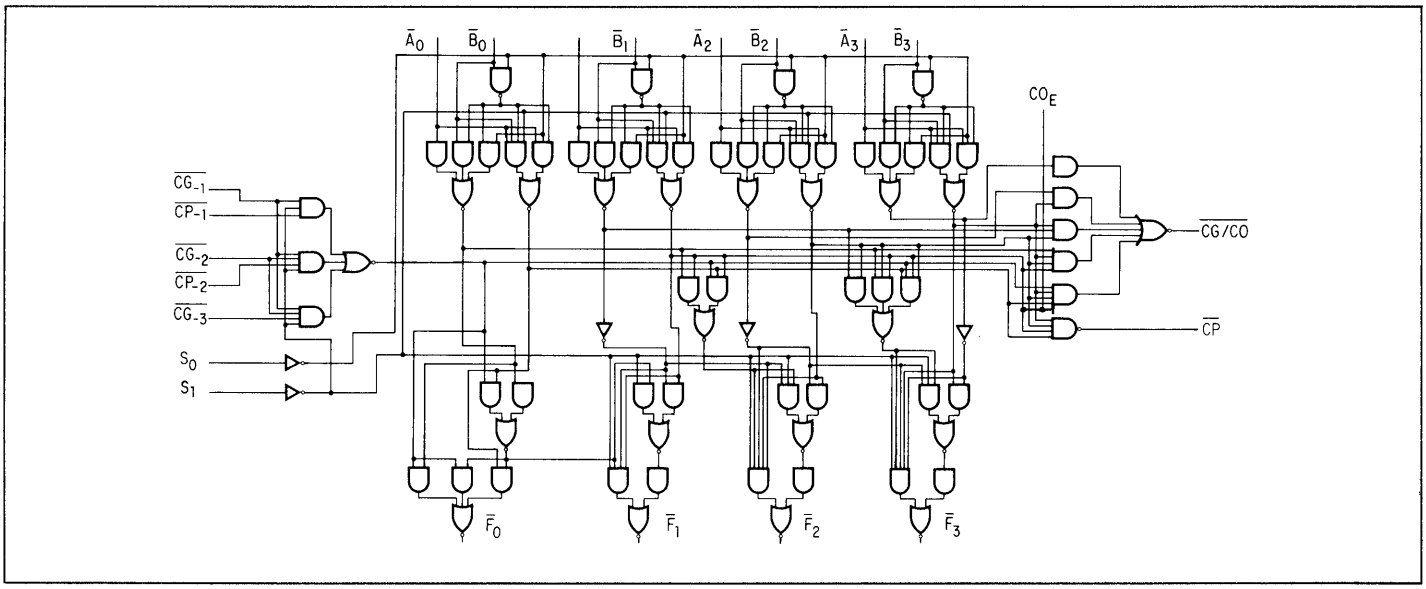
FUNCTION TABLE ACTIVE LOW OPERANDS

S_0	S_1	FUNCTION		
L	L	A	SUBTRACT	B
H	L	A	ADD	B
L	H	A	EX OR	B
H	H	A	AND	B

H = High Voltage Level
L = Low Voltage Level

DELAY TABLE

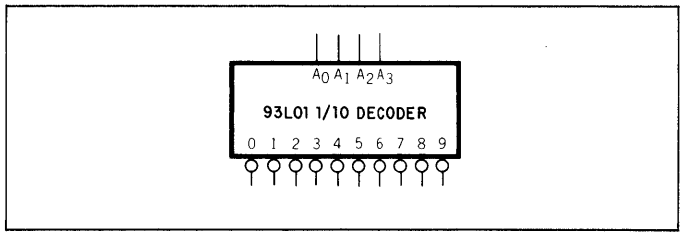
WORD LENGTH (in bits)	ADD (in ns)	SUBTRACT (in ns)
1–4	85	95
5–16	135	145
17–28	185	195
29–40	235	245
41–52	285	295
53–64	335	345



93L01
ONE OF TEN DECODER

DESCRIPTION The 93L01 accepts four binary weighted inputs and provides one of ten mutually exclusive active low outputs. When a binary code greater than nine is applied, all outputs are high. This facilitates BCD to decimal conversions and eight channel demultiplexing and decoding. The active low decoder outputs are compatible with the low enables of other MSI elements making the 93L01 useful in logic selection schemes.

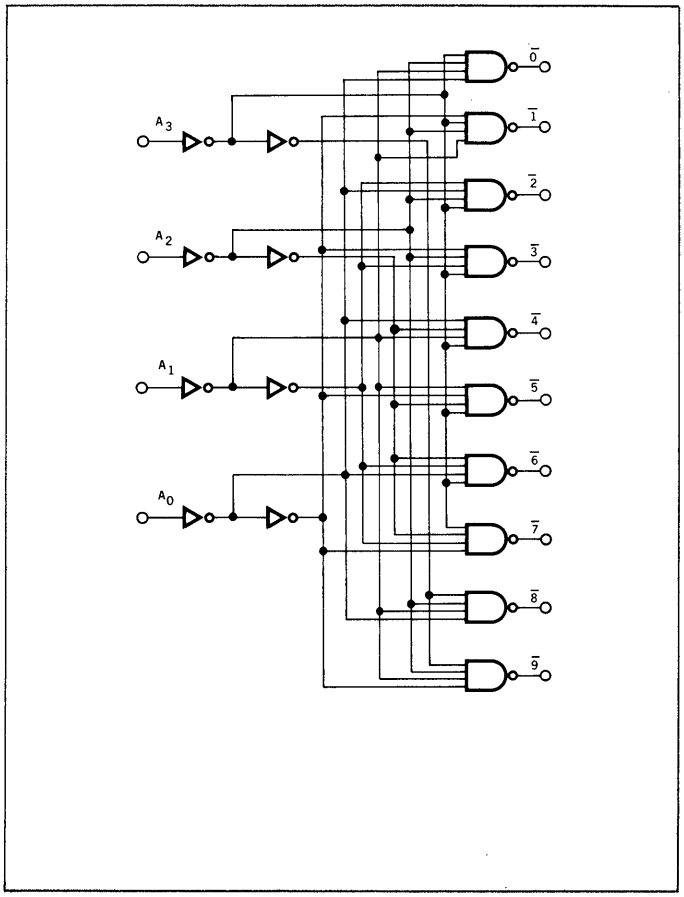
The 93L01 can serve as a one of eight decoder with an active low enable, the A_3 input acting as the active low enable. Eight channel demultiplexing results when data is applied to the A_3 input and the desired output is addressed by A_0, A_1, A_2.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	.25 UL
$\overline{0}$ to $\overline{9}$	Outputs (Active Low)	2.5 UL

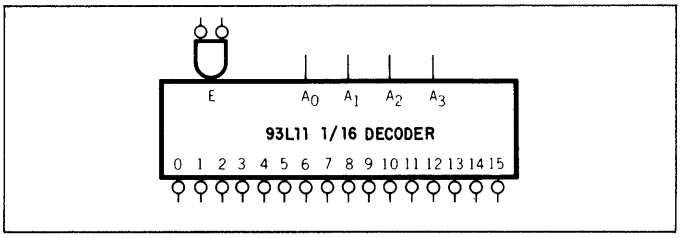
CHARACTERISTICS

TYPICAL DELAY	A to Output 63 ns
PACKAGE	16 Pin Dip (7B) and Flatpack (4L)
TYPICAL POWER DISSIPATION	35 mW



93L11
ONE OF SIXTEEN DECODER

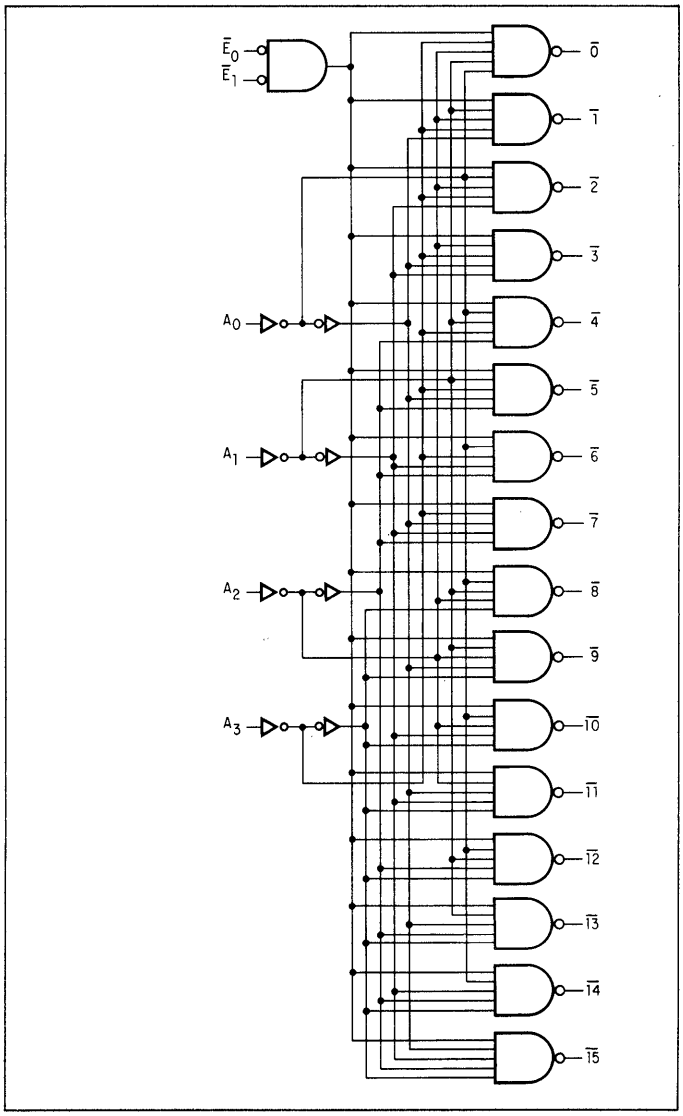
DESCRIPTION The 93L11 one of sixteen decoder accepts four binary weighted inputs and provides one low output corresponding to the input code.



PIN NAMES		LOADING
A_0, A_1, A_2, A_3	Address Inputs	.25 UL
$\overline{E_0}$, $\overline{E_1}$	AND Enable (Active Low) Inputs	.25 UL
$\overline{0}$ to $\overline{15}$	(Active Low) Outputs	2.5 UL

CHARACTERISTICS

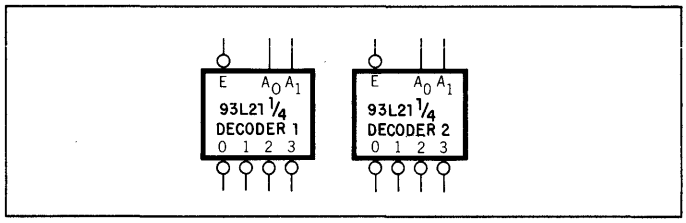
TYPICAL DELAYS	$\overline{A}$ to Output 70 ns $\overline{E}$ to Output 48 ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)
TYPICAL POWER DISSIPATION	40 mW



93L21 DUAL ONE OF FOUR DECODERS

DESCRIPTION The 93L21 consists of two independent one of four decoders, each with an active low enable. Each decoder accepts two inputs and provides one of four mutually exclusive active low outputs. An active low enable is provided on each decoder which must be low for any output to be low.

Each decoder can be used as a 4 output demultiplexer by using the enable line as a data input.



PIN NAMES		LOADING
Decoder 1 and 2		
$\overline{E}$	Enable (Active Low) Input	.25 UL
A_0, A_1	Address Inputs	.25 UL
$\overline{0}$, $\overline{1}$, $\overline{2}$, $\overline{3}$	(Active Low) Outputs	2.5 UL

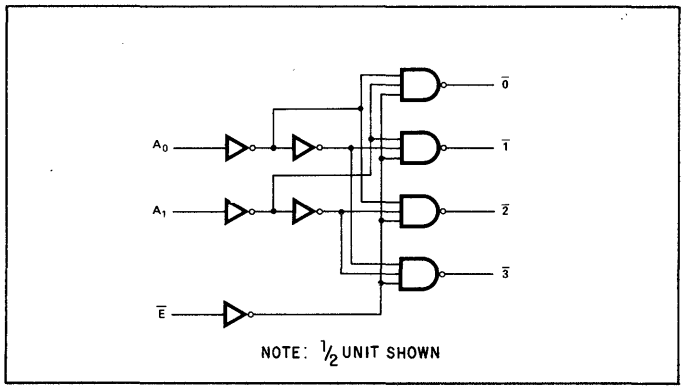
CHARACTERISTICS

TYPICAL DELAY	A to Output	49 ns
	$\overline{E}$ to Output	38 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	40 mW	

TRUTH TABLE

$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

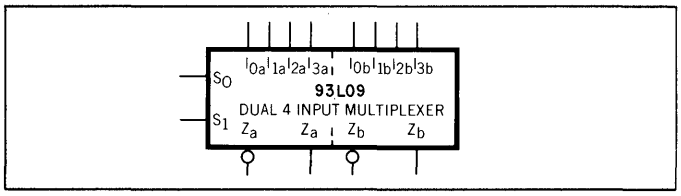


NOTE: 1/2 UNIT SHOWN

93L09 DUAL FOUR-INPUT MULTIPLEXER

DESCRIPTION The 93L09 consists of two 4-input multiplexers with common input select logic. It allows two bits of data to be switched in parallel to the appropriate outputs from two 4 bit data sources. Both polarities of outputs are available.

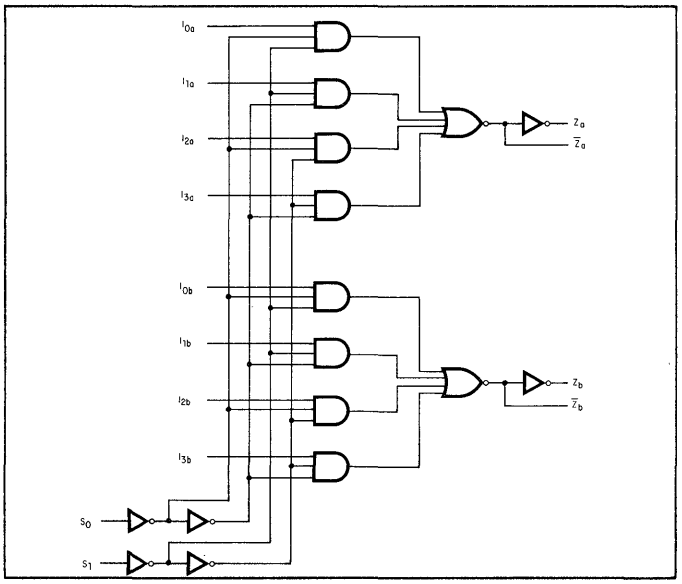
An obvious use of the 93L09 is the moving of data from a group of registers to a common output buss. The particular register from which the data comes is determined by the state of the select inputs. A less obvious use is as a function generator. The 93L09 can generate two functions of three variables. This is useful for implementing random gating functions.



PIN NAMES		LOADING
S_0, S_1	Common Select Inputs	.25 UL
Multiplexer A		
I_{0a}, I_{1a}, I_{2a}, I_{3a}	Multiplexer Inputs	.25 UL
Z_a	Multiplexer Output	2.5 UL
$\overline{Z}_a$	Complementary Multiplexer Output	2.25 UL
Multiplexer B		
I_{0b}, I_{1b}, I_{2b}, I_{3b}	Multiplexer Inputs	.25 UL
Z_b	Multiplexer Output	2.5 UL
$\overline{Z}_b$	Complementary Multiplexer Output	2.25 UL

CHARACTERISTICS

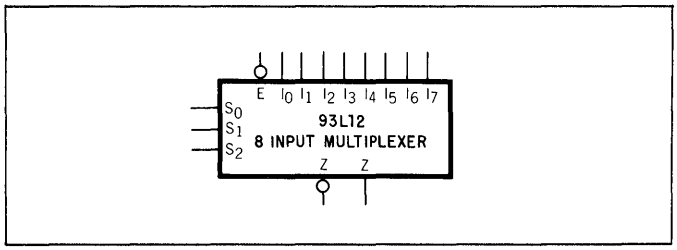
TYPICAL DELAYS	S to Z	48 ns
PACKAGE	16 Pin Dip (6B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	40 mW	



93L12
8-INPUT MULTIPLEXER

DESCRIPTION The 93L12 is an 8-input multiplexer which can select one bit of data from up to eight sources. It has complementary outputs, active low enable, and internal select decoding. With the enable inactive, the multiplexer output is low and the complementary multiplexer output high regardless of all input conditions. Data is routed from a particular multiplexer input to the outputs according to the three input binary code applied to the select inputs.

The 93L12 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 93L12 can provide any logic function of four variables and its negation.



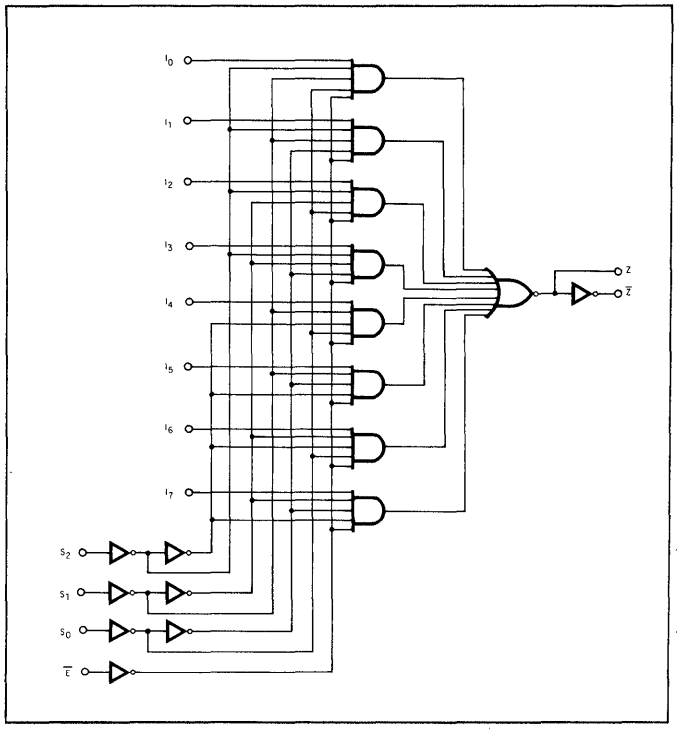
PIN NAMES		LOADING
S_0, S_1, S_2	Select Inputs	.25 UL
$\overline{E}$	Enable (Active Low) Input	.25 UL
I_0 to I_7	Multiplexer Inputs	.25 UL
Z	Multiplexer Output	2.5 UL
$\overline{Z}$	Complementary Multiplexer Output	2.25 UL

CHARACTERISTICS

TYPICAL DELAYS S to Z 80 ns

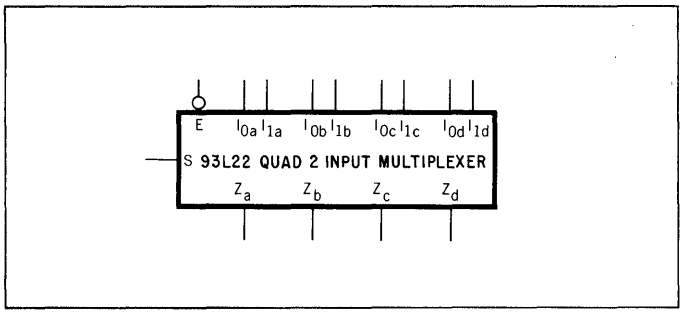
PACKAGE 16 Pin Dip (7B) or Flat Pack (4L)

TYPICAL POWER DISSIPATION 34 mW



93L22 QUAD
2-INPUT MULTIPLEXER

DESCRIPTION The 93L22 consists of four 2-input multiplexers with common input select logic, common active low enable and active high outputs. It allows four bits of data to be switched in parallel to the appropriate outputs from four 2-bit data sources. When the enable is not active, all the outputs are held low.



PIN NAMES		LOADING
S	Common Select Input	.25 UL
$\overline{E}$	Enable (Active Low) Input	.25 UL
Multiplexers A, B, C, D		
I_0, I_1	Multiplexer Inputs	.25 UL
Z	Multiplexer Output	2.5 UL

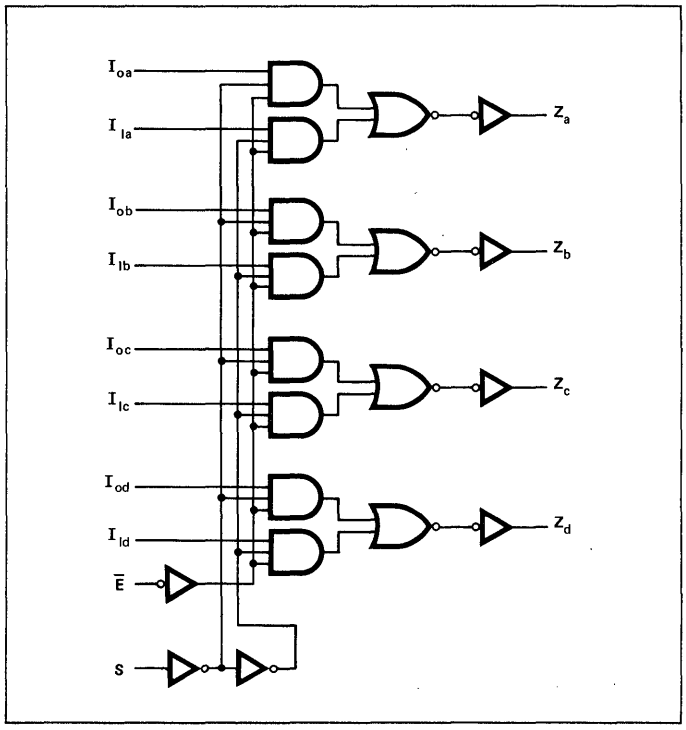
CHARACTERISTICS

TYPICAL DELAYS

S to Z 44 ns

PACKAGE 16 Pin Dip (7B) or Flat Pack (4L)

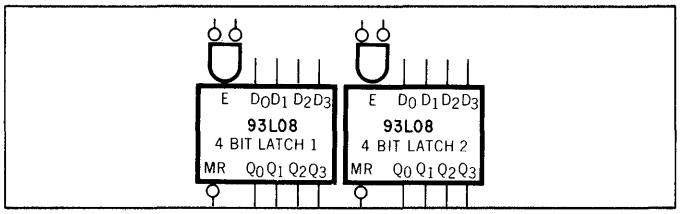
TYPICAL POWER DISSIPATION 45 mW



93L08
DUAL 4-BIT LATCH

DESCRIPTION The 93L08 consists of two separate 4-bit latch sections which provide high speed parallel gated data storage. Each 4-bit latch section has four assertion outputs, overriding master reset, and a two-input active low AND enable.

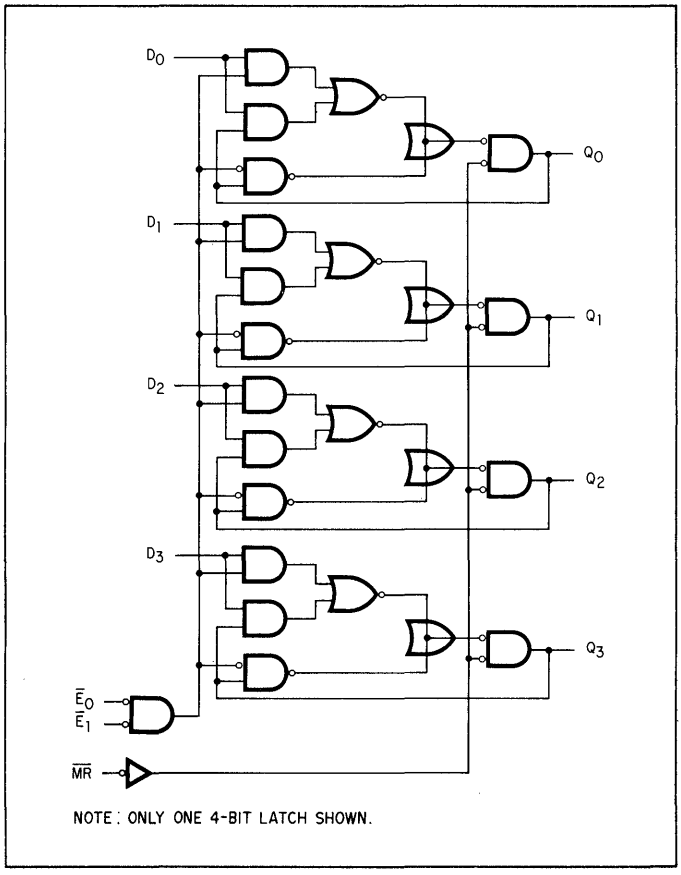
Data enters a latch when both enable inputs are low. As long as this logic condition exists, the output of the latch will follow the input. If either of the enable inputs go high, the data present in the latch at that time is held in the latch and is no longer affected by the data input. Active low master reset overrides all other input conditions and when activated forces the outputs of all the latches low.



PIN NAMES		LOADING
D_0, D_1, D_2, D_3	Parallel Latch Inputs	.37 UL
$\overline{E}_0$, $\overline{E}_1$	AND Enable (Active Low) Inputs	.25 UL
$\overline{MR}$	Master Reset (Active Low) Input	.25 UL
Q_0, Q_1, Q_2, Q_3	Parallel Latch Outputs	2.25 UL

CHARACTERISTICS

TYPICAL DELAYS	$\overline{E}$ to Output	53 ns
	D to Output	45 ns
PACKAGE	24 Pin Dip (6N) or Flat Pack (4M)	
TYPICAL POWER DISSIPATION	90 mW	



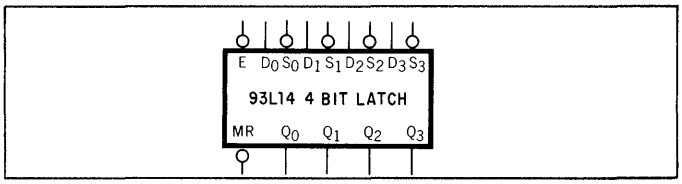
NOTE: ONLY ONE 4-BIT LATCH SHOWN.

93L14
4-BIT LATCH

DESCRIPTION The 93L14 is a 4 bit latch which can be used in applications where D type latches or set/reset latches are required. The latches have assertion outputs, a common active low enable and overriding active low master reset.

When the common enable goes high data present in the latches is stored and the state of the latches is no longer affected by the $\overline{S}$ and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs low.

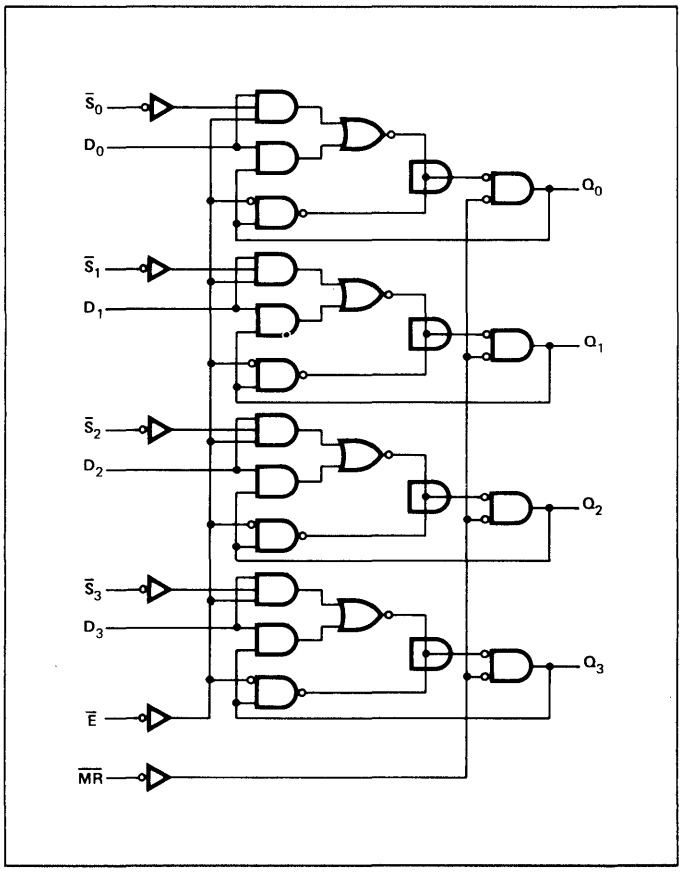
Each of the four latches can be operated either as an active low set/reset latch with reset override or, with $\overline{S}$ low, a D type storage latch.



PIN NAMES		LOADING
$\overline{E}$	(Active Low) Enable Input	.25 UL
D_0, D_1, D_2, D_3	Parallel Data Inputs	.37 UL
$\overline{S}_0$, $\overline{S}_1$, $\overline{S}_2$, $\overline{S}_3$	Set (Active Low) Inputs	.25 UL
$\overline{MR}$	Master Reset (Active Low) Input	.25 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	2.25 UL

CHARACTERISTICS

TYPICAL DELAYS	$\overline{E}$ to Q	68 ns
		38 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	55 mW	



93L10
DECADE COUNTER

DESCRIPTION The 93L10 is a synchronous decade counter It has synchronous parallel load facility, overridng asynchronous master reset, terminal count and carry lookahead logic for high speed multidecade operation.

The counter is synchronous, with the counter outputs changing state after the low to high transition of the clock. When conditions are satisfied for counting, a clock pulse will change the counter to the next state of the count sequence shown below. Whenever the parallel enable input is low the parallel inputs determine the next state of the counter synchronously with the clock.

Mode selection is accomplished as shown below. However, a restriction is placed on the manner of selection. The transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high.

By utilizing the two count enable inputs and terminal count outputs multi-stage synchronous counting is obtained, with operating speed equivalent to that of a single stage.

When the asynchronous master reset is active outputs Q_{0-3} will be forced low regardless of all other input conditions.

MODE SELECTION

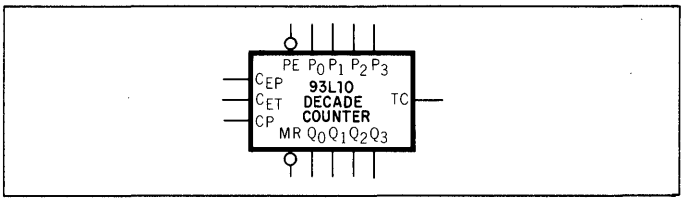
$\overline{PE}$	CE (Count Enable)	MODE
H	H	Count Up
H	L	No Change
L	X	Presetting

Where CE (Count Enable) = CEP · CET

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

LOGIC EQUATION FOR TERMINAL COUNT

$TC = CET \cdot Q_0 \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot Q_3$

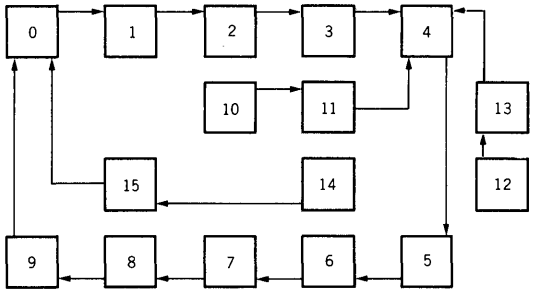


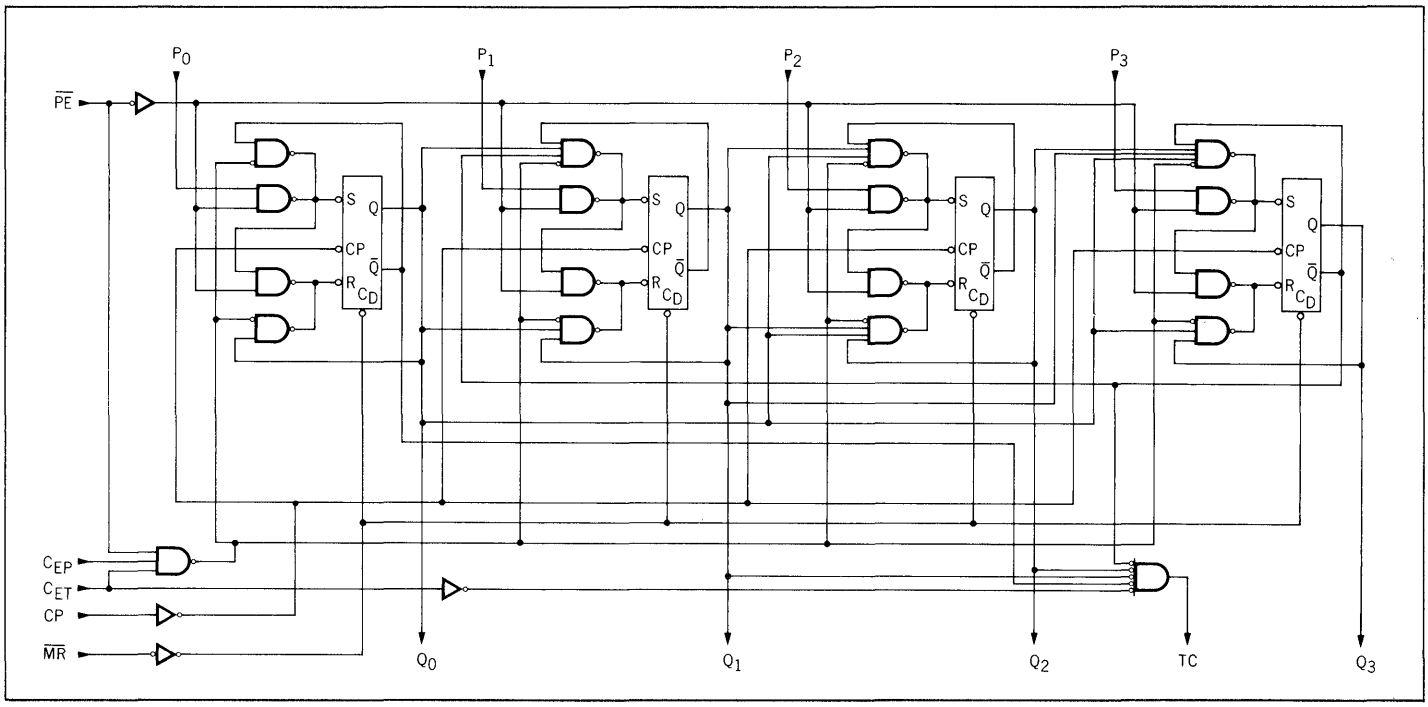
PIN NAMES		LOADING
$\overline{PE}$	Parallel Enable (Active Low) Input	.5 UL
P_0, P_1, P_2, P_3	Parallel Inputs	.17 UL
CEP	Count Enable Parallel Input	.25 UL
CET	Count Enable Trickle Input	.5 UL
CP	Clock Active High Going Edge Input	.5 UL
$\overline{MR}$	Master Reset (Active Low) Input	.25 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	1.5 UL
TC	Terminal Count Output	1.5 UL

CHARACTERISTICS

TYPICAL SPEED	10 MHz	Counting Frequency
TYPICAL DELAY	CP to Q	45 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	75 mW	

STATE DIAGRAM





93L16 4-BIT BINARY COUNTER

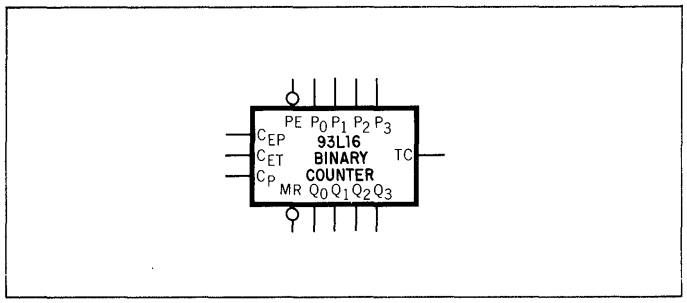
DESCRIPTION The 93L16 is a 4-bit synchronous binary counter. It has synchronous parallel load facility, overriding asynchronous master reset, and carry lookahead logic for high speed multistage operation.

The counter is synchronous, with the counter outputs changing state after the low to high transition of the clock. When conditions are satisfied for counting, a clock pulse will change the counter to the next state of a binary sequence. When the parallel enable is low the parallel inputs determine the next state of the counter synchronously with the clock.

Mode selection is accomplished as shown below. However a restriction is placed on the manner of selection. The transition of CEP or CET from high to low or of $\overline{PE}$ from low to high may only be done when CP is high.

By utilizing the two count enable inputs and terminal count output, multi-stage synchronous counting is obtained, with operating speeds equivalent to that of a single stage.

When the asynchronous master reset is active outputs Q_{0-3} will be forced low regardless of all other input conditions.



PIN NAMES

		LOADING
$\overline{PE}$	Parallel Enable (Active Low) Input	.5 UL
P_0, P_1, P_2, P_3	Parallel Inputs	.17 UL
CEP	Count Enable Parallel Input	.25 UL
CET	Count Enable Trickle Input	.5 UL
CP	Clock Active High Going Edge Input	.5 UL
$\overline{MR}$	Master Reset (Active Low) Input	.25 UL
Q_0, Q_1, Q_2, Q_3	Parallel Outputs	1.5 UL
TC	Terminal Count Output	1.5 UL

CHARACTERISTICS

TYPICAL SPEED	10 MHz	Counting Frequency
TYPICAL DELAY	CP to Q	45 ns
PACKAGE	16 Pin Dip (7B) or Flat Pack (4L)	
TYPICAL POWER DISSIPATION	75 mW	

MODE SELECTION

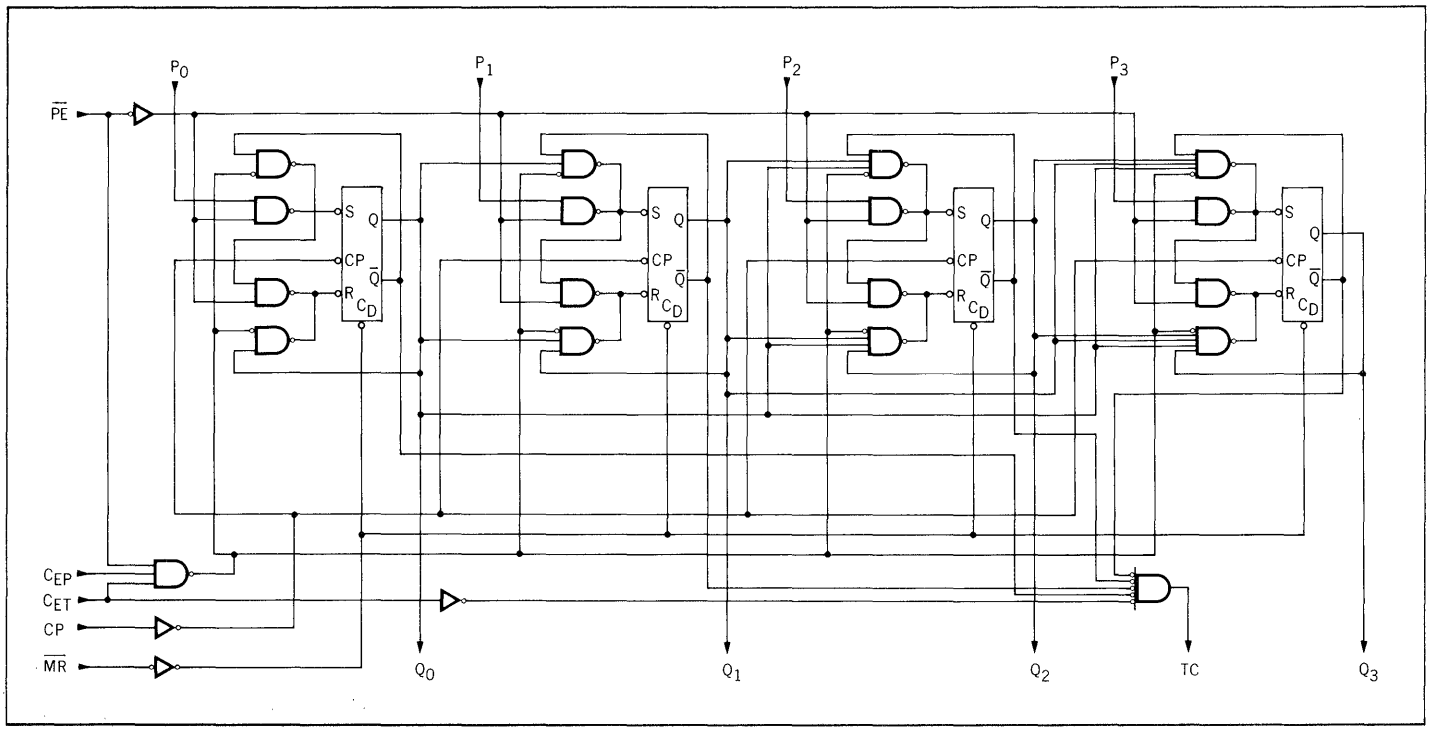
$\overline{PE}$	CE (Count Enable)	MODE
H	H	Count Up
H	L	No Change
L	X	Presetting

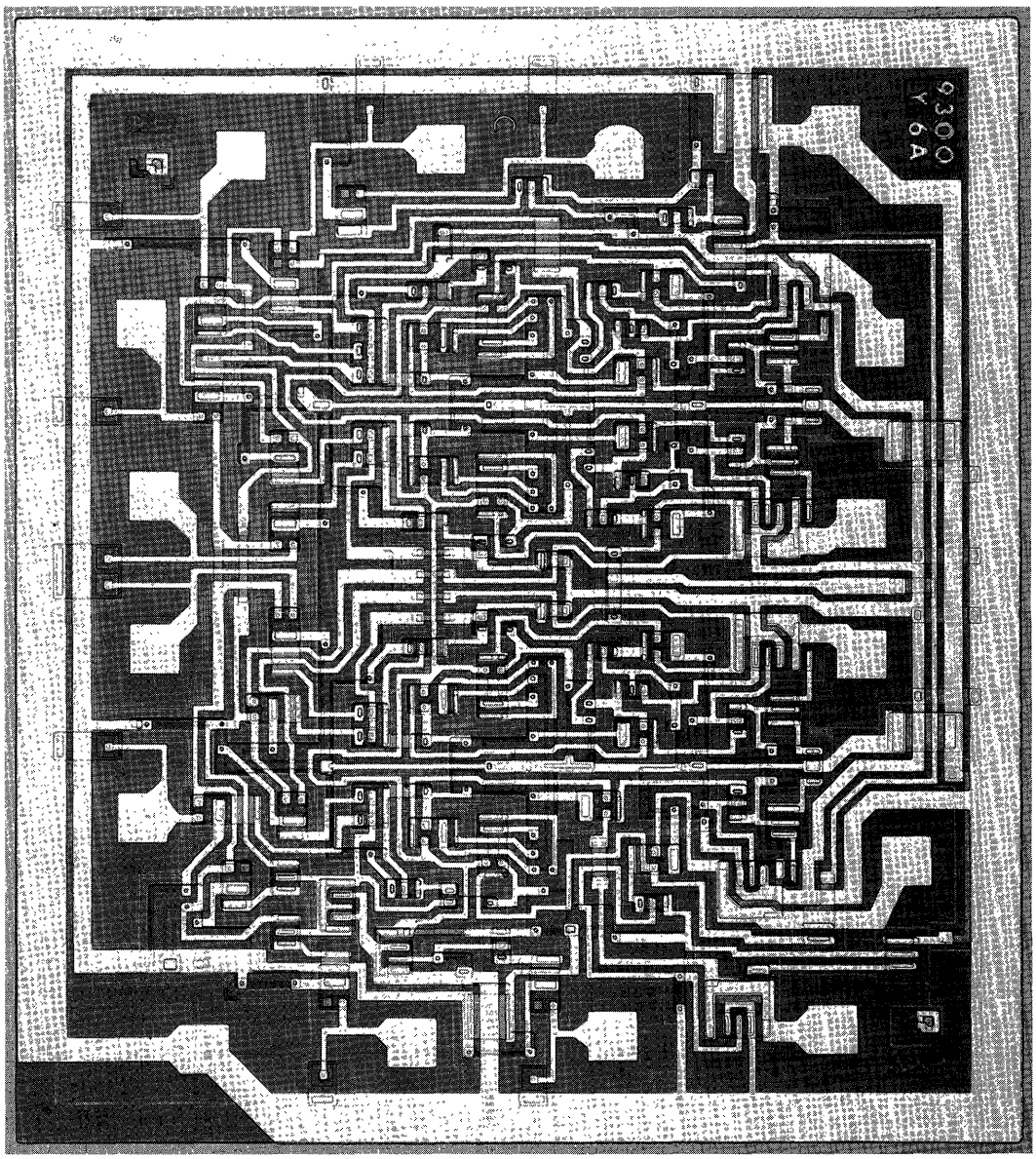
Where CE (Count Enable) = CEP · CET

H = High Voltage Level
L = Low Voltage Level
X = Don't Care Condition

LOGIC EQUATION FOR TERMINAL COUNT

$TC = CET \cdot Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3$

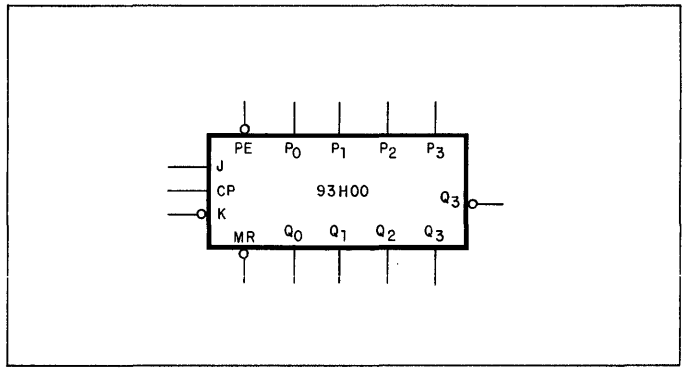




Photomicrograph of the TTL/MSI 9300 4-Bit Shift Register

93H00 HIGH SPEED 4-BIT SHIFT REGISTER

DESCRIPTION The 93H00 high speed Four Bit Shift Register is a multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTμL circuitry for high speed and high fanout capability, and is compatible with all Fairchild TTL integrated circuits.



TRUTH TABLE FOR SERIAL ENTRY

($\overline{PE}$ = HIGH, $\overline{MR}$ = HIGH, (n + 1) indicates state after next clock)

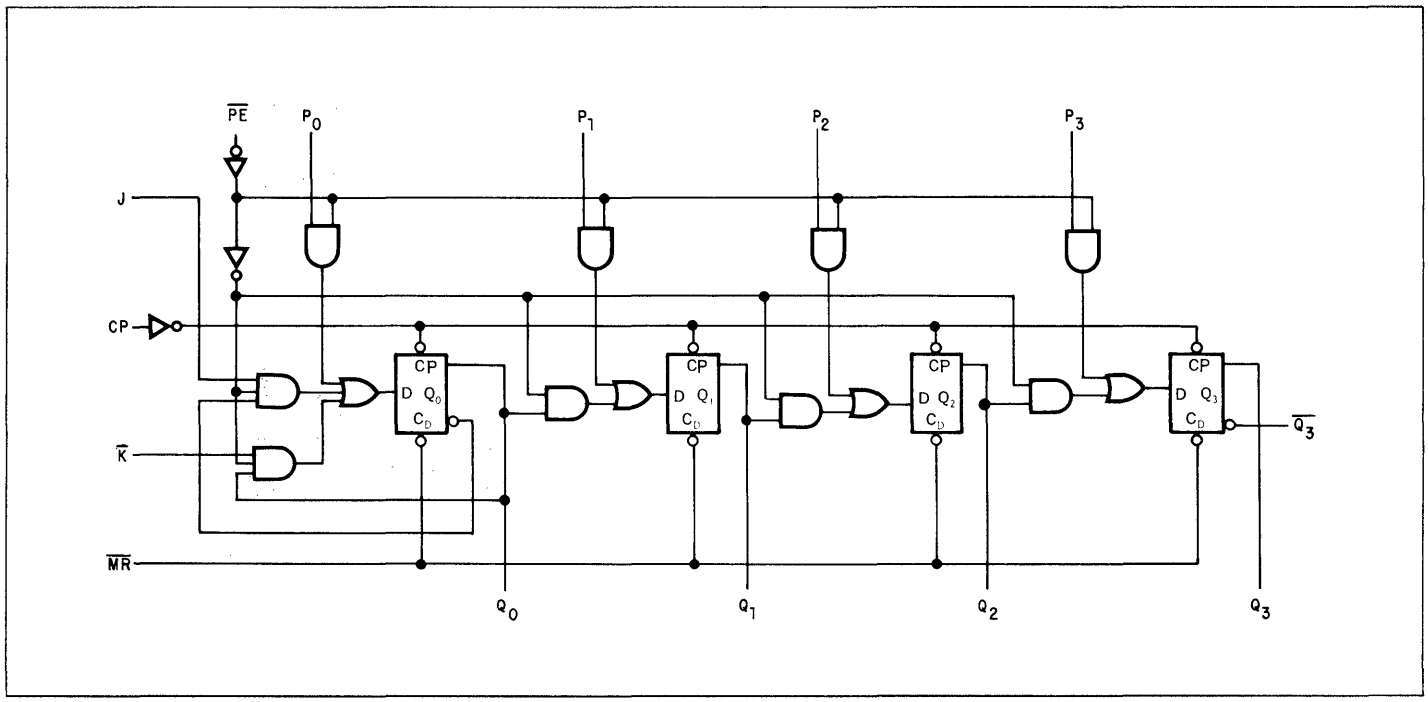
J	$\overline{K}$	Q_0 at t_{n+1}
L	L	L
L	H	Q_0 at t_n (no change)
H	L	Q_0 at t_n (toggles)
H	H	H

CHARACTERISTICS

SHIFT RATE	40 MHz
POWER DISSIPATION	375 mW
PACKAGE	16 Pin DIP (7B) or 16 Pin Flat Pak (4L)

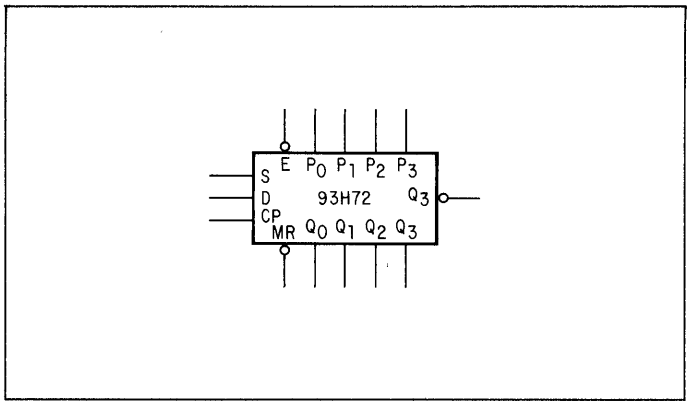
PIN NAMES

$\overline{PE}$	Parallel Enable
P_0 to P_3	Parallel Data Inputs
J	First Stage J Input
$\overline{K}$	First Stage K Input
$\overline{MR}$	Master Reset
Q_0 to Q_3	Parallel Outputs
CP	Clock Input



93H72
HIGH SPEED 4-BIT SHIFT REGISTER WITH CLOCK ENABLE

DESCRIPTION The 93H72 high speed Four Bit Shift Register is a multi-functional sequential logic block which is useful in a wide variety of register and counter applications. As a register it may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data transfers. The circuit uses TTμL circuitry for high speed and high fanout capability, and is compatible with all Fairchild TTL integrated circuits.



MODE SELECT TRUTH TABLE

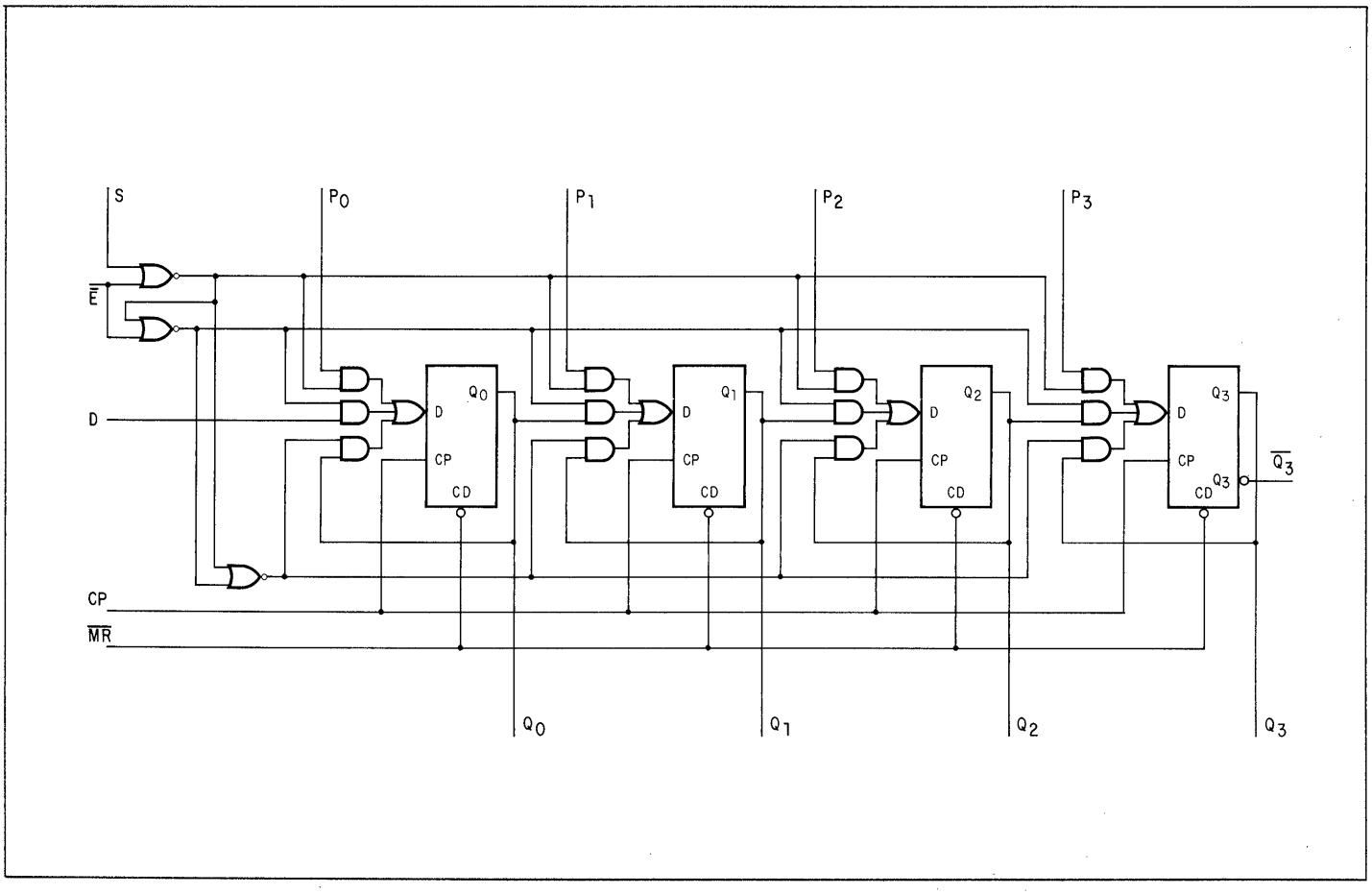
$\overline{E}$	S	MODE
0	0	Parallel Load
0	1	Shift Right
1	0	Hold
1	1	Hold

CHARACTERISTICS

SHIFT RATE	40 MHz
POWER DISSIPATION	400 mW
PACKAGE	16 Pin DIP (7B) or 16 Pin Flat Pak (4L)

PIN NAMES

$\overline{E}$	Parallel Load Enable
S	Shift Enable
P_0, P_1, P_2, P_3	Parallel Data Inputs
CP	Clock Input
$\overline{MR}$	Master Reset
Q_0 to Q_3	Parallel Outputs
D	Serial Data Input



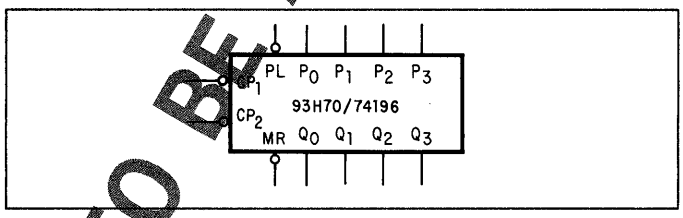
93H70/74196 HIGH SPEED DECADE COUNTER

DESCRIPTION The 93H70/74196 Decade Counter is a high speed device providing a wide variety of counter/storage register applications with a minimum number of packages.

The 93H70 Decade Counter can be connected in the familiar BCD counting mode, in a divide-by-two and divide-by-five configuration or in the Bi-Quinary mode. The Bi-Quinary mode produces a square wave output which is particularly useful in frequency synthesizer applications.

This device has strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, the unit is provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.



PIN NAMES

$\overline{PL}$	Parallel Load Input
P_0 to P_3	Parallel Inputs
$\overline{CP}_1$	Clock Input First Stage
$\overline{CP}_2$	Clock Input
$\overline{MR}$	Master Reset
Q_0, Q_1, Q_2, Q_3	Counter Outputs

CHARACTERISTICS

COUNTING FREQUENCY	50 MHz
POWER DISSIPATION	200 mW
PACKAGE	14 Pin DIP (6A) or 14 Pin Flat Pak (3I)

TRUTH TABLES

DECADE (BCD)
(See Note 1)

Count	Output			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note 2)

Count	Output			
	Q_0	Q_3	Q_2	Q_1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: 1. Output Q_0 connected to $\overline{CP}_2$ input.
2. Output Q_3 connected to $\overline{CP}_1$ input.

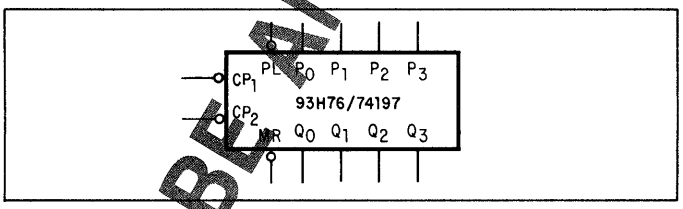
93H76/74197 HIGH SPEED BINARY COUNTER

DESCRIPTION The 93H76/74197 Binary Counter is a high speed device providing a wide variety of counter/storage register applications with a minimum number of packages.

The 93H76/74197 Binary Counter may be connected as a divide-by-two, four, eight, or sixteen counter.

This device has strobed parallel-entry capability so that the counter may be set to any desired output state. A "1" or "0" at a data input will be transferred to the associated output when the strobe input is put at the "0" level. For additional flexibility, the unit is provided with a reset input which is common to all four bits. A "0" on the reset line produces "0" at all four outputs.

The counting operation is performed on the falling (negative-going) edge of the input clock pulse.



PIN NAMES

$\overline{PL}$	Parallel Load Input
P_0 to P_3	Parallel Inputs
$\overline{CP}_1$	Clock Input First Stage
$\overline{CP}_2$	Clock Input Second Stage
$\overline{MR}$	Master Reset
Q_0, Q_1, Q_2, Q_3	Counter Outputs

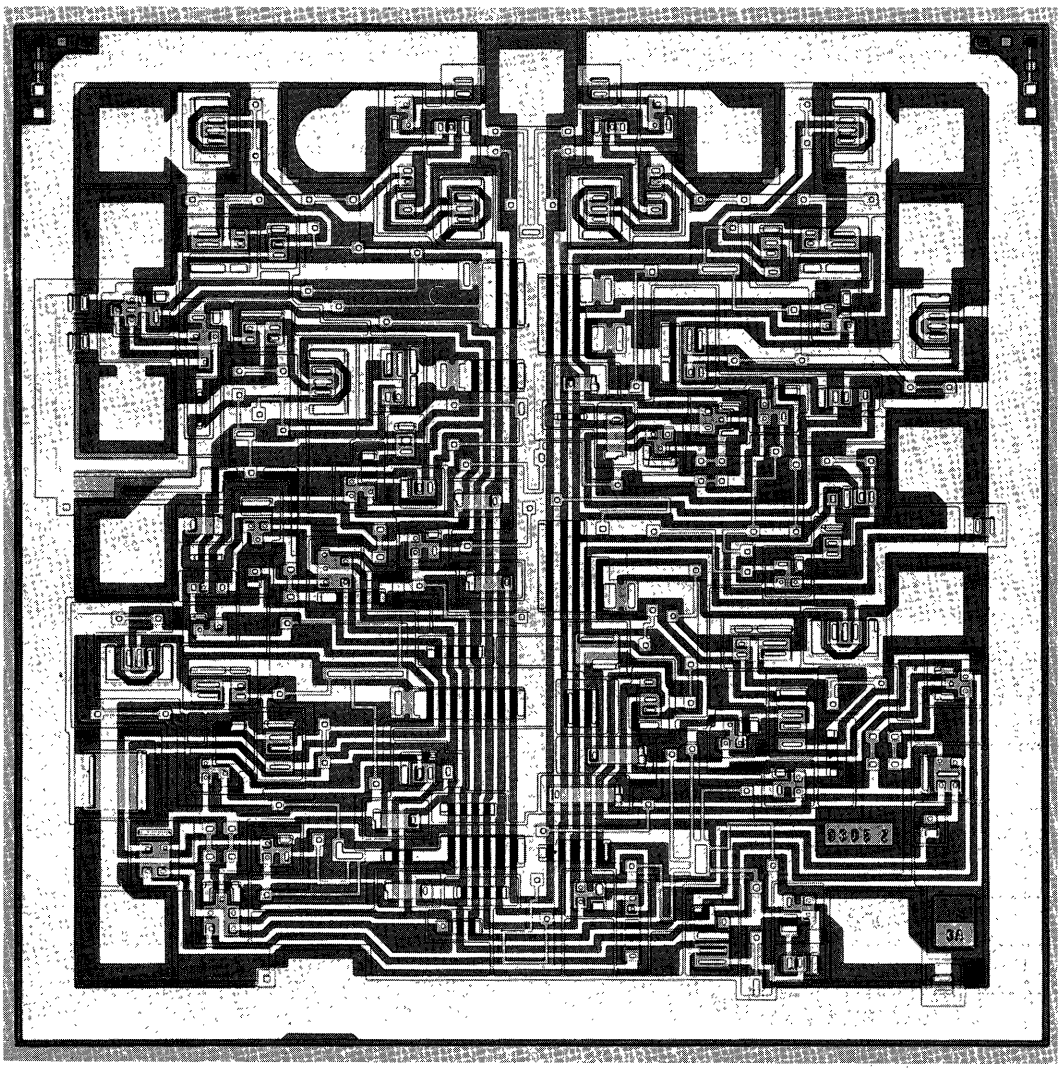
CHARACTERISTICS

COUNTING FREQUENCY	50 MHz
POWER DISSIPATION	200 mW
PACKAGE	14 Pin DIP (6A) or 14 Pin Flat Pak (3I)

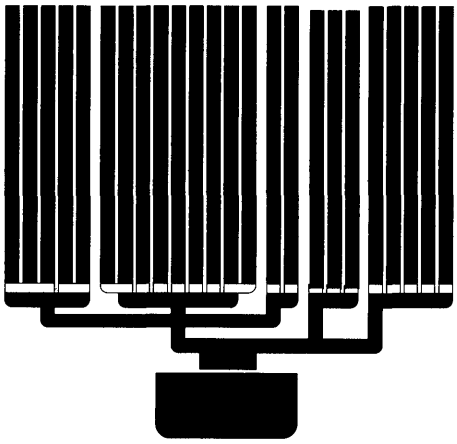
TRUTH TABLE (See Note 1)

COUNT	OUTPUT			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE 1: Output Q_0 connected to $\overline{CP}_2$ input.



Photomicrograph of the TTL/MSI 9305 Variable Modulo Counter



TTL/MEMORY

INTRODUCTION The Fairchild TTL/memory product line includes a variety of high speed memory devices suitable for use in all types of data processing equipment. Three general types of memory products are included in the TTL/memory product line. These are read only memories (ROM), random access read/write (RAM), and associative or content addressable memories (CAM).
The following table summarizes the functions and products available in the TTL/memory product line.

RANDOM ACCESS READ/WRITE MEMORIES (RAM)

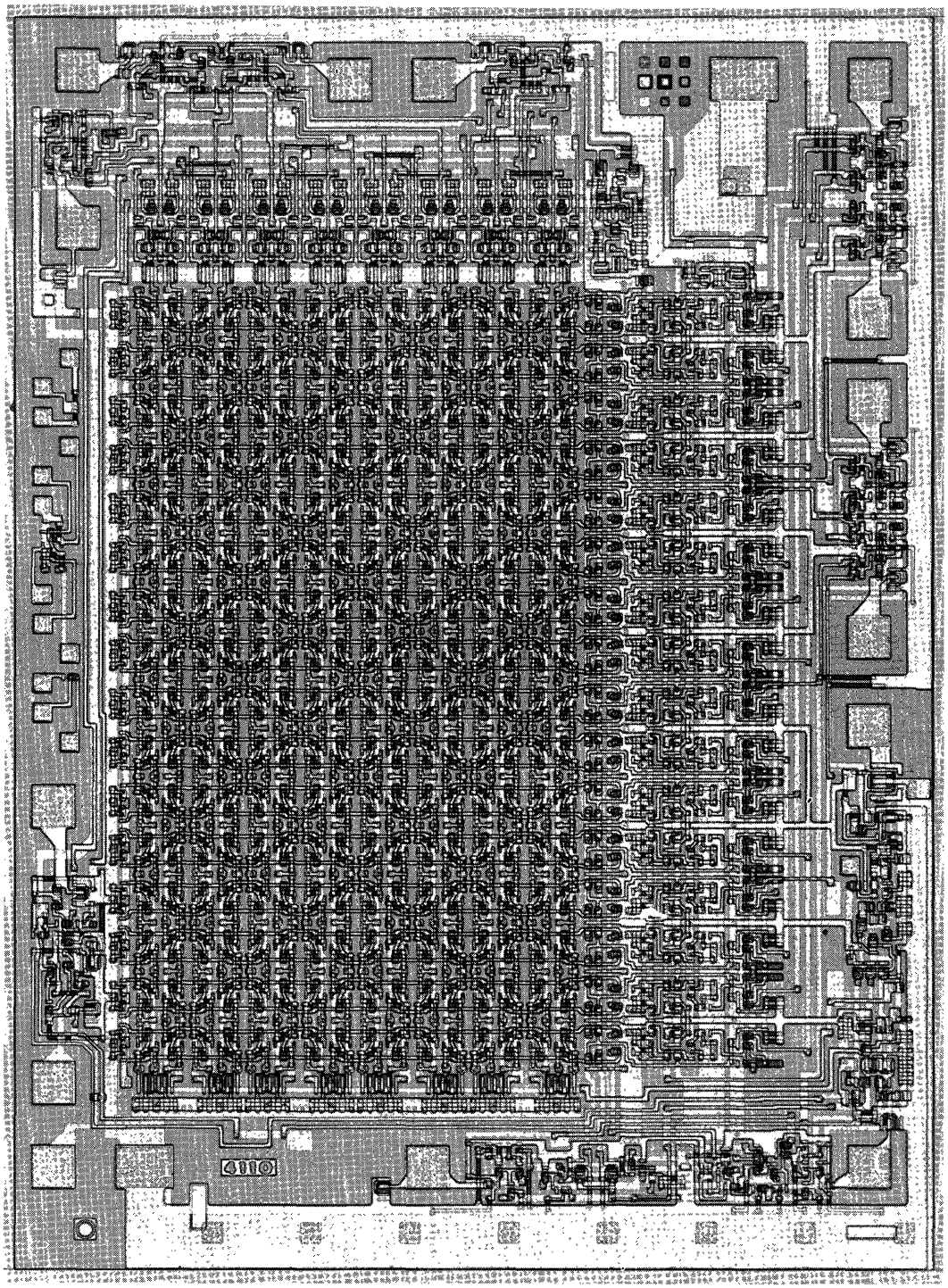
16 BIT	16 WORD X 1 BIT	COINCIDENT SELECT	18 ns	93433
16 BIT	16 WORD X 1 BIT	COINCIDENT SELECT	18 ns	93407
64 BIT	16 WORD X 4 BIT	LINEAR SELECT	22 ns	93435
64 BIT	16 WORD X 4 BIT	FULL DECODE	40 ns	93403
256 BIT	256 WORD X 1 BIT	3 OF 6 DECODE	70 ns	93400
256 BIT	256 WORD X 1 BIT	FULL DECODE	40 ns	93410
1024 BIT	1024 WORD X 1 BIT	FULL DECODE	80 ns	93415

READ ONLY MEMORIES (ROM)

256 BIT	32 WORD X 8 BIT	FIELD PROGRAMMABLE	30 ns	93412
256 BIT	32 WORD X 8 BIT	MASK PROGRAMMABLE	30 ns	93434
1024 BIT	256 WORD X 4 BIT	MASK PROGRAMMABLE	50 ns	93406

ASSOCIATIVE/CONTENT ADDRESSABLE MEMORIES (CAM)
PROGRAMMABLE DECODERS

16 BIT	4 WORD X 4 BIT	LINEAR SELECT	25 ns	93402

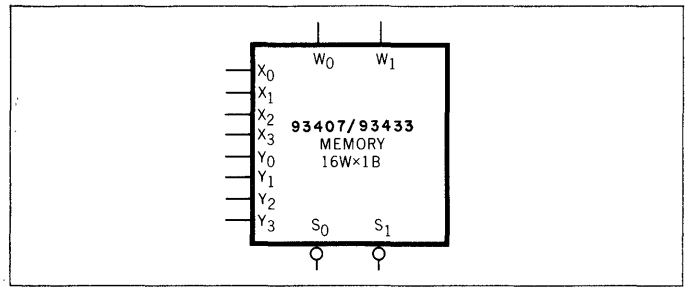


Photomicrograph of the TTL/Memory 93410 256-Bit (256 Word x 1 Bit) fully decoded RAM

93407, 93433 16-BIT RAM FULLY DECODED (FORMERLY 5033/9033)

DESCRIPTION The 93407 and 93433 are 16-bit random access read/write memories organized 16 word x 1-bit. The 93433 has standard corner power supply pins, while the 93407 uses pins 4 and 10 for power supply.

The memory is arranged in an addressable 4 x 4 matrix, a desired bit location being selected by raising the coincident X-Y lines to logic "1" while holding non-selected address lines at "0". As many as four locations may be addressed simultaneously without destroying stored information. The outputs are open collector and may be wire "OR-ed" for word expansion.



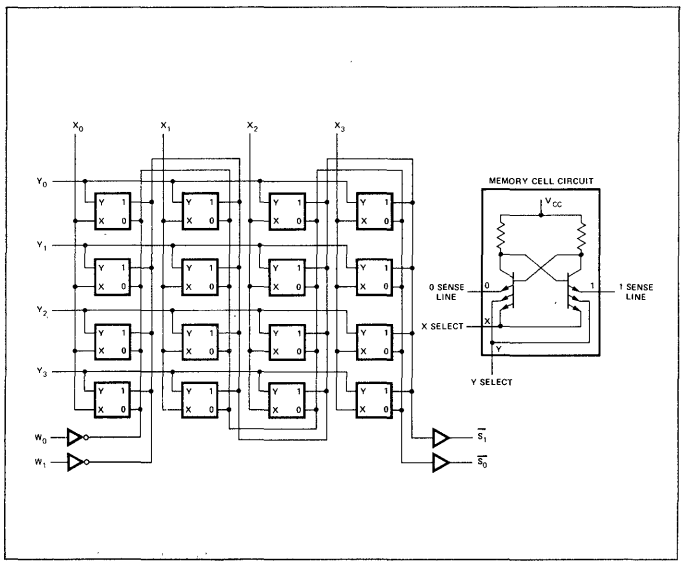
PIN NAMES		LOADING
X_0 to X_3	X Address Inputs	11 mA at 2.1 V
Y_0 to Y_3	Y Address Inputs	11 mA at 2.1 V
W_0	Write '0' Input	*1 UL
W_1	Write '1' Input	*1 UL
$\overline{S_0}$	Data '0' (Active Low) Output	†20/40 mA at 0.45 V
$\overline{S_1}$	Data '1' (Active Low) Output	†20/40 mA at 0.45 V

† NOTE: Two versions are available 20 mA and 40 mA I_{OL}

* NOTE: 1.67 UL in high state
1 UL in low state

CHARACTERISTICS

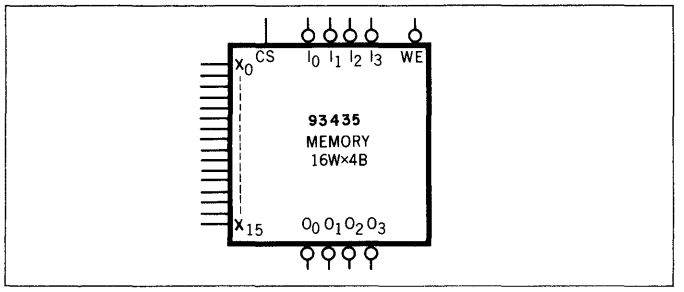
TYPICAL DELAYS	Access Time	18 ns
	Cycle Time	30 ns
PACKAGE	14 Pin Dip (6A) or Flat Pack (3I)	
TYPICAL POWER DISSIPATION	250 mW	



93435 64-BIT RAM NON-DECODED (FORMERLY 9035)

DESCRIPTION The 93435 is a high speed 64-bit read/write memory designed for use in high speed scratch pad memories. It is a linear select 16 word by 4-bit array.

In addition to 16 address inputs, 4 data outputs, and 4 data inputs, the 93435 has a chip select and a write enable. When the chip select is high, a word may be addressed by a high on one of the address inputs. Data is written into the addressed word location only when the write enable is held low. While the address is present, the outputs continuously show the contents of the word selected.



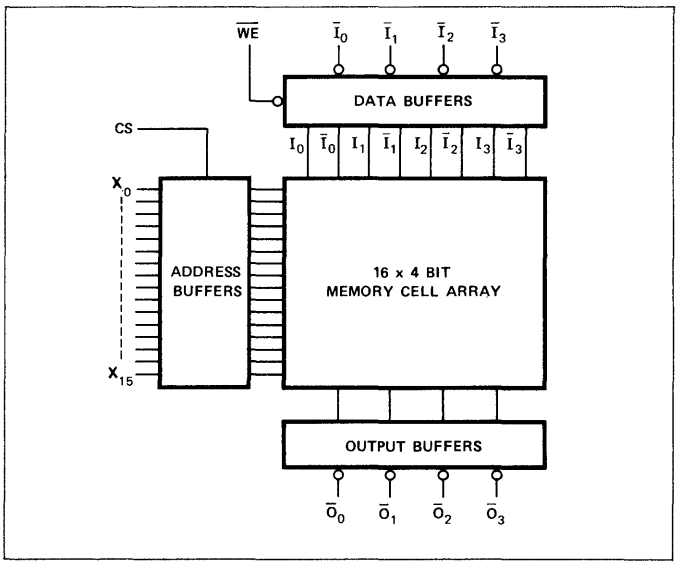
PIN NAMES		LOADING
X_0 to X_{15}	Address (Active High) Inputs	*1 UL
$\overline{I_0}$ to $\overline{I_3}$	Data (Active Low) Inputs	*2 UL
$\overline{CS}$	Chip Select (Active High) Input	†1 UL
$\overline{WE}$	Write Enable (Active Low) Input	*1 UL
$\overline{O_0}$ to $\overline{O_3}$	Data (Active Low) Outputs	10 mA at 0.4 V

* NOTE: 1.67 UL in high state
1 UL in low state

† NOTE: Increases by 1 UL in low state for each address held in high state.
1.6 mA in high state

CHARACTERISTICS

TYPICAL DELAYS	Access Time	22 ns
	Cycle Time	30 ns
PACKAGE	36 Pin Dip (6P)	
TYPICAL POWER DISSIPATION	500 mW	



93403 64-BIT RAM
(16 WORD × 4 BIT) FULLY DECODED (FORMERLY 4103)

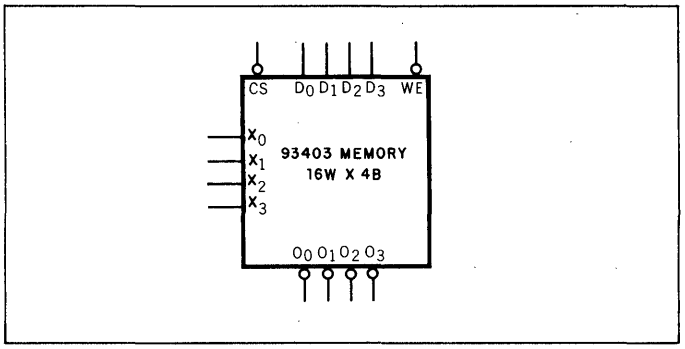
DESCRIPTION The 93403 is a high speed 64-bit read/write memory cell organized in 16 words of 4-bits. Internal decoding is employed with the 16 words selected through four address lines. A chip select input, read/write control line, and active low OR-tieable outputs are also provided.

When the chip select input is low, a word can be selected according to the code applied to the address inputs. Data on the inputs is written into the addressed word location only when the write enable is held low. While the address is present, the outputs continuously show the contents of the word selected.

Uncommitted collector outputs are provided on the 93403 to allow maximum flexibility in output connections. In many applications such as memory expansion, the outputs of many 93403's can be tied together. An external resistor of value R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O. } (1.6)} \leq R \leq \frac{2.1}{N(0.1) + \text{F.O. } (0.06)}$$

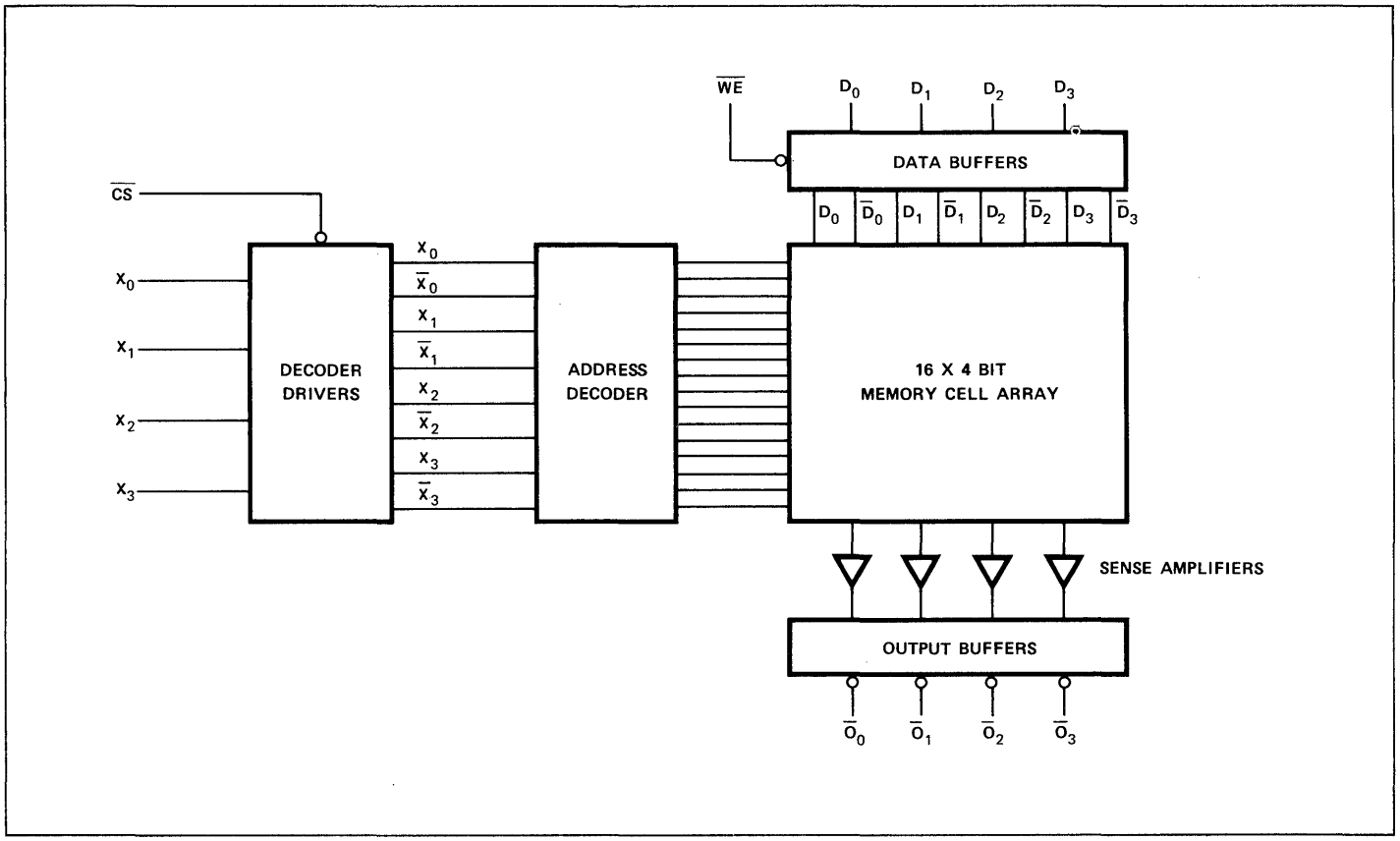
R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTμL loads driven



PIN NAMES		LOADING
X_0 to X_3	Address Inputs	1 UL
D_0 to D_3	Data Inputs	1 UL
$\overline{CS}$	Chip Select (Active Low) Input	1 UL
$\overline{WE}$	Write Enable (Active Low) Input	1 UL
$\overline{O}_0$ to $\overline{O}_3$	(Active Low) Outputs	10 mA at 0.4 V

CHARACTERISTICS

TYPICAL DELAYS	Access Time 40 ns Cycle Time 120 ns
PACKAGE	16 Pin Dip (7B)
TYPICAL POWER DISSIPATION	400 mW



93400/93400B 256-BIT RAM PARTIALLY DECODED 93401 MEMORY DECODER DRIVER(FORMERLY 4100/4101)

DESCRIPTION The 93400 is a medium speed 256 bit Read/Write random access with partial decoding on chip. The memory is organized in 256 words by one bit. The memory is packaged in a 16 lead ceramic Dual In-Line package allowing high density printed circuit board packing. The outputs have uncommitted collectors which allow easy wire or memory expansion.

OPERATION The 93400 uses a 3 of 6 code on the X and Y address inputs to decode the 16 internal X and Y lines. The truth table is shown in the table below. A companion product, the 93401 binary to 3 of 6 decoder driver, is capable of converting a 4 bit binary address to the 3 of 6 code driving the X or Y lines. Thus, a large memory store can be made with very few packages needed for the address line decoding and driving.

The data input and output share a common Input/Output pin. An uncommitted collector gate with an external pullup resistor should be used for the data input gate. A typical connection is shown in the application. To read, the Read/Write line is held "Low"; to write the Read/Write line is brought "High". The collectors of several 93400 can be wired-OR tied to provide word expansion.

PIN NAMES

93400

$X_0 \ldots X_5$	X Address Inputs
$Y_0 \ldots Y_5$	Y Address Inputs
R/W	Read/Write Control Input
I/O	Input/Output Line

93400

$A_0 \ldots A_3$	BCD Data Input
$\overline{O}_0 \ldots \overline{O}_5$	6 Line Decoded Output
$E_0 \ldots \overline{E}_3$	Enable Inputs

CHARACTERISTICS

93400

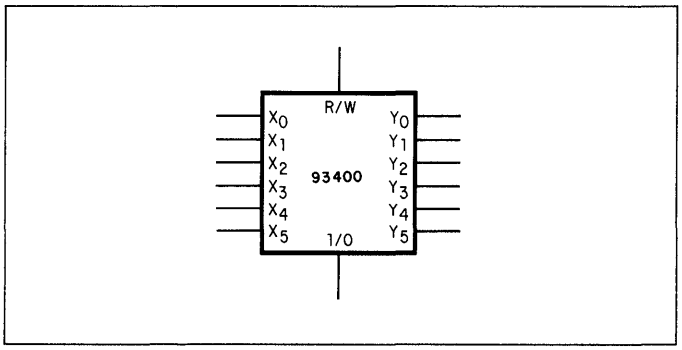
ACCESS TIME	70 ns
POWER DISSIPATION	500 mW
PACKAGE	16 Pin DIP (7B)

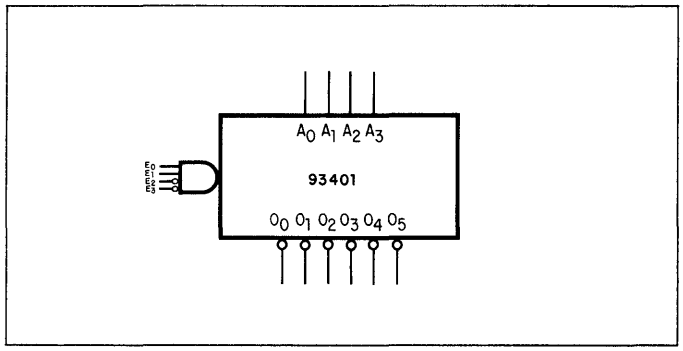
93400B

ACCESS TIME	100 ns
POWER DISSIPATION	500 mW
PACKAGE	16 Pin DIP (7B)

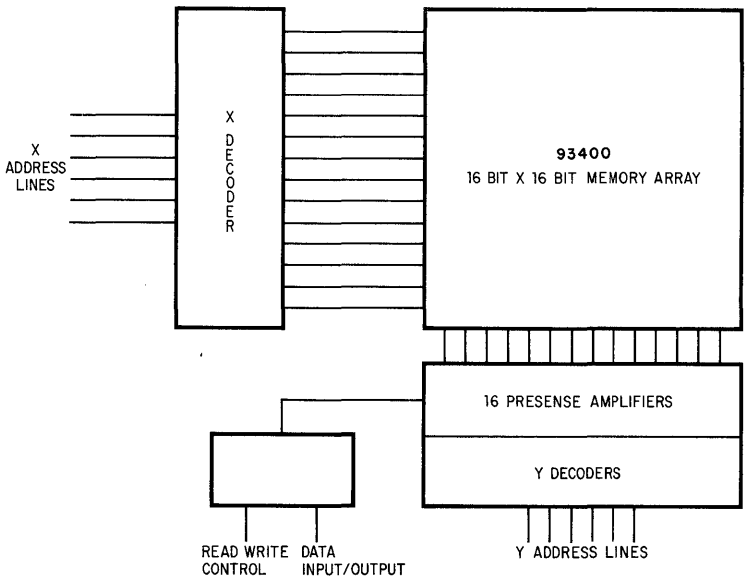
93401

DELAY TIME	20 ns
POWER DISSIPATION	400 mW
PACKAGE	16 Pin DIP (7B)





93400 BLOCK DIAGRAM

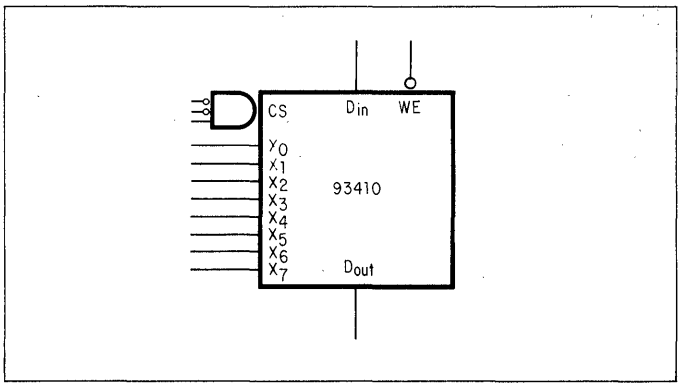


93410 256-BIT RAM (256 WORD × 1 BIT) FULLY DECODED(FORMERLY 4110)

DESCRIPTION The 93410 is a high speed 256-bit read/write random access memory with full decoding on chip. The memory, organized 256 words x 1 bit, is designed for scratchpad, buffer and distributed main memory applications.

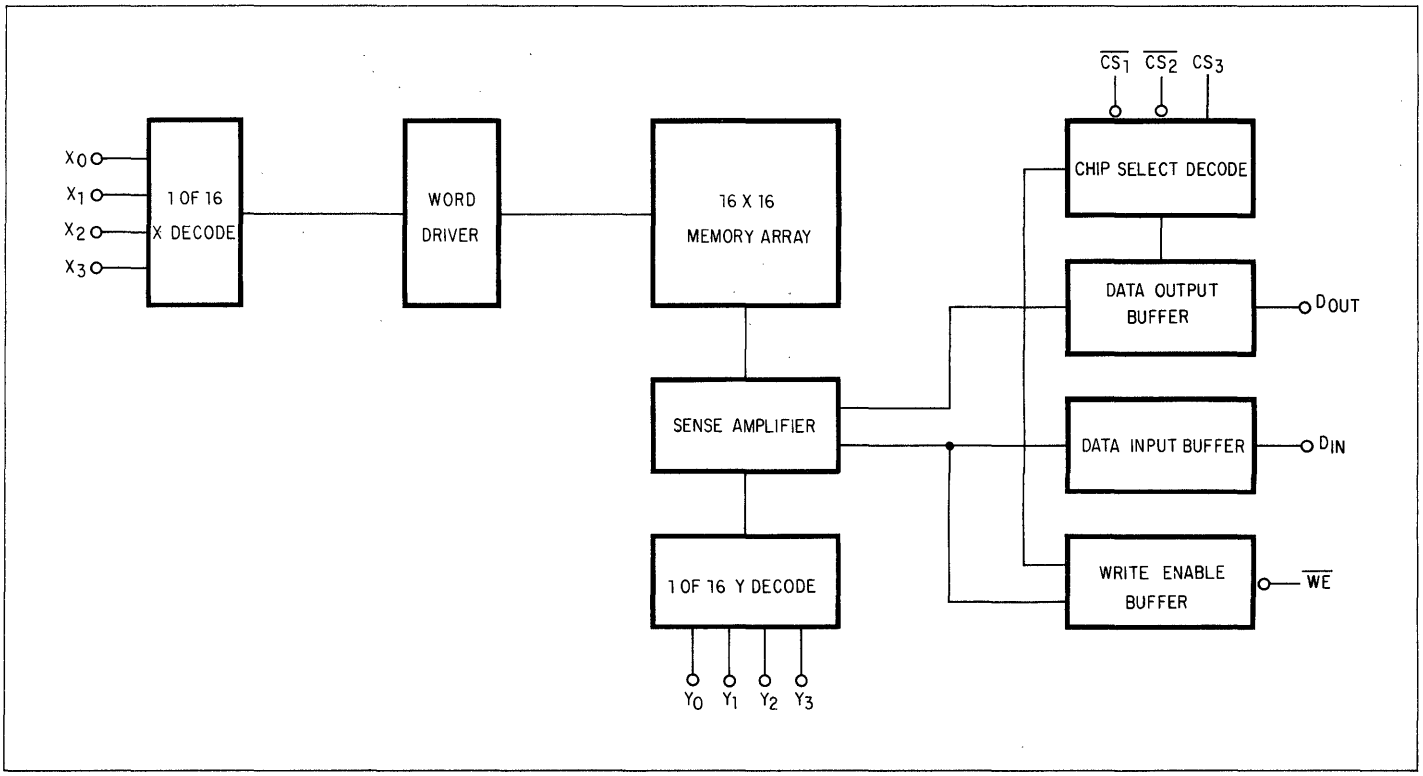
The device has three chip select lines. Two lines are active LOW and the third active HIGH for maximum logic flexibility. In a small system (up to 1K words), the chip selects can be used to decode two address bits, for "row selection" with only a single NAND gate required. In larger systems, the two active LOW chip selects can be drawn from two decoders in a coincident select scheme. The active HIGH chip select could be used as an output strobe.

The 93410 is designed with uncommitted collector outputs to permit "OR-ties" for ease of memory expansion.



PIN NAMES		LOADING
$\overline{CS_1}$, $\overline{CS_2}$, CS_3	Chip Select	0.5 UL
X_0 - X_3 , Y_0 - Y_3	Address Inputs	0.5 UL
D_{IN}	Data Input	0.5 UL
D_{OUT}	Data Output	10 UL
$\overline{WE}$	Write Enable	0.5 UL

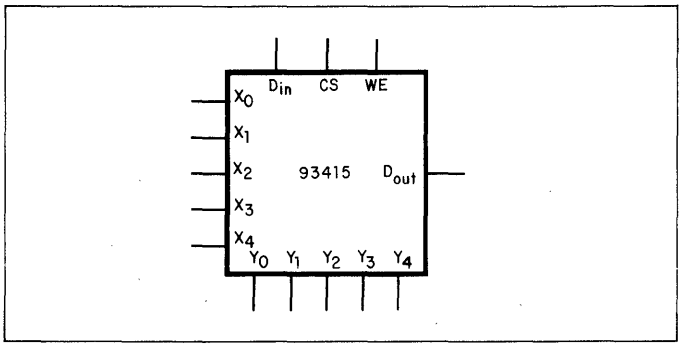
CHARACTERISTICS		
CHIP SELECT	Access Time	20 ns
ADDRESS	Access Time	40 ns
PACKAGE	16 Pin Dip (7B)	
TYPICAL POWER DISSIPATION	500 mW	



93415
1024-BIT RAM (1024 WORD × 1 BIT) FULLY DECODED

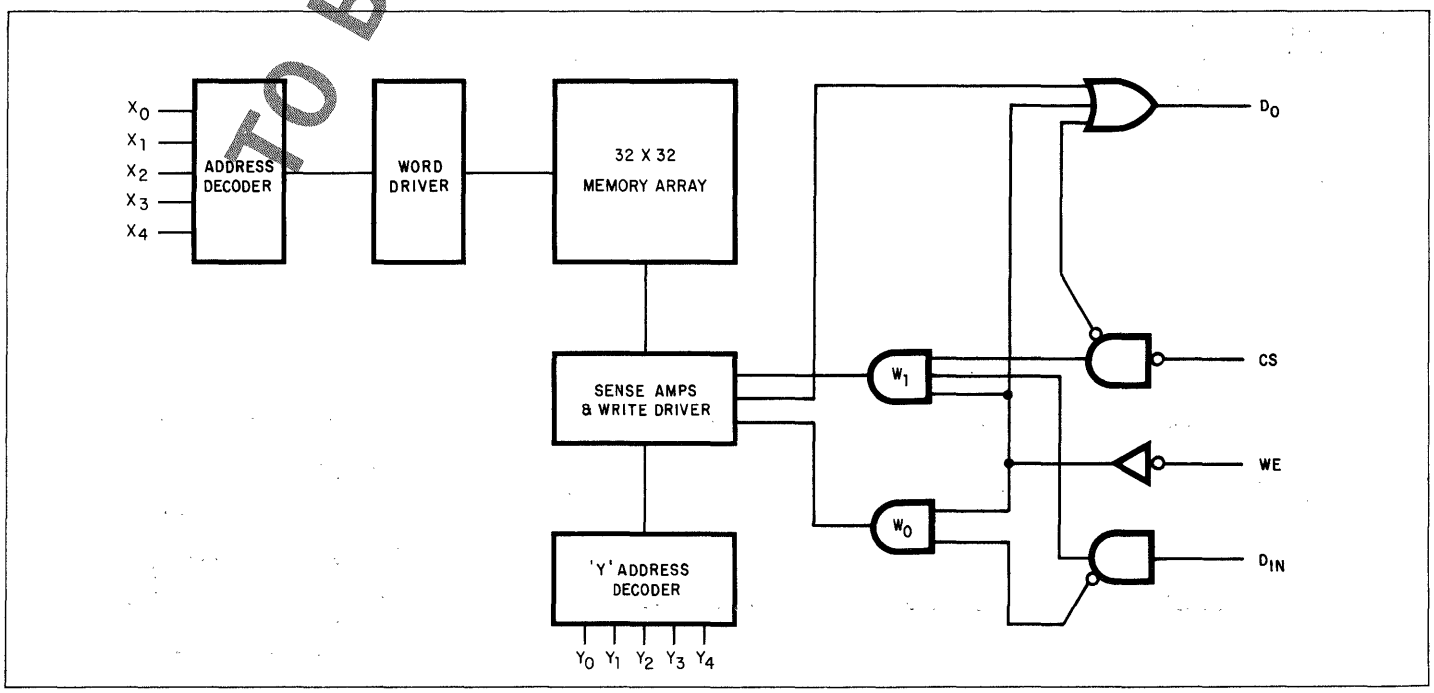
DESCRIPTION The 93415 is a high speed TTL Read/Write Random Access Memory with full decoding on chip, utilizing ISOPLANAR technology. The memory is organized as 1024 words x 1 bit, and is designed for high speed mainframe applications. The 93415 is designed with uncommitted collector outputs to permit 'OR-ties' for ease of memory expansion.

This is advance information on a new product in development. Specifications are subject to change without notice.



PIN NAMES		LOADING
CS	Chip Select	0.25 U.L.
X0-X4	Address Inputs	0.25 U.L.
Y0-Y4	Address Inputs	0.25 U.L.
D_{in}	Data Input	0.25 U.L.
D_{out}	Data Output	10 U.L.
WE	Write Enable	0.25 U.L.

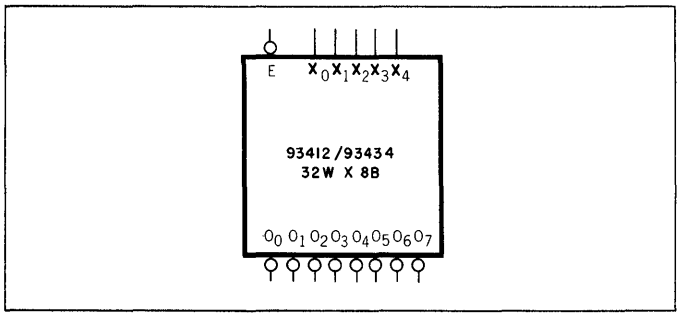
CHARACTERISTICS	
TYPICAL READ ACCESS TIME	
ADDRESS TO DATA OUT	<100 ns
CHIP SELECT TO DATA OUT	<50 ns
TYPICAL POWER	0.5 mW/Bit
PACKAGE	16 Pin DIP (7B)



93412, 93434 256-BIT ROM (32 WORD × 8 BIT) FORMERLY 9034

DESCRIPTION The 93412 and 93434 are 256-bit read only memories organized 32 word x 8-bit. The words are selected through 5 address lines. The 8 outputs of the words are uncommitted collectors to allow wire-OR memory expansion. An Enable input is provided for additional decoding flexibility.

The 93412 is a field programmable device intended for rapid turnaround of prototype units. The 93434 requires a separate metal mask for each customer code but is more economical in high volume.

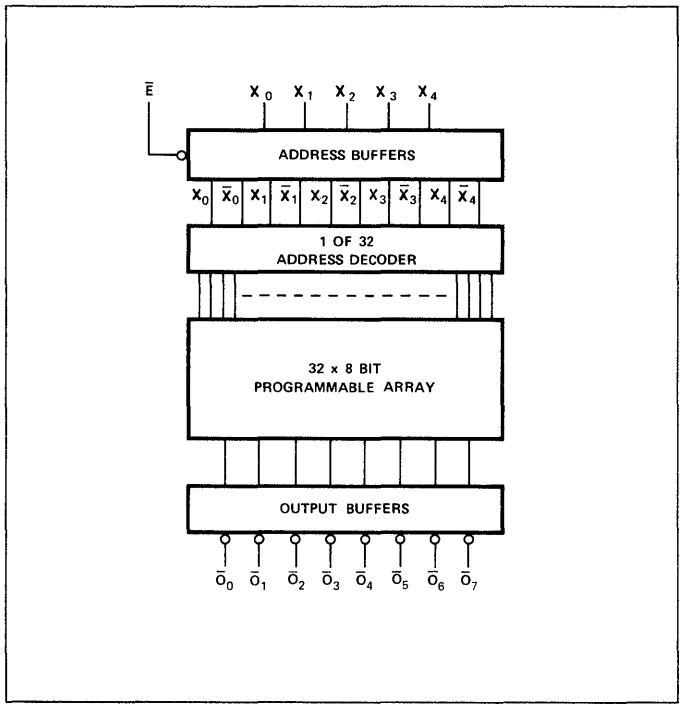


PIN NAMES		LOADING
X_0 to X_4	Address Inputs	*1 UL
$\overline{E}$	Enable (Active Low) Input	*1 UL
$\overline{O_0}$ to $\overline{O_7}$	(Active Low) Outputs	10 mA at 0.4 V

* NOTE: 1.67 UL in high state
1 UL in low state

CHARACTERISTICS

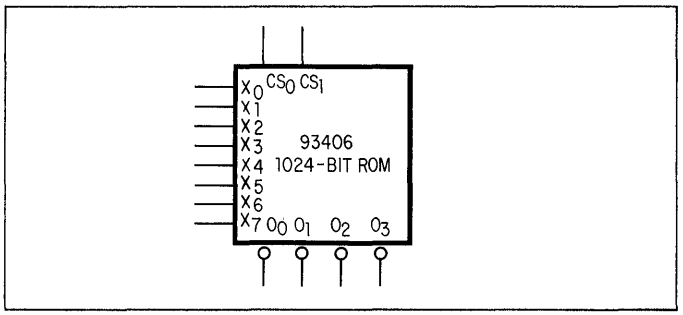
TYPICAL DELAY	Access Time 50 ns
PACKAGE	16 Pin Dip (7B)
TYPICAL POWER DISSIPATION	400 mW



93406 1024-BIT ROM (256 WORD × 4 BIT) FORMERLY 4106

DESCRIPTION The 93406 is a 1024-bit, Read-Only-Memory. The Memory is organized as 256 words of 4 bits each. The words are selected through 8 address inputs. The 4 outputs have uncommitted collectors which may be wired-OR with outputs of other ROM's to expand the word size. Programmable enable inputs provide additional decoding flexibility.

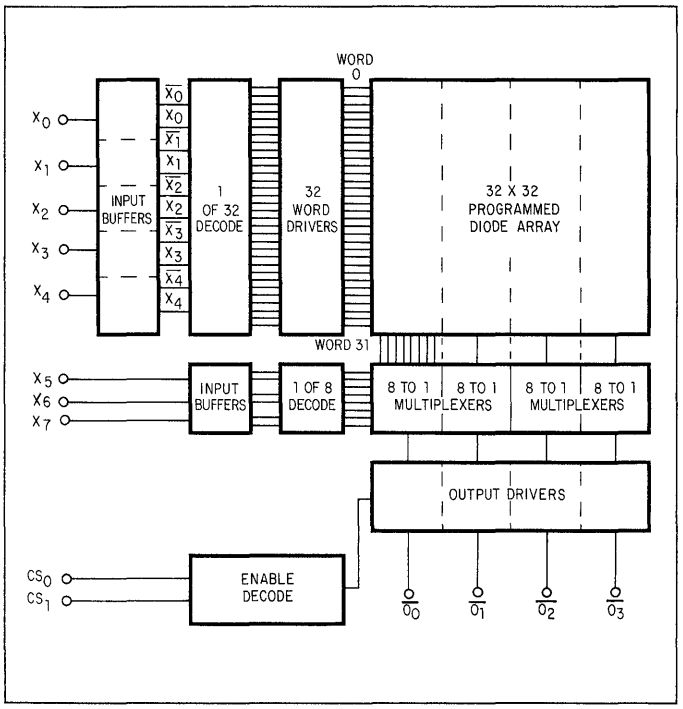
The contents of the memory and the enable are permanently mask programmed on customer request.



PIN NAMES		LOADING
X_0 to X_7	Address Inputs	0.5 UL
CS_0, CS_1	Chip Select Inputs	0.5 UL
$\overline{O}_0$ to $\overline{O}_3$	Data Outputs	10 UL

CHARACTERISTICS

ADDRESS TO OUTPUT	<50 ns
CHIP SELECT TO OUTPUT	<50 ns
PACKAGE	16 Pin Dip (7B)



93402 16-BIT CAM (4 WORD × 4 BIT) CONTENT ADDRESSABLE/ASSOCIATIVE MEMORY(FORMERLY 4102)

DESCRIPTION The 93402 is a four word by four bit read/write associative memory. Word selection is accomplished by four active low linear select address lines. Individual bit enable lines are provided so that individual bits can be written into and matched.

When an address is present, the outputs will continuously show the contents of the word selected. If more than one word is selected, the output will be the "OR" combination of the stored information. Writing is accomplished by addressing the desired word or words and holding the write enable line low.

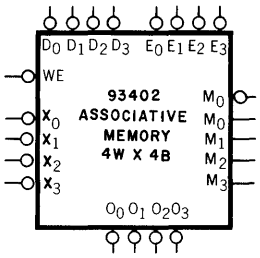
Each data input has a corresponding active low enable. Data on an input will be ignored while writing and matching, if the corresponding bit enable is not activated.

Data stored in the memory can be compared with the data on enabled inputs. If the word on the inputs matches a stored word, then the match output for that word will go high.

Uncommitted collecter outputs are provided on the 93402 to allow maximum flexibility in output connections. In many applications such as memory expansion, the outputs of many 93402's can be tied together. An external pullup resistor of value R within the range specified below may be used.

$$\frac{5.1}{10 - \text{F.O. } (1.6)} \leq R \leq \frac{2.1}{N(0.1) + \text{F.O. } (0.06)}$$

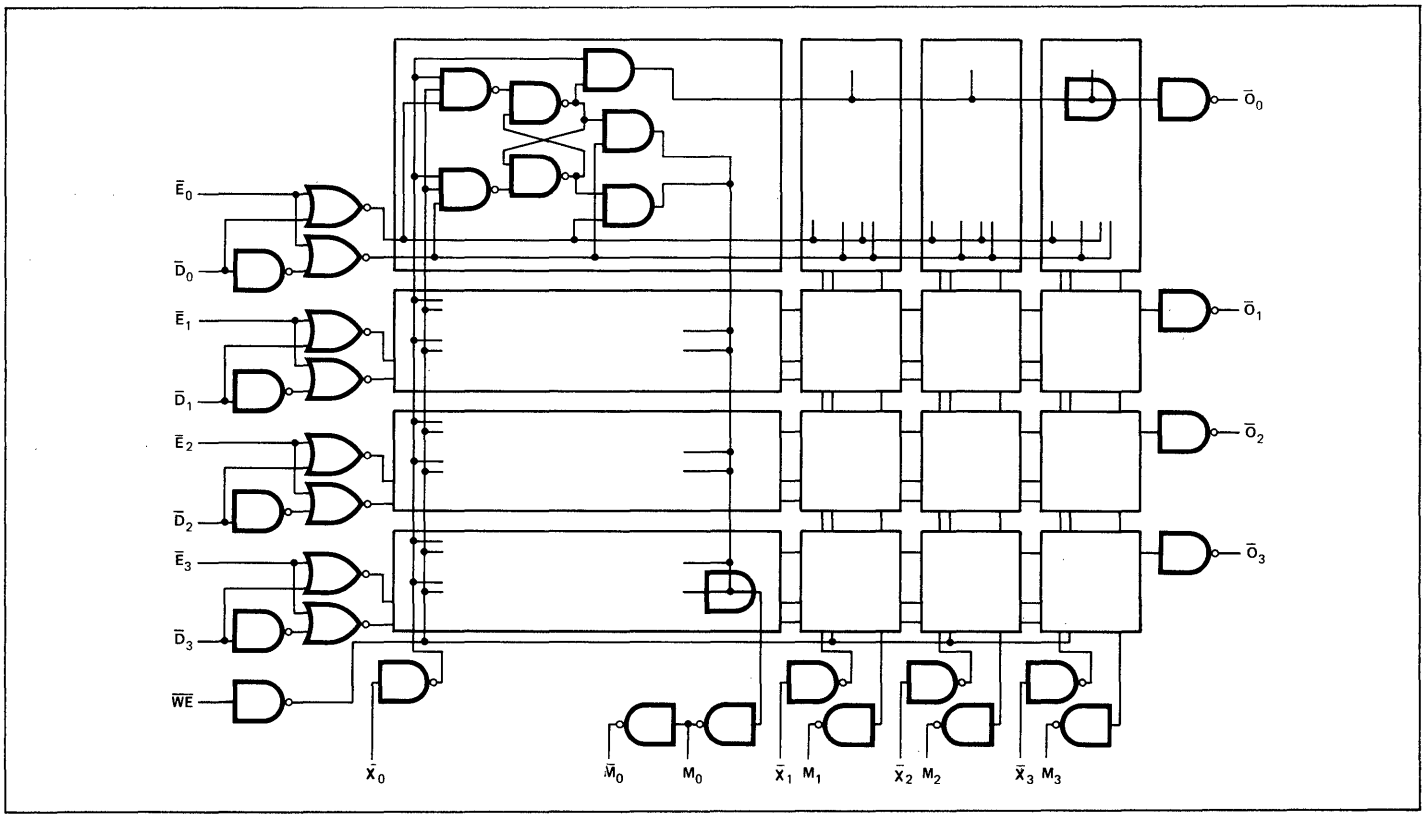
R is in kΩ
N = number of wired-OR outputs
F.O. = number of TTμL loads driven

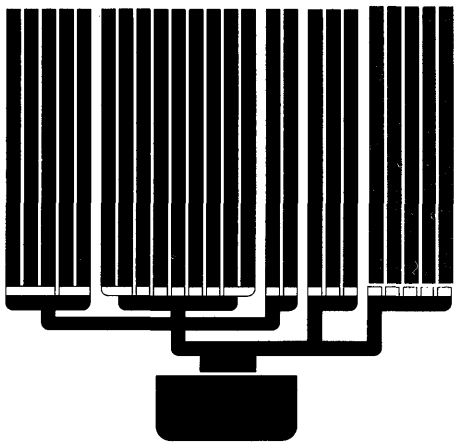


PIN NAMES		LOADING
$\bar{X}_0$ to $\bar{X}_3$	Address (Active Low) Inputs	1 UL
$\bar{D}_0$ to $\bar{D}_3$	Data (Active Low) Inputs	1 UL
$\bar{E}_0$ to $\bar{E}_3$	Bit Enable (Active Low) Inputs	1.5 UL
$\overline{WE}$	Write Enable (Active Low) Input	1.5 UL
M_0 to M_3	Match (Active High) Outputs	10 mA at 0.4 V
$\bar{M}_0$	First Match (Active Low) Output	10 mA at 0.4 V
$\bar{O}_0$ to $\bar{O}_3$	Data (Active Low) Outputs	10 mA at 0.4 V

CHARACTERISTICS

TYPICAL DELAYS	Access Time	25 ns
	Cycle Time	35 ns
	Match Time	25 ns
PACKAGE	24 Pin Dip (6N)	
TYPICAL POWER DISSIPATION	500 mW	





TTL/INTERFACE

INTRODUCTION The 9600 TTL/Interface family includes a wide range of special purpose circuits such as monostable multivibrators, line drivers and receivers, lamp drivers, relay drivers, TTL to MOS and MOS to TTL translators and core memory sense amplifiers. The following table summarizes the functions and circuits presently available in the 9600 series TTL/Interface product line.

PULSE SHAPERS

9600	Retriggerable, Resettable Monostable Multivibrator (One-Shot)
9601	Retriggerable Monostable Multivibrator (One-Shot)
9602	Dual Retriggerable, Resettable Multivibrator (One-Shot)

DRIVERS

9644	Dual High-Voltage, High Current Driver

LINE DRIVERS/RECEIVERS

9614	Dual Differential Line Driver
9615	Dual Differential Line Receiver
9616	Triple EIA Line Driver
9617	Triple EIA Line Receiver
9620	Dual Differential Line Receiver
9621	Dual Line Driver
9622	Dual Line Receiver

TRANSLATORS

9624	Dual TTL to MOS Interface Element
9625	Dual MOS to TTL Interface Element

SENSE AMPLIFIERS

9664/7524	Two Channel Core Memory Sense Amplifier
9665/7525	Two Channel Core Memory Sense Amplifier

9600, 9601, 9602 MONOSTABLE MULTIVIBRATORS(1-SHOTS)

DESCRIPTION The 9600, 9601 and 9602 are DC level sensitive retriggerable monostable multivibrators which provide an output pulse whose duration and accuracy is a function of external timing components.

The inputs are D.C. coupled making triggering independent of input transition times. If the input signal is applied to an active high input, triggering will occur on the rising edge of the waveform. By applying the input signal to an active low input, triggering will occur on the falling edge of the waveform.

The input conditions to be satisfied for triggering are indicated by the external logic symbols.

Each time the input conditions for triggering are met, the external capacitor is discharged and a new cycle is started. Successive inputs with a period shorter than the delay time retrigger the monostable resulting in a continuous true output. Retriggering may be inhibited by tying the negation ($\overline{Q}$) output back to an active level low input.

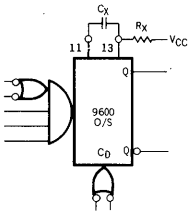
The 9600 and 9602 have active low reset inputs ($\overline{CD}$) which allow the one shot to be reset.

NOTE: Refer to Data Sheet for Output Pulse width versus R_x and C_x.

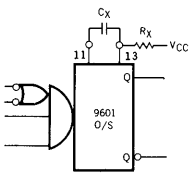
CHARACTERISTICS

PACKAGE	9600, 9601	14 Pin Dip (6A) or Flat Pack (3I)
	9602	16 Pin Dip (7B) or Flat Pack (4L)
TYPICAL POWER DISSIPATION PER ONE SHOT	125 mW	
PULSE WIDTH RANGE	50 ns to ∞	
EXT. RESISTOR RANGE	5KΩ to 50KΩ	
EXT. CAPACITOR RANGE	0 to any practical value	
TYPICAL DELAYS	Trigger Input to Q 25 ns	
LOADING	Input 1 UL	Output 6 UL
APPLICATIONS	See Application Note 173	

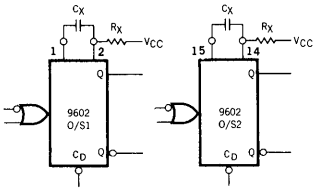
9600
Retriggerable, Resettable



9601
Retriggerable



9602 Dual
Retriggerable, Resettable

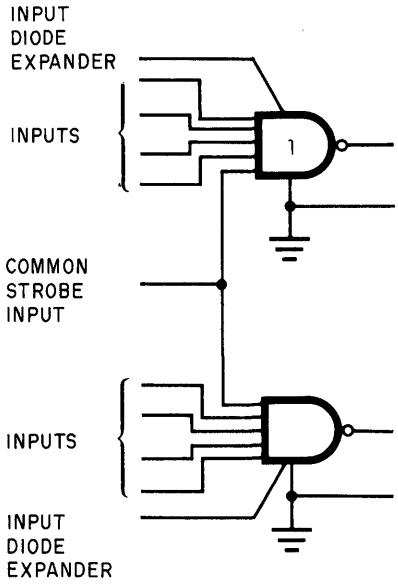


9644 DUAL HIGH-VOLTAGE, HIGH-CURRENT DRIVER

DESCRIPTION The 9644 is a Dual 4-Input NAND Gate whose output can sink 500 mA in the low state, and maintain 30 volts in the high state. The outputs are uncommitted collectors in a Darlington configuration which have typical saturation voltages of 0.8 volts at low currents and 1.2 volts at 500 mA. The inputs are TTμL Compatible and feature input clamp diodes. The input fan-in requirement is typically ½ a normal DTμL Unit Load. An input strobe common to both gates is provided, and an expander input node on each gate is available for input diode expansion. Separate ground pins are provided for each gate to minimize ground pin offset voltages at high current levels.

CHARACTERISTICS

PROPAGATION DELAY	50 ns
OUTPUT CURRENT	500 mA
OUTPUT VOLTAGE	30 V
POWER DISSIPATION	30 mW/Gate
PACKAGE	16 Pin DIP (7B)

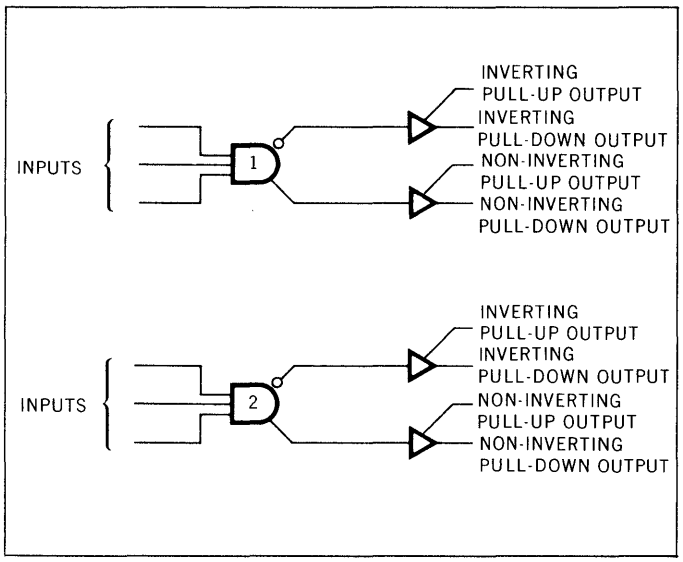


9614 DUAL DIFFERENTIAL LINE DRIVER

DESCRIPTION The 9614 is a TTμL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTμL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other . The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing "NAND" and "AND" functions of the inputs adding greater flexibility. The input and output levels are TTμL compatible with clamp diodes provided at both input and output to handle line transients.

CHARACTERISTICS

PROPAGATION DELAY	16 ns
POWER DISSIPATION	87 mW/Driver
PACKAGE	16 Pin DIP (7B) or Flat Pak (4L)

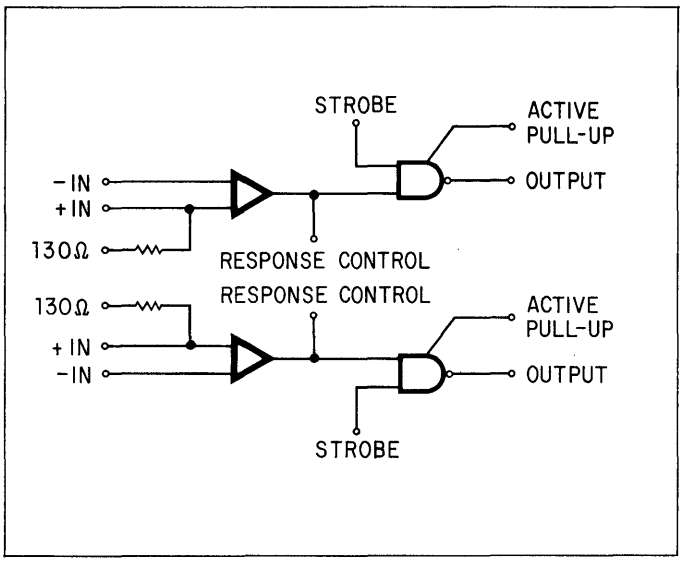


9615 DUAL DIFFERENTIAL LINE RECEIVER

DESCRIPTION The 9615 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTμL logic to the output.
The response time can be controlled by use of an external capacitor. A strobe is provided along with a 130 Ω terminating resistor (at the inputs). The output has an uncommitted collector with an active pull-up available on an adjacent pin.

CHARACTERISTICS

COMMON MODE VOLTAGE	±17.5 V
DIFFERENTIAL INPUT THRESHOLD	80 mV
POWER DISSIPATION	75 mW/Line Receiver
PACKAGE	16 Pin DIP (7B) or Flat Pak (4L)



9616 TRIPLE EIA RS232C LINE DRIVER

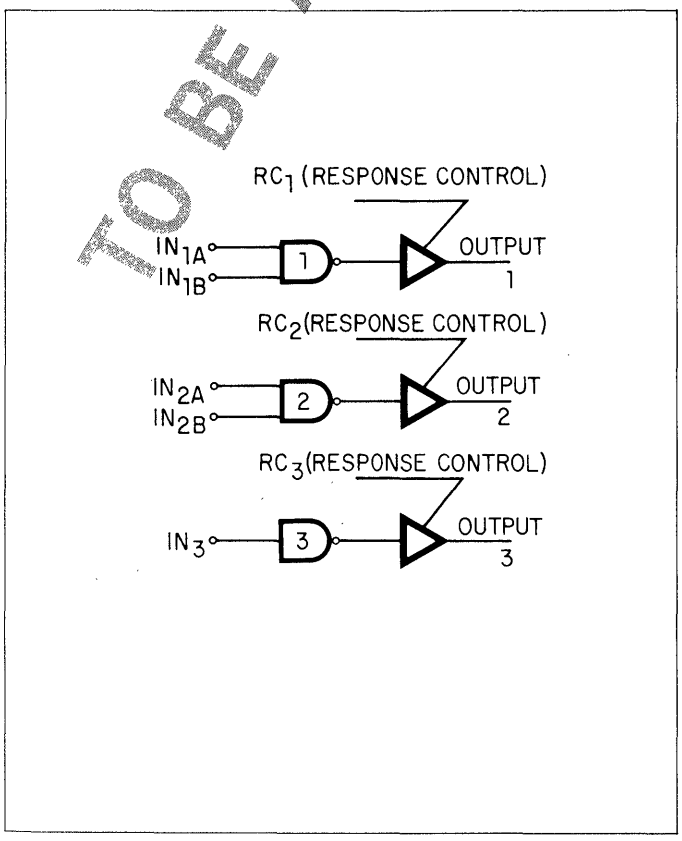
DESCRIPTION The 9616 is a triple line driver which meets the requirements of EIA Specification RS232C. The three independent line drivers feature single ended inputs and outputs, a response control receiving only, a single capacitor, and output voltage protection up to ±25 volts as defined by the EIA Spec. The 9616 operates from +12 V and −12 V power supplies and is designed for use in industrial and military data communications applications.

PIN NAMES

IN_1, IN_2, IN_3	Data Inputs
OUT_1, OUT_2, OUT_3	Data Outputs
RC_1, RC_2, RC_3	Response Control Input

CHARACTERISTICS

OUTPUT VOLTAGE	±6.0 V
PROPAGATION DELAY	200 ns
POWER DISSIPATION	120 mW/Driver
PACKAGE	14 Pin DIP and Flat Pak



9617 TRIPLE EIA RS232C LINE RECEIVER

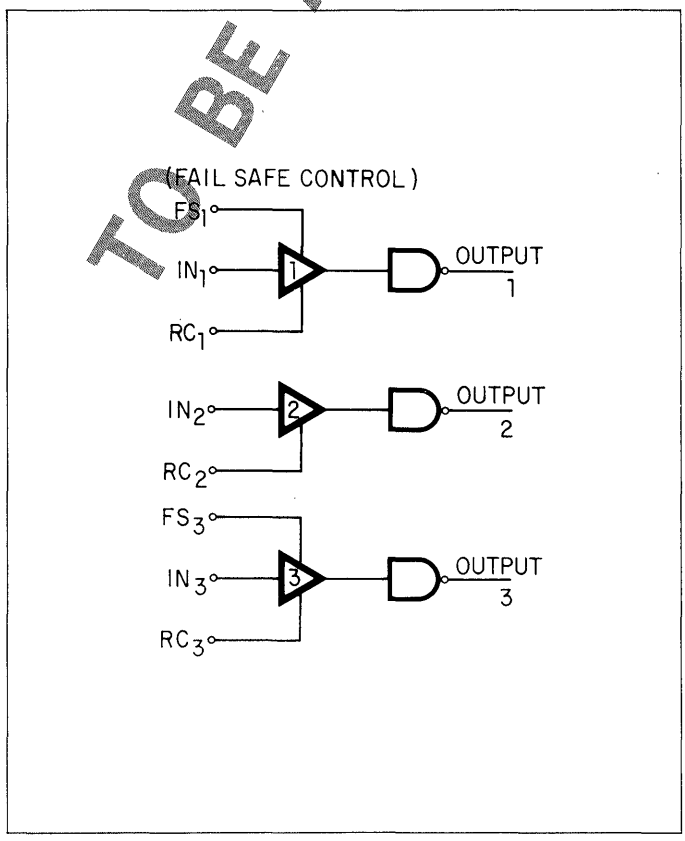
DESCRIPTION The 9617 is a triple line receiver which meets the requirements of EIA Specification RS232C. The three independent line receivers feature single ended inputs and outputs, a frequency response control input and selection of a "Fail Safe" control which provides a predetermined output level for line disconnect, line short, or driver power off conditions. The 9617 operates from +12 V and −12 V power supplies and is designed for use in industrial data communications applications.

PIN NAMES

IN_1, IN_2, IN_3	Data Inputs
OUT_1, OUT_2, OUT_3	Data Outputs
RC_1, RC_2, RC_3	Response Control
FS_1, FS_3	Fail Safe Control

CHARACTERISTICS

INPUT VOLTAGE RANGE	±25 V
PROPAGATION DELAY	200 ns
POWER DISSIPATION	80 mW/Receiver
PACKAGE	14 Pin DIP and Flat Pak



9620 DUAL DIFFERENTIAL LINE RECEIVER

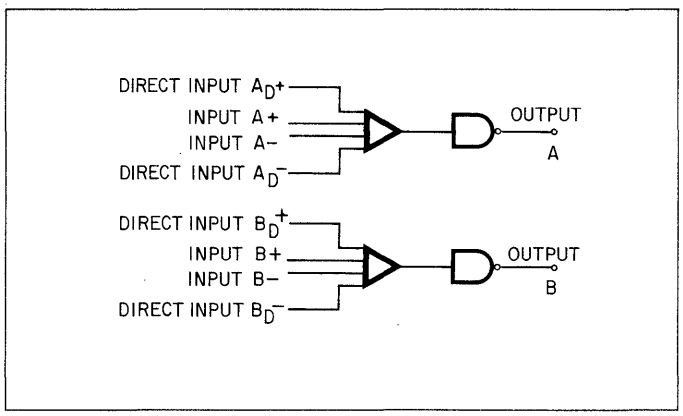
DESCRIPTION The 9620 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTμL logic to the output. In addition to line reception the 9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTμL, HLLDTμL, RTμL and TTL. HLLDTμL logic can be provided by tying the output to V_{CC2}(+12 V) through a resistor. The outputs can also be wire-OR'ed. The 9620 offers the advantages of logic compatible voltages (+5 V, +12 V), TTL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

PIN NAMES

A^+, B^+, A^-, B^-	Inputs
$A_D{}^+$, $B_D{}^+$, $A_D{}^-$, $B_D{}^-$	Direct Inputs
OUT_A, OUT_B	Data Outputs

CHARACTERISTICS

COMMON MODE VOLTAGE	±17.5 V
DIFFERENTIAL INPUT THRESHOLD	120 mV
POWER DISSIPATION	120 mW/Recover
PACKAGE	14 Pin DIP (6A) or Flat Pak (3I)

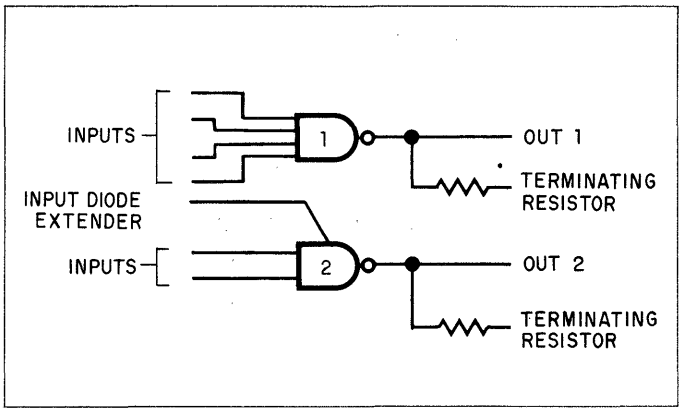


9621 DUAL LINE DRIVER

DESCRIPTION The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130 Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

CHARACTERISTICS

CLAMPED OUTPUT VOLTAGE	6.0 V
PROPAGATION DELAY	11 ns
POWER DISSIPATION	95 mW/Driver
PACKAGE	14 Pin DIP (6A) or Flat Pak (3I)



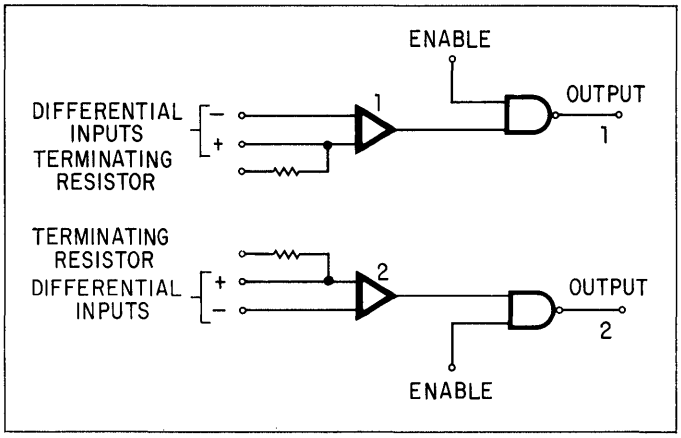
9622 DUAL LINE RECEIVER

DESCRIPTION The 9622 is a dual line receiver designed to discriminate a worst case logic swing of 2 volts from a ± 10 volt common mode noise signal or ground shift. A 1.5 volt threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ± 5% (75 mV) over the military and industrial temperature ranges.

The 9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S3. A 130 Ω terminating resistor is provided at the input of the each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to +12 V by tying it to a positive supply through a resistor. The outputs can be wire-OR'ed.

CHARACTERISTICS

COMMON MODE VOLTAGE	±12 V
DIFFERENTIAL INPUT THRESHOLD	1.5 V
POWER DISSIPATION	150 mW/Line Receiver
PACKAGE	14 Lead DIP (6A) or Flat Pak (3I)

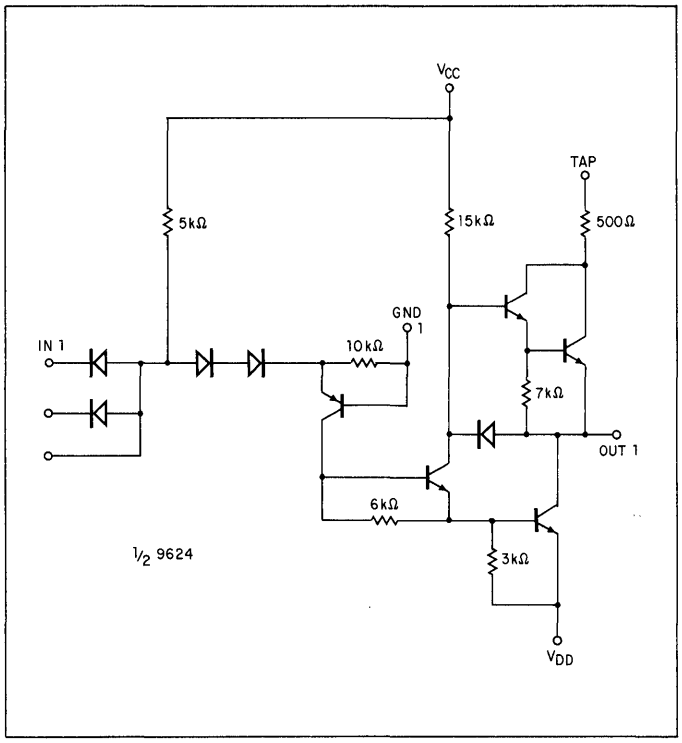


9624 DUAL TTL TO MOS INTERFACE ELEMENT

DESCRIPTION The 9624 is a dual two-input TTμL compatible interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

CHARACTERISTICS

PROPAGATION DELAY	120 ns
POWER DISSIPATION	30 mW/Gate
PACKAGE	14 Pin DIP (6A) or Flat Pak (3I)

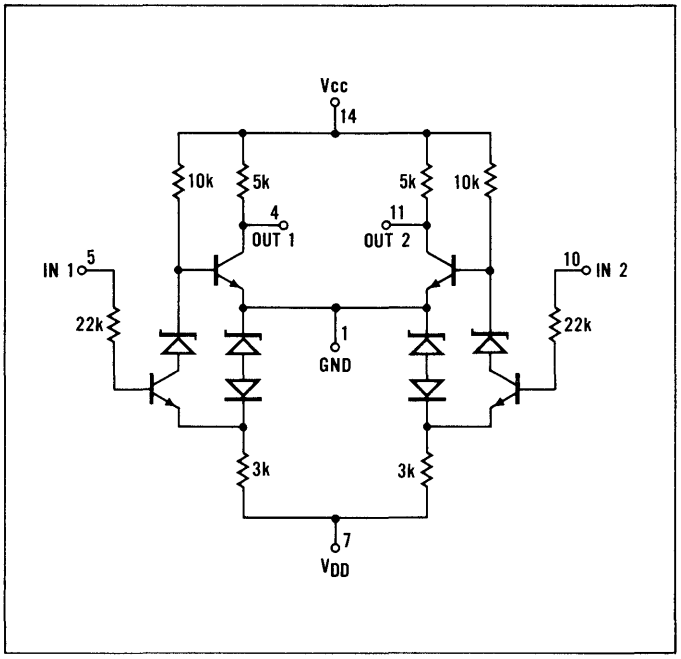


9625 DUAL MOS TO TTL INTERFACE ELEMENT

DESCRIPTION The 9625 is a dual MOS to TTμL level converter. It is designed to convert standard negative MOS logic levels to TTμL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

CHARACTERISTICS

PROPAGATION DELAY	73 ns
POWER DISSIPATION	25 mW/Gate
PACKAGE	14 Pin DIP (6A) or Flat Pak (3I)

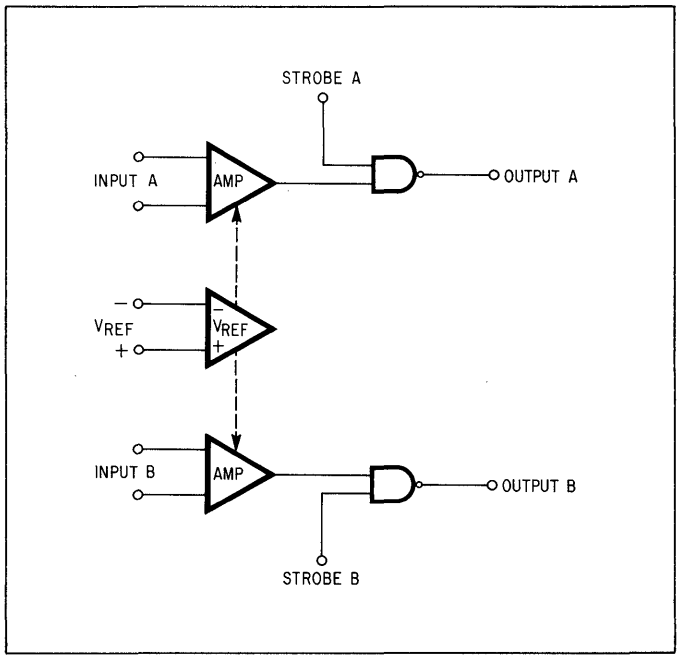


9664/7524 • 9665/7525 CORE MEMORY SENSE AMPLIFIERS

DESCRIPTION The 9664 and 9665 are two channel core memory sense amplifiers constructed on a silicon chip using the patented Fairchild Planar® epitaxial process. They can be used for small (1k to 8k words) memories as well as larger memory systems. These devices are suitable for small core sizes facilitating very fast memory cycle times. The 9664 and 9665 feature tight threshold accuracy, fast response time, independent strobe selection and are intended to be pin for pin replacements for the 7524 and 7525. Unit to unit variations are minimized so that individual adjustments of the threshold and strobe timing are unnecessary. The 9664 and 9665 are identical except for the guaranteed threshold accuracy (±4 mV for the 9664 and ±7 mV for the 9665).

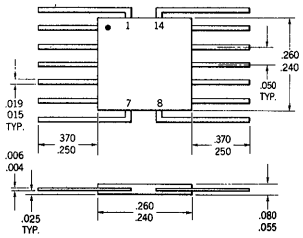
CHARACTERISTICS

THROUGH DELAY	30 ns
THRESHOLD UNCERTAINTY	±2 mV
POWER DISSIPATION	175 mW Total
PACKAGE	16 Lead DIP (7B)



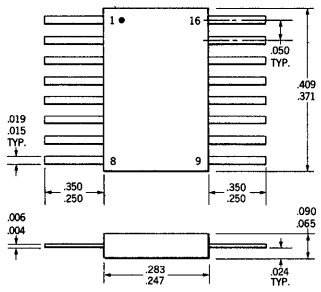
TTL PACKAGE DRAWINGS

in accordance with JEDEC (TO-86) outline 14 Lead Cerpak — 3I*



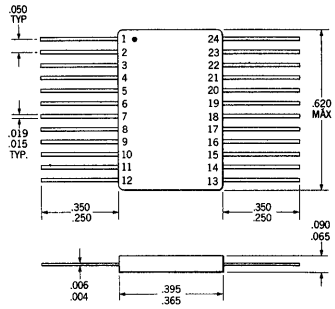
NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.26 gram.
3B is used for larger die, the outline dimensions are the same as 3I.

16 Lead BeO Cerpak — 4L



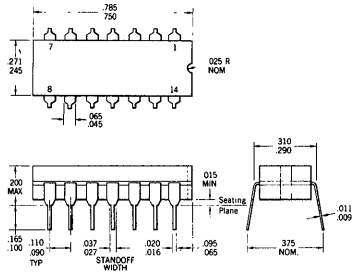
NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.4 gram.

24 Lead BeO Cerpak — 4M



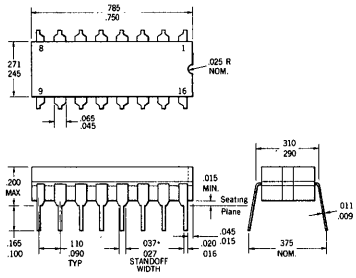
NOTES:
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 0.8 gram.

in accordance with JEDEC (TO-116) outline 14 Lead Dual In-line — 6A



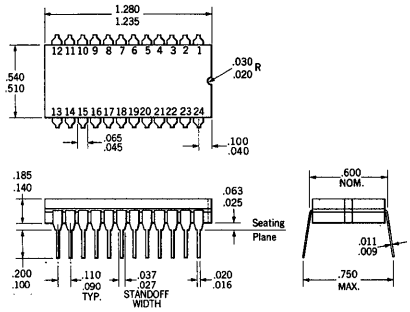
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.0 grams.

16 Lead SSI Dual In-line — 6B



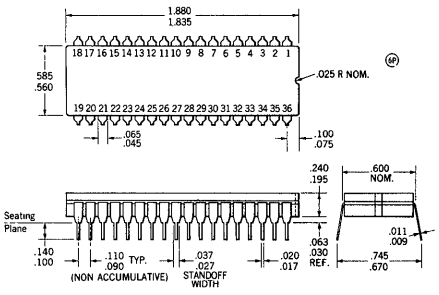
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are tin-plated kovar.
Package weight is 2.0 grams.
Hermetically sealed alumina ceramic package.
* The .037/.027 dimension does not apply to the corner leads.

24 Lead Dual In-line — 6N



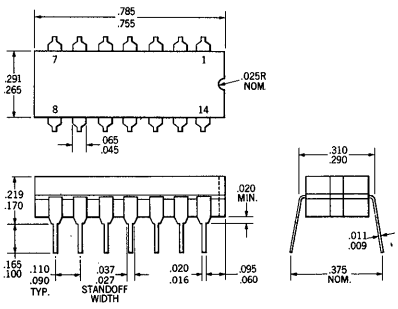
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .600" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Leads are tin-plated kovar.
Package weight is 6.5 grams.

36 Lead MSI Dual In-line — 6P



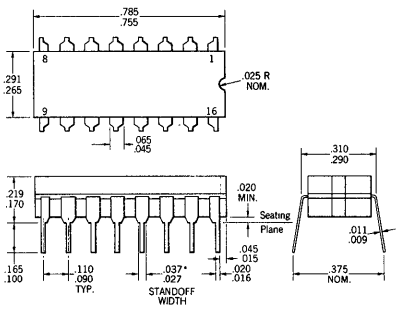
NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .600" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Leads are tin-plated kovar.
Package weight is 14.3 grams.

Similar* to JEDEC (TO-116) outline 14 Lead MSI Dual In-line — 7A

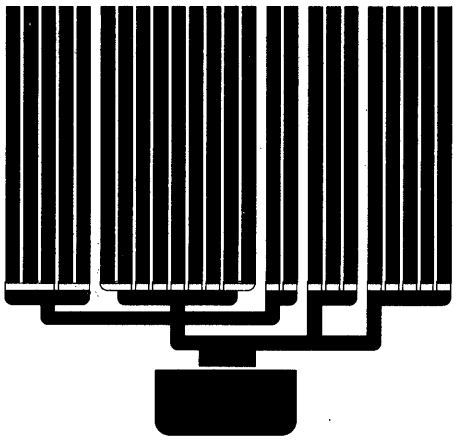


NOTES:
All dimensions in inches.
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.2 grams.
* Similar to JEDEC TO-116 except for package width.

16 Lead MSI Dual In-line — 7B



NOTES:
All dimensions in inches.
Lead are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Hermetically sealed alumina ceramic package.
Leads are tin-plated kovar.
Package weight is 2.2 grams.
* The .027 dimension does not apply to the corner leads.



LOADING CHARTS

INTRODUCTION The optimum design of a data processing system should take into account the difference in speed requirements for various parts of the system. It may be advantageous to mix high-speed, standard, and low-power TTL devices in the same system in order to minimize cost and power consumption and increase performance. For this reason, all devices in the Fairchild TTL family are completely compatible in supply voltage, logic input and output voltages and noise margins.

Still, there are some variations in input and output loading characteristics of high-speed, standard and low-power TTL circuits. These differences must be considered when mixing circuits in a system. The following tables list the input and output loading factors for each device in the Fairchild TTL family.

These loading tables are normalized around the standard TTL family. The input and output loads of the standard TTL circuits are given a numerical value of 1, and all other devices are defined in relation to the standard circuits.

The devices within any particular family are generally designed to drive up to 10 similar circuits. For example, a 9N or 9300-series device can drive up to 10 similar devices; however, a 9N-series device will drive only eight 9H-series circuits. A 9L or 93L-series circuit will drive up to 10 9L or 93L circuits, but will drive only two 9N or 9H-series devices.

The table below shows the actual and normalized relationship between the three TTL families.

	SERIES 9000 9N/54, 74 9300/54, 74	SERIES 9H/54H, 74H 93H	SERIES 9L 93L
Max Input "O" Current	1.6 mA	2.0 mA	0.40 mA
Normalized Fan In	1	1.25	0.25
Max Output "O" Current	16 mA	20 mA	4.0 mA
Normalized Fan Out	10	12.5	2.5

TTL/SSI 9000 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9000	J, K, C_P Inputs JK Input $\overline{S}_D$, $\overline{C}_D$ Outputs	1.0 2.0 2.7	 10.0
9001	J, K, C_P Inputs JK Input $\overline{S}_D$, $\overline{C}_D$ Outputs	1.0 2.0 2.7	 10.0
9002	Any Input Any Output	1.0	 10.0
9003	Any Input Any Output	1.0	 10.0
9004	Any Input Any Output	1.0	 10.0
9005	Any Input Any Output	1.5	 10.0
9006	Any Input Any Output	1.5	 N/A
9007	Any Input Any Output	1.0	 10.0
9008	Any Input Any Output	1.5	 10.0
9009	Any Input Any Output	2.0	 30.0
9012	Any Input Any Output	1.0	 O.C.
9014	Any Input Any Output	1.5	 10.0

LOADING CHARTS

TTL/SSI 9000 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9015	Any Input Any Output	1.0	 10.0
9016	Any Input Any Output	1.0	 10.0
9017	Any Input Any Output	1.0	 O.C.
9020	J, K Inputs C_P Input $\overline{C}_D$ Inputs JK Input Outputs	1.0 2.0 2.7 4.0	 10.0
9022	J, $\overline{K}$ Inputs C_P Input $\overline{S}_D$, $\overline{C}_D$ Inputs JK Input Outputs	1.0 2.0 2.7 4.0	 10.0
9024	J, $\overline{K}$ Inputs C_P, $\overline{S}_D$ Inputs $\overline{C}_D$ Input Outputs	1.0 2.0 3.0	 10.0

TTL/SSI 9N/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9N00/ 7400, 5400	Any Input Any Output	1.0	 10.0
9N01/ 7401, 5401	Any Input Any Output	1.0	 O.C.
9N02/ 7402, 5402	Any Input Any Output	1.0	 10.0
9N03/ 7403, 5403	Any Input Any Output	1.0	 O.C.
9N04/ 7404, 5404	Any Input Any Output	1.0	 10.0
9N05/ 7405, 5405	Any Input Any Output	1.0	 O.C.
9N08/ 7408, 5408	Any Input Any Output	1.0	 10.0

TTL/SSI 9N/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9N10/ 7410, 5410	Any Input Any Output	1.0	 10.0
9N11/ 7411, 5411	Any Input Any Output	1.0	 10.0
9N20/ 7420, 5420	Any Input Any Output	1.0	 10.0
9N30/ 7430, 5430	Any Input Any Output	1.0	 10.0
9N40/ 7440, 5440	Any Input Any Output	1.0	 30.0
9N50/ 7450, 5450	A, B, C, or D Input X and $\overline{X}$ Input Any Output	1.0 N/A	 10.0
9N51/ 7451, 5451	Any Input Any Output	1.0	 10.0
9N53/ 7453, 5453	A, B, C, D, E, F, G and H Input X or $\overline{X}$ Input Output	1.0 N/A	 10.0
9N54/ 7454, 5454	Any Input Any Output	1.0	 10.0
9N60/ 7460, 5460	Any Input X or $\overline{X}$ Output	1.0	 N/A
9N70/ 7470, 5470	J_1, J_2, J*, K_1, K_2, K* Inputs Clock Input Preset or Clear Input Q or $\overline{Q}$ Output	1.0 1.0 2.0	 10.0
9N72/ 7472, 5472	J_1, J_2, J_3, K_1, K_2, K_3 Inputs Clock Input Preset or Clear Inputs Q or $\overline{Q}$ Output	1.0 2.0 2.0	 10.0
9N73/ 7473, 5473	J or K Input Clock Input Clear Input Q or $\overline{Q}$ Output	1.0 2.0 2.0	 10.0

LOADING CHARTS

TTL/SSI 9N/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9N74/ 7474, 5474	D Input Clock Input Preset Input Clear Input Q or $\overline{Q}$ Output	1.0 2.0 2.0 3.0	 10.0
9N76/ 7476, 5476	J or K Input Clock Input Clear Input Preset Input Q or $\overline{Q}$ Output	1.0 2.0 2.0 2.0	 10.0
9N86/ 7486, 5486	Any Input Any Output	1.0	 10.0

TTL/SSI 9L SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9L00	Any Input Any Output	0.25	 2.5
9L04	Any Input Any Output	0.25	 2.5
9L24	J, $\overline{K}$ Inputs C_P, $\overline{S}_D$ Inputs $\overline{C}_D$ Input Outputs	0.25 0.50 0.75	 2.5
9L54	Any Input Any Output	0.25	 2.5

TTL/SSI 9H SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9H00/ 74H00, 54H00	Any Input Any Output	1.25	 12.5
9H01/ 74H01, 54H01	Any Input Any Output	1.25	 O.C.
9H04/ 74H04, 54H04	Any Input Any Output	1.25	 12.5
9H05/ 74H05, 54H05	Any Input Any Output	1.25	 O.C.
9H10/ 74H10, 54H10	Any Input Any Output	1.25	 12.5
9H20/ 74H20, 54H20	Any Input Any Output	1.25	 12.5
9H30/ 74H30, 54H30	Any Input Any Output	1.25	 12.5
9H40/ 74H40, 54H40	Any Input Any Output	1.25	 37.5
9H72/ 74H72, 54H72	J_1, J_2, J_3, K_1, K_2, K_3 Inputs Preset or Clear Inputs Clock Input Q or $\overline{Q}$ Output	1.25 2.50 1.25	 12.5
9H73/ 74H73, 54H73	J, K, or Clock Input Clear Input Q or $\overline{Q}$ Output	1.25 2.50	 12.5
9H76/ 74H76, 54H76	J, K, or Clock Input Clear or Preset Input Q or $\overline{Q}$ Output	1.25 2.50	 12.5

TTL/MSI 93/54, 74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9300	$\overline{PE}$ Input P_0 to P_3, J, $\overline{K}$, $\overline{MR}$ Inputs C_P Input All Outputs	2.3 1.0 2.0	 6.0
9301	All Inputs All Outputs	1.0	 10.0
9304	A, B, C, $\overline{A}_2$, $\overline{B}_2$, $\overline{C}_2$ Inputs C_0 Output S Output $\overline{S}$ Output	4.0	 7.0 10.0 9.0
9305	S_0, S_1 Inputs All Other Inputs All Outputs	2.0 1.0	 8.0

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9306	P_0 to P_3 Inputs $\overline{PE}$, CP Inputs CE_0 to CE_5, $\overline{C}_D$ Inputs All Outputs	0.67 2.0 1.0	 6.0
9307	A_0 to A_3 Inputs $\overline{LT}$ Input $\overline{RBI}$ Input $\overline{RBO}$ Output All Other Outputs	1.0 4.0 0.5	 1.5 7.0
9308	D_0 to D_3 Inputs $\overline{E}_0$, $\overline{E}_1$, $\overline{MR}$ Inputs Q_0 to Q_3 Outputs	1.5 1.0	 9.0
9309	All Inputs Z_a, Z_b Outputs $\overline{Z}_a$, $\overline{Z}_b$ Outputs	1.0	 10.0 9.0

LOADING CHARTS

TTL/MSI 93/54,74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9310	$\overline{PE}$, CET, C_P Inputs	2.0	
	CEP, $\overline{MR}$ Inputs	1.0	
	P_0 to P_3	0.67	
	All Outputs		6.0
9311	All Inputs	1.0	
	All Outputs		10.0
9312	All Inputs	1.0	
	$\overline{Z}$ Output		10.0
	$\overline{Z}$ Output		9.0
9314	$\overline{E}$, $\overline{S}_0$ to $\overline{S}_3$, $\overline{MR}$ Inputs	1.0	
	D_0 to D_3 Inputs	1.5	
	All Outputs		9.0
9315/ 7441	All Inputs	1.0	
	All Outputs		N/A
9316	$\overline{PE}$, CET, C_P Inputs	2.0	
	CEP, $\overline{MR}$ Inputs	1.0	
	P_0 to P_3 Inputs	0.67	
	All Outputs		6.0
9317	A_0, A_1, A_2, A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		N/A
9318	$\overline{0}$ Input	1.0	
	$\overline{1}$ to $\overline{7}$, $\overline{EI}$ Inputs	2.0	
	$\overline{EO}$ Output		5.0
	$\overline{GS}$ Output		6.0
	$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ Outputs		10.0
9321	All Inputs	1.0	
	All Outputs		10.0
9322	All Inputs	1.0	
	All Outputs		10.0
9324	All Inputs	2.0	
	A<B, A>B Outputs		9.0
	A = B Output		10.0
9325/ 54141, 74141	All Inputs	1.0	
	All Outputs		N/A
9327	A_0, A_1, A_2, A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		N/A

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9328	D_S Input	2.0	
	D_0, D_1, $\overline{MR}$ Inputs	1.0	
	C_P (Common)	3.0	
	C_P (Separate)	1.5	
	All Outputs		6.0
9334	A_0, A_1, A_2, D, $\overline{C}$ Inputs	1.0	
	$\overline{E}$ Input	1.5	
	All Outputs		6.0
9337	A_0, A_1, A_2, A_3 Inputs	1.0	
	$\overline{LT}$ Input	4.0	
	$\overline{RBI}$ Input	0.5	
	$\overline{RBO}$ Output		1.5
	All Other Outputs		N/A
9338	A_0, A_1, A_2 Inputs	0.67	
	B_0, B_1, B_2 Inputs	0.67	
	C_0, C_1, C_2 Inputs	0.67	
	D_A, C_P, $\overline{SLE}$	0.67	
	All Outputs		10.0
9340	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, $\overline{CG}_1$ Inputs	3.0	
	S_0, S_1, $\overline{CP}_1$, $\overline{CP}_2$, $\overline{CG}_3$ Inputs	1.0	
	$\overline{CG}_2$ Input	2.0	
	COE Input	1.5	
	All Outputs		10.0
9341/ 54181, 74181	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, Inputs	3.0	
	S_0 to S_3 Inputs	4.0	
	C_{IN} Input	5.0	
	$\overline{CE}$ Input	1.0	
	C_0, $\overline{CG}$, A = B Outputs		8.0
	$\overline{CP}$ Output		7.0
	$\overline{F}_0$ to $\overline{F}_3$ Outputs		10.0
9342/ 54182, 74182	C_{IN} Input	2.0	
	$\overline{CP}_0$ to $\overline{CP}_3$ Inputs	4.0	
	$\overline{CG}_0$, $\overline{CG}_2$ Inputs	9.0	
	$\overline{CG}_1$ Input	10.0	
	$\overline{CG}_3$ Input	5.0	
	All Outputs		10.0
9348	All Inputs	2.0	
	All Outputs		10.0
9350	$\overline{MR}$, MS Inputs	1.0	
	$\overline{CP}_0$ Input	2.0	
	$\overline{CP}_1$ Input	4.0	
	All Outputs		10.0
9352/ 5442, 7442	All Inputs	1.0	
	All Outputs		10.0
9353/ 5443, 7443	All Inputs	1.0	
	All Outputs		10.0
9354/ 5444, 7444	All Inputs	1.0	
	All Outputs		10.0

LOADING CHARTS

TTL/MSI 93/54,74 SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9356	MR Input	1.0	
	$\overline{CP_0}$, $\overline{CP_1}$ Inputs	2.0	
	All Outputs		10.0
9357A/ 5446, 7446	A, B, C, D, $\overline{RBI}$, $\overline{LT}$ Inputs	1.0	
	$\overline{BI/RBO}$ Input	2.6	
	$\overline{a}$ to $\overline{g}$ Outputs		12.5
	BI/RBO Output		5.0
9357B/ 5447, 7447	A, B, C, D, $\overline{RBI}$, $\overline{LT}$ Inputs	1.0	
	$\overline{BI/RBO}$ Input	2.6	
	$\overline{a}$ to $\overline{g}$ Outputs		12.5
	$\overline{BI/RBO}$ Output		5.0
9358/ 5448, 7448	A, B, C, D, $\overline{RBI}$, $\overline{LT}$ Inputs	1.0	
	$\overline{BI/RBO}$ Input	2.6	
	a to g Outputs		6.0
	$\overline{BI/RBO}$ Output		5.0
9359/ 5449, 7449	All Inputs	1.0	
	All Outputs		6.0
9360/ 54192, 74192	All Inputs	1.0	
	All Outputs		10.0
9366/ 54193, 74193	All Inputs	1.0	
	All Outputs		10.0
9375/ 5475, 7475	D_1, D_2, D_3, D_4 Input	2.0	
	CP_{1-2}, CP_{2-3} Input	4.0	
9377/ 5477, 7477	All Outputs		10.0
9380/ 5480, 7480	A_1, A_2, B_1, B_2, A_C, B_C Input	1.0	
	A* or B* Input	1.65	
	C Input	5.0	
	Σ or $\overline{\Sigma}$ Output		10.0
	$\overline{C_{n+1}}$ Output		5.0
	A* or B* Output		3.0
9382/ 5482, 7482	A_1 or B_1 Input	4.0	
	A_2 or B_2 Input	1.0	
	C_{IN} Input	4.0	
	C_2 Output		5.0
	Σ_1 or Σ_2 Output		10.0
9383/ 5483, 7483	A_1, B_1, A_3, B_3 Inputs	4.0	
	A_2, B_2, A_4, B_4 Inputs	1.0	
	C_{IN} Input	4.0	
	C_4 Output		5.0
	Σ_1, Σ_2, Σ_3, Σ_4, Outputs		10.0
9390/ 5490, 7490	R_{01}, R_{02}, R_{91}, R_{92} Input	1.0	
	$\overline{CP_{B-D}}$ Input	4.0	
	$\overline{CP_A}$ Input	2.0	
	All Outputs		10.0
9391/ 5491, 7491	A or B Input	1.0	
	CP Input	1.0	
	Q or $\overline{Q}$ Output		10.0
9392/ 5492, 7492	R_{01} or R_{02} Input	1.0	
	$\overline{CP_{B-C}}$ Input	4.0	
	$\overline{CP_A}$ Input	2.0	
	All Outputs		10.0
9393/ 5493, 7493	R_{01} or R_{02} Input	1.0	
	$\overline{CP_B}$ Input	2.0	
	$\overline{CP_A}$ Input	2.0	
	All Outputs		10.0
9394/ 5494, 7494	P_{1A} to P_{1D}, P_{2A} to P_{2D} Inputs	1.0	
	D_S, CP, C_L Inputs	1.0	
	PE_1, PE_2 Inputs	4.0	
	All Outputs		10.0
9395/ 5495, 7495	M Input	2.0	
	P_A to P_D, $\overline{CP_1}$, $\overline{CP_2}$, D_S Inputs	1.0	
	All Outputs		10.0
9396/ 5496, 7496	PE Input	5.0	
	P_A to P_E, D_S, CP, $\overline{C_L}$ Inputs	1.0	
	All Outputs		10.0

LOADING CHARTS

TTL/MSI 93L SERIES

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93L00	$\overline{PE}$ Input	0.575	
	P_0 to P_3, J, $\overline{K}$, $\overline{MR}$ Inputs	0.25	
	C_P Input	0.50	
	All Outputs		2.0
93L01	All Inputs	0.25	
	All Outputs		2.5
93L08	D_0 to D_3 Inputs	0.375	
	$\overline{E}_0$, $\overline{E}_1$, $\overline{MR}$ Inputs	0.25	
	Q_0 to Q_3 Outputs		2.25
93L09	All Inputs	0.25	
	Z_a Z_b Outputs		2.50
	$\overline{Z}_a$ $\overline{Z}_b$ Outputs		2.25
93L10	$\overline{PE}$, CET, C_P Inputs	0.5	
	CEP, $\overline{MR}$ Inputs	0.25	
	P_0 to P_3 Inputs	0.17	
	All Outputs		1.5
93L11	All Inputs	0.25	
	All Outputs		2.5
93L12	All Inputs	0.25	
	Z Output		2.5
	$\overline{Z}$ Output		2.25
93L14	$\overline{E}$, $\overline{S}_0$ to $\overline{S}_3$, $\overline{MR}$ Inputs	0.25	
	D_0 toD_3 Inputs	0.375	
	All Outputs		2.25

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93L16	$\overline{PE}$, CET, C_P Inputs	0.5	
	CEP, $\overline{MR}$ Inputs	0.25	
	P_0 toP_3 Inputs	0.17	
	All Outputs		1.5
93L18	$\overline{0}$ Input	0.25	
	$\overline{I}$ to $\overline{7}$, EI Inputs	0.5	
	$\overline{EO}$ Output		1.25
	$\overline{GS}$ Output		1.5
	$\overline{A}_0$, $\overline{A}_1$, $\overline{A}_2$ Outputs		2.5
93L21	All Inputs	0.25	
	All Outputs		2.5
93L22	All Inputs	0.25	
	All Outputs		2.5
93L24	All Inputs	0.5	
	A < B A > B Output		2.25
	A = B Output		2.5
93L28	D_S Input	0.5	
	D_0, D_1, $\overline{MR}$ Inputs	0.25	
	C_P (Common)	0.75	
	C_P Separate	0.375	
	All Outputs		2.0
93L40	$\overline{A}_0$ to $\overline{A}_3$, $\overline{B}_0$ to $\overline{B}_3$, $\overline{CG}_{-1}$ Inputs	0.75	
	S_0, S_1, $\overline{CP}_{-1}$, $\overline{CP}_{-2}$, $\overline{CG}_{-3}$ Inputs	0.25	
	$\overline{CG}_{-2}$ Input	0.5	
	COE Input	0.375	
	All Outputs		2.5

TTL/MEMORY

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93400	X_0 to X_5 Inputs	1.0	
	Y_0 to Y_5 Inputs	0.18	
	R/W Input	0.12	
	Output		6.0
93401	E_1 to E_4 Inputs	0.25	
	A_0 to A_3 Inputs	0.25	
	X_0 to X_5 Outputs		8.0
93402	$\overline{A}_0$ to $\overline{A}_3$ Inputs	1.0	
	$\overline{D}_0$ to $\overline{D}_3$ Inputs	1.0	
	$\overline{E}_0$ to $\overline{E}_3$ Inputs	1.5	
	$\overline{WE}$ Input	1.5	
	M_0 to M_3, $\overline{M}_0$ Outputs		6.0
	$\overline{O}_0$ to $\overline{O}_3$ Outputs		6.0
93403	A_0 to A_3 Inputs	1.0	
	D_0 to D_3 Inputs	1.0	
	$\overline{WE}$, $\overline{CS}$ Inputs	1.0	
	$\overline{O}_0$ to $\overline{O}_3$ Outputs		6.0

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
93406	A_0 to A_7 Inputs	0.5	
	CS_0 to CS_1 Inputs	0.5	
	O_0 to O_3 Outputs		10.0
93433	X_0 to X_3 Inputs	11 mA at 2.1 V	
	Y_0 to Y_3 Inputs	11 mA at 2.1 V	
	W_0, W_1 Inputs	1.0	
	$\overline{S}_0$, $\overline{S}_1$ Outputs		12.5/25
93434	A_0 to A_4 Inputs	1.0	
	$\overline{E}$ Input	1.0	
	$\overline{O}_0$ to $\overline{O}_7$ Outputs		6.0
93435	A_0 to A_{15} Inputs	1.0	
	I_0 to I_3 Inputs	2.0	
	$\overline{CS}$, $\overline{WE}$ Inputs	1.0	
	$\overline{O}_0$ to $\overline{O}_3$ Outputs		6.0

LOADING CHARTS

TTL/INTERFACE 9600 SERIES

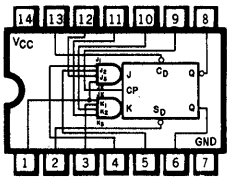
DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9600	Any Input Any Output	1.0	 6.0
9601	Any Input Any Output	1.0	 6.0
9602	Any Input Any Output	1.0	 6.0
9614	Input Output	1.0	 15 mA
9615	Input Output	N/A	 10.0
9616	Input Output	1.0	 15 mA
9617	Input Output	N/A	 10.0
9620	Line Input Output	N/A	 10.0

DEVICE TYPE	TERMINAL	NORMALIZED INPUT FACTOR	NORMALIZED OUTPUT FACTOR
9621	Line Input Output	1.5	 20 mA
9622	Line Input Strobe Input Output	N/A 1.0	 8.0
9624	Input Output	1.0	 N/A
9625	Input Output	N/A	 1.0
9644	Input Output	0.5	 500 mA, 30 V
9664/ 7524, 9665/ 7525	Sense Input Strobe Input Output	N/A 1.0	 10.0

TTL/SSI

TOP VIEW

9000



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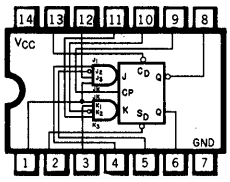

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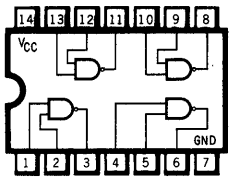

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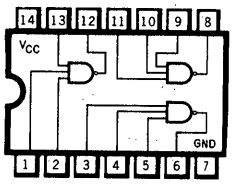
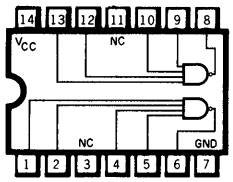


9004



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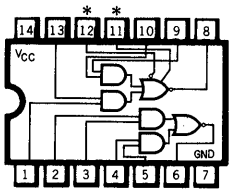
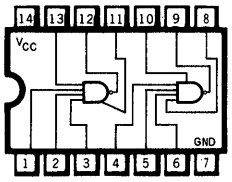
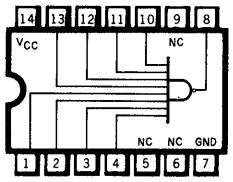


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS.

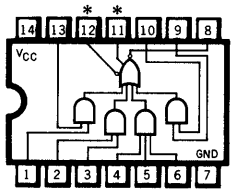
9006



9007



9008



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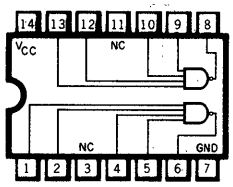
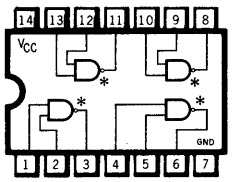
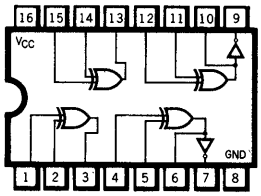
9009



9012

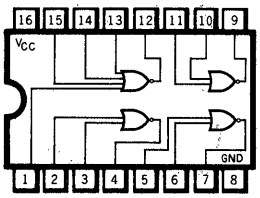


9014



*OPEN COLLECTOR

9015



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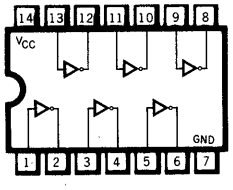
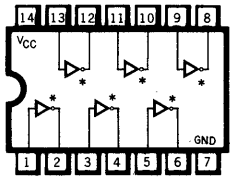


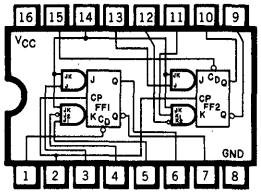
9017



*OPEN COLLECTOR

TTL/SSI

9020



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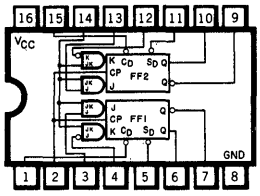
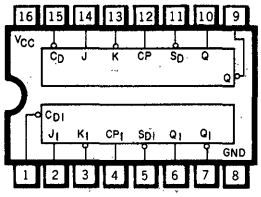
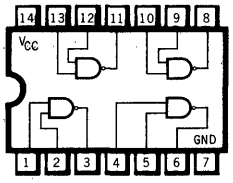


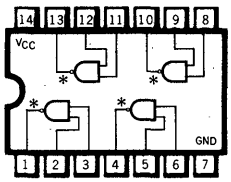
9024



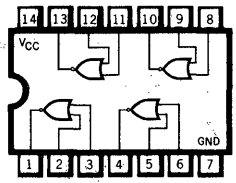
9N00/5400, 7400



9N01/5401, 7401



9N02/5402, 7402



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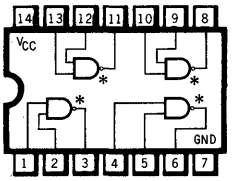
9N03/5403, 7403



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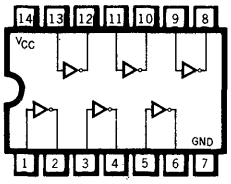
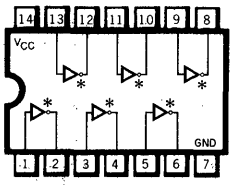
9N04/5404, 7404



9N05/5405, 7405



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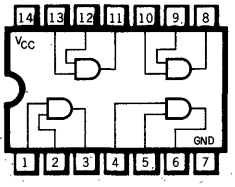
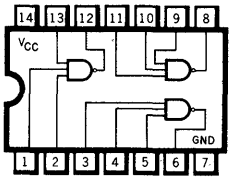
9N08/5408, 7408



9N10/5410, 7410



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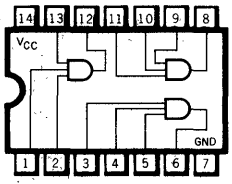

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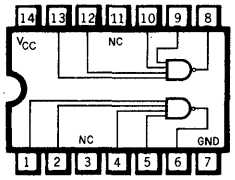

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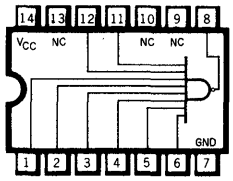

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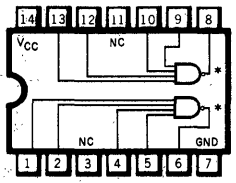

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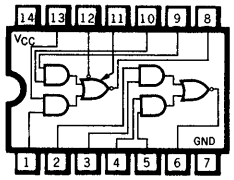

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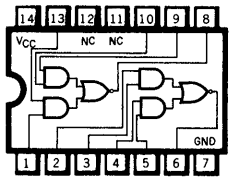

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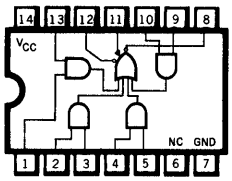

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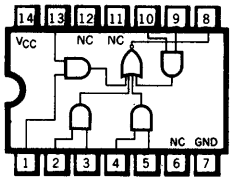

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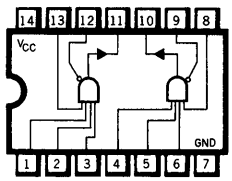

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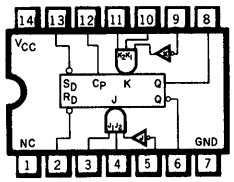

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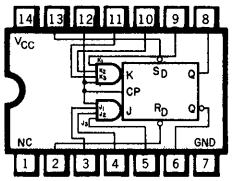

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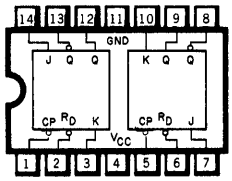

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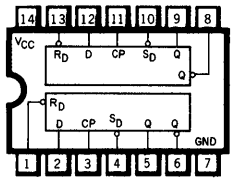

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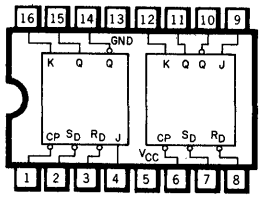

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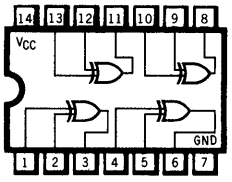

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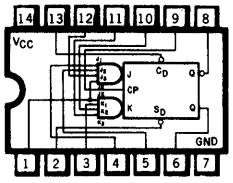

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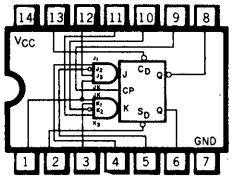

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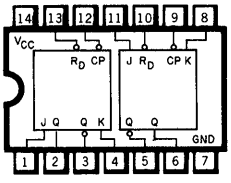

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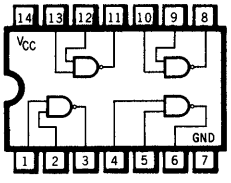

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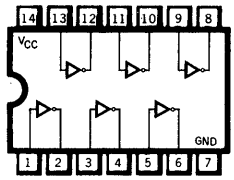

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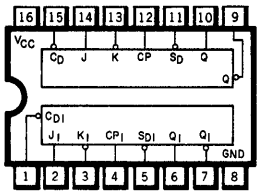

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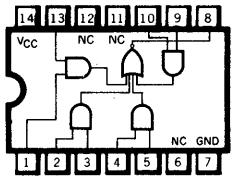

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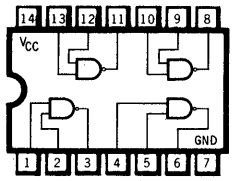

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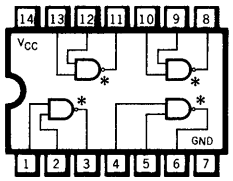

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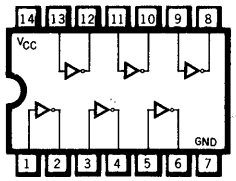

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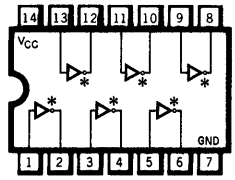

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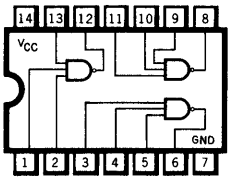

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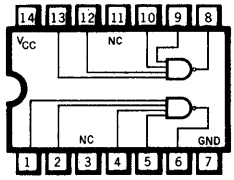

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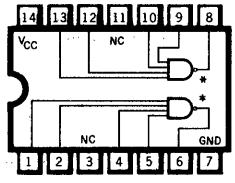

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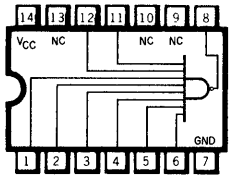

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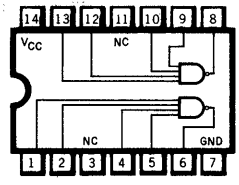

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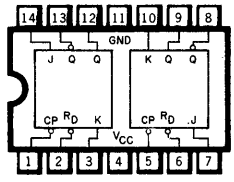

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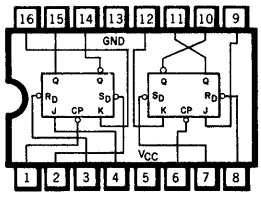

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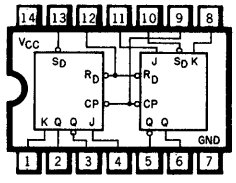

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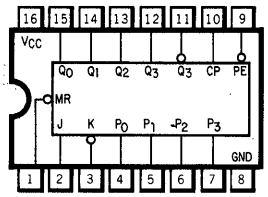

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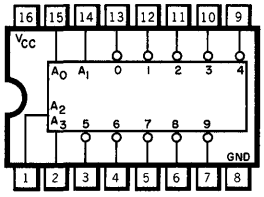

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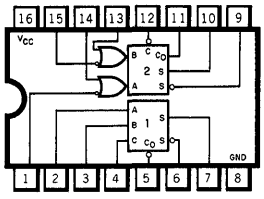

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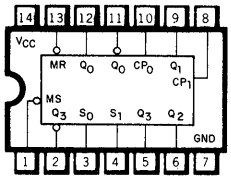

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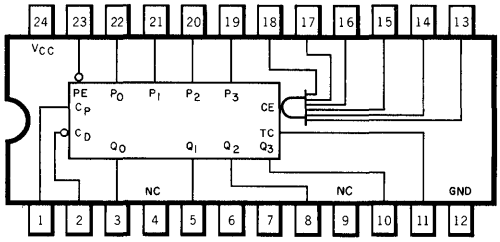

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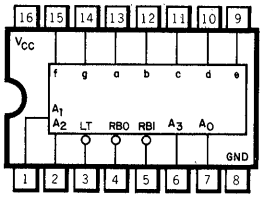

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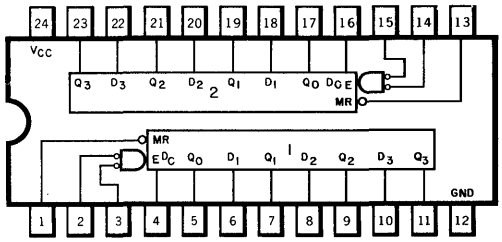

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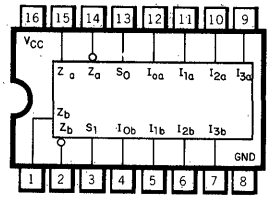

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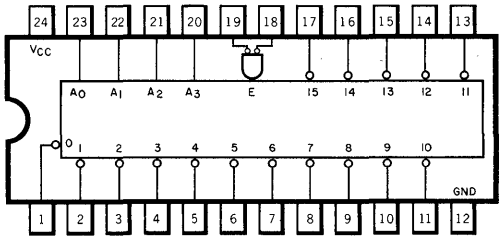

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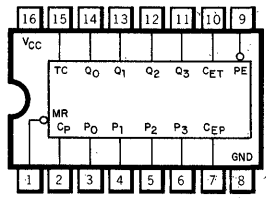

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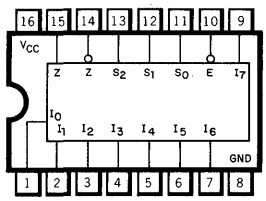

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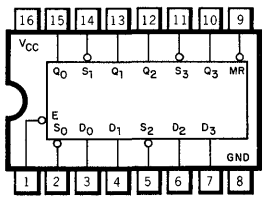
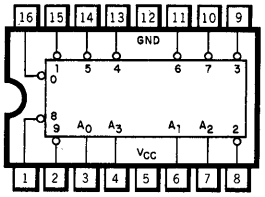


TTL/MSI

9315/7441



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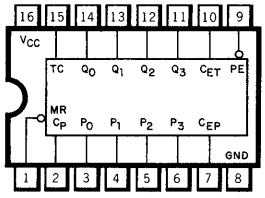

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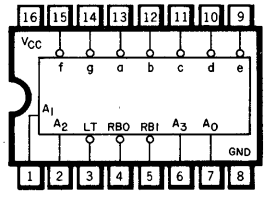

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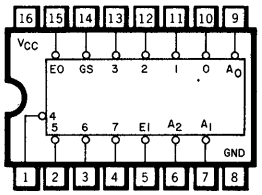

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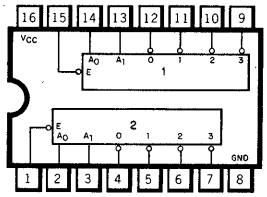

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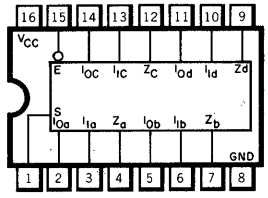

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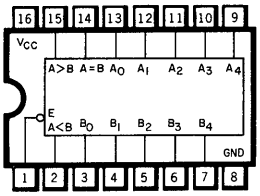

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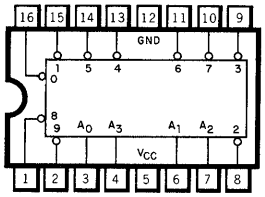

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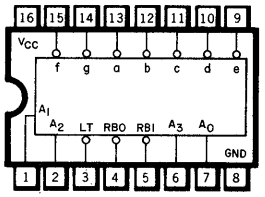

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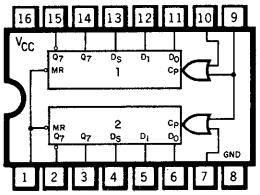

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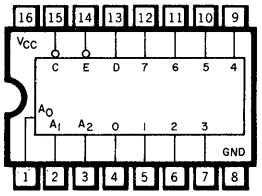

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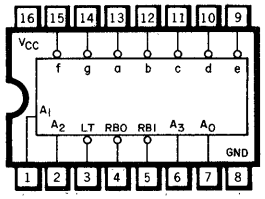

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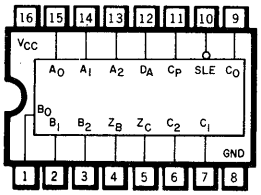

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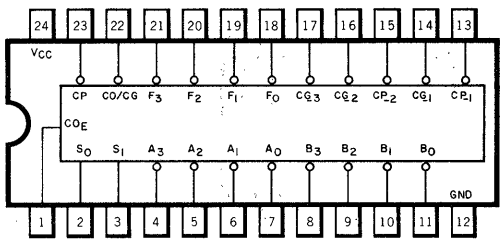
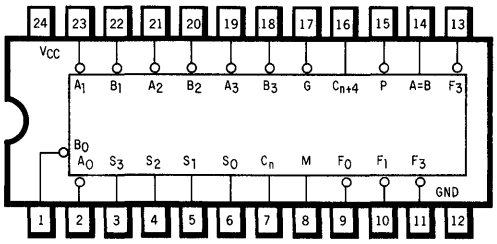
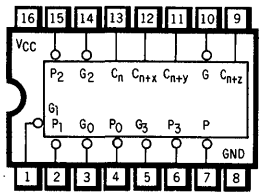


TTL/MSI

9341/54181, 74181



9342/54182, 74182



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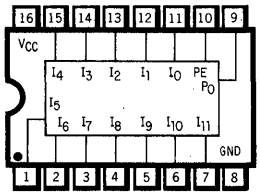

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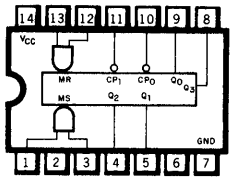
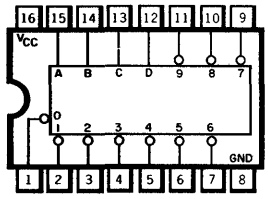
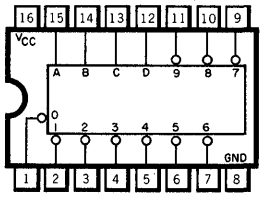


9352/5442, 7442



9353/5443, 7443



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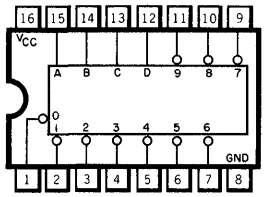

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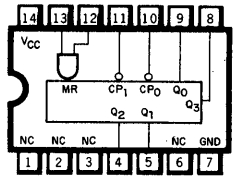
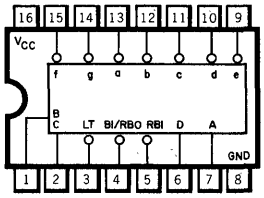


9357A/5446, 7446



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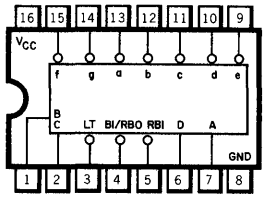

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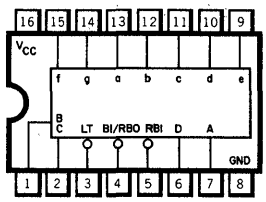

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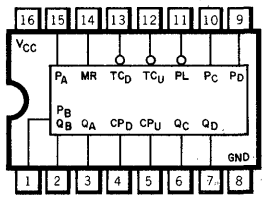

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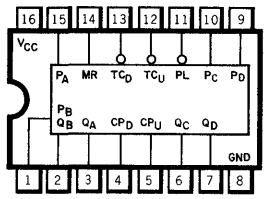

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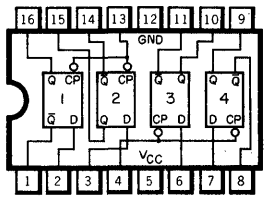
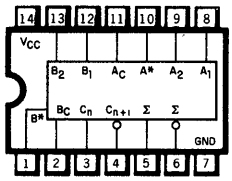


TTL/MSI

9380/5480, 7480



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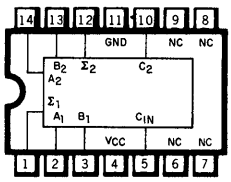

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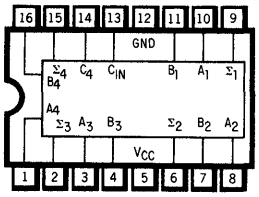
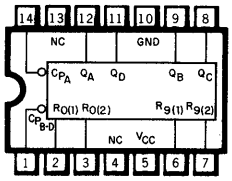


9390/5490, 7490



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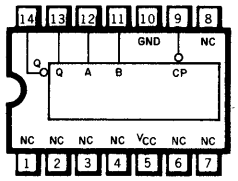

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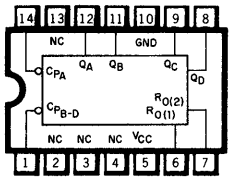

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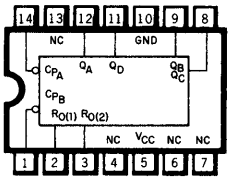

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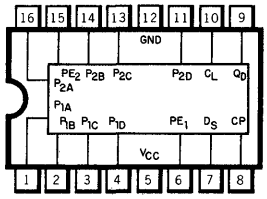

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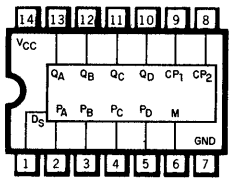

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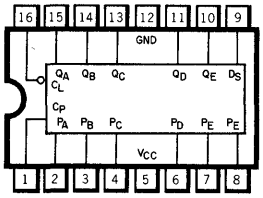
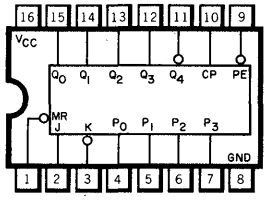


93L00



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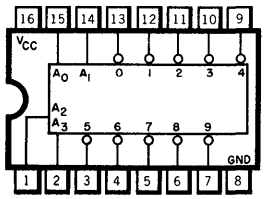

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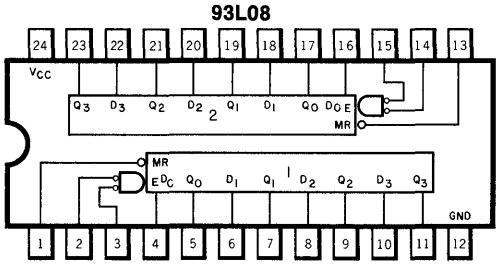

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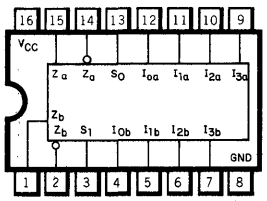
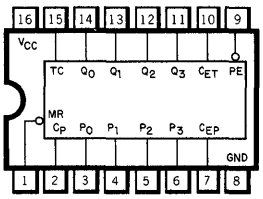


TTL/MSI

93L10



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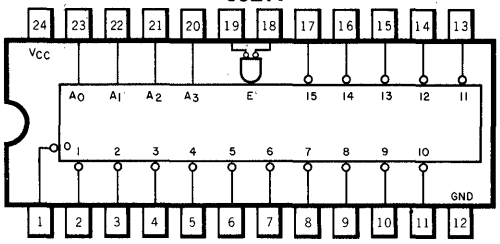
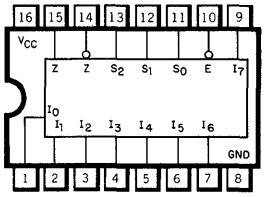


93L12



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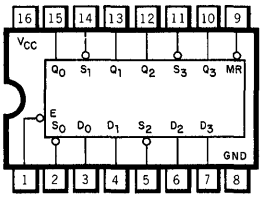

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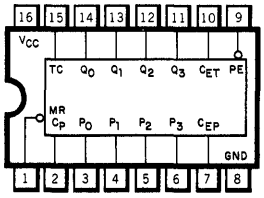
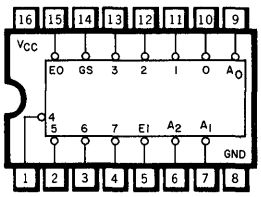
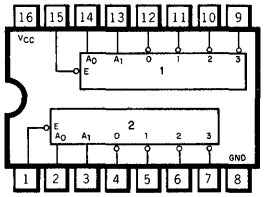


93L18



93L21



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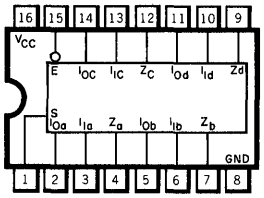

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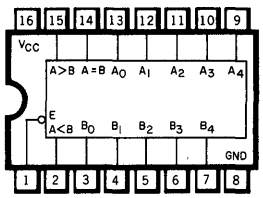

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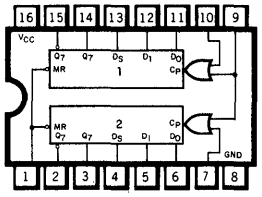

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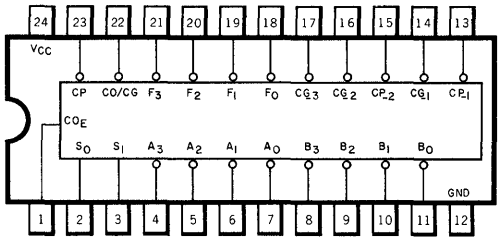
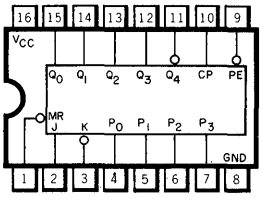


93H00



93H70/74196

TO BE ANNOUNCED

93H72

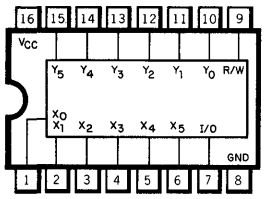
TO BE ANNOUNCED

93H76/74197

TO BE ANNOUNCED

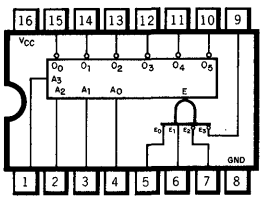
TTL/MEMORY

93400



FORMERLY 4100

93401



FORMERLY 4101

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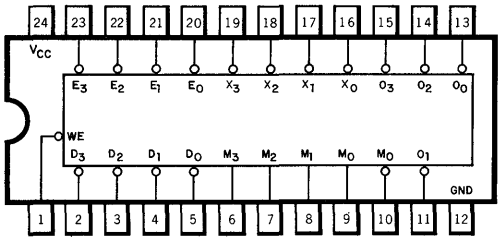

FORMERLY 4102

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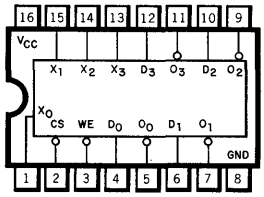

FORMERLY 4103

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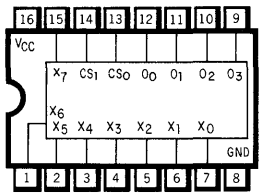

FORMERLY 4106

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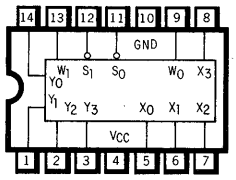

FORMERLY 5033

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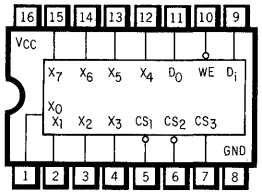
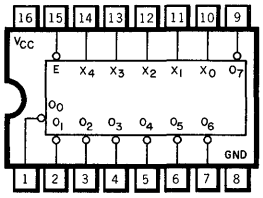


FORMERLY 4110

93412, 93434



FORMERLY 4112, 9034

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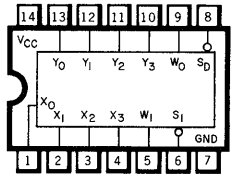
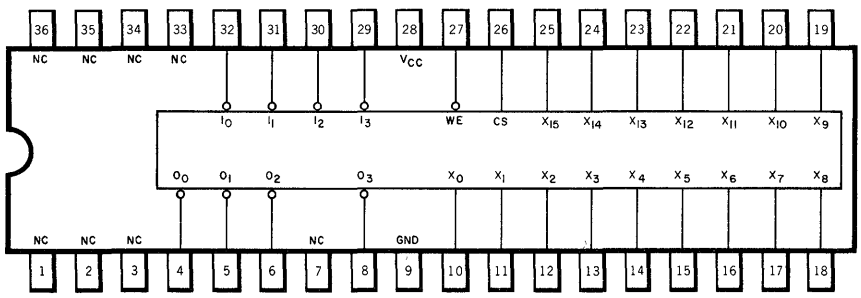


FORMERLY 9033

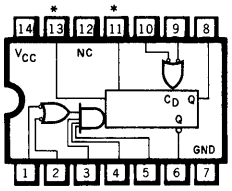
93435



FORMERLY 9035

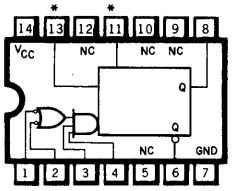
TTL/INTERFACE

9600



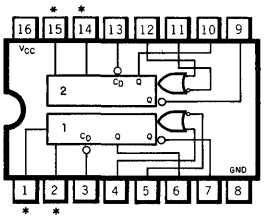
*PINS FOR EXTERNAL TIMING.

9601



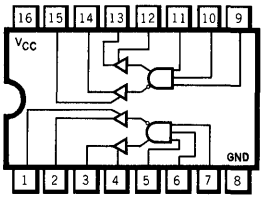
*PINS FOR EXTERNAL TIMING.

9602

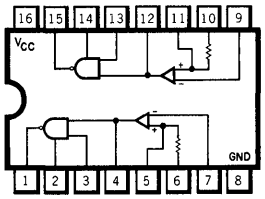


*PINS FOR EXTERNAL TIMING.

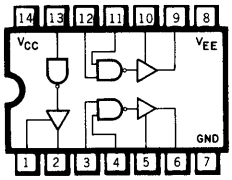
9614



9615



9616



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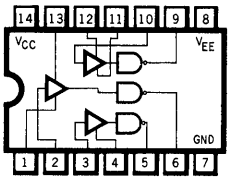

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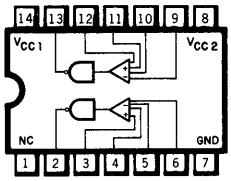

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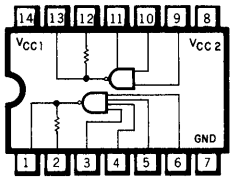

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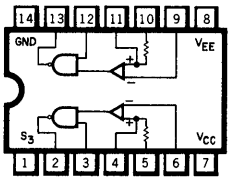

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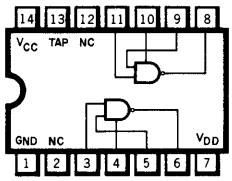

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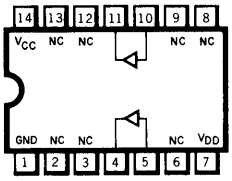

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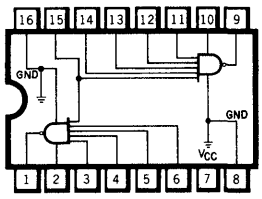

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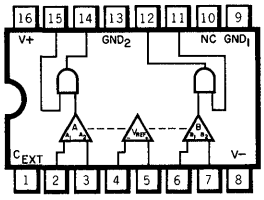

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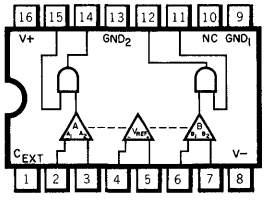
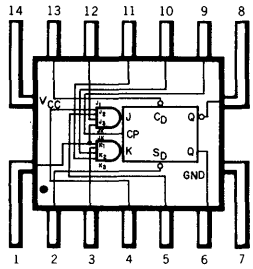


TTL/SSI

TOP VIEW

9000



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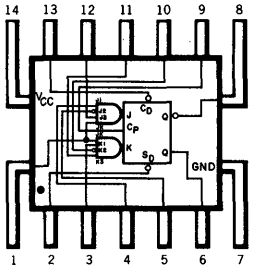

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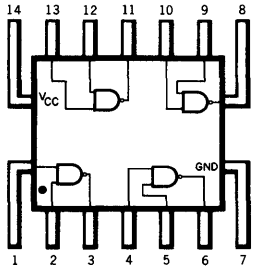

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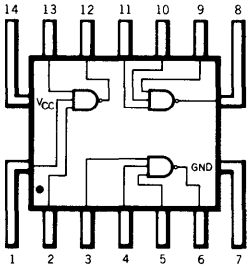

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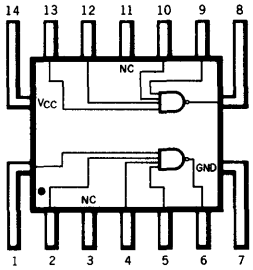

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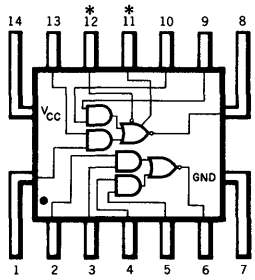
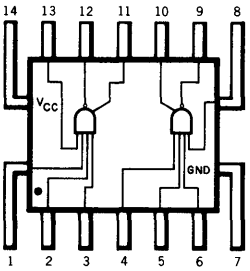


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS.

9006



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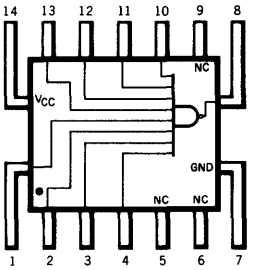

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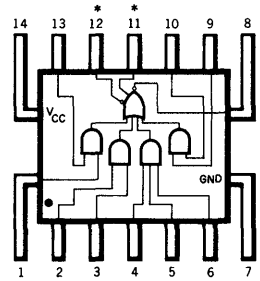
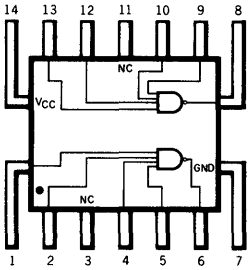


*FOUR EXTENDERS (9006) MAY BE TIED TO THESE PINS

9009



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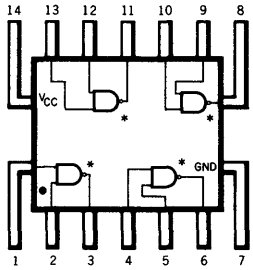

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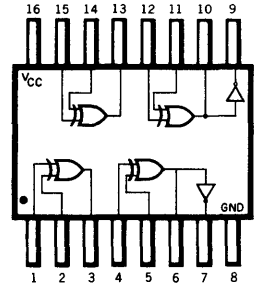

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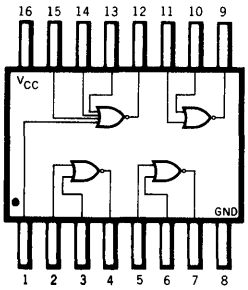

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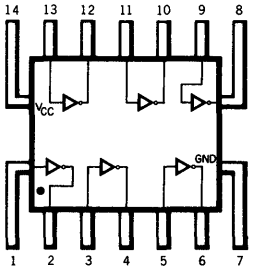

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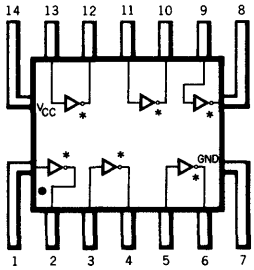

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TTL/SSI

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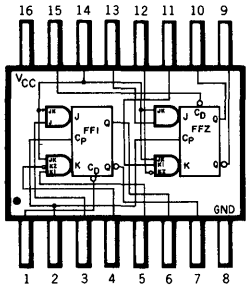

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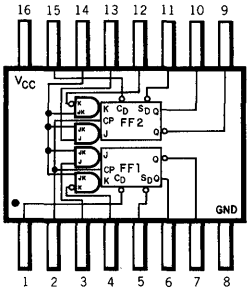

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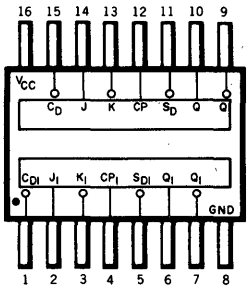

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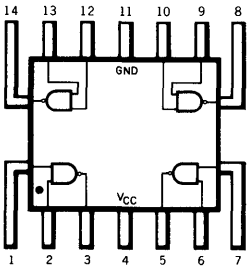

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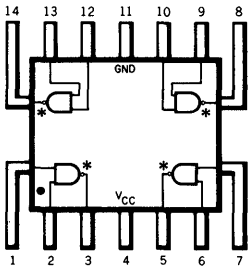

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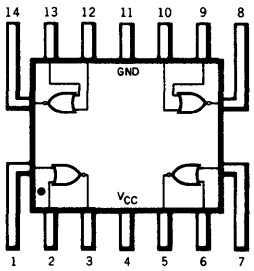
9N02/5402, 7402



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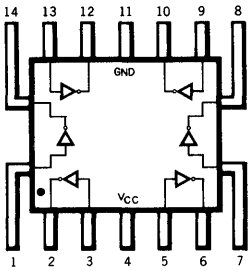

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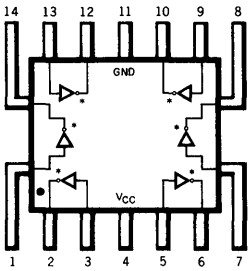

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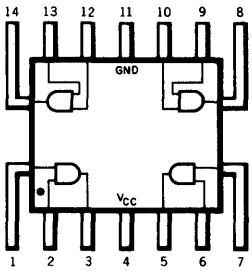

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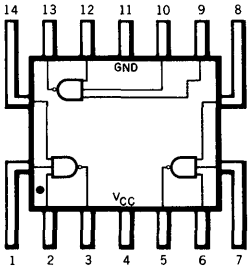

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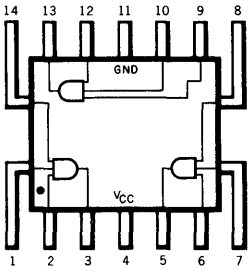

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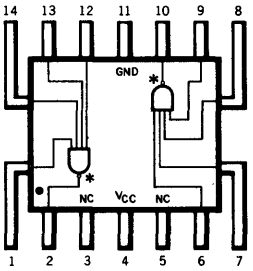

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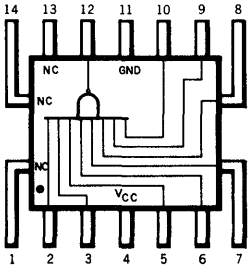

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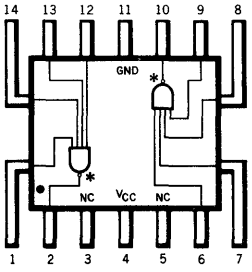

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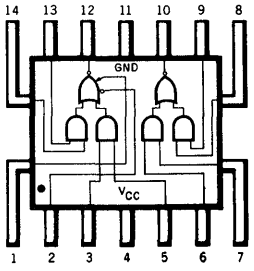
9N50/5450, 7450



TTL/SSI

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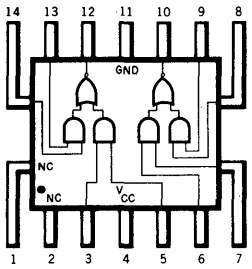

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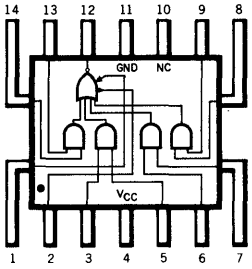

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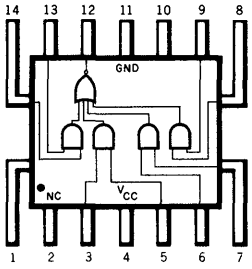

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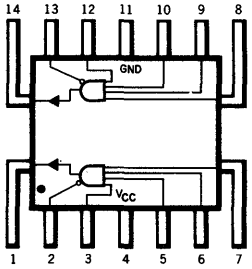

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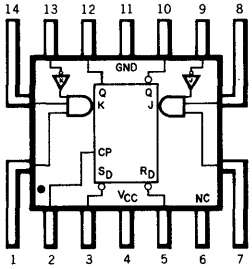

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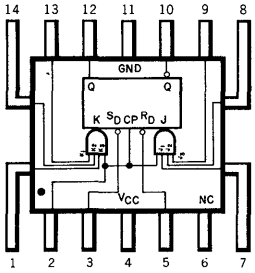

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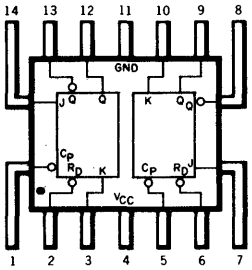

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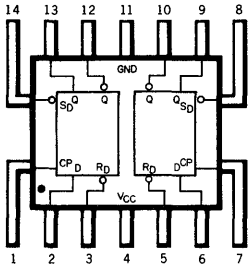

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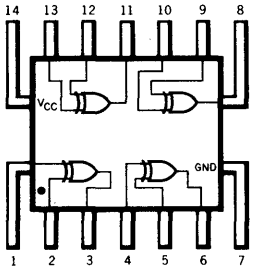
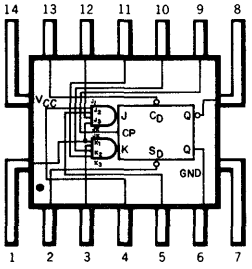


9N104/54104, 74104



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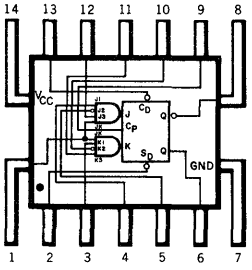

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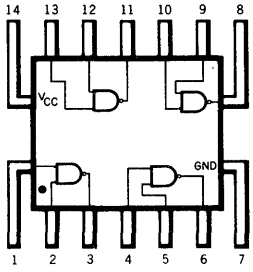
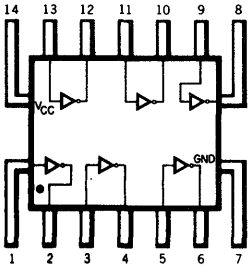


9L04



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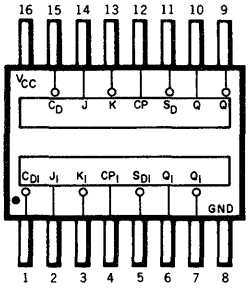
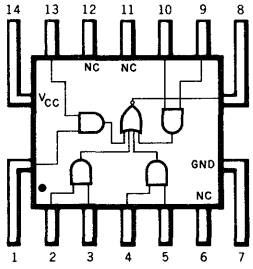
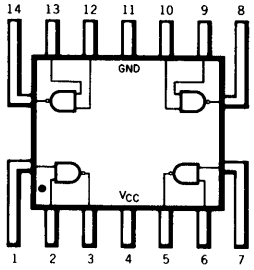


9L54

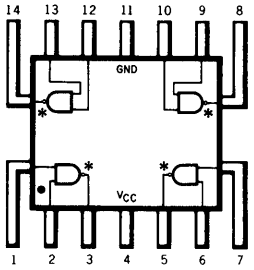


TTL/SSI

9H00/54H00, 74H00



9H01/54H01, 74H01



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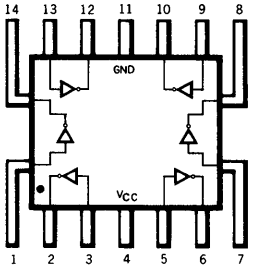
9H04/54H04, 74H04



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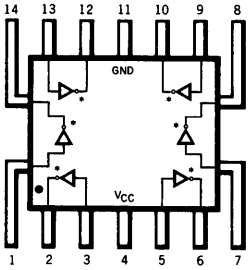

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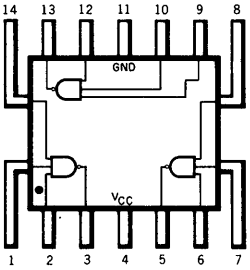
9H10/54H10, 74H10



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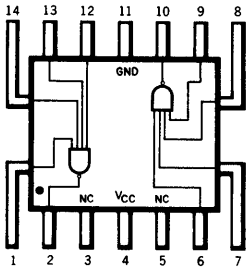
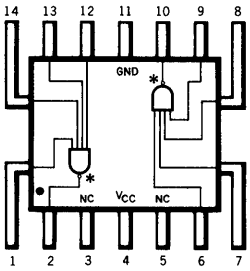


9H22/54H22, 74H22



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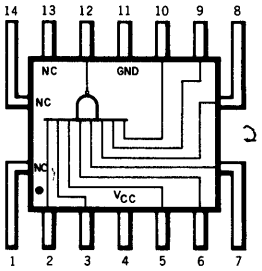
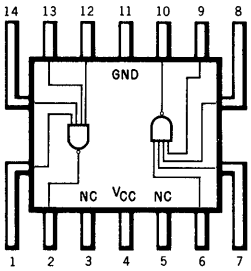


9H40/54H40, 74H40



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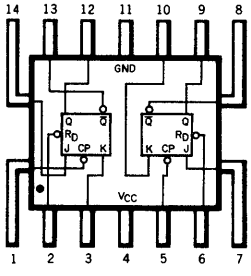
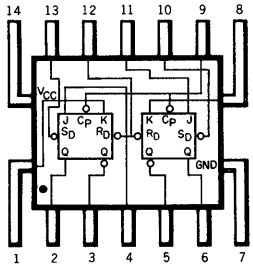
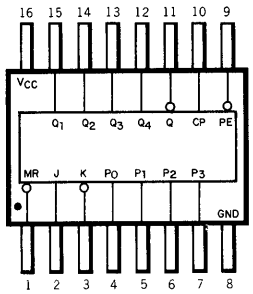


9H78/54H78, 74H78



TTL/MSI

9300



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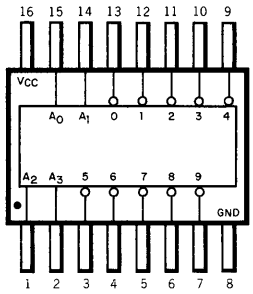

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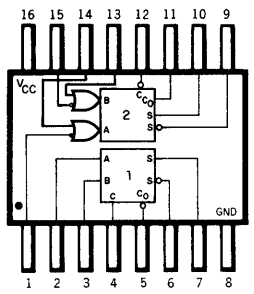

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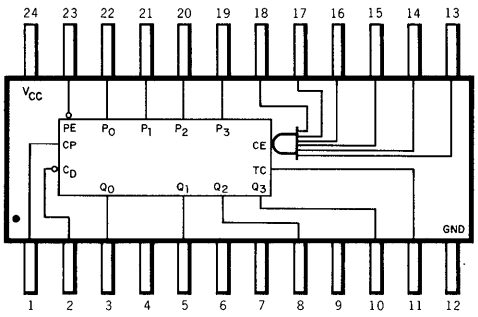

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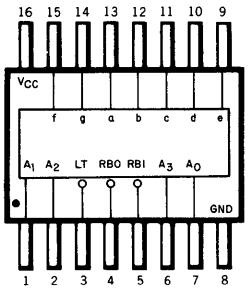

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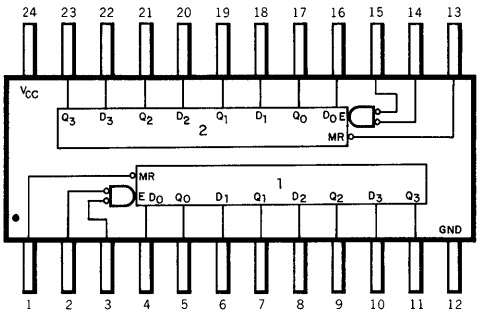

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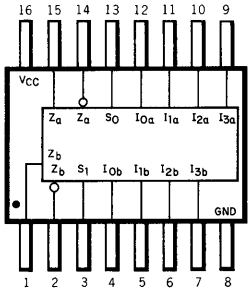

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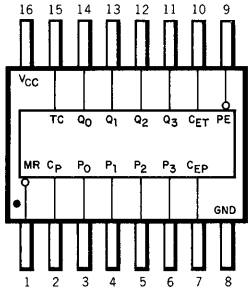

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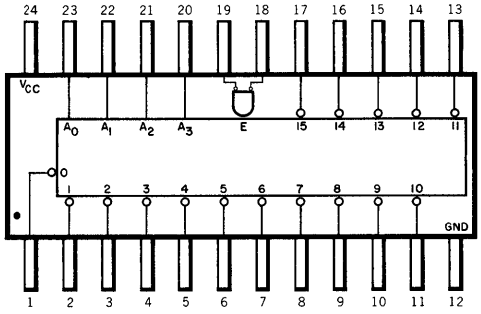

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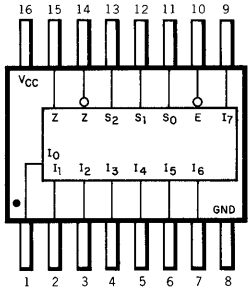

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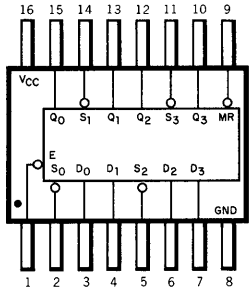

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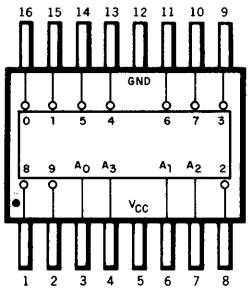

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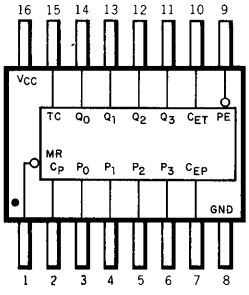

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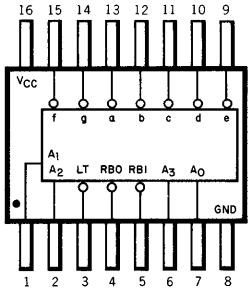

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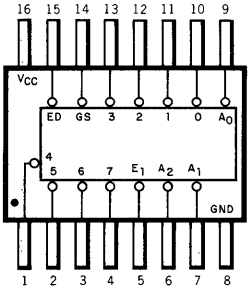

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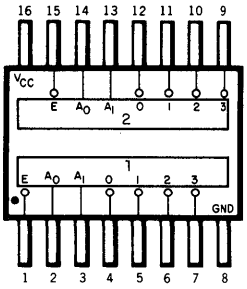

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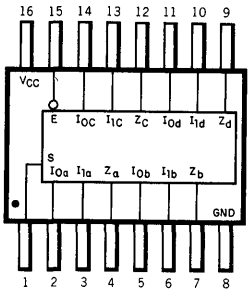

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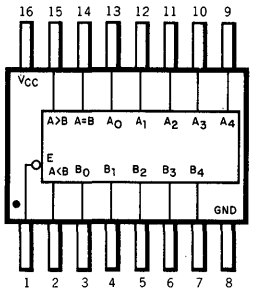

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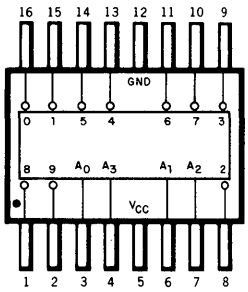

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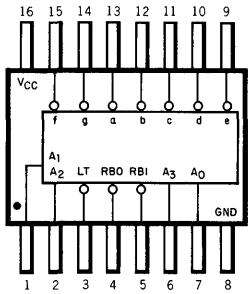

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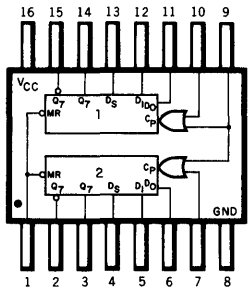

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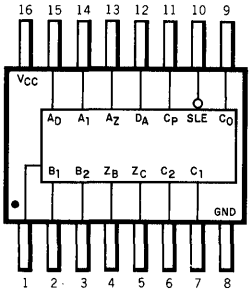

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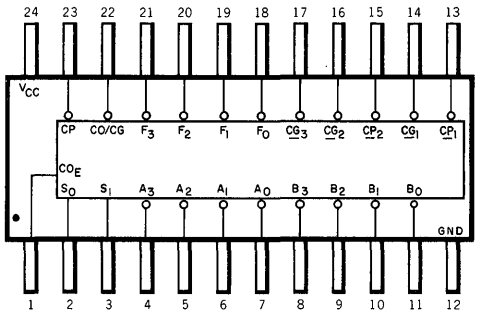

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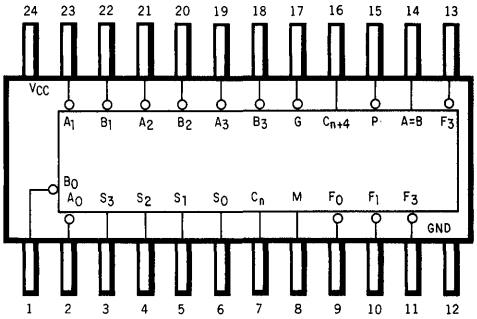

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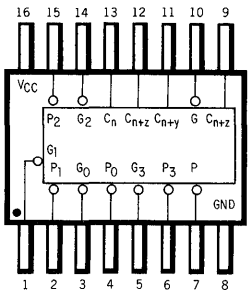

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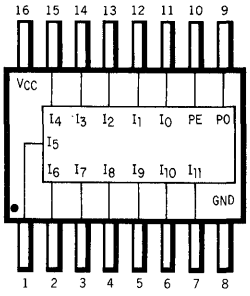

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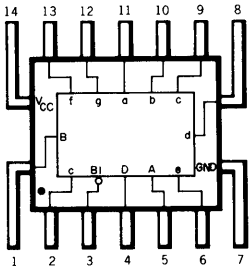

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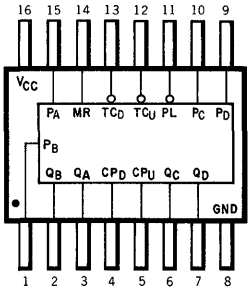

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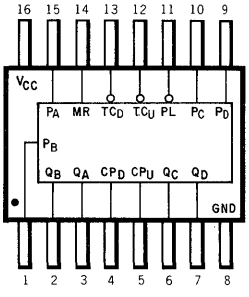

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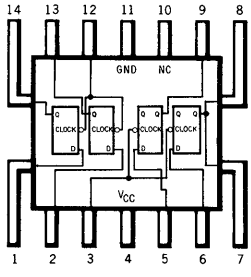

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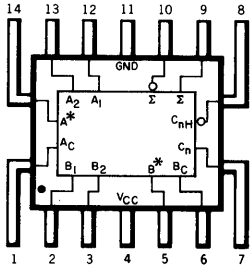
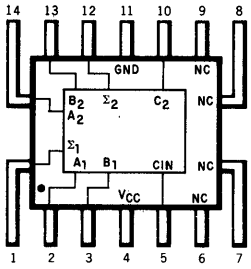


TTL/MSI

9382/5482, 7482



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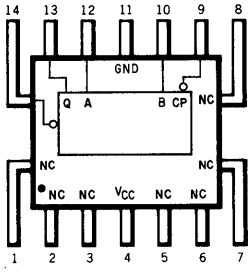

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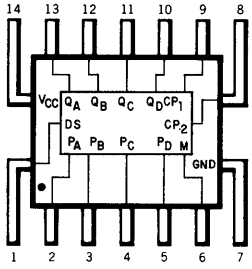

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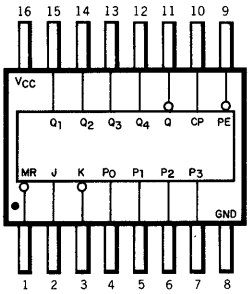

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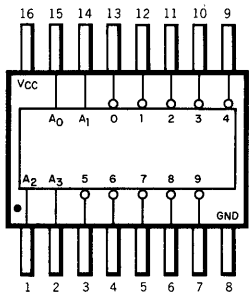

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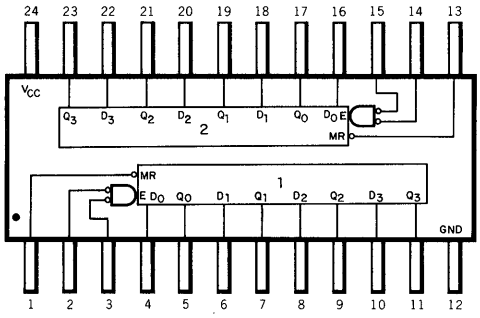

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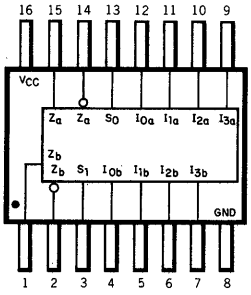

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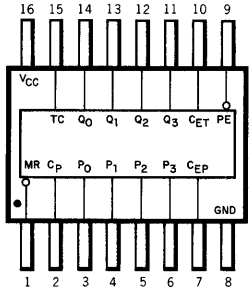

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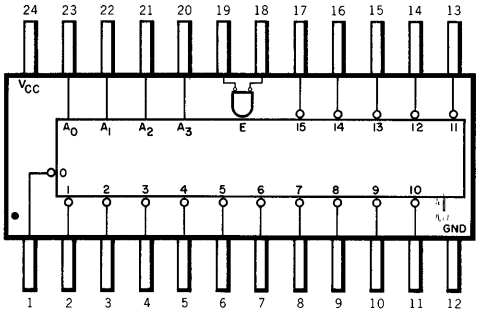

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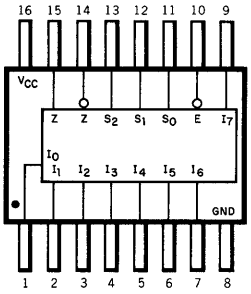

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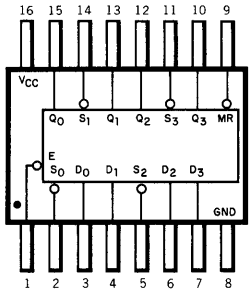

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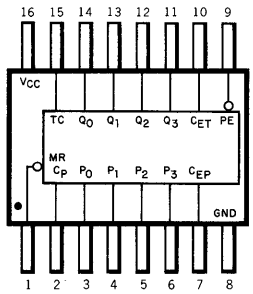

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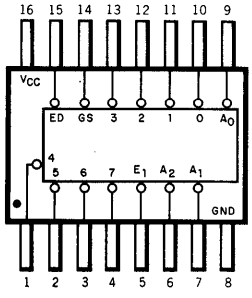

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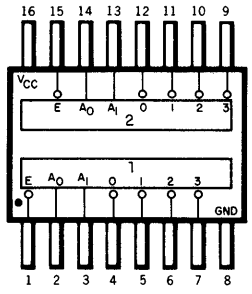

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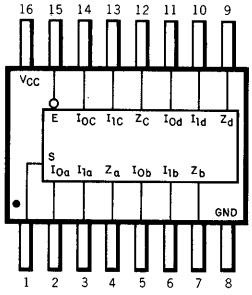

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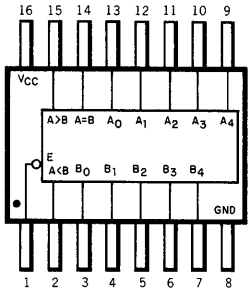
93L24



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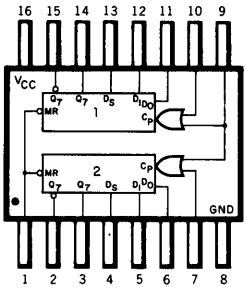

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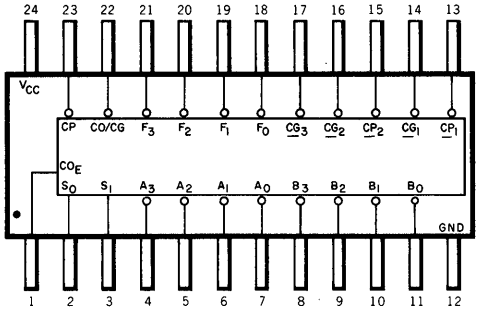

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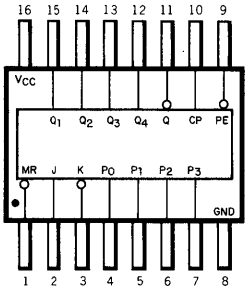


93H70/74196

TO BE ANNOUNCED

93H72

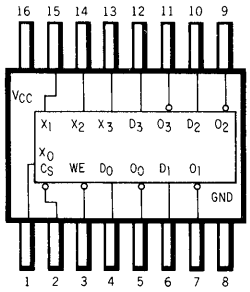
TO BE ANNOUNCED

93H76/74197

TO BE ANNOUNCED

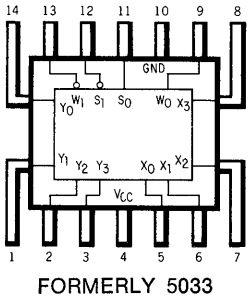
TTL/MEMORY

93403



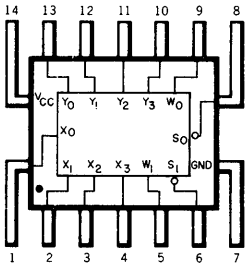
FORMERLY 4103

93407



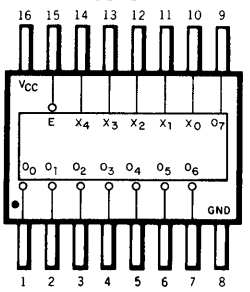
FORMERLY 5033

93433



FORMERLY 9033

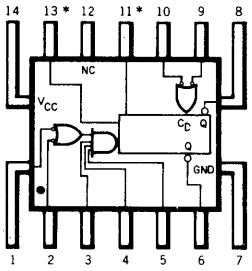
93434



FORMERLY 9034

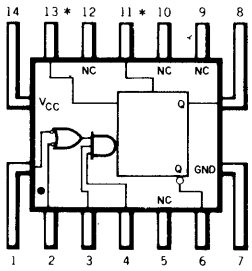
TTL/INTERFACE

9600



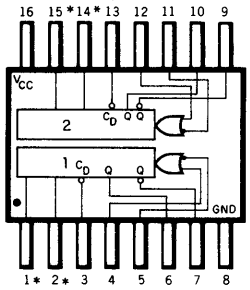
*PINS FOR EXTERNAL TIMING.

9601



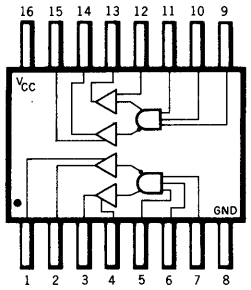
*PINS FOR EXTERNAL TIMING.

9602

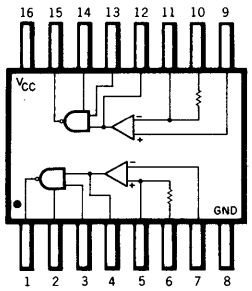


*PINS FOR EXTERNAL TIMING.

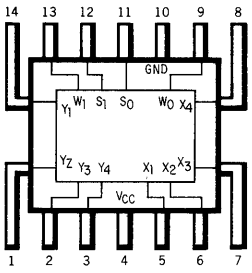
9614



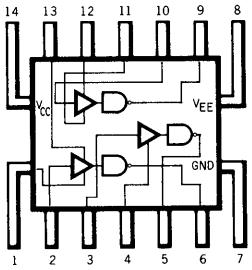
9615



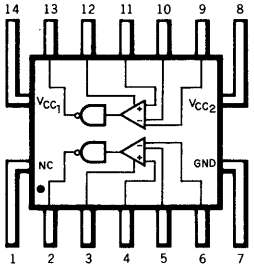
9616



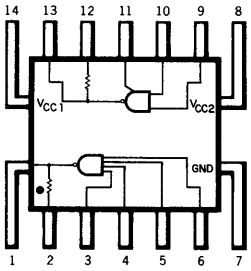
9617



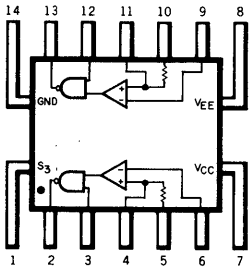
9620



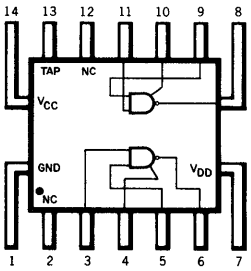
9621



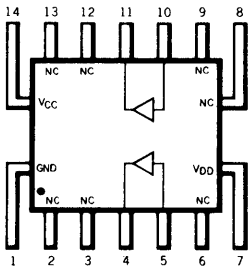
9622

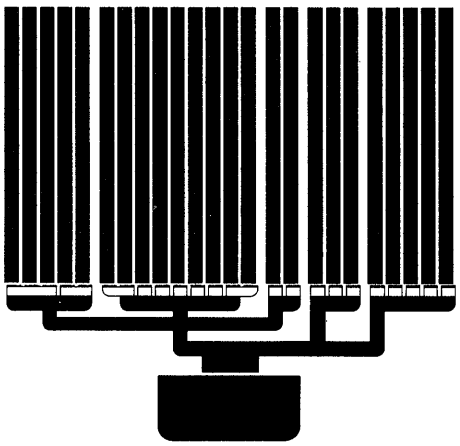


9624



9625





ORDERING INFORMATION

DEVICE	INDUSTRIAL (0° to +70°C)		MILITARY (−55° to +125°C)	
	DUAL IN LINE	FLAT PACK	DUAL IN LINE	FLAT PACK
93400B	A7B9340059B			
93400	A7B9340059X			
93401	A7B9340159X			
93402	A6N9340259X			
93403	A7B9340359X	A4L9340359X	A7B9340351X	A4L9340351X
93407 (40mA F.O.)	A6A93407591	A3I93407591	A6A93407511	A3I93407511
(20mA F.O.)	A6A93407592	A3I93407592	A6A93407512	A3I93407512
93412	A7B9341259X		A7B9341251X	
93433 (40mA F.O.)	A6A93433591	A3I93433591	A6A93433511	A3I93433511
(20mA F.O.)	A6A93433592	A3I93433592	A6A93433512	A3I93433512
93434	A7B9343459X		A7B9343451X	
93435	A6P9343559X		A6P9343551X	
5400 (9N00)			U6A540051X	U3I540051X
5401 (9N01)			U6A540151X	U3I540151X
5402 (9N02)			U6A540251X	U3I540251X
5403 (9N03)			U6A540351X	
5404 (9N04)			U6A540451X	U3I540451X
5405 (9N05)			U6A540551X	U3I540551X
5408 (9N08)			U6A540851X	U3I540851X
5410 (9N10)			U6A541051X	U3I541051X
5411 (9N11)			U6A541151X	U3I541151X
5420 (9N20)			U6A542051X	U3I542051X
5430 (9N30)			U6A543051X	U3I543051X
5440 (9N40)			U6A544051X	U3I544051X
5442 (9352)			U7B544251X	
5443 (9353)			U7B544351X	
5444 (9354)			U7B544451X	
5446 (9357A)			U7B544651X	
5447 (9357B)			U7B544751X	
5448 (9358)			U7B544851X	
5449 (9359)				U3I544951X
5450 (9N50)			U6A545051X	U3I545051X
5451 (9N51)			U6A545151X	U3I545151X
5453 (9N53)			U6A545351X	U3I545351X
5454 (9N54)			U6A545451X	U3I545451X
5460 (9N60)			U6A546051X	U3I546051X
5470 (9N70)			U6A547051X	U3I547051X
5472 (9N72)			U6A547251X	U3I547251X
5473 (9N73)			U6A547351X	U3I547351X
5474 (9N74)			U6A547451X	U3I547451X
5475 (9375)			U6B547551X	
5476 (9N76)			U6B547651X	U4L547651X
5477 (9377)				U3I547751X
5480 (9380)			U6A548051X	U3I548051X
5482 (9382)			U6A548251X	U3I548251X
5483 (9383)			U6B548351X	U4L548351X

ORDERING INFORMATION

DEVICE	INDUSTRIAL (0° to +70°C)		MILITARY (−55° to +125°C)	
	DUAL IN LINE	FLAT PACK	DUAL IN LINE	FLAT PACK
5486 (9N86)			U6A548651X	U3I548651X
5490 (9390)			U6A549051X	U3I549051X
5491 (9391)			U6A549151X	U3I549151X
5492 (9392)			U6A549251X	U3I549251X
5493 (9393)			U6A549351X	U3I549351X
5494 (9394)			U7B549451X	U4L549451X
5495 (9395)			U6A549551X	U3I549551X
5496 (9396)			U7B549651X	U4L549651X
54104 (9N104)			U6A5410451X	U3I5410451X
54105 (9N105)			U6A5410551X	U3I5410551X
54107 (9N107)			U6A5410751X	U3I5410751X
54181 (9341)			U6N5418151X	U4M5418151X
54182 (9342)			U7B5418251X	U4L5418251X
54192 (9360)			U7B5419251X	U4L5419251X
54193 (9366)			U7B5419351X	U4L5419351X
54H00 (9H00)			U6A54H0051X	U3I54H0051X
54H01 (9H01)			U6A54H0151X	U3I54H0151X
54H04 (9H04)			U6A54H0451X	U3I54H0451X
54H05 (9H05)			U6A54H0551X	U3I54H0551X
54H10 (9H10)			U6A54H1051X	U3I54H1051X
54H20 (9H20)			U6A54H2051X	U3I54H2051X
54H30 (9H30)			U6A54H3051X	U3I54H3051X
54H40 (9H40)			U6A54H4051X	U3I54H4051X
54H73 (9H73)			U6A54H7351X	U3I54H7351X
54H76 (9H76)			U6A54H7651X	U3I54H7651X
54H78 (9H78)			U6A54H7851X	U3I54H7851X
7400 (9N00)	U6A740059X	U3I740059X		
7401 (9N01)	U6A740159X	U3I740159X		
7402 (9N02)	U6A740259X	U3I740259X		
7403 (9N03)	U6A740359X	U3I740359X		
7404 (9N04)	U6A740459X	U3I740459X		
7405 (9N05)	U6A740559X	U3I740559X		
7408 (9N08)	U6A740859X	U3I740859X		
7410 (9N10)	U6A741059X	U3I741059X		
7411 (9N11)	U6A741159X	U3I741159X		
7420 (9N20)	U6A742059X	U3I742059X		
7430 (9N30)	U6A743059X	U3I743059X		
7440 (9N40)	U6A744059X	U3I744059X		
7441 (9315)	U6B744159X			
7442 (9352)	U7B744259X			
7443 (9353)	U7B744359X			
7444 (9354)	U7B744459X			
7446 (9357A)	U7B744659X			
7447 (9357B)	U7B744759X			
7448 (9358)	U7B744859X			
7449 (9359)		U3I744959X		
7450 (9N50)	U6A745059X	U3I745059X		
7451 (9N51)	U6A745159X	U3I745159X		
7453 (9N53)	U6A745359X	U3I745359X		
7454 (9N54)	U6A745459X	U3I745459X		
7460 (9N60)	U6A746059X	U3I746059X		
7470 (9N70)	U6A747059X	U3I747059X		
7472 (9N72)	U6A747259X	U3I747259X		
7473 (9N73)	U6A747359X	U3I747359X		
7474 (9N74)	U6A747459X	U3I747459X		
7475 (9375)	U6B747559X	U3I747559X		
7476 (9N76)	U6B747659X			
7477 (9377)		U3I747759X		
7480 (9380)	U6A748059X	U3I748059X		
7482 (9382)	U6A748259X	U3I748259X		
7483 (9383)	U6B748359X			
7486 (9N86)	U6A748659X	U3I748659X		

ORDERING INFORMATION

DEVICE	INDUSTRIAL (0° to +70°C)		MILITARY (−55° to +125°C)	
	DUAL IN LINE	FLAT PACK	DUAL IN LINE	FLAT PACK
7490 (9390)	U6A749059X	U3I749059X		
7491 (9391)	U6A749159X	U3I749159X		
7492 (9392)	U6A749259X	U3I749259X		
7493 (9393)	U6A749359X	U3I749359X		
7494 (9394)	U7B749459X			
7495 (9395)	U6A749559X	U3I749559X		
7496 (9396)	U7B749659X			
74104 (9N104)	U6A7410459X	U3I7410459X		
74105 (9N105)	U6A7410559X	U3I7410559X		
74107 (9N107)	U6A7410759X			
74141 (9325)	U6B7414159X			
74181 (9341)	U6N7418159X	U4M7418159X		
74182 (9342)	U7B7418259X	U4L7418259X		
74192 (9360)	U7B7419259X	U4L7419259X		
74193 (9366)	U7B7419359X	U4L7419359X		
74H00 (9H00)	U6A74H0059X	U3I74H0059X		
74H01 (9H01)	U6A74H0159X	U3I74H0159X		
74H04 (9H04)	U6A74H0459X	U3I74H0459X		
74H05 (9H05)	U6A74H0559X	U3I74H0559X		
74H10 (9H10)	U6A74H1059X	U3I74H1059X		
74H20 (9H20)	U6A74H2059X	U3I74H2059X		
74H30 (9H30)	U6A74H3059X	U3I74H3059X		
74H40 (9H40)	U6A74H4059X	U3I74H4059X		
74H73 (9H73)	U6A74H7359X	U3I74H7359X		
74H76 (9H76)	U6A74H7659X	U3I74H7659X		
74H78 (9H78)	U6A74H7859X	U3I74H7859X		
7524 (9664)	U7B7524392			
7525 (9665)	U7B7524393			
9000	U6A900059X	U3I900059X	U6A900051X	U3I900051X
9001	U6A900159X	U3I900159X	U6A900151X	U3I900151X
9002	U6A900259X	U3I900259X	U6A900251X	U3I900251X
9003	U6A900359X	U3I900359X	U6A900351X	U3I900351X
9004	U6A900459X	U3I900459X	U6A900451X	U3I900451X
9005	U6A900559X	U3I900559X	U6A900551X	U3I900551X
9006	U6A900659X	U3I900659X	U6A900651X	U3I900651X
9007	U6A900759X	U3I900759X	U6A900751X	U3I900751X
9008	U6A900859X	U3I900859X	U6A900851X	U3I900851X
9009	U6A900959X	U3I900959X	U6A900951X	U3I900951X
9012	U6A901259X	U3I901259X	U6A901251X	U3I901251X
9014	U6B901459X	U4L901459X	U6B901451X	U4L901451X
9015	U6B901559X	U4L901559X	U6B901551X	U4L901551X
9016	U6A901659X	U3I901659X	U6A901651X	U3I901651X
9017	U6A901759X	U3I901759X	U6A901751X	U3I901751X
9020	U7B902059X	U4L902059X	U7B902051X	U4L902051X
9022	U7B902259X	U4L902259X	U7B902251X	U4L902251X
9024	U7B902459X	U4L902459X	U7B902451X	U4L902451X
9H00/54H00, 74H00	U6A9H0059X	U3I9H0059X	U6A9H0051X	U3I9H0051X
9H01/54H01, 74H01	U6A9H0159X	U3I9H0159X	U6A9H0151X	U3I9H0151X
9H04/54H04, 74H04	U6A9H0459X	U3I9H0459X	U6A9H0451X	U3I9H0451X
9H05/54H05, 74H05	U6A9H0559X	U3I9H0559X	U6A9H0551X	U3I9H0551X
9H10/54H10, 74H10	U6A9H1059X	U3I9H1059X	U6A9H1051X	U3I9H1051X
9H20/54H20, 74H20	U6A9H2059X	U3I9H2059X	U6A9H2051X	U3I9H2051X
9H30/54H30, 74H30	U6A9H3059X	U3I9H3059X	U6A9H3051X	U3I9H3051X
9H40/54H40, 74H40	U6A9H4059X	U3I9H4059X	U6A9H4051X	U3I9H4051X
9H73/54H73, 74H73	U6A9H7359X	U3I9H7359X	U6A9H7351X	U3I9H7351X
9H76/54H76, 74H76	U6A9H7659X	U3I9H7659X	U6A9H7651X	U3I9H7651X
9H78/54H78, 74H78	U6A9H7859X	U3I9H7859X	U6A9H7851X	U3I9H7851X

ORDERING INFORMATION

DEVICE	INDUSTRIAL (0° to +70°C)		MILITARY (−55° to +125°C)	
	DUAL IN LINE	FLAT PACK	DUAL IN LINE	FLAT PACK
9L00	U6A9L0059X	U3I9L0059X	U6A9L0051X	U3I9L0051X
9L04	U6A9L0459X	U3I9L0459X	U6A9L0451X	U3I9L0451X
9L24	U7B9L2459X	U4L9L2459X	U7B9L2451X	U4L9L2451X
9L54	U6A9L5459X	U3I9L5459X	U6A9L5451X	U3I9L5451X
9N00/5400, 7400	U6A9N0059X	U3I9N0059X	U6A9N0051X	U3I9N0051X
9N01/5401, 7401	U6A9N0159X	U3I9N0159X	U6A9N0151X	U3I9N0151X
9N02/5402, 7402	U6A9N0259X	U3I9N0259X	U6A9N0251X	U3I9N0251X
9N03/5403, 7403	U6A9N0359X		U6A9N0351X	
9N04/5404, 7404	U6A9N0459X	U3I9N0459X	U6A9N0451X	U3I9N0451X
9N05/5405, 7405	U6A9N0559X	U3I9N0559X	U6A9N0551X	U3I9N0551X
9N08/5408, 7408	U6A9N0859X	U3I9N0859X	U6A9N0851X	U3I9N0851X
9N10/5410, 7410	U6A9N1059X	U3I9N1059X	U6A9N1051X	U3I9N1051X
9N11/5411, 7411	U6A9N1159X	U3I9N1159X	U6A9N1151X	U3I9N1151X
9N20/5420, 7420	U6A9N2059X	U3I9N2059X	U6A9N2051X	U3I9N2051X
9N30/5430, 7430	U6A9N3059X	U3I9N3059X	U6A9N3051X	U3I9N3051X
9N40/5440, 7440	U6A9N4059X	U3I9N4059X	U6A9N4051X	U3I9N4051X
9N50/5450, 7450	U6A9N5059X	U3I9N5059X	U6A9N5051X	U3I9N5051X
9N51/5451, 7451	U6A9N5159X	U3I9N5159X	U6A9N5151X	U3I9N5151X
9N53/5453, 7453	U6A9N5359X	U3I9N5359X	U6A9N5351X	U3I9N5351X
9N54/5454, 7454	U6A9N5459X	U3I9N5459X	U6A9N5451X	U3I9N5451X
9N60/5460, 7460	U6A9N6059X	U3I9N6059X	U6A9N6051X	U3I9N6051X
9N70/5470, 7470	U6A9N7059X	U3I9N7059X	U6A9N7051X	U3I9N7051X
9N72/5472, 7472	U6A9N7259X	U3I9N7259X	U6A9N7251X	U3I9N7251X
9N73/5473, 7473	U6A9N7359X	U3I9N7359X	U6A9N7351X	U3I9N7351X
9N74/5474, 7474	U6A9N7459X	U3I9N7459X	U6A9N7451X	U3I9N7451X
9N76/5476, 7476	U6A9N7659X	U3I9N7659X	U6A9N7651X	U3I9N7651X
9N86/5486, 7486	U6A9N8659X	U3I9N8659X	U6A9N8651X	U3I9N8651X
9N104/54104, 74104	U6A9N10459X	U3I9N10459X	U6A9N10451X	U3I9N10451X
9N105/54105, 74105	U6A9N10559X	U3I9N10559X	U6A9N10551X	U3I9N10551X
9N107/54107, 74107	U6A9N10759X		U6A9N10751X	
9300	U7B930059X	U4L930059X	U7B930051X	U4L930051X
9301	U7B930159X	U4L930159X	U7B930151X	U4L930151X
9304	U6B930459X	U4L930459X	U6B930451X	U4L930451X
9305	U7A930559X	U3B930559X	U7A930551X	U3B930551X
9306	U6N930659X	U4M930659X	U6N930651X	U4M930651X
9307	U6B930759X	U4L930759X	U6B930751X	U4L930751X
9308	U6N930859X	U4M930859X	U6N930851X	U4M930851X
9309	U6B930959X	U4L930959X	U6B930951X	U4L930951X
9310	U7B931059X	U4L931059X	U7B931051X	U4L931051X
9311	U6N931159X	U4M931159X	U6N931151X	U4M931151X
9312	U7B931259X	U4L931259X	U7B931251X	U4L931251X
9313	U7B931359X	U4L931359X	U7B931351X	U4L931351X
9314	U7B931459X	U4L931459X	U7B931451X	U4L931451X
9315/7441	U6B931559X	U4L931559X	U6B931551X	U4L931551X
9316	U7B931659X	U4L931659X	U7B931651X	U4L931651X
9317A	U7B9317591	U4L9317591	U7B9317511	U4L9317511
9317B	U7B9317592	U4L9317592	U7B9317512	U4L9317512
9317C	U7B9317593	U4L9317593	U7B9317513	U4L9317513
9317D	U7B9317594	U4L9317594	U7B9317514	U4L9317514
9318	U7B931859X	U4L931859X	U7B931851X	U4L931851X
9321	U7B932159X	U4L932159X	U7B932151X	U4L932151X
9322	U7B932259X	U4L932259X	U7B832251X	U4L932251X
9324	U7B932459X	U4L932459X	U7B932451X	U4L932451X
9325/54141, 74141	U6B932559X	U4L932559X	U6B932551X	U4L932551X
9327A	U7B9327591	U4L9327591	U7B9327511	U4L9327511
9327B	U7B9327592	U4L9327592	U7B9327512	U4L9327512
9328	U7B932859X	U4L932859X	U7B932851X	U4L932851X
9334	U7B933459X	U4L933459X	U7B933451X	U4L933451X
9337	U7B933759X			
9338	U7B933859X	U4L933859X	U7B933851X	U4L933851X

ORDERING INFORMATION

DEVICE	INDUSTRIAL (0° to +70°C)		MILITARY (−55° to +125°C)	
	DUAL IN LINE	FLAT PACK	DUAL IN LINE	FLAT PACK
9340	U6N934059X	U4M934059X	U6N934051X	U4M934051X
9341/54181, 74181	U6N934159X	U4M934159X	U6N934151X	U4M934151X
9342/54182, 74182	U7B934259X	U4L934259X	U7B934251X	U4L934251X
9348	U6B934859X	U4L934859X	U6B934851X	U4L934851X
9350	U7A935059X	U3B935059X	U7A935051X	U3B935051X
9352/5442, 7442	U7B935259X			
9353/5443, 7443	U7B935359X			
9354/5444, 7444	U7B935459X			
9356	U7A935659X	U3B935659X	U7A935651X	U3B935651X
9357A/5446, 7446	U7B9357591			
9357B/5447, 7447	U7B9357592			
9358/5448, 7448	U6B935859X		U6B935851X	
9359/5449, 7449		U3B935959X		U3B935951X
9360/54192, 74192	U7B936059X	U4L936059X	U7B936051X	U4L936051X
9366/54193, 74193	U7B936659X	U4L936659X	U7B936651X	U4L936651X
9375/5475, 7475	U6B937559X		U6B937551X	
9377/5477, 7477		U3I937759X		U3I937751X
9380/5480, 7480	U6A938059X	U3I938059X	U6A938051X	U3I938051X
9382/5482, 7482	U6A938259X	U3I938259X	U6A938251X	U3I938251X
9383/5483, 7483	U6B938359X	U4L938359X	U6B938351X	U4L938351X
9390/5490, 7490	U6A939059X	U3B939059X	U6A939051X	U3B939051X
9391/5491, 7491	U6A939159X	U3I939159X	U6A939151X	U3I939151X
9392/5492, 7492	U6A939259X	U3B939259X	U6A939251X	U3B939251X
9393/5493, 7493	U6A939459X	U3B939359X	U6A939351X	U3B939351X
9394/5494, 7494	U7B939459X		U7B939451X	
9395/5495, 7495	U6A939559X	U3I939559X	U6A939551X	U3I939551X
9396/5496, 7496	U7B939659X		U7B939651X	
93H00 *	U7B93H0059X	U4L93H0059X	U7B93H0051X	U4L93H0051X
93H70/74196 *	U6A93H7059X	U3I93H7059X	U6A93H7051X	U3I93H7051X
93H72 *	U7B93H7259X	U4L93H7259X	U7B93H7251X	U4L93H7251X
93H76/74197 *	U6A93H7659X	U3I93H7659X	U6A93H7651X	U3I93H7651X
93L00	U7B93L0059X	U4L93L0059X	U7B93L0051X	U4L93L0051X
93L01	U7B93L0159X	U4L93L0159X	U7B93L0151X	U4L93L0151X
93L08	U6N93L0859X	U4M93L0859X	U6N93L0851X	U4M93L0851X
93L09	U6B93L0959X	U4L93L0959X	U6B93L0951X	U4L93L0951X
93L10	U7B93L1059X	U4L93L1059X	U7B93L1051X	U4L93L1051X
93L11	U6N93L1159X	U4M93L1159X	U6N93L1151X	U4L93L1151X
93L12	U7B93L1259X	U4L93L1259X	U7B93L1251X	U4L93L1251X
93L14	U7B93L1459X	U4L93L1459X	U7B93L1451X	U4L93L1451X
93L16	U7B93L1659X	U4L93L1659X	U7B93L1651X	U4L93L1651X
93L18	U7B93L1859X	U4L93L1859X	U7B93L1851X	U4L93L1851X
93L21	U7B93L2159X	U4L93L2159X	U7B93L2151X	U4L93L2151X
93L22	U7B93L2259X	U4L93L2259X	U7B93L2251X	U4L93L2251X
93L24	U7B93L2459X	U4L93L2459X	U7B93L2451X	U4L93L2451X
93L28	U7B93L2859X	U4L93L2859X	U7B93L2851X	U4L93L2851X
93L40	U6N93L4059X	U4M93L4059X	U6N93L4051X	U4M93L4051X
9600	U6A960059X	U3I960059X	U6A960051X	U3I960051X
9601	U6A960159X	U3I960159X	U6A960151X	U3I960151X
9602	U7B960259X	U4L960259X	U7B960251X	U4L960251X
9614	U7B961459X	U4L961459X	U7B961451X	U4L961451X
9615	U7B961559X	U4L961559X	U7B961551X	U4L961551X
9616 *	U6A961659X		U6A961651X	
9617 *	U6A961759X		U6A961751X	
9620	U6A962059X	U3I962059X	U6A962051X	U3I962051X
9621	U6A962159X	U3I962159X	U6A962151X	U3I962151X
9622	U6A962259X	U3I962259X	U6A962251X	U3I9962251X
9624	U6A962459X	U3I962459X	U6A962451X	U3I962451X
9625	U6A962559X	U3I962559X	U6A962551X	U3I962551X
9644	U7B964459X		U7B964451X	
9664/7524	U7B9664592			
9665/7525	U7B9665593			

* TO BE ANNOUNCED

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Printed in U.S.A./01-10-0253-031/50M