

FEATURES

- Pin-to-Pin Compatible with National DS34C86
- Low Power CMOS Design
- Three-State Outputs with Enable Pin
- Meets the EIA RS-422 Requirements
- Low Propagation Delays
- High Speed

GENERAL DESCRIPTION

The ST34C86 is a CMOS quad differential line receiver designed to meet the standard RS-422, RS-423 requirements. The ST34C86 has an input sensitivity of 200mv over the common mode input voltage range of 7V. To improve noise margin and output stability for slow changing input signal, special hysteresis is built in the ST34C86 circuit. The ST34C86 is a high speed line

receiver designed to operate with MFM / RLL controllers and hard disk drives as well as RS-422 and RS-423 differential applications. ST34C86 provides TTL compatible outputs to interface with standard 74LS and CMOS design environments. ST34C86 is suitable for low power 5V operation.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
ST34C86CP16	16 Lead 300 Mil PDIP	0°C to +70°C
ST34C86CF16	16 Lead 150 Mil JEDEC SOIC	0°C to +70°C
ST34C86IP16	16 Lead 300 Mil PDIP	-40°C to +85°C
ST34C86IF16	16 Lead 150 Mil JEDEC SOIC	-40°C to +85°C

BLOCK DIAGRAM

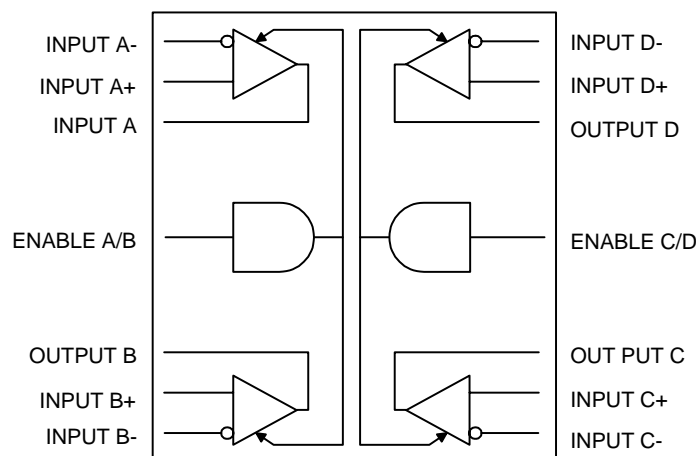
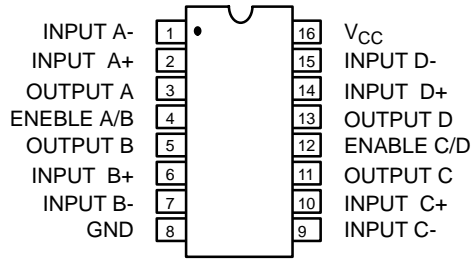
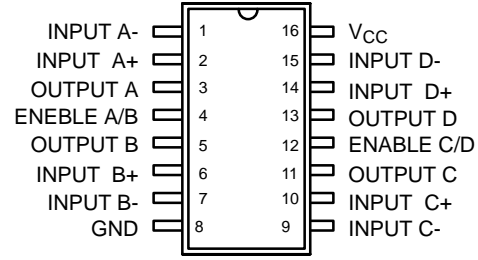


Figure 1. Block Diagram

PIN CONFIGURATION



16 Lead PDIP (0.300")



16 Lead SOIC (Jedec, 0.150")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	INPUT A-	I	Receiver A differential inverting input pin.
2	INPUT A+	I	Receiver A differential non-inverting input pin.
3	OUTPUT A	O	Receiver A output pin.
4	ENABLE A/B	I	Gate control (active high). This pin enables/disables the two line receiver outputs (out A and out B).
5	OUTPUT B	O	Receiver B output pin.
6	INPUT B+	I	Receiver B differential non-inverting input pin.
7	INPUT B-	I	Receiver B differential inverting input pin.
8	GND	O	Signal and power ground.
9	INPUT C-	I	Receiver C differential inverting input pin.
10	INPUT C+	I	Receiver C differential non-inverting input pin.
11	OUTPUT C	O	Receiver C output pin.
12	ENABLE C/D	I	Gate control (active high). This pin enables/disables the two line receiver outputs (output C and output D).
13	OUTPUT D	O	Receiver D output pin.
14	INPUT D+	I	Receiver D differential non-inverting input pin.
15	INPUT D-	I	Receiver D differential inverting input pin.
16	V _{CC}	I	Power supply pin.

AC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40^{\circ}\text{C} - +85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_1	Propagation Delay, Input to Output		8	10	ns	$S1=V_{CC}$
T_2	Propagation Delay, Input to Output		18	20	ns	$S1=GND$
T_3	Output Enable Time		18	20	ns	$V_{DIF}=2.5\text{V}$
T_4	Output Disable Time		18	20	ns	$V_{DIF}=2.5\text{V}$

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = -40^{\circ}\text{C} - +85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Enable High Level	2.0			V	
V_{IL}	Enable Low Level			0.8	V	
V_{OH}	Output High Level	3.8	4.2		V	$I_{OH} = -6\text{mA}$
V_{OL}	Output Low Level			0.4	V	$-7\text{V} < V_{CM} < +7\text{V}$
V_{ID}	Differential Input Level	-0.2		0.2	V	$I_{OH} = 6\text{mA}$
V_H	Input Hysteresis		50		mV	
I_{IN}	Input Current			± 1.0	μA	
I_{CC}	Operating Current		12		mA	$V_{DIF} = +1\text{V}$
I_{OZ}	Three-State Output Leakage		± 1.0	± 5.0	μA	$V_{OUT} = V_{CC}$ or GND
I_{EN}	Enable Input Current		± 1.0		μA	$V_{IN} = V_{CC}$ or GND
V_R	Input Resistance	5		15	$\text{K}\Omega$	$-7\text{V} < V_{CM} < +7\text{V}$

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Supply Range 7V
 Voltage at Any Pin $GND - 0.3\text{V}$ to $V_{CC} + 0.3\text{V}$
 Operating Temperature -40°C to $+85^{\circ}\text{C}$

Storage Temperature -60°C to $+160^{\circ}\text{C}$
 Package Dissipation 500mW

Enable A/B C/D	Output	Differential Non-Inverting Output	Differential Inverting Output
L	Z	X	X
H	L	L	H
H	H	H	L

Notes

X = Don't care

Z = Three-State (high impedance)

Table 1. Functional Table

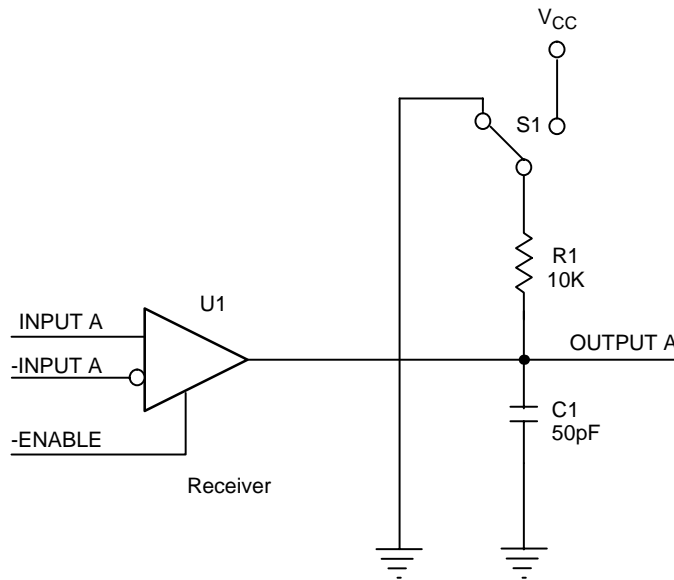


Figure 2. Test Condition

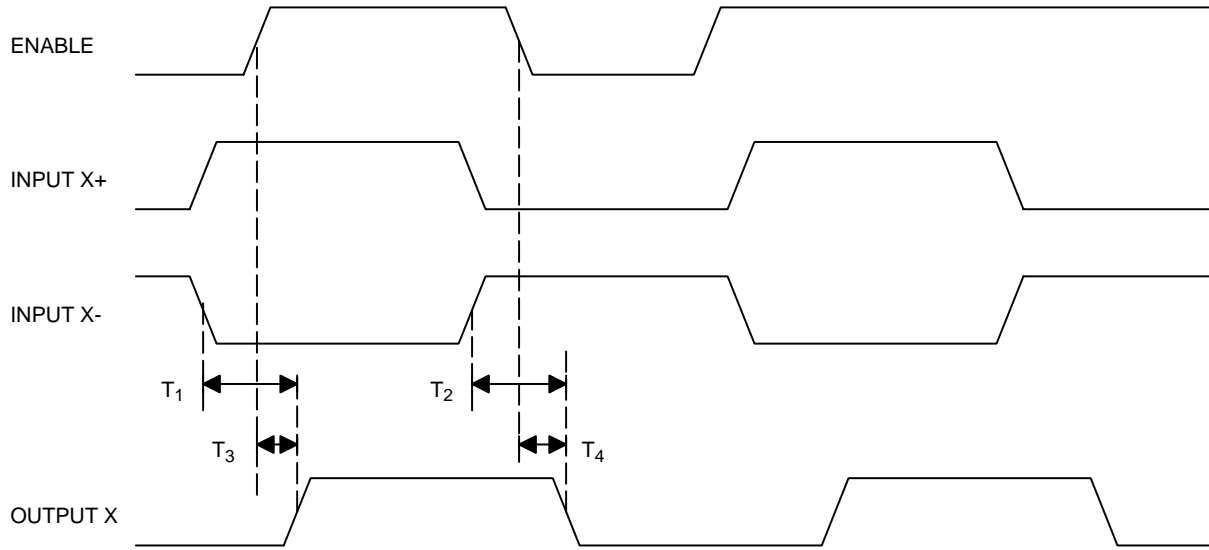
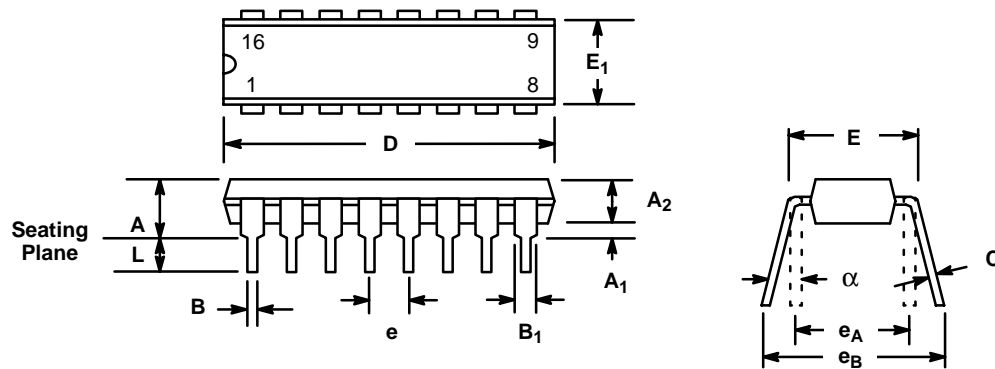


Figure 3. Differential Line Receiver Timing

16 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

Rev. 1.00

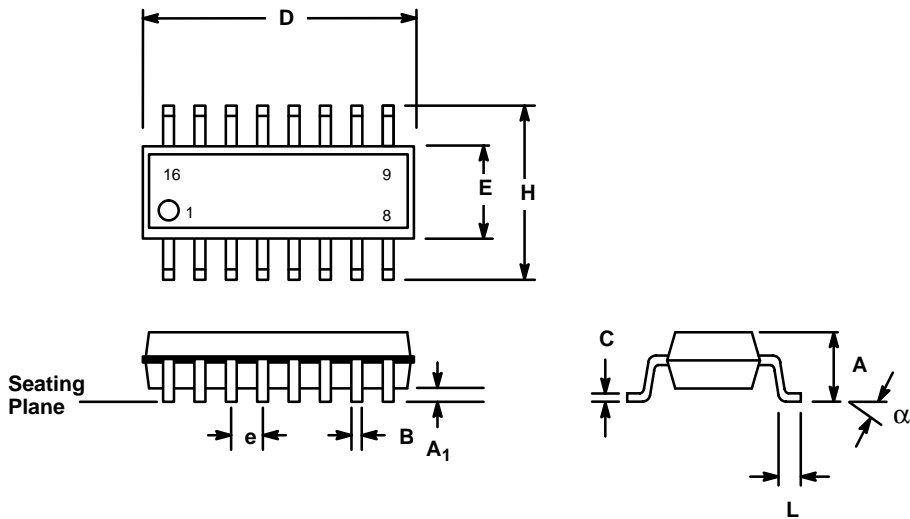


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A ₁	0.015	0.070	0.38	1.78
A ₂	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B ₁	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.745	0.840	18.92	21.34
E	0.300	0.325	7.62	8.26
E ₁	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e _A	0.300 BSC		7.62 BSC	
e _B	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
α	0°	15°	0°	15°

Note: The control dimension is the inch column

**16 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)**

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A ₁	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

Note: The control dimension is the millimeter column

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