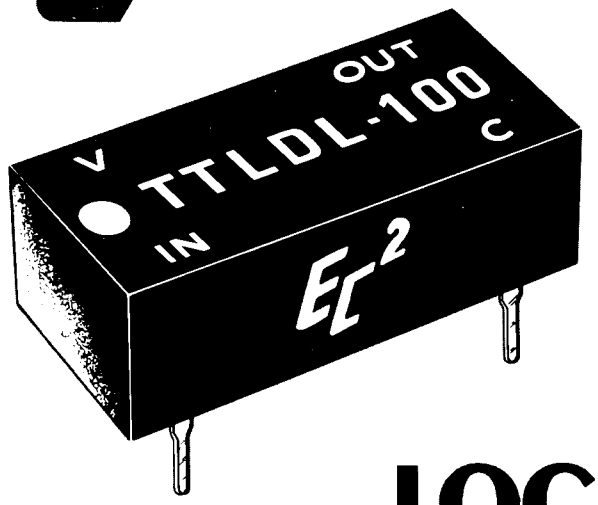
EC²



low profile

T²L COMPATIBLE

LOGIC DELAY LINE

- T²L input and output
- Delay stable and precise
- 14-pin DIP package (.250 high)
- Available in delays from 5 to 1000ns
- Output isolated and with 10 T²L fan-out capacity
- Rise time 4ns maximum

design notes

The "DIP Series" Logic Delay Lines developed by Engineered Components Company have been designed to provide precise delays with required driving and pick-off circuitry contained in a single 14-pin DIP package compatible with Schottky T²L and DTL circuits. These logic delay lines are of hybrid construction utilizing the proven technologies of active integrated circuitry and of passive networks utilizing capacitive, inductive and resistive elements. The ICs utilized in these modules are burned-in to Level B of MIL-STD-883 to ensure a high MTBF. The MTBF on these modules, when calculated per MIL-HDBK-217 for a 50°C ground fixed environment, is in excess of 3 million hours. Module design includes compensation for propagation delays and incorporates internal termination at the output; no additional external components are needed to obtain the desired delay.

The TTLDL is offered in 53 delays from 5ns to 1000ns. Delay tolerances are maintained as shown in the accompanying part number table, when tested under the "Test Conditions" shown. Delay time is measured at the +1.5V level on the leading edge. Rise time for all modules is 4ns maximum when measured from 0.75V to 2.4V. Temperature coefficient of delay is approximately +1200ppm/°C over the operating temperature range of 0 to +70°C.

These modules accept either logic "1" or logic "0" inputs and reproduce the logic at the output without inversion. The delay modules are intended primarily for use with positive going pulses and are calibrated to the tolerances shown in the table on rising edge delay; where best accuracy is desired in applications using falling edge timing, it is recommended that a special unit be calibrated for the specific application. Each module has the capability of driving up to 10 T²L loads.

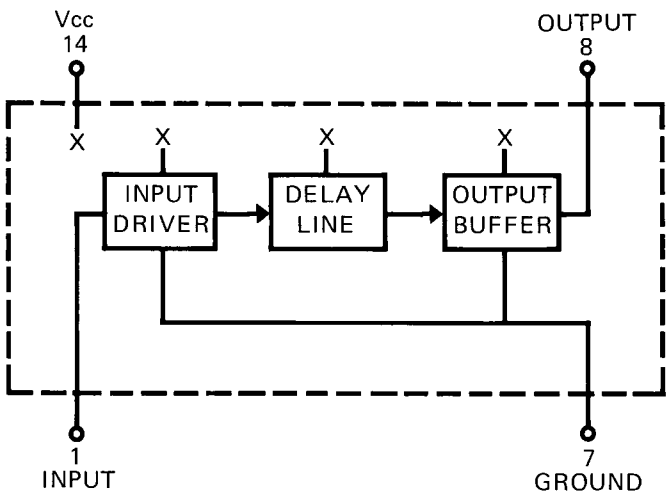
These "DIP Series" modules are packaged in a 14-pin DIP housing, molded of flame-proof Diallyl Phthalate per MIL-M-14, Type SDG-F, and are fully encapsulated in epoxy resin. Flat metal leads meet the solderability requirements of MIL-STD-202, Method 208. Leads provide positive standoff from the printed circuit board to permit solder-fillet formation and flush cleaning of solder-flux residues for improved reliability.

EC² **engineered components company**
3580 Sacramento Drive, P. O. Box Y, San Luis Obispo, CA 93406
Phone (805) 544-3800

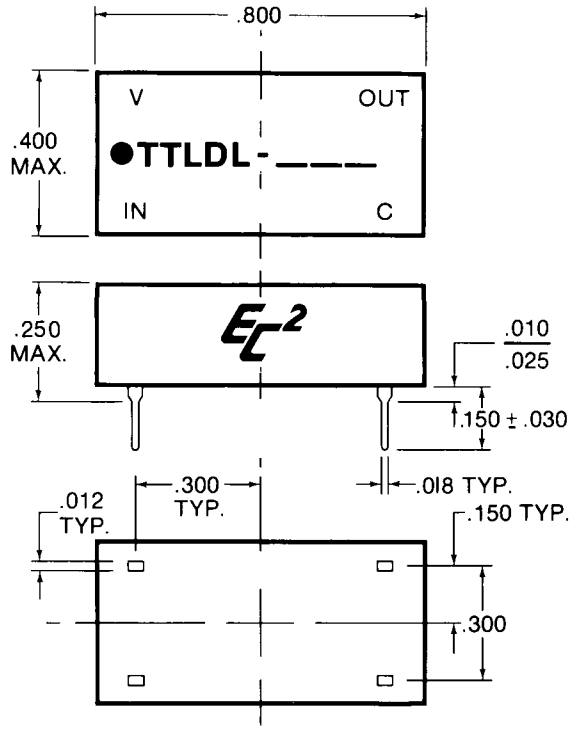
DESIGN NOTES (continued)

Marking consists of manufacturer's name, logo (EC^2), part number, terminal identification and date code of manufacture. All marking is applied by silk screen process using white epoxy paint in accordance with MIL-STD-130, to meet the permanency of identification required by MIL-STD-202, Method 215.

BLOCK DIAGRAM IS SHOWN BELOW



MECHANICAL DETAIL IS SHOWN BELOW



TEST CONDITIONS

1. All measurements are made at 25°C.
2. V_{CC} supply voltage is maintained at 5.0V DC.
3. All units are tested using a Schottky toggle-type positive input pulse and one Schottky T^{2}L load at the output.
4. ϕ Input pulse width used is 100% longer than delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

OPERATING SPECIFICATIONS

* V_{CC} supply voltage:	4.75 to 5.25V DC
V_{CC} supply current:	
Constant "0" in	60ma typical
Constant "1" in	20ma typical
Logic 1 input:	
Voltage	2V min.; 5.5V max.
Current	2.4V = 50ua max.
	5.5V = 1ma max.
Logic 0 input:	
Voltage	.8V max.
Current	−2ma max.
Logic 1 Voltage out:	2.4V min.
Logic 0 Voltage out:	.4V max.
Operating temperature range:	0 to 70°C.
Storage temperature:	−55 to +125°C.

* Delays increase or decrease approximately 4% for a respective increase or decrease of 5% in supply voltage.

PART NUMBER TABLE

ϕ DELAYS AND TOLERANCES (in ns)			
PART NO.	OUTPUT	PART NO.	OUTPUT
TTLDL-5	5 ±1	TTLDL-60	60 ±2
TTLDL-6	6 ±1	TTLDL-65	65 ±2.5
TTLDL-7	7 ±1	TTLDL-70	70 ±2.5
TTLDL-8	8 ±1	TTLDL-75	75 ±2.5
TTLDL-9	9 ±1	TTLDL-80	80 ±2.5
TTLDL-10	10 ±1	TTLDL-85	85 ±3
TTLDL-11	11 ±1	TTLDL-90	90 ±3
TTLDL-12	12 ±1	TTLDL-95	95 ±3
TTLDL-13	13 ±1	TTLDL-100	100 ±3
TTLDL-14	14 ±1	TTLDL-125	125 ±4
TTLDL-15	15 ±1	TTLDL-150	150 ±4.5
TTLDL-16	16 ±1	TTLDL-175	175 ±5
TTLDL-17	17 ±1	TTLDL-200	200 ±6
TTLDL-18	18 ±1	TTLDL-225	225 ±7
TTLDL-19	19 ±1	TTLDL-250	250 ±8
TTLDL-20	20 ±1	TTLDL-275	275 ±9
TTLDL-21	21 ±1	TTLDL-300	300 ±10
TTLDL-22	22 ±1	TTLDL-350	350 ±11
TTLDL-23	23 ±1	TTLDL-400	400 ±12
TTLDL-24	24 ±1	TTLDL-450	450 ±14
TTLDL-25	25 ±1	TTLDL-500	500 ±15
TTLDL-30	30 ±1.5	TTLDL-600	600 ±18
TTLDL-35	35 ±1.5	TTLDL-700	700 ±20
TTLDL-40	40 ±1.5	TTLDL-800	800 ±22
TTLDL-45	45 ±2	TTLDL-900	900 ±24
TTLDL-50	50 ±2	TTLDL-1000	1000 ±26
TTLDL-55	55 ±2		

ϕ All modules can be operated with a minimum input pulse width of 100% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.

028121 ✓ _ _

FEB 2 5 1992 Catalog No. C/112279