A DIVISION OF CIRRUS LOGIC

CS5334
CS5335

20-Bit, Stereo A/D Converter for Digital Audio

Features

- CS5334
  - Dynamic Range: 100 dB
  - THD+N: -90 dB
- CS5335
  - Dynamic Range: 105 dB
  - THD+N: -95 dB
- 128X Oversampling
- Fully Differential Inputs
- Linear Phase Digital Anti-Alias Filtering
  - 21.7 kHz passband (fs = 48 kHz)
  - 85 dB stop band attenuation
  - 0.0025 dB pass band ripple
- High Pass Filter - DC offset removal
- Peak Signal Level Detector
  - High Resolution and Bar Graph Modes

Description

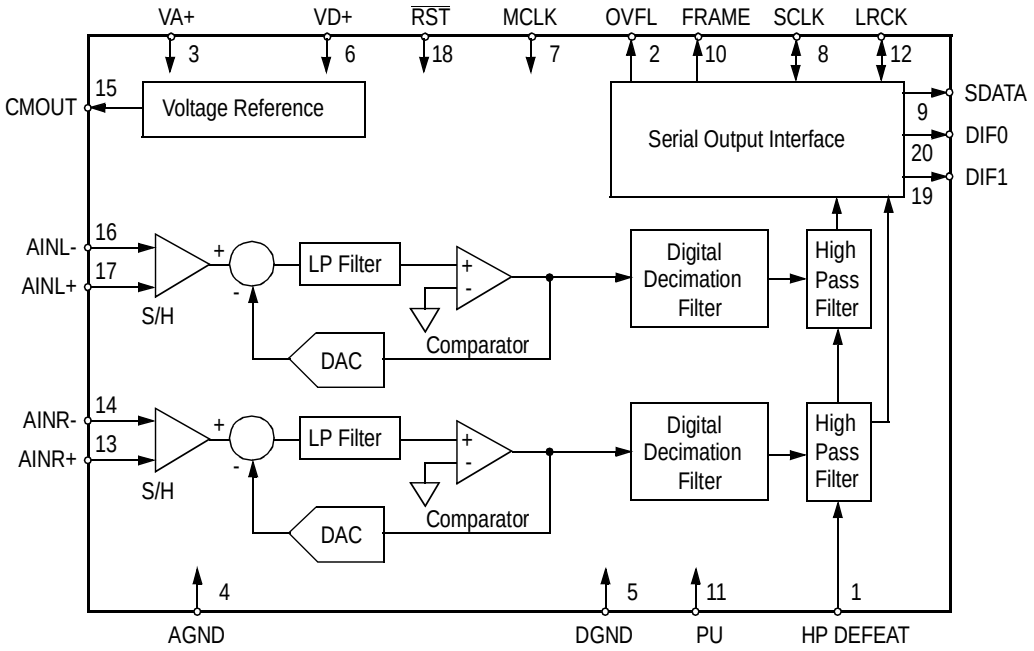
The CS5334 and CS5335 are 2-channel, single +5 V supply, pin compatable analog-to-digital converters for digital audio systems. The CS5334 and CS5335 perform sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5334 and CS5335 use 4th-order, delta-sigma modulation with 128X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. These ADCs use a differential architecture which provides excellent noise rejection.

The CS5334 and CS5335 have a filter passband to 21.7 kHz. The filter has linear phase, 0.0025 dB passband ripple, and >85 dB stopband rejection. An on-chip high pass filter is also included to remove DC offsets.

ORDERING INFORMATION

CS5334-KS	-10° to 70° C	20-pin Plastic SSOP
CS5335-KS	-10° to 70° C	20-pin Plastic SSOP



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25°C; VA+ = VD+ = 5V; -1 dBFS Input Sinewave, 997 Hz; Fs = 48 kHz; MCLK = 12.288 MHz; SCLK = 3.072 MHz; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified; Logic 0 = 0V, Logic 1 = VD+)

Parameter	Symbol	CS5334 Min	CS5334 Typ	CS5334 Max	CS5335 Min	CS5335 Typ	CS5335 Max	Units
Resolution		20	-	-	20	-	-	Bits
Dynamic Performance								
Dynamic Range A-weighted		TBD TBD	100 97	- -	TBD TBD	105 102	- -	dB dB
Total Harmonic Distortion + Noise -1 dB	THD+N	-	-90	TBD	-	-95	TBD	dB
-20 dB		-	-77	TBD	-	-82	TBD	dB
-60 dB		-	-37	TBD	-	-42	TBD	dB
Interchannel Phase Deviation		-	0.01	-	-	0.01	-	Degree
Interchannel Isolation (dc to 20 kHz)		-	100	-	-	105	-	dB
dc Accuracy								
Interchannel Gain Mismatch		-	0.05	-	-	0.05	-	dB
Gain Error		-	-	±5	-	-	±5	%
Gain Drift		-	200	-	-	200	-	ppm/°C
Offset Error with HPF		-	0	-	-	0	-	LSB
HP defeat with CAL		-	+/- 100	-	-	+/- 100	-	LSB
Analog Input								
Input Voltage Range (Differential)	VIN	1.9	2.0	2.1	1.9	2.0	2.1	Vrms
Input Impedance	ZIN	-	30	-	-	30	-	kΩ
Input Bias Voltage		-	2.2	-	-	2.2	-	V
Power Supplies								
Power Supply Current I_A		-	38	TBD	-	40	TBD	mA
I_D		-	25	TBD	-	25	TBD	mA
Power Down (I_A+I_D)		-	0.2	-	-	0.2	-	mA
Power Dissipation Normal		-	315	TBD	-	325	TBD	mW
Power Down		-	1.0	-	-	1.0	-	mW
Power Supply Rejection Ratio		-	50	-	-	55	-	dB

Specifications are subject to change without notice

DIGITAL FILTER CHARACTERISTICS (T_A = 25 °C; VA+ = VD+ = 5V ± 5%; Fs = 48 kHz)

Parameter			Symbol	Min	Typ	Max	Units
Passband		(Note 1)		0.02	-	21.7	kHz
Passband Ripple				-	-	±0.0025	dB
Stopband		(Note 1)		26.3	-	6118	kHz
Stopband Attenuation		(Note 2)		85	-	-	dB
Group Delay (Fs = Output Sample Rate)			t_{gd}	-	32/Fs	-	s
Group Delay Variation vs. Frequency			Δt_{gd}	-	-	0	µs
High Pass Filter Characteristics							
Frequency Response:	-3 dB -0.01 dB	(Note 1)		- -	0.9 20	- -	Hz Hz
Phase Deviation	@ 20 Hz	(Note 1)		-	2.6	-	Degree
Passband Ripple				-	-	0	dB

Notes: 1. Filter characteristic scales with output sample rate.
2. The analog modulator samples the input at 6.144 MHz for an output sample rate of 48 kHz. There is no rejection of input signals which are multiples of the sampling frequency (n x 6.144 MHz ±21.7kHz where n = 0,1,2,3...).

DIGITAL CHARACTERISTICS (T_A = 25 °C; VA+ = VD+ = 5V ± 5%)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.4	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage at Io = -20 µA	V_{OH}	(VD+)-1.0	-	-	V
Low-Level Output Voltage at Io = 20 µA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	µA

ABSOLUTE MAXIMUM RATINGS (AGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supply:		VA+	-0.3	-	+6.0	V
Input Current, Any Pin Except Supplies	(Note 3)	Iin	-	-	±10	mA
Analog Input Voltage	(Note 4)	V_{INA}	-0.7	-	(VA+)+0.7	V
Digital Input Voltage	(Note 4)	V_{IND}	-0.7	-	(VA+)+0.7	V
Ambient Temperature (power applied)		T_A	-55	-	+125	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 3. Any Pin except supplies. Transient currents of up to +/- 100 mA on the analog input pins will not cause SCR latch-up.
4. The maximum over/under voltage is limited by the input current.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS

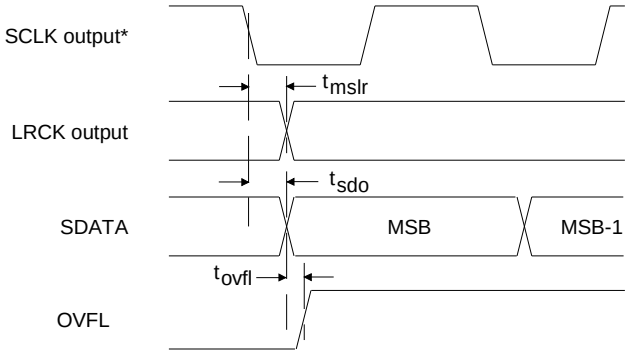
(T_A = 25 °C; VA+ = 5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VA+ = VD+; C_L = 20 pF)

Parameter		Symbol	Min	Typ	Max	Units
Output Sample Rate		F_s	2.0	-	50	kHz
MCLK Period	MCLK / LRCK = 256	t_{clkw}	78	-	1953	ns
MCLK Low	MCLK / LRCK = 256	t_{clkl}	31	-	-	ns
MCLK High	MCLK / LRCK = 256	t_{clkh}	31	-	-	ns
MCLK Period	MCLK / LRCK = 384	t_{clkw}	52	-	1302	ns
MCLK Low	MCLK / LRCK = 384	t_{clkl}	20	-	-	ns
MCLK High	MCLK / LRCK = 384	t_{clkh}	20	-	-	ns
MCLK Period	MCLK / LRCK = 512	t_{clkw}	39	-	976	ns
MCLK Low	MCLK / LRCK = 512	t_{clkl}	15	-	-	ns
MCLK High	MCLK / LRCK = 512	t_{clkh}	15	-	-	ns
MASTER MODE						
SCLK falling to LRCK	(Note 5)	t_{mslr}	-10	-	10	ns
SCLK falling to SDATA valid	(Note 5)	t_{sdo}	-10	-	35	ns
SCLK Duty cycle			-	50	-	%
SCLK falling to Frame Valid	(Note 5)	t_{sfo}	-10	-	(Note 6)	ns
LRCK edge to OVFL Valid		t_{ovfl}	-10	-	30	ns
LRCK edge to OVFL edge delay		t_{ovfl}	-10	-	(Note 10)	ns
SLAVE MODE						
LRCK duty cycle			25	50	75	%
SCLK Period		t_{sclkw}	(Note 7)	-	-	ns
SCLK Pulse Width Low	(Note 8)	t_{sclkl}	(Note 11)	-	-	ns
SCLK Pulse Width High	(Note 9)	t_{sclkh}	50	-	-	ns
SCLK falling to SDATA valid	(Note 5)	t_{dss}	-	-	(Note 11)	ns
LRCK edge to MSB valid		t_{lrdss}	-	-	(Note 11)	ns
SCLK rising to LRCK edge delay	(Note 12)	t_{slr1}	50	-	-	ns
LRCK edge to rising SCLK setup time	(Note 12)	t_{slr2}	(Note 11)	-	-	ns
SCLK falling to Frame delay		t_{sfo}	-	-	(Note 13)	ns

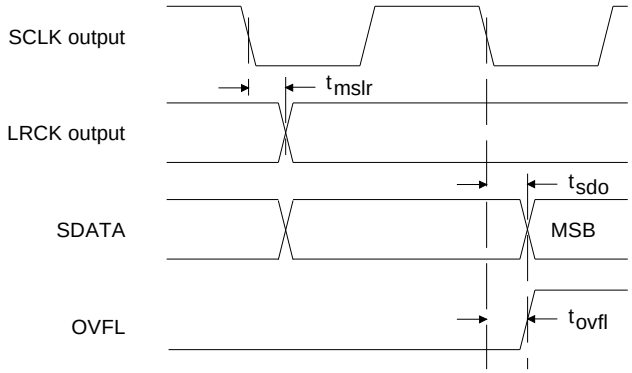
Notes: 5. SCLK rising for Mode 1. 6. $\frac{1}{(1024)(F_S)} + 30ns$ 7. $\frac{1}{(96)(F_S)}$ 8. Pulse Width High for Mode 1

9. Pulse Width Low for Mode 1 10. $\frac{1}{(512)(F_S)} + 20ns$ 11. $\frac{1}{(512)(F_S)} + 50ns$

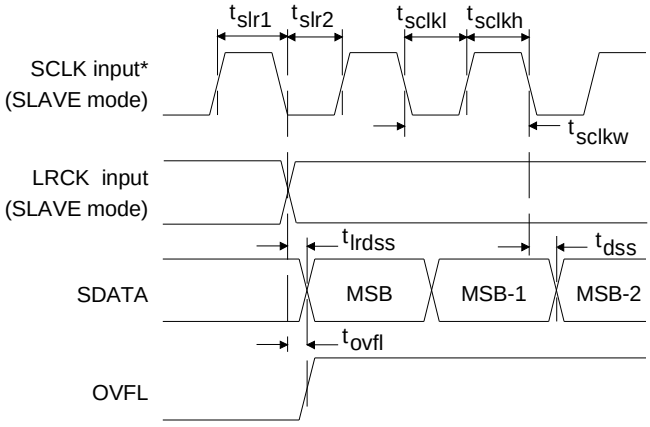
12. SCLK Falling for Mode 1 13. $\frac{1}{(384)(F_S)} + 35ns$



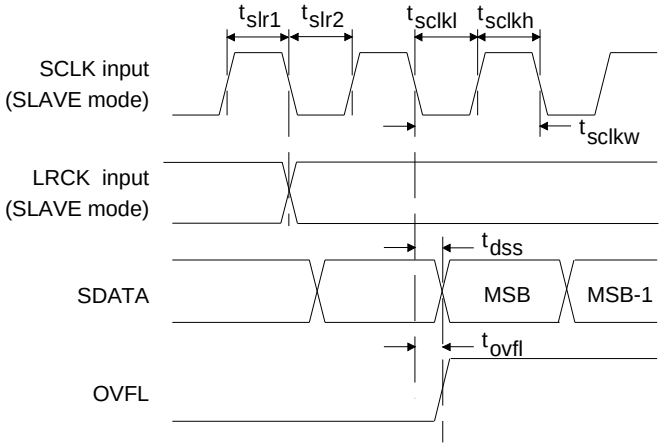
SCLK to SDATA & LRCK - MASTER mode
Format 0 and 1



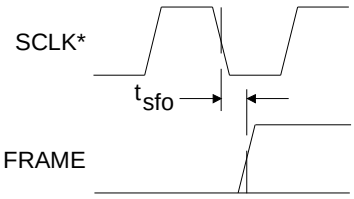
SCLK to SDATA & LRCK - MASTER mode
Format 2



SCLK to LRCK & SDATA - SLAVE mode
Format 0 & 1



SCLK to LRCK & SDATA - SLAVE mode
Format 2



SCLK to Frame Delay

***SCLK is inverted for Format 1**

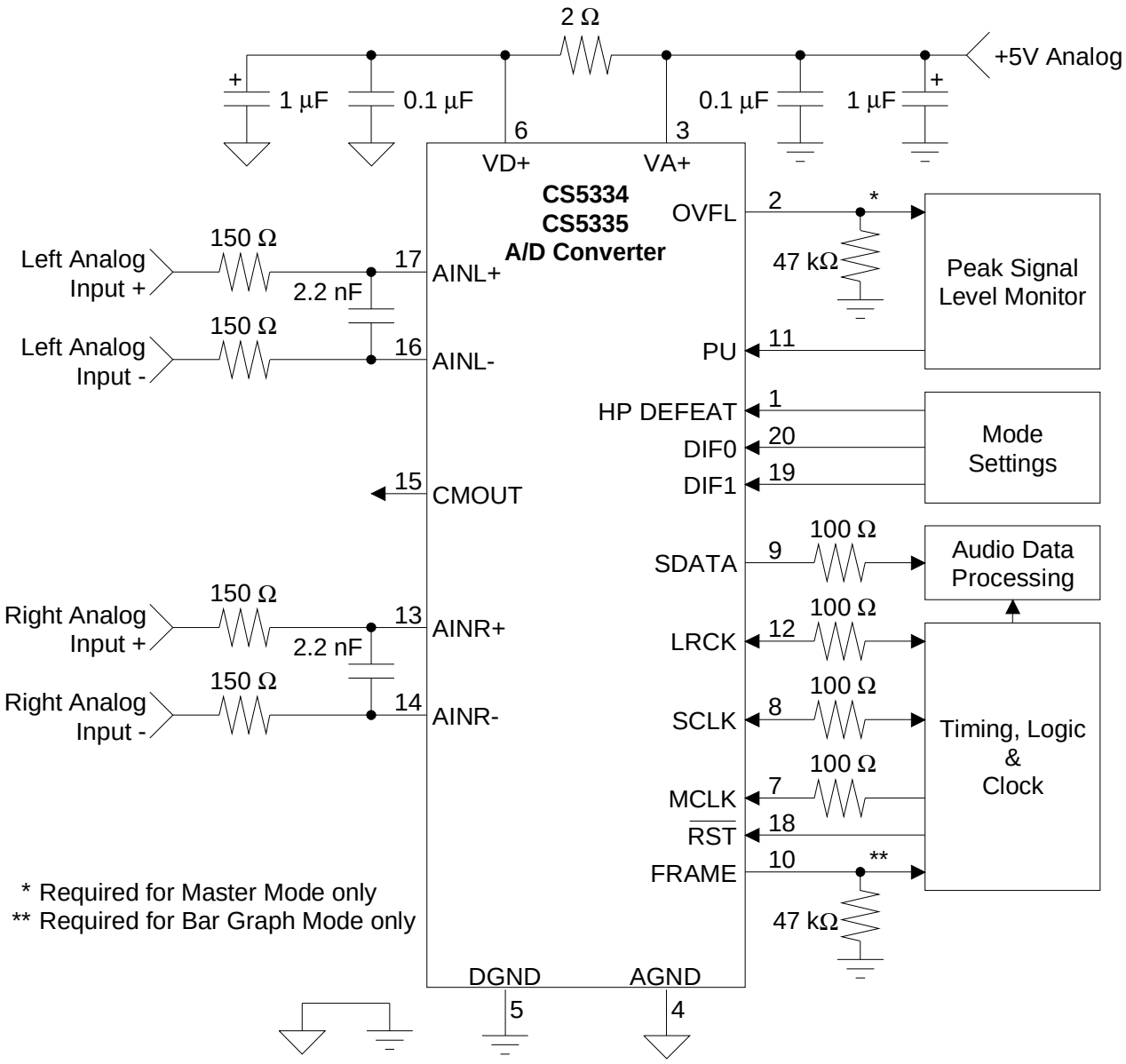


Figure 1. Typical Connection Diagram

SYSTEM DESIGN

The CS5334 and CS5335 are 20-bit, 2-channel Analog-to-Digital Converters designed for digital audio applications. These devices use two one-bit delta-sigma modulators which simultaneously sample the analog input signals at 128 times the output sample rate (Fs). The resulting serial bit streams are digitally filtered, yielding a pair of 20-bit values. This technique yields nearly ideal conversion performance independent of input frequency and amplitude. The converter does not require difficult-to-design or expensive anti-alias filters and does not require external sample-and-hold amplifiers or a voltage reference. Very few external components are required to support these ADCs. Normal power supply decoupling components and a resistor and capacitor on each input for anti-aliasing are all that's required, as shown in Figure 1.

An on-chip voltage reference provides for a differential input signal range of 2.0 Vrms. Output data is available in serial form, coded as 2's complement, 20-bit numbers. Typical power consumption is 325 mW which can be reduced to 1.0 mW using the power-down feature.

Master Clock

The master clock (MCLK) is the clock source for the delta-sigma modulator sampling and digital filters. In Master Mode, the frequency of this clock must be 256× Fs. In Slave Mode, the master clock must be either 256×, 384× or 512× Fs. Table 1 shows some common master clock frequencies.

LRCK (kHz)	MCLK (MHz)		
	256 X	384 X	512 X
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 1. Common Clock Frequencies

SERIAL DATA INTERFACE

The CS5334 and CS5335 support three serial data formats, including I^2S, which are selected via the digital input format pins DIF0 and DIF1. The digital input format determines the relationship between the serial data, left/right clock and serial clock. Table 2 lists the three formats, along with the associated figure number. The serial data interface is accomplished via the serial data output, SDATA, serial data clock, SCLK, and the left/right clock, LRCK.

DIF1	DIF0	FORMAT	FIGURE
0	0	0	3
0	1	1	4
1	0	2	5
1	1	power-down	-

Table 2. Digital Input Formats

Serial Data

The serial data block consists of 20 bits of audio data presented in 2's-complement format with the MSB-first, followed by 4 bits of zero and 8 Peak Signal Level, PSL, bits as shown in Figure 2. The data is clocked from SDATA by the serial clock and the channel is determined by the Left/Right clock.

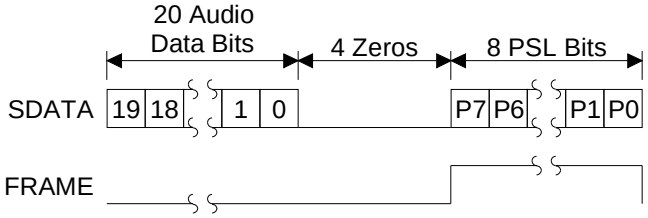
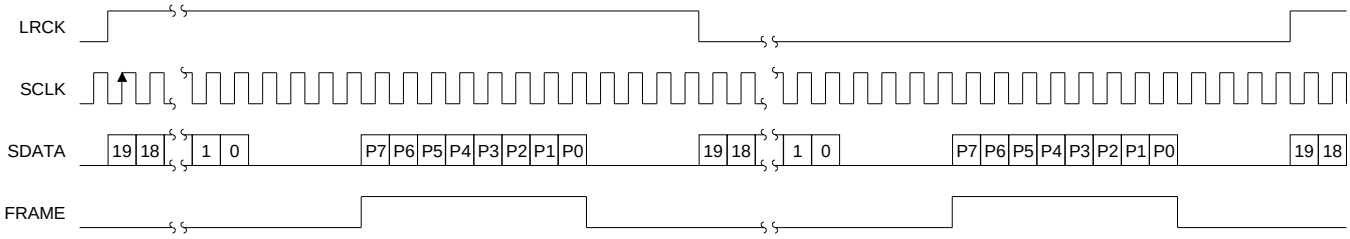
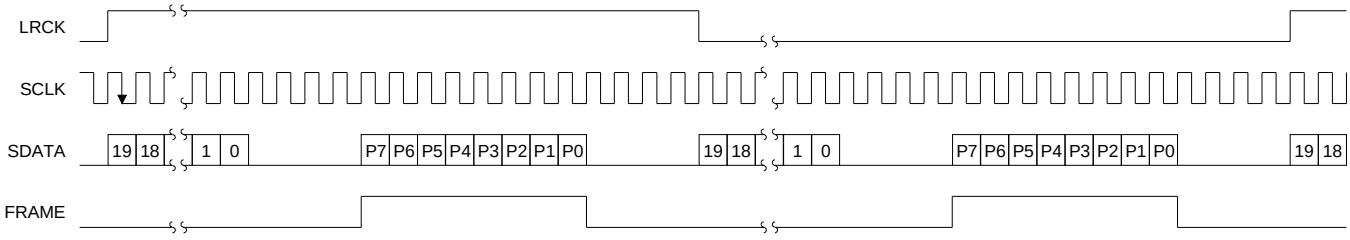


Figure 2. Data Block and Frame



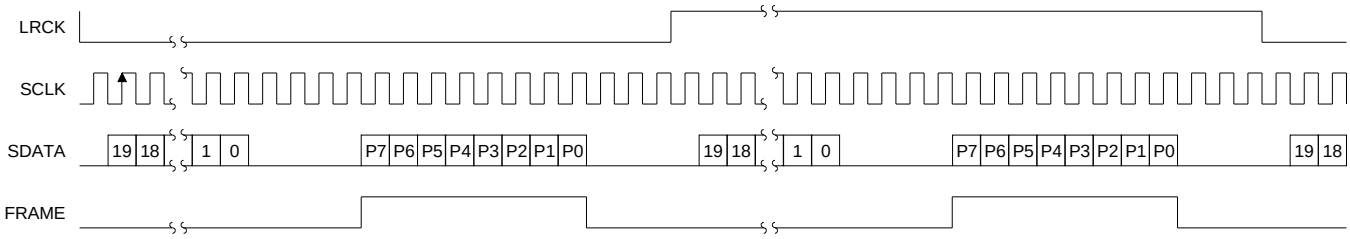
MASTER	SLAVE
20-Bit Left Justified Data	20-Bit Left Justified Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x F_S	MCLK equal to 256x, 384x or 512x F_S

Figure 3. Serial Data Format 0



MASTER	SLAVE
20-Bit Left Justified Data	20-Bit Left Justified Data
Data Valid on Falling Edge of 64x SCLK	Data Valid on Falling Edge of SCLK
MCLK equal to 256x F_S	MCLK equal to 256x, 384x or 512x F_S

Figure 4. Serial Data Format 1



MASTER	SLAVE
I^2S 20-Bit Data	I^2S 20-Bit Data
Data Valid on Rising Edge of 64x SCLK	Data Valid on Rising Edge of SCLK
MCLK equal to 256x F_S	MCLK equal to 256x, 384x or 512x F_S

Figure 5. Serial Data Format 2

Serial Clock

The serial clock shifts the digitized audio data from the internal data registers via the SDATA pin. SCLK is an output in Master Mode. Internal dividers will divide the master clock by 4 to generate a serial clock which is 64× Fs. In Slave Mode, SCLK is an input with a serial clock typically between 48× and 128× Fs. However, the serial clock must be a minimum of 64× Fs to access the Peak Signal Level bits.

Left / Right Clock

The Left/Right clock determines which channel, left or right, is to be output on SDATA. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In Master Mode, LRCK is an output whose frequency is equal to Fs. In Slave Mode, LRCK is an input whose frequency must be equal to the output sample rate, Fs.

Master Mode

In Master mode, SCLK and LRCK are outputs which are internally derived from the Master Clock. Internal dividers will divide MCLK by 4 to generate a SCLK which is 64× Fs and by 256 to generate a LRCK which is equal to Fs. Master mode is only supported with a 256× master clock. The CS5334/5 is placed in the Master mode with a 47 kΩ pull-down resistor on the OVFL pin.

Slave Mode

LRCK and SCLK become inputs in SLAVE mode. LRCK must be externally derived from MCLK and be equal to Fs. The serial clock is typically between 64× and 128× Fs. A 48× Fs serial clock is possible though will not allow access to the Peak Signal Level bits. Master clock frequencies of 256×, 384× and 512× Fs are supported. The ratio of the applied master clock to the left/right clock is automatically detected during power-up and internal dividers are set to generate the appropriate internal clocks.

Analog Connections

Figure 1 shows the analog input connections. The analog inputs are presented to the modulators via the AINR+/- and AINL+/- pins. Each analog input pin will accept a maximum of 1 Vrms centered at +2.2 Volt as shown in Figure 6. Input signals can be AC or DC coupled and the CMOUT output may be used as a reference for DC coupling. However, CMOUT is not buffered and the maximum current is 10 µA.

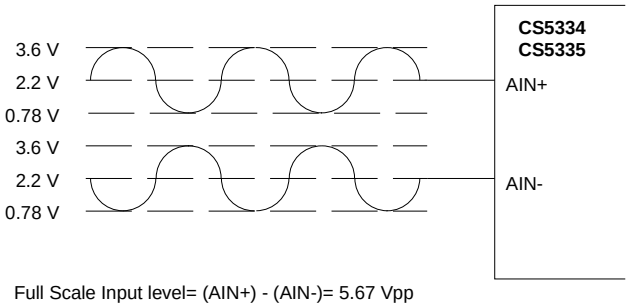


Figure 6. Full Scale Input Levels

The CS5334 and CS5335 sample the analog inputs at 128×Fs, 6.144 MHz for a 48 kHz sample-rate. The digital filter rejects all noise above 26.3 kHz except for frequencies right around 6.144 MHz ± 21.7 kHz (and multiples of 6.144 MHz). Most audio signals do not have significant energy at 6.144 MHz. Nevertheless, a 150 Ω resistor in series with each analog input and a 2.2 nF capacitor across the inputs will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors which have a large voltage coefficient must be avoided since these will degrade signal linearity. NPO and COG capacitors are acceptable. If active circuitry precedes the ADC, it is recommended that the above RC filter is placed between the active circuitry and the AINR and AINL pins. The above example frequencies scale linearly with sample rate.

High Pass Filter

The operational amplifiers in the input circuitry driving the CS5334/5 may generate a small DC offset into the A/D converter. The CS5334 and CS5335 include a high pass filter after the decimator to remove any DC offset which could result in recording a DC level, possibly yielding "clicks" when switching between devices in a multichannel system. The high pass filter can be disabled with the HP DEFEAT pin. The high pass filter works by continuously subtracting a measure of the dc offset from the output of the decimation filter. If the HP DEFEAT pin is taken high during normal operation, the current value of the dc offset register is frozen and this dc offset will continue to be subtracted from the conversion result. This feature makes it possible to perform a system calibration by;
1. removing the signal source (or grounding the input signal) at the input to the subsystem containing the CS5334/5,
2. running the CS5334/5 with the HP DEFEAT pin low (high pass filter enabled) until the filter settles (approximately 1 second), and
3. taking the HP DEFEAT pin high, disabling the high pass filter and freezing the stored dc offset.

A system calibration performed in this way will eliminate offsets anywhere in the signal path between the calibration point and the CS5334/5.

The characteristics of the first-order high pass filter are outlined below for an output sample rate of 48 kHz. This filter response scales linearly with sample rate.

Frequency response:	-3 dB @ 0.9 Hz
	-0.01 dB @ 20 Hz
Phase deviation:	2.6 degrees @ 20 Hz
Passband ripple:	None

INPUT LEVEL MONITORING

The CS5334 and CS5335 include independent Peak Input Level Monitoring for each channel. The analog-to-digital converter continually monitors the peak digital signal for both channels, prior to the digital limiter, and records these values in the Active registers. This information can be transferred to the Output registers by a high to low transition on the Peak Update pin (PU) which will also reset the Active register. The Active register contains the peak signal level since the previous peak update request.

The 8-bit contents of the output registers are available in all interface modes and are present in the data block as shown in Figure 2. The monitoring function can be formatted to indicate either High Resolution Mode or Bar Graph Mode. The monitoring function is determined on power-up by the presence of a 47 kohm pull-down resistor on FRAME. The addition of a 47 kohm pull-down resistor on the FRAME pin sets the monitoring function to the Bar Graph mode.

High Resolution Mode

Bits P7-P0 indicate the peak input level since the previous peak update (or low transition on the Peak Update pin). If the full scale input level is exceeded (Bit P7 high), bits P5-P0 represent the peak value up to 3 dB above full-scale in 1 dB steps. If the ADC input level is less than full-scale, bits P5-P0 represent the peak value from -60 dB to 0 dB of full scale in 1 dB steps. The PSL outputs are accurate to within 0.25 dB. Bit P6 provides a coarse means of determining an ADC input idle condition. Bit P7 indicates an ADC overflow condition, if the ADC input level is greater than full-scale.

P7 - Overrange
0 - Analog input less than full-scale level
1 - Analog input greater than full-scale

P6 - Idle channel
0 - Analog input >-60 dB from full-scale
1 - Analog input <-60 dB from full-scale

P5 to P0 - Peak Signal Level Bits (1 dB steps)

Inputs <0 dB	P5 - P0
0 dB	000000
-1 dB	000001
-2 dB	000010
-60 dB	111100

Inputs >0 dB	P5 - P0
0 dB	000000
+1 dB	000001
+2 dB	000010
+3 dB	000011

Bar Graph Mode

This mode provides a decoded output format which indicates the peak Peak Signal Level in a "Bar Graph" format.

Input Level	P7 - P0
Overflow	11111111
0 dB to -3 dB	01111111
-3 dB to -6 dB	00111111
-6 dB to -10 dB	00011111
-10 dB to -20 dB	00001111
-20 dB to -30 dB	00000111
-30 dB to -40 dB	00000011
-40 dB to -60 dB	00000001
< - 60 dB	00000000

Overflow

Overflow indicates analog input overrange, for both the Left and Right channels, since the last update request on the Peak Update pin. A value of 1 indicates an overrange condition. The left channel information is output on OVFL during the left channel portion of LRCK. The right channel information is available on OVFL during the right channel portion of LRCK.

Initialization

Upon initial power-up, the digital filters and delta-sigma modulators are reset and the internal voltage reference is powered down. The CS5334/5 will remain in the power-down mode until valid clocks are presented. A valid MCLK is required to exit power-down in Master Mode. However, in Slave Mode, MCLK and LRCK of the proper ratio are required to exit power-down. MCLK occurrences are also counted over one LRCK period to determine the MCLK / LRCK frequency ratio in Slave Mode. Power is then applied to the internal voltage reference, the analog inputs will move to approximately 2.2V and output clocks will begin (Master Mode only). This process requires 32 periods of LRCK and is followed by the initialization sequence.

Initialization with High Pass Filter Enabled

28,672 LRCK cycles are required for the initialization sequence with the high pass filter enabled. This time is dominated by the settling time required for the high pass filter.

Initialization and Internal Calibration with High Pass Filter Disabled

If the HP DEFEAT pin is high (high pass filter disabled) during the initialization sequence, the CS5334/5 will perform an internal dc calibration by:
1. disconnecting the internal ADC inputs from the input pins,
2. connecting the (differential) ADC inputs to a common reference voltage,

3. running the high pass filter with a fast settling time constant,
4. freezing the dc offset register, and
5. reconnecting the internal ADC inputs to the input pins.

This procedure takes 4,160 cycles of LRCK. Unlike the system calibration procedure described in the High Pass Filter section, a dc calibration performed during start-up will only eliminate offsets internal to the CS5334/5, and should result in output codes which accurately reflect the differential dc signal at the pins.

Power-Down

The CS5334 and CS5335 have a power-down mode wherein typical consumption drops to 1.0 mW. This is initiated when a loss of clock is detected (either LRCK or MCLK in Slave Mode or MCLK in Master Mode), $\overline{\text{RST}}$ is enabled or DIF0 / DIF1 are at a logic 1. The initialization sequence will begin whenever valid clocks are restored, $\overline{\text{RST}}$ is disabled and DIF0 / DIF1 are restored. If the MCLK / LRCK frequency ratio changes during power-down, the CS5334/5 will adapt to these new operating conditions. However, only the $\overline{\text{RST}}$ method of power-down will include the Master/Slave decision in the initialization sequence.

Grounding and Power Supply Decoupling

As with any high resolution converter, the CS5334 and CS5335 require careful attention to power supply and grounding arrangements to optimize performance. Figure 1 shows the recommended power arrangements with VA+ connected to a clean +5 volt supply. VD+ should be derived from VA+ through a 2 ohm resistor. VD+ should not be used to power additional digital circuitry. All mode pins which require VD+ should be connected to pin 6 of the CS5334/5. All mode pins which require DGND should be connected to pin 5 of the CS5334/5. AGND and DGND, Pins 4 and 5, should be connected together at the CS5334/5. DGND for the CS5334/5 should not be confused with the ground for the digital section of the system. The CS5334/5 should be positioned over the analog ground plane near the digital / analog ground plane split. The analog and digital ground planes must be connected elsewhere in the system. The CS5334/5 evaluation board, CDB5334/5, demonstrates this layout technique. This technique minimizes digital noise and insures proper power supply matching and sequencing. Decoupling capacitors should be located as near to the CS5334/5 as possible.

Digital Filter

Figures 7-10 show the performance of the digital filter included in the CS5334/5. All plots are normalized to Fs. Assuming a sample rate of 48 kHz, the 0.5 frequency point on the plot refers to 24 kHz. The filter frequency response scales precisely with the sample rate.

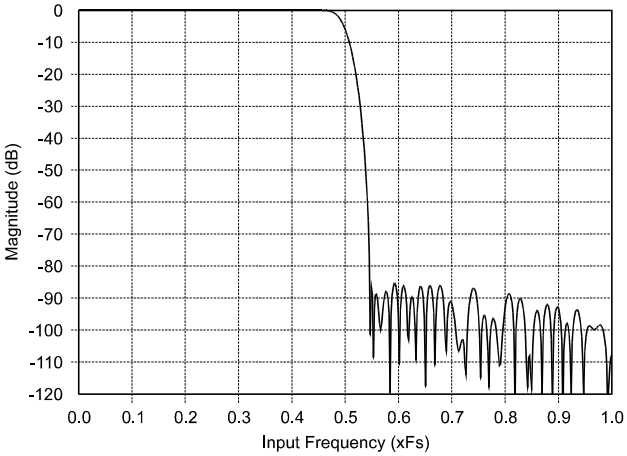


Figure 7. CS5334/5 Digital Filter Stopband Rejection

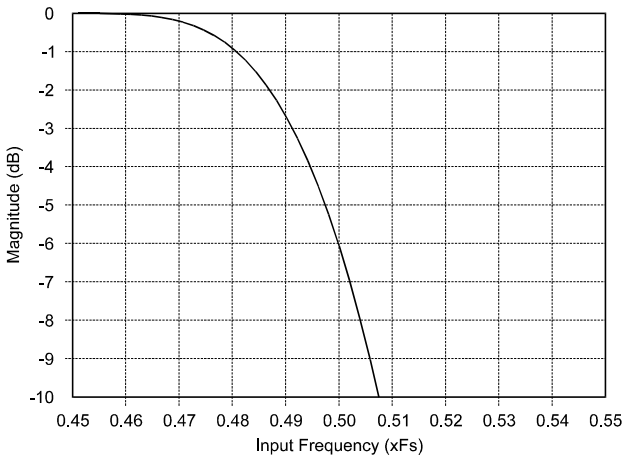


Figure 8. CS5334/5 Digital Filter Transition Band

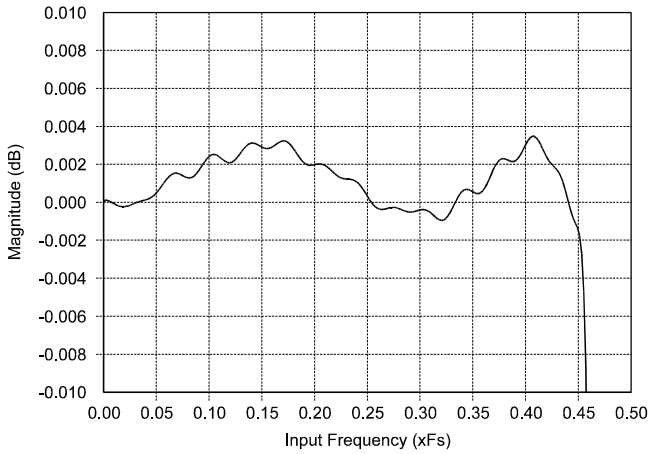


Figure 9. CS5334/5 Digital Filter Passband Ripple

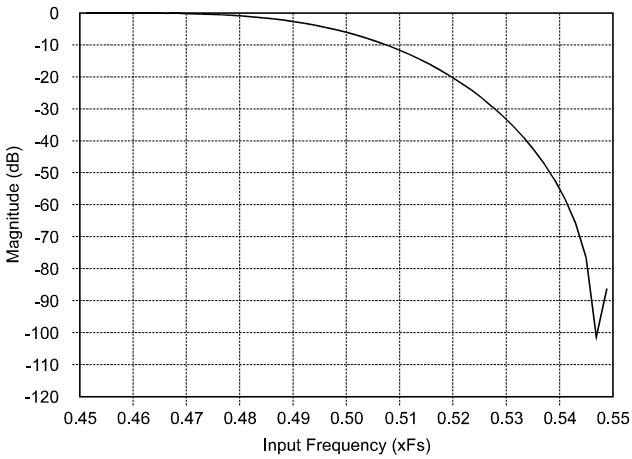
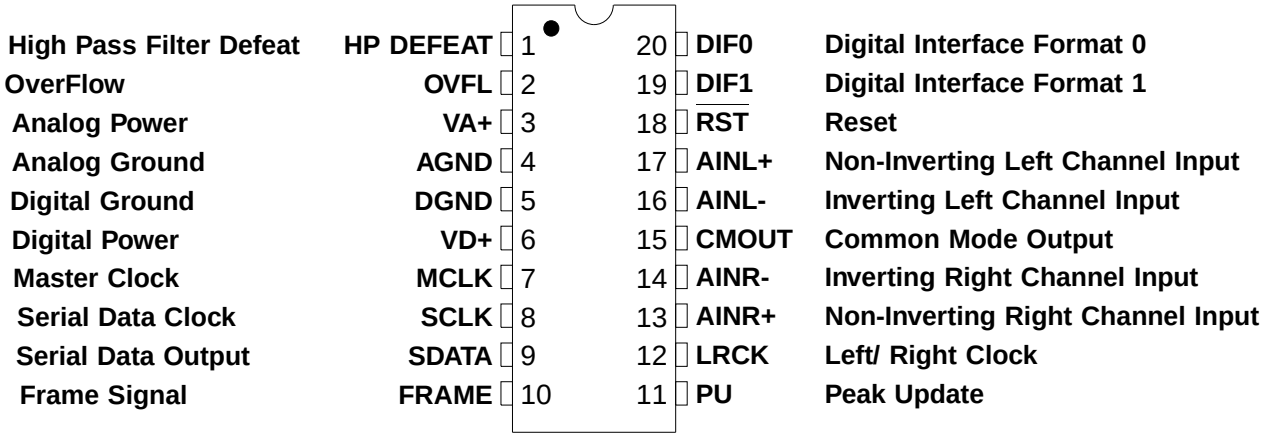


Figure 10.CS5334/5 Digital Filter Transition Band

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, Pin 3.
Positive analog supply. Nominally +5 volts.

VD+ - Positive Digital Power, Pin 6.
Positive digital supply. Nominally +5 volts.

AGND - Analog Ground, Pin 4.
Analog ground reference.

DGND - Digital Ground, Pin 5.
Digital ground reference.

Analog Inputs

AINR-, AINR+ - Differential Right Channel Analog Input, Pin 14 and Pin 13.
Analog input connections of the right channel differential inputs. Typically 2 Vrms differential (1Vrms for each input pin) for a full-scale analog input signal.

AINL-, AINL+ - Differential Left Channel Analog Input, Pin 16 and Pin 17.
Analog input connections of the left channel differential inputs. Typically 2 Vrms differential (1Vrms for each input pin) for a full-scale analog input signal.

Analog Outputs

CMOUT - Common Mode Output, Pin 15.
This output, nominally 2.2V, can be used to bias the analog input circuitry to the common mode voltage of the CS5334/5.

Digital Inputs

MCLK - Master Clock, Pin 7.

Clock source for the delta-sigma modulator sampling and digital filters.

In Master Mode, the frequency of this clock must be 256× the output sample rate, Fs.

In Slave Mode, the frequency of this clock must be either 256×, 384× or 512× Fs.

DIF0, DIF1 - Digital Interface Format, Pins 19 and 20.

These two pins select one of 3 digital interface formats or power-down. The format determines the relationship between SCLK, LRCK and SDATA. The formats are detailed in Figures 3-5.

$\overline{\text{RST}}$ - Reset, Pin 18.

A low logic level on this pin activates Reset.

HP DEFEAT - High Pass Filter Defeat, Pin 1.

A high logic level on this pin disables the digital high pass filter. A low logic level on this pin enables the high pass filter.

PU - Peak Update, Pin 11.

Transfers the Peak Signal Level contents of the Active Registers to the Output Registers on a high to low transition on this pin. This transition will also reset the Active register.

Digital Inputs / Outputs

LRCK - Left/Right Clock, Pin 12.

LRCK determines which channel, left or right, is to be output on SDATA. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1. Although the outputs for each channel are transmitted at different times, Left/Right pairs represent simultaneously sampled analog inputs. In Master Mode, LRCK is an output clock whose frequency is equal to the output sample rate, Fs. In Slave Mode, LRCK is an input clock whose frequency must be equal to Fs.

SCLK - Serial Data Clock, Pin 8.

Clocks the individual bits of the serial data out from the SDATA pin. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1.

In Master Mode, SCLK is an output clock with a frequency of 64x the output sample rate, Fs.

In Slave Mode, SCLK is an input.

Digital Outputs

SDATA - Serial Data Output, Pin 9.

Two's complement MSB-first serial data of 20 bits is output on this pin. Included in the serial data output is the 8-bit Input Signal Level Bits. The data is clocked out via the SCLK clock and the channel is determined by LRCK. The relationship between LRCK, SCLK and SDATA is controlled by DIF0 and DIF1.

$\overline{\text{OVFL}}$ - Overflow, Pin 2.

Overflow indicates analog input overrange, for both the Left and Right channels, since the last update request on the PEAK UPDATE (PU) pin. A value of 1 in the register indicates an overrange condition. The left channel information is output on OVFL during the left channel portion of LRCK. The right channel information is available on OVFL during the right channel portion of LRCK. The registers are updated with a high to low transition on the PEAK UPDATE pin. A 47 kohm pull-down resistor on this pin will set the CS5334/5 in Master Mode.

FRAME - Frame Signal, Pin 10.

Frames the Peak Signal Level (PSL) Bits. FRAME goes high coincident with the leading edge of the first PSL bit and falls coincident with the trailing edge of the last PSL bit as shown in Figures 3-5. A 47 kohm pull-down resistor on this pin will set the Peak Signal Level Monitoring format to "Bar Graph" mode.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60dBFs signal. 60dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFs as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter’s output with no signal at the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog input for a full-scale digital output.

Gain Drift

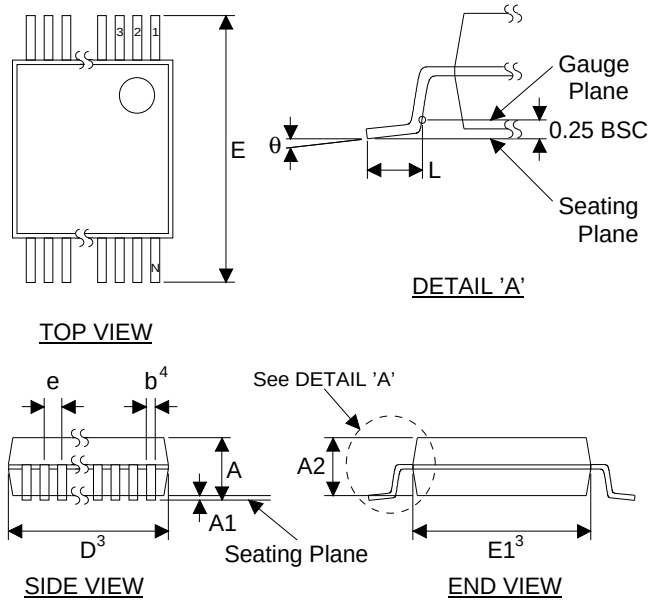
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

PACKAGE DIMENSIONS

SSOP
Package Dimensions



Notes:
1. Dimensioning and tolerance per ANSI.Y14.5M-1982.
2. Symbols are defined in the "MO Series Symbol List" in section 2.2 of JEDEC Publication 95.
3. "D" and "E1" are reference datums and do not include mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20mm per side.
4. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13mm total in excess of b dimension at maximum material condition. Dambar intrusion shall not reduce dimension b by more than 0.07mm at least material condition.
5. These dimensions apply to the flat section of the lead between 0.10 and 0.25mm from lead tips.

	MILLIMETERS			
DIM	MIN	NOM	MAX	Note
A	-	-	2.13	
A1	0.05	-	0.25	
A2	1.62	1.75	1.88	
b	0.22	-	0.38	4, 5
D	see other table			3
E	7.40	7.80	8.20	
E1	5.00	5.30	5.60	3
e	0.65 BSC			
L	0.63	0.90	1.03	
N	see other table			
θ	0°	4°	8°	

	D			
N	MIN	NOM	MAX	Note
8	2.70	3.00	3.30	3
14	5.90	6.20	6.50	3
16	5.90	6.20	6.50	3
18	6.90	7.20	7.50	3
20	6.90	7.20	7.50	3
22	7.90	8.20	8.50	3
24	7.90	8.20	8.50	3
28	9.90	10.20	10.50	3
30	9.90	10.20	10.50	3

A DIVISION OF CIRRUS LOGIC

CDB5334/35/60

Evaluation Board for CS5334/CS5335/CS5360

Features

- Demonstrates recommended layout and grounding arrangements
- CS8402A Generates AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Buffered Serial Output Interface
- Digital and Analog Patch Areas
- On-board or externally supplied system timing

Description

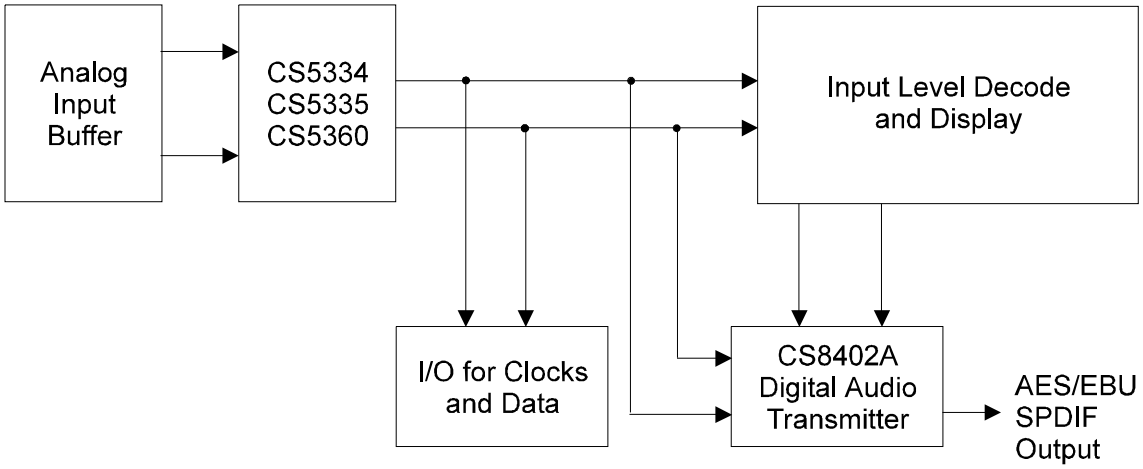
The CDB5334/35/60 evaluation board is an excellent means for quickly evaluating the CS5334, CS5335, or CS5360 stereo A/D converters. Evaluation requires a digital signal processor, a low distortion analog signal source and a power supply. Analog inputs are provided via XLR connectors for both channels.

Also included is a CS8402A digital audio interface transmitter which generates AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The digital audio data is available via RCA phono, and optical connectors.

The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFO

CDB5334/35/60



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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CDB5334/35/60 SYSTEM OVERVIEW

The CDB5334/35/60 evaluation boards are an excellent means of quickly evaluating the CS5334, CS5335, or CS5360. The CS8402A digital audio interface transmitter provides an easy interface to digital audio signal processors, including the majority of digital audio test equipment. The evaluation board has been designed to accept an analog input, and provide optical and coaxial digital outputs. The evaluation board also allows the user to access clocks and data through a 10-pin header for system development. In addition, the evaluation board supports the input level monitoring function provided by the CS5334, CS5335, and CS5360. The Peak Signal Level bits are displayed on bargraph LEDs or 7 segment displays for both left and right channels.

The CDB5334/35/60 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the system diagram also includes the connections between the partitioned schematics.

Power Supply Circuitry and Grounding

Power is supplied to the evaluation board by six binding posts as shown in Figure 2. +5VA provides 5 Volt power to the converter and the reset circuitry. The ±12 V binding posts provide power to the analog input buffer. C1-C3 and C5-C7 provide general power supply filtering for the analog supplies. Z1-Z3 are transient suppression diodes which also provide protection from incorrectly connected power supply leads. +5VD supplies 5 Volt power to the digital section of the board. C41 and C10 provide general power supply filtering. Z4 is a transient suppressor.

Localized decoupling for the CS5334, CS5335, or CS5360 is provided by C16, C17, C32, and C33, as shown in Figure 4. R10, C16, and C32 form a low pass filter which isolates VA+ from noise on VD+.

The evaluation board uses separate analog and digital ground planes which are joined together underneath resistors R6, R41, and R52-R55. This arrangement isolates the analog circuitry from the digital logic.

Reset Circuit and Offset Calibration

Two methods of placing the CS5334, CS5335, or CS5360 into power-down mode are provided on the evaluation board. The CAL switch, shown in Figure 8, pulls the DIF0 and DIF1 lines high on the CS5334, CS5335, or CS5360, thus placing the ADC into power-down mode. Releasing the CAL switch causes the DIF0 and DIF1 settings to be restored, upon which an initialization sequence begins, as described in the CS5334/CS5335 and CS5360 data sheets.

The reset circuit provided on the evaluation board is shown in Figure 2. Upon power up, this circuit sends a reset to the RST pin of the CS5334, CS5335, or CS5360. Power-down, followed by offset calibration, can also be performed by pressing and then releasing the RST switch. It should be noted that only the RST method of powering down the CS5334, CS5335, or CS5360 will include the decision of master or slave operation.

Input Buffer and Protection Circuits

The differential input circuit shown in Figure 3 is well-suited for the CS5334, CS5335, and CS5360 in professional applications. The circuit will accept a differential or single-ended signal of either polarity and provide a differential signal with the proper DC offset to the CS5334, CS5335, or CS5360. The circuit also incorporates 6 dB of attenuation to scale down professional input levels to the input voltage range of the CS5334, CS5335, or CS5360. A nominal input level of 4 Volts rms to the evaluation board will achieve a full scale digital output from the CS5334, CS5335, or CS5360. The common mode rejection of the system is limited by the passive component matching of the input buffer

circuit. The analog input connector is a standard female XLR with Pin 2 positive, Pin 3 return, and Pin 1 shield.

R1, R5, and C8 form an RC network which provides anti-alias filtering and the optimum source impedance for the CS5334, CS5335, or CS5360 right channel inputs. R2, R3, and C42 duplicate this function for the left channel.

Space has been left on the evaluation board for input protection diodes D1-D4 on the right channel, and D8-D11 on the left channel, shown in Figure 3. These diodes are optional as the CS5334, CS5335, and CS5360 are able to withstand input currents of 100mA maximum, as stated in the CS5334/CS5335 and CS5360 data sheets. The output current from the op-amp used in the analog filter on the evaluation board is not able to deliver a current that exceeds 100mA. Input protection diodes are recommended if there is a possibility that over-range signals could be applied at the ADC inputs which exceed this level. See the application note, "A/D Converter Input Protection Techniques" in the 1994 Crystal Semiconductor Audio Databook.

CS5334, CS5335, and CS5360 A/D Converters

The CS5334, CS5335, and CS5360 A/D converters are shown in Figure 4. A description of these devices are included in the CS5334/CS5335 and CS5360 data sheets.

CS8402A Digital Audio Interface

Figure 5 shows the circuitry for the CS8402A digital audio interface transmitter. The CS8402A can implement AES/EBU, S/PDIF, and EIAJ-340 interface standards. The Digital Interface Format (DIF) for the transmitter is set automatically to match the format chosen for the CS5334, CS5335, or CS5360 (the DIF is selected by the DIF1 and DIF0 switches on SW1, as defined in Table 3). SW2 provides 8 DIP switches to select various modes and bits for the CS8402A; switch definitions and the default settings for SW2 are listed in Tables 4 and 5. Digital outputs are provided on an RCA connector via isolation transformer and on an optical transmitter. For more detailed information on the CS8402A and the digital audio standards, see the CS8401A/CS8402A data sheet.

Serial Output Interface

A serial output interface is provided on HDR2, as shown in Figure 6. When the SMODE1 and SMODE2 jumpers, defined in Table 2, are set to the MASTER position, MCLK, SCLK, LRCK, SDATA, and FRAME signals are outputs. When the SMODE1 and SMODE2 jumpers are in the SLAVE position, MCLK, SDATA, and FRAME are outputs, while SCLK and LRCK become inputs. Hence, in SLAVE mode, the SCLK and LRCK signals must be externally derived from MCLK to run the ADC. All signals are buffered in order to isolate the converter from external circuitry. Signal buffering is provided by a 74HCT243 transceiver (U10) and a 74HCT541 buffer (U11).

ALTERA PLD AND PEAK SIGNAL LEVEL LEDS

The Altera EPM7128 programmable logic device (PLD), shown in Figure 8, is designed to support three major features on the evaluation board. First, it automatically configures the CS8402A transmitter to accept the Digital Interface Format chosen for the CS5334, CS5335, or CS5360. Second, the PLD provides a 128x Fs master clock for the CS8402A. Third, it decodes and updates the Peak Signal Level (PSL) bits which give information about the amplitude of the input signal.

CS8402A Format Configuration

The CS5334, CS5335, and CS5360 support three Digital Interface Formats for both master and slave configurations. Format 0 has valid data on the rising edge of SCLK. The CS8402A transmitter has no corresponding mode which matches Format 0,

but inverting the SCLK so that data is valid on the falling edge of SCLK will make the Format 0 interface lines match the Format 1 interface lines on the CS8402A. The PLD configures the CS8402A to Format 1 and performs SCLK inversion automatically when the DIF1, DIF0 switches on SW1 are set to 00.

Digital Interface Format 1 on the CS5334, CS5335, and CS5360 has valid data on the falling edge of SCLK. This interface format matches Format 1 on the CS8402A, so no modification is performed on the digital interface lines. The PLD configures the CS8402A to FORMAT 1 and passes the interface lines from the CS5334, CS5335, or CS5360 through to the CS8402A unchanged when the DIF1, DIF0 switches are set to 01.

Digital Interface Format 2 is the I2S compatible mode. It matches Format 4 on the transmitter. The PLD configures the CS8402A to Format 4 and passes the interface lines from the CS5334, CS5335, or CS5360 through to the CS8402A unchanged when the DIF1, DIF0 switches are set to 10.

CS8402A MCLK Generation

When the CDB5334/35/60 is set up for SLAVE mode, the crystal oscillator (U5) can be 256x, 384x, or 512x Fs. The CS8402A requires a master clock frequency of 128x Fs to operate. The PLD can be configured to divide MCLK_5335 (the oscillator output) by 2, 3, or 4 to generate MCLK_8402, thus accommodating the various possible frequencies of the oscillator. The switches on SW1 labeled MCLK_S1 and MCLK_S0 select the degree of clock division as defined in Table 3.

Decoding PSL bits / Driving LEDs

The PLD decodes and displays the Peak Signal Level bits for both High Resolution and Bargraph modes (for detailed information on the PSL bits, see the CS5334/CS5335 and CS5360 datasheets). When the TMODE1 and TMODE2 jumpers, defined in Table 2, are set to BARGRAPH, the PLD decodes the PSL bits and drives bargraph LEDs for the left and right channels. When the TMODE1 and TMODE2 jumpers are set to HI RES (High Resolution mode), the PLD drives the 7 segment displays for left and right channels.

The PLD also provides a Peak Update (PU) signal, which adjusts the rate at which the PSL bits are updated. Four settings provide update rates ranging from 42 ms to 2.7 s (for a 48 kHz sample rate). The switches on SW1 labeled PU_S1 and PU_S0 select the PU frequency as shown in Table 3.

GROUNDING AND POWER SUPPLY DECOUPLING

The CS5334, CS5335, and CS5360 require careful attention to power supply and grounding arrangements to optimize performance. Figure 4 shows the recommended power arrangements. The CS5334, CS5335, or CS5360 is positioned over the analog ground plane, near the digital/analog ground plane split, to minimize the distance that the clocks travel. The series resistors are present on the clock and data lines to reduce the effects of transient currents when driving a capacitive load in MASTER mode, and to reduce clock overshoot when applying external clocks to the ADC in SLAVE mode.

This layout technique is used to minimize digital noise and to insure proper power supply matching/sequencing. The decoupling capacitors are located as close to the ADC as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5VA	input	+5 Volts for analog section
+5VD	input	+5 Volts for digital section
±12V	input	±12 Volts for analog input
AGND	input	analog ground connection from power source
DGND	input	digital ground connection from power source
AINL	input	left channel differential/single ended analog input
AINR	input	right channel differential/single ended analog input
LRCK, SCLK	input/output	I/O for serial and left/right clocks
MCLK	output	master clock output
SDATA	output	serial data output
FRAME	output	framing signal output for PSL bits
coaxial output	output	CS8420A digital output via transformer
optical output	output	CS8420A digital output via optical transmitter

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
SMODE1, SMODE2	Selects master/slave operation for CS5334, CS5335, and CS5360 and I/O status of HDR2. SMODE1 and SMODE2 should always be set to the same position.	*MASTER SLAVE	Timing generation onboard. External clock generation, derived from MCLK.
TMODE1, TMODE2	Selects the functionality of the PSL bits. TMODE1 and TMODE2 should always be set to the same position.	HI RES *BARGRAPH	PSL bits display the input level PSL bits display the bargraph
HPSEL	Enables or disables the input highpass filter on the CS5334, CS5335, and CS5360	DEFEAT *ENABLE	Defeats highpass filter Enables highpass filter

Table 2. Jumper Selectable Options

Switch #	0 = closed, 1 = open	Comment
8, 7	MCLK_S1, MCLK_S0	Divides MCLK_5335 to generate MCLK_8402 for the CS8402A trnsmitter
	*0 0	Generates a 128x Fs clock when using a 256x Fs oscillator
	0 1	RESERVED
	1 0	Generates a 128x Fs clock when using a 384x Fs oscillator
	1 1	Generates a 128x Fs clock when using a 512x Fs oscillator
6, 5	*0 0	RESERVED
4, 3	DIF1, DIF0	Selects the digital interface format for the CS5334/35/60, and CS8402A
	*0 0	Configures the CS5334/35/60 for Format 0, and the CS8402A for Format 1
	0 1	Configures the CS5334/35/60 for Format 1, and the CS8402A for Format 1
	1 0	Configures the CS5334/35/60 for Format 2 (I^2S), and the CS8402A for Format 4 (I^2S)
	1 1	Places the CS5334/35/60 in power down mode
2, 1	PU_S1, PU_S0	Adjusts the frequency of the Peak Update signal for PSL bits
	*0 0	Updates the PSL bits at a frequency of LRCK/2^{11}
	0 1	Updates the PSL bits at a frequency of LRCK/2^{13}
	1 0	Updates the PSL bits at a frequency of LRCK/2^{15}
	1 1	Updates the PSL bits at a frequency of LRCK/2^{17}

Table 3. Switch Definitions

Switch #	0 = closed, 1 = open	Comment
6	$\overline{PRO}$ = 0	Consumer Mode (C0 = 0)
8, 5	FC1, FC0	C24, C25, C26, C27 - Sample Frequency
	0 0	0000 - 44.1 kHz
	*0 1	0100 - 48 kHz
	1 0	1100 - 32 kHz
	1 1	0000 - 44.1 kHz, CD Mode
7	$\overline{C3}$	C3, C4, C5 - Emphasis (1 of 8 bits)
	*1	000 - None
	0	100 - 50/15 µs
4	$\overline{C2}$	C2 - Copy/Copyright
	*1	0 - Copy Inhibited /Copyright Assered
	0	1 - Copy Permitted/Copyright Not Asserted
3	$\overline{C15}$	C15 - Generates Status
	*1	0 - Definition is based on category code
	0	1 - See CS8402A Data Sheet, App. A
1, 2	$\overline{C8}$, $\overline{C9}$	C8 - C14 - Category Code (2 of 7 bits)
	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - Compact Disk - CD
	*0 0	1100000 - Digital Audio Tape - DAT

* Default setting from factory

Table 4. CS8402A Switch Definitions - Consumer Mode

Switch #	0 = closed, 1 = open	Comment
6	$\overline{PRO}$ = 1	Pofessional Mode (C0 = 1)
8	CRE	Local Sample Address Counter and Reliability Flags
	0 1	Disabled Internally Generated
7, 4	$\overline{C6}$, $\overline{C7}$	C6, C7 - Sample Frequency
	0 0 0 1 1 0 1 1	00 - Not Indicated - Default to 48 kHz 01 - 48 kHz 10 - 44.1 kHz 11 - 32 kHz
5	$\overline{C1}$	C1 - Audio
	1 0	0 - Normal Audio 1 - Non-Audio
3	$\overline{C9}$	C8, C9, C10, C11 - Channel Mode (1 of 4 bits)
	1 0	0000 - Not Indicated - Default to 2-channel 0100 - Stereophonic
1, 2	EM1, EM0	C2, C3, C4 - Emphasis (2 of 3 bits)
	1 1 1 0 0 1 0 0	000 - Not Indicated - Default to none 100 - No emphasis 110 - 50/15 µs 111 - CCITTJ.17

Table 5. CS8402A Switch Definitions - Professional Mode

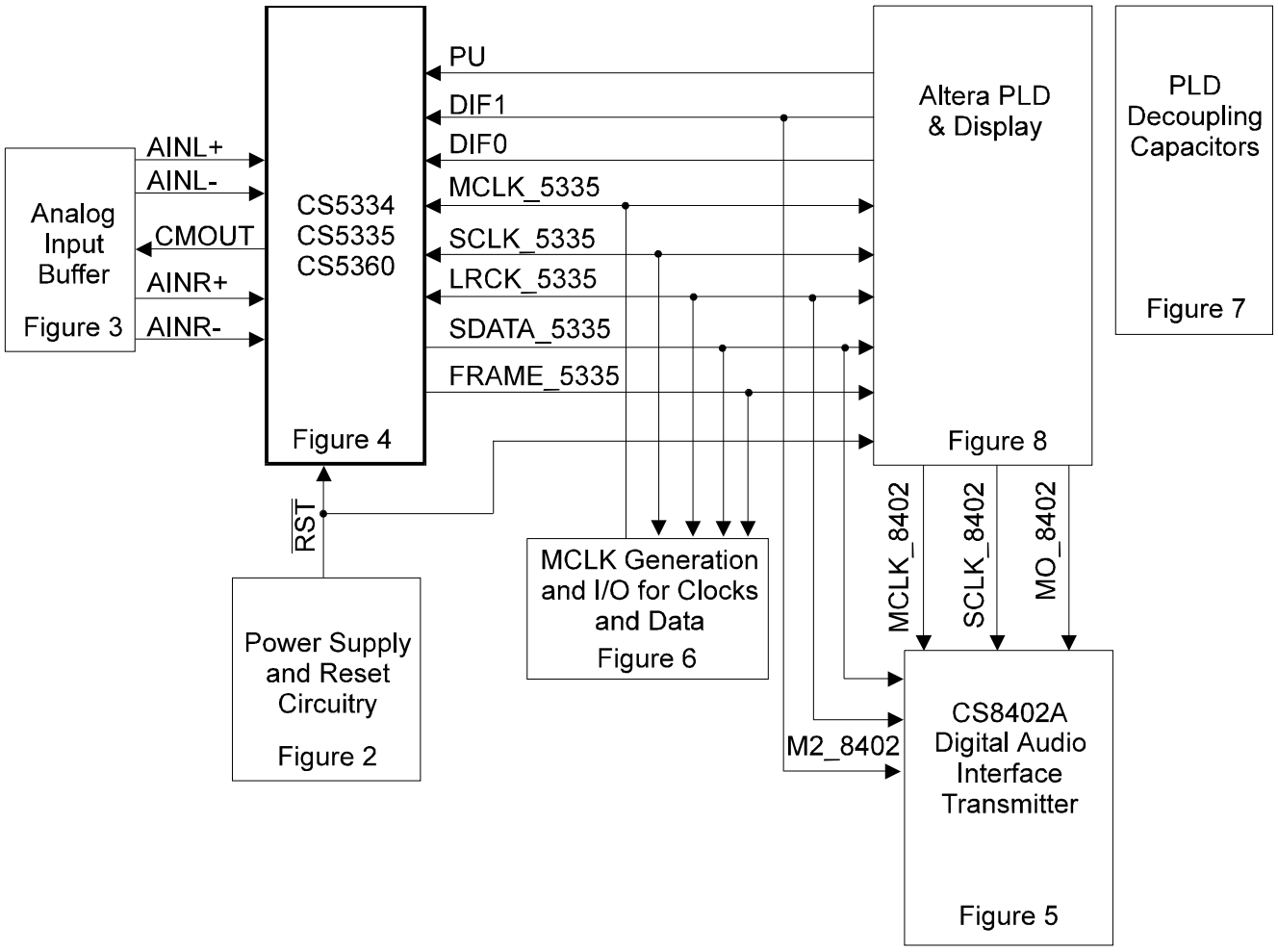


Figure 1. System Block Diagram and Signal Flow

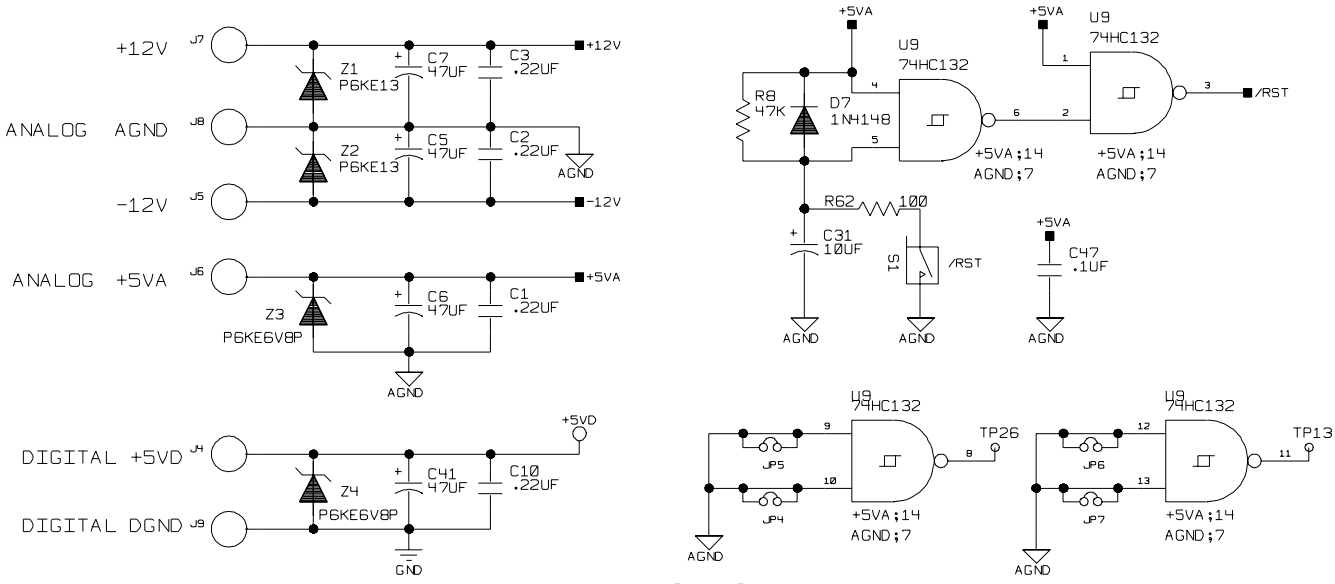
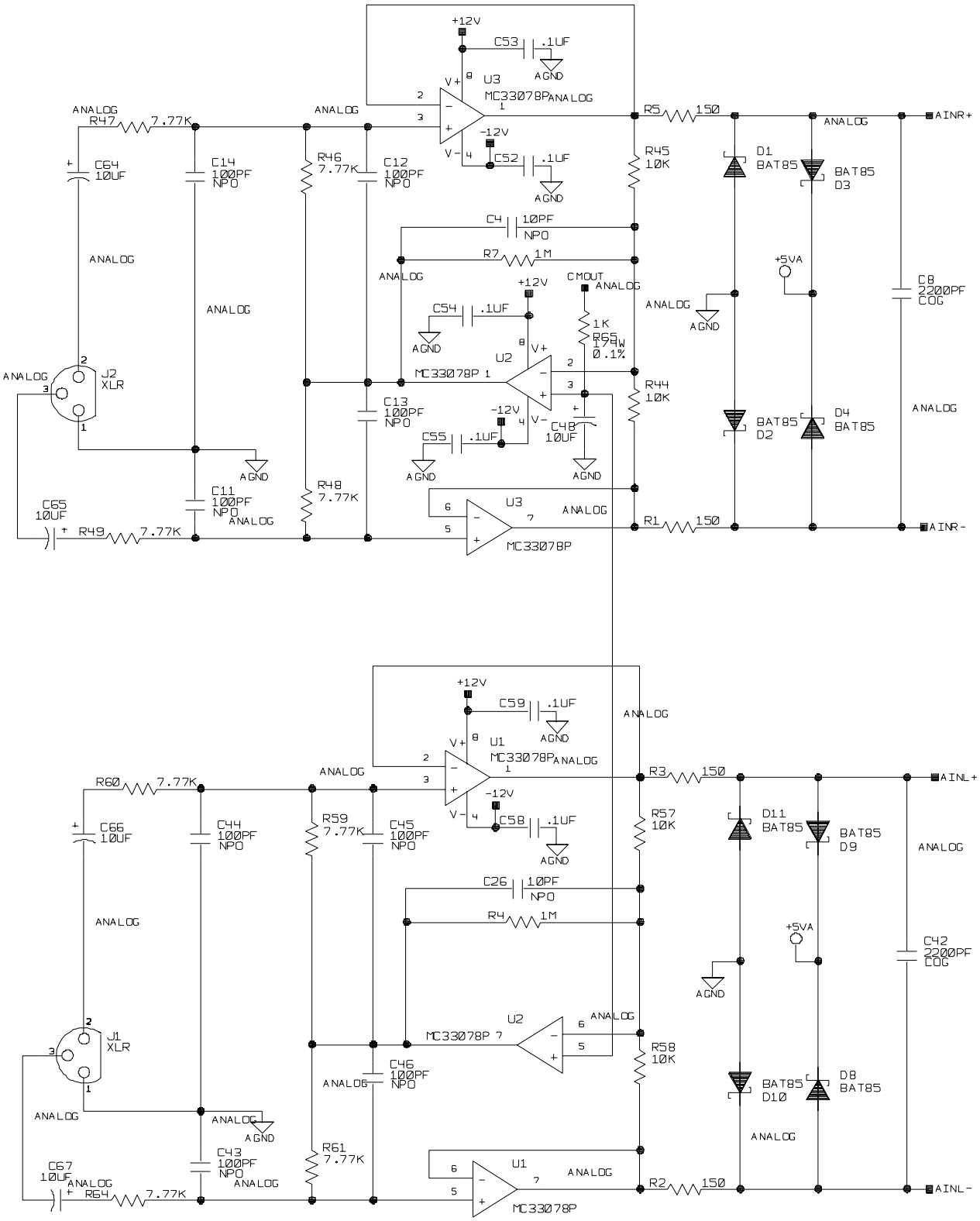


Figure 2. Power Supply and Reset Circuitry



NOTE: BAT85 Diodes are not installed on the Evalutation Board (see text)

Figure 3. Analog Input Buffer

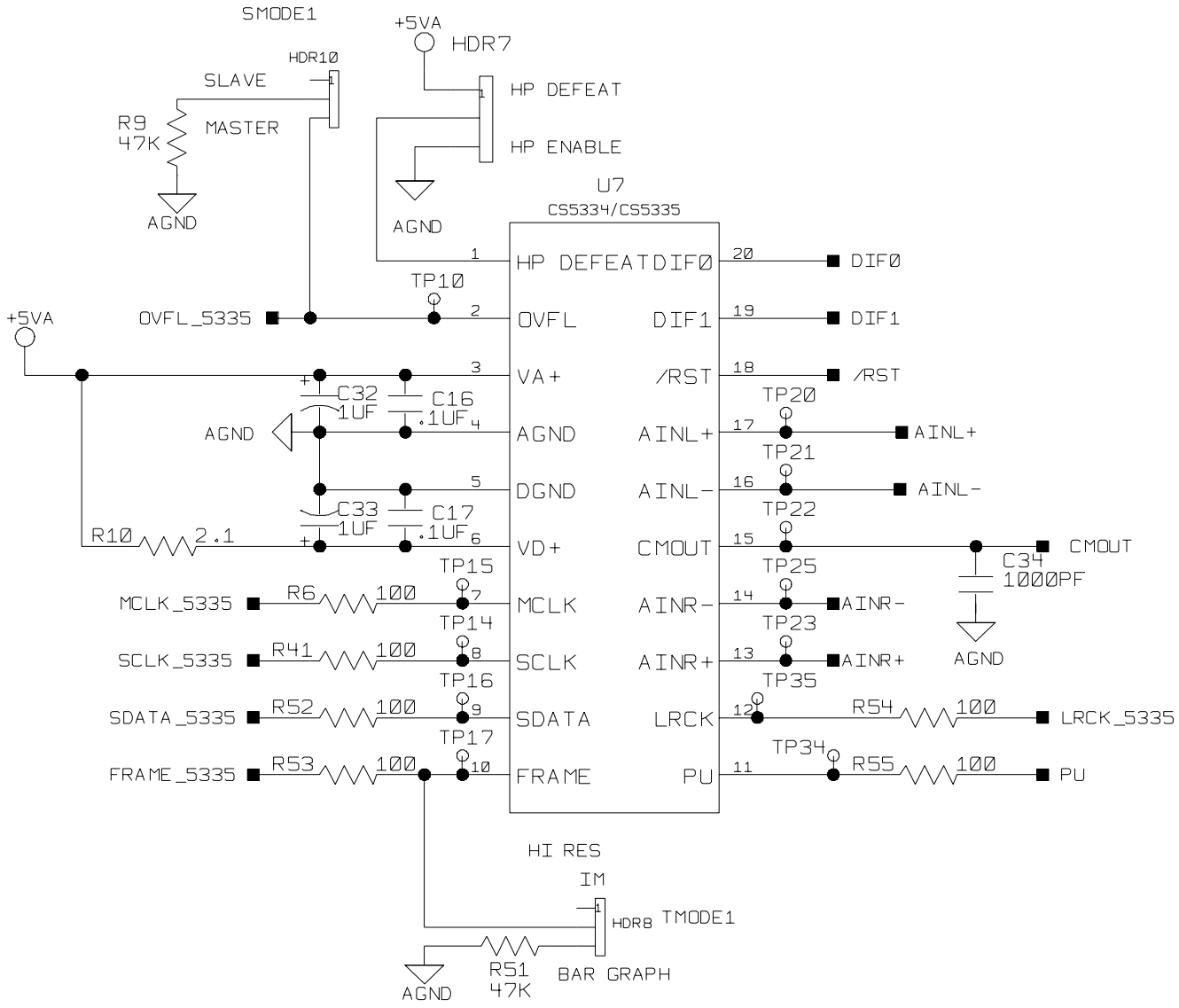


Figure 4. CS5334, CS5335, and CS5360 Connections

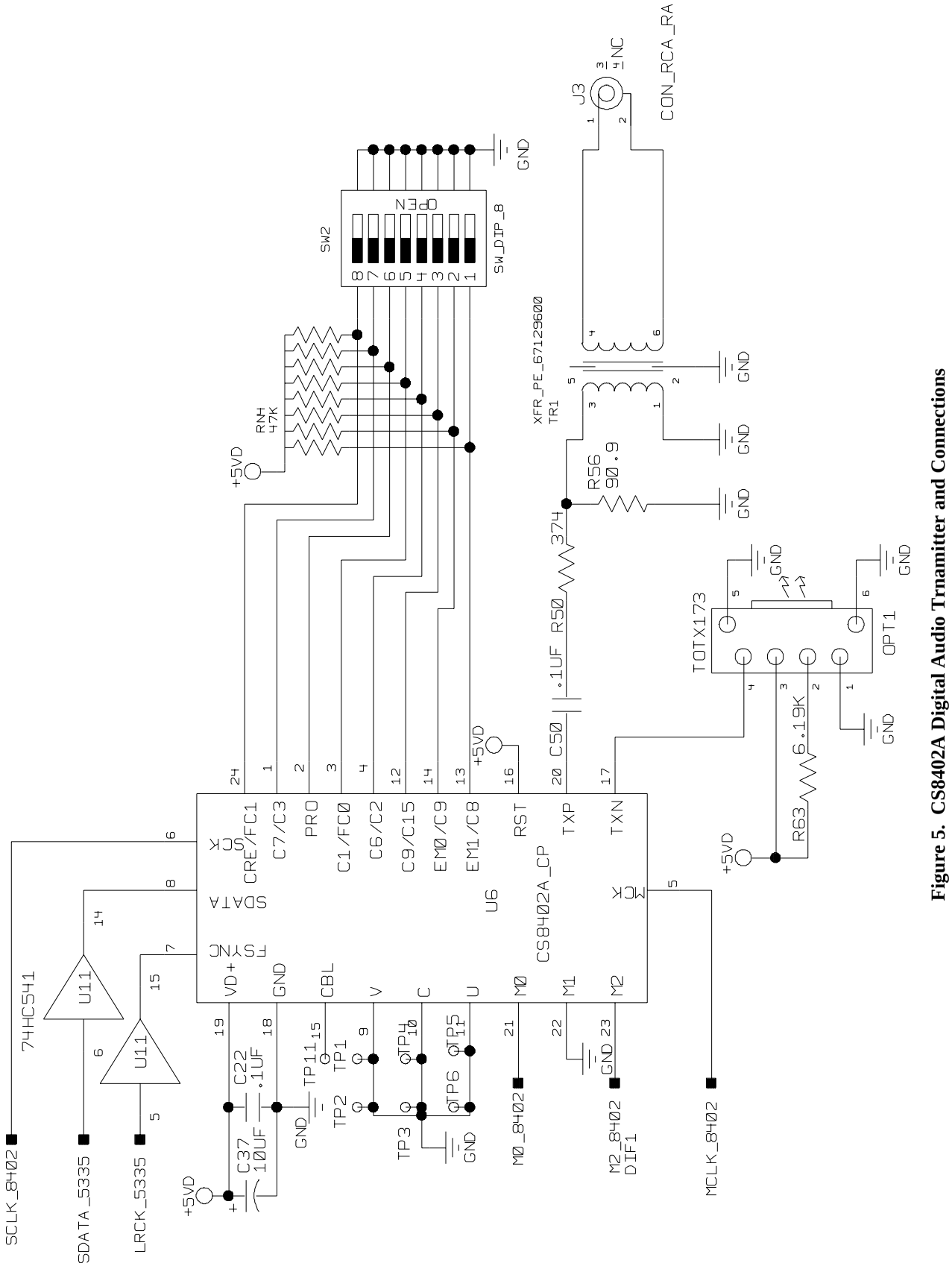


Figure 5. CS8402A Digital Audio Trnamitter and Connections

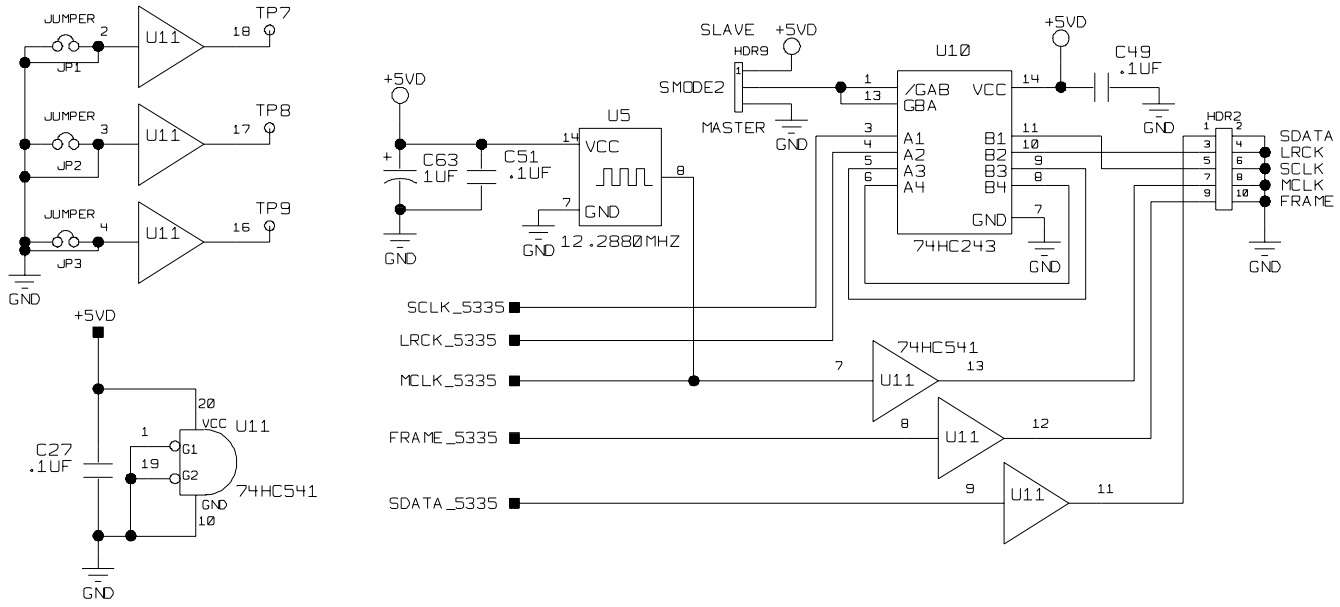


Figure 6. I/O Interface for Clocks and Data

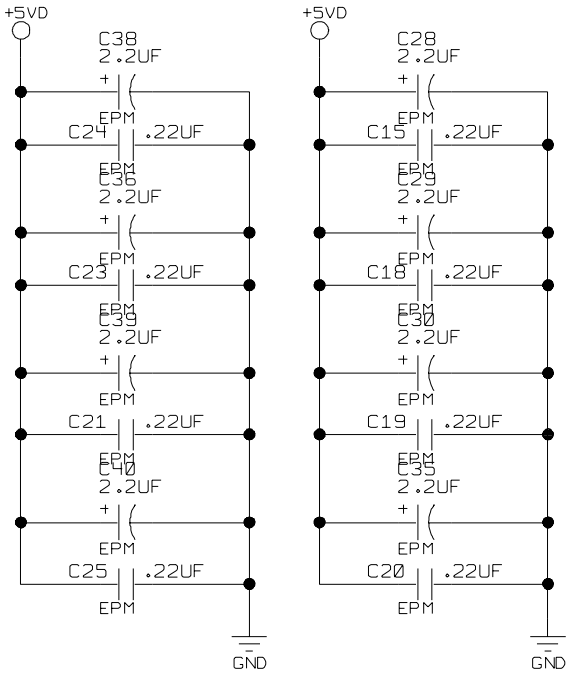


Figure 7. Decoupling Caps for PLD

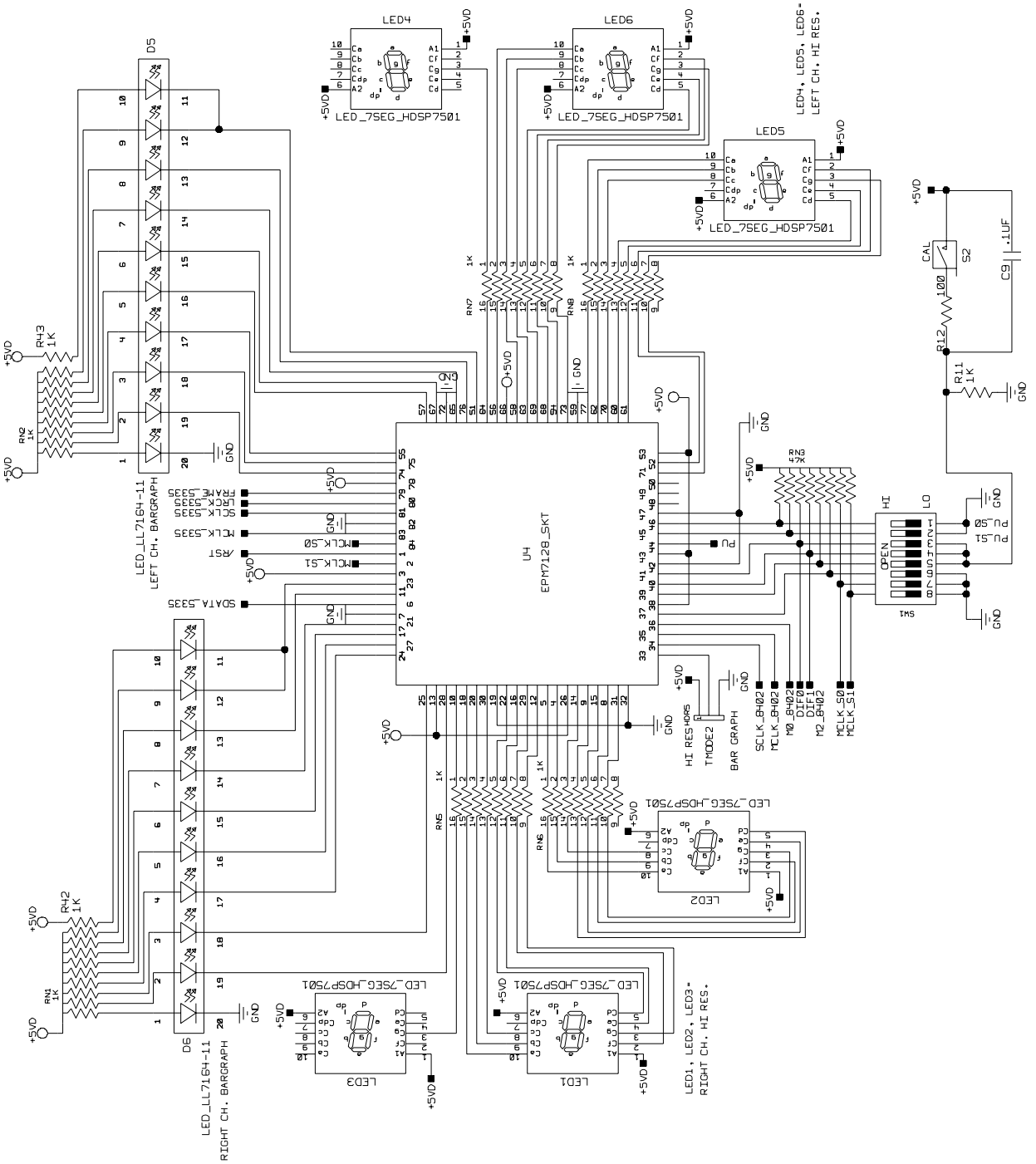


Figure 8. Altera PLD and Display LEDs

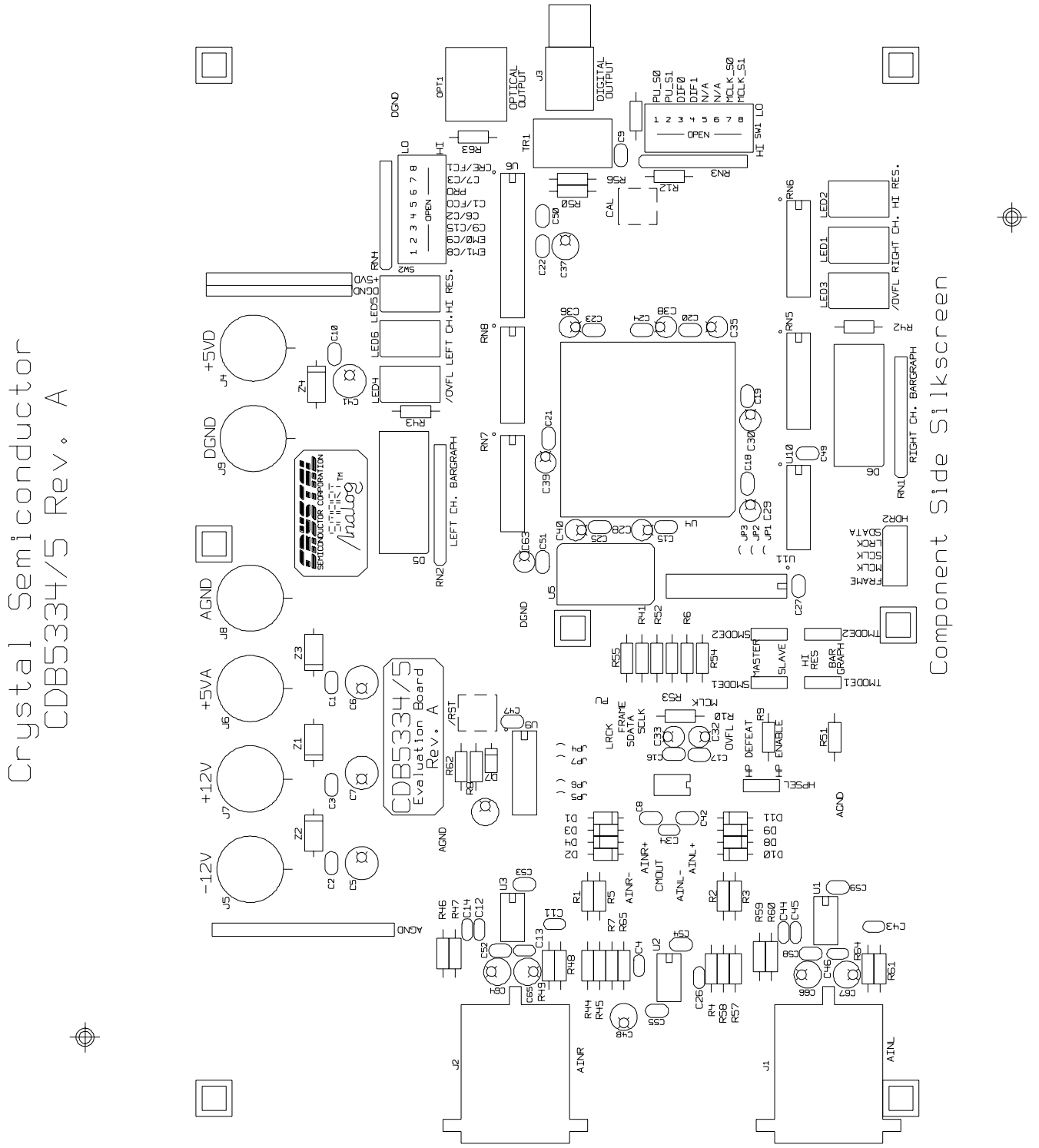


Figure 9. CDB5334/35/60 Component side (top)

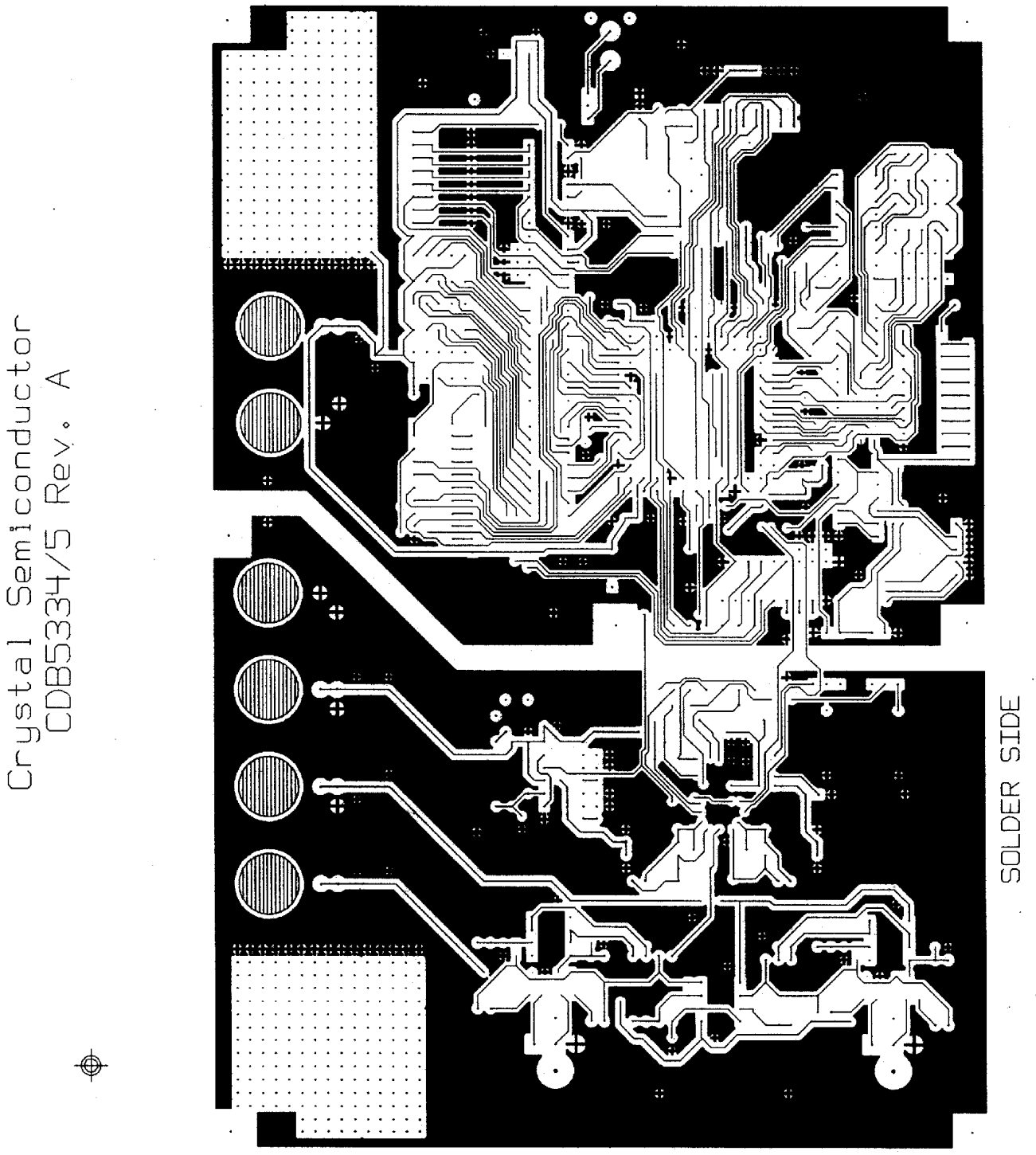


Figure 10. CDB5334/35/60 Component side (bottom)

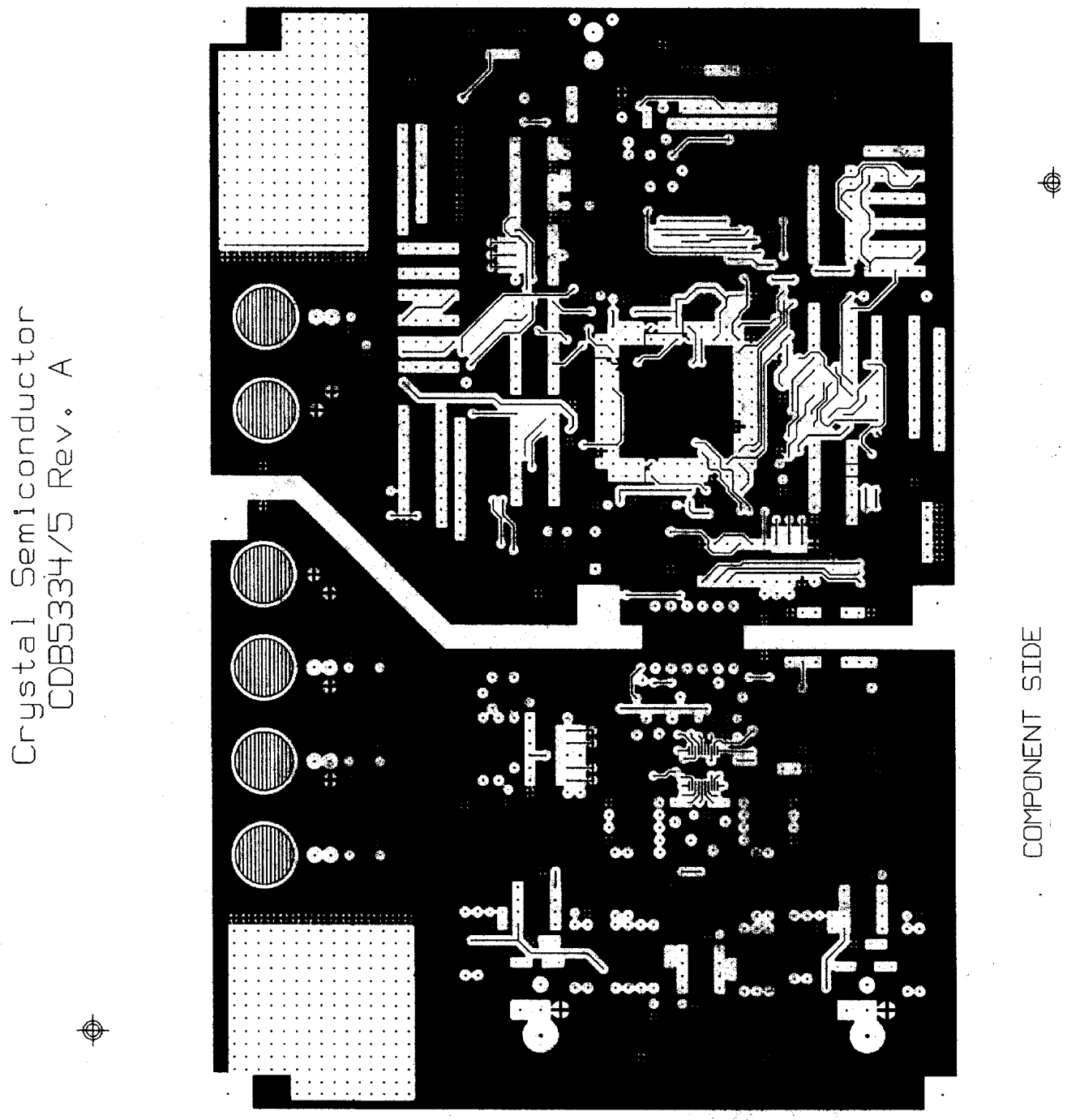


Figure 11. CDB5334/35/60 Solder side (bottom)

• Notes •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