Am29338

Byte Queue

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Queuing/Dequeuing**
  - Allows one to four bytes to be queued or dequeued in one cycle.
- **Four 32 x 9 RAMs**
  - Queues up to 128 bytes
- **Asynchronous/Synchronous Operation**
  - Supports system communication with different rates or with different data sizes.
- **Retransmit Capability**
  - Allows re-dequeuing of the block data repeatedly.
- **Horizontal Cascading**
  - Allows simultaneous output of 1 to 16 bytes in synchronous operation.
- **Parity Checking**
  - Provides data transmission on the inputs and outputs.

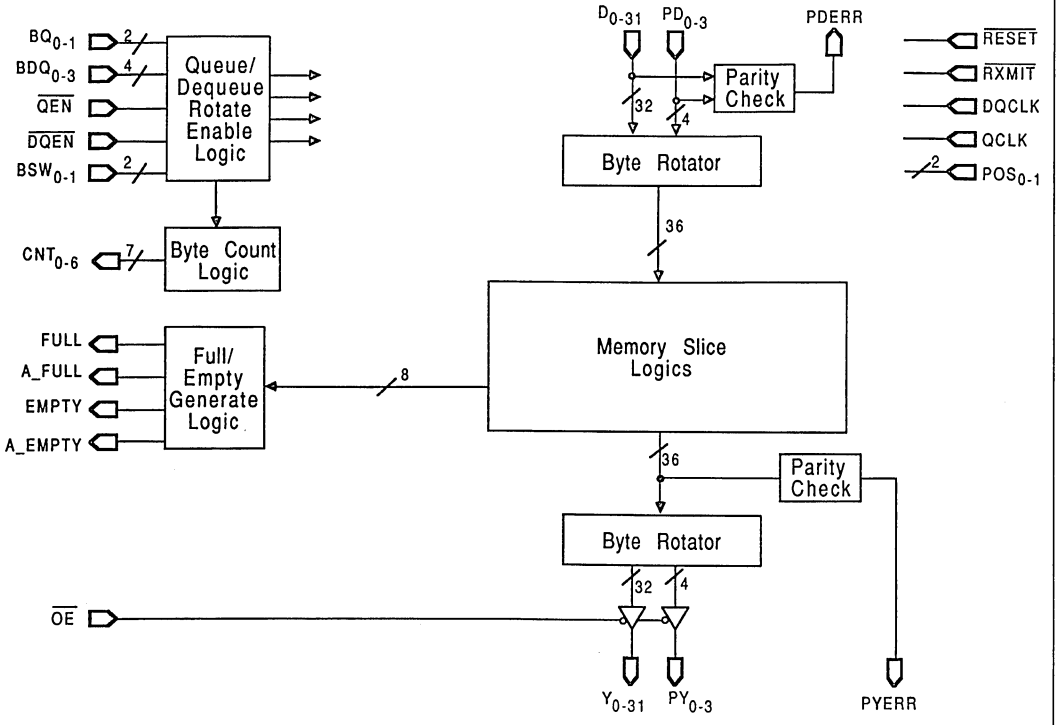
GENERAL DESCRIPTION

The Am29338 is a general-purpose byte queue that allows up to four bytes to be queued and up to four bytes to be dequeued in a single cycle. When four byte queues are cascaded horizontally, up to sixteen bytes can be dequeued in a single cycle.

With the retransmit capability, the part can repeatedly resend the block data stored in the queue without having to requeue it. This is useful for retransmitting a block of data upon receipt of an error in I/O applications or for loop-locking in instruction-prefetch applications, for example.

Along with the above features, the byte queue operates in synchronous or asynchronous mode. These features make the part useful as instruction-prefetch queue or as general-purpose FIFO buffer.

BLOCK DIAGRAM



BD006891

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication # 08815 Rev. A Amendment /0
Issue Date: January 1987

RELATED AMD PRODUCTS

Part No.	Description
Am2900 Family	4-Bit Microprocessor Slice Family
Am29C00 Family	CMOS 4-Bit Microprocessor Slice Family
Am29C101	CMOS 16-Bit Microprocessor Slice
Am29112	8-Bit Slice Microprogram Sequencer
Am29114	Real-Time Interrupt Controller
Am29116	16-Bit Bipolar Microprocessor
Am29116A	High-Speed 16-Bit Bipolar Microprocessor
Am29L116A	Low-Power 16-Bit Bipolar Microprocessor
Am29C116	CMOS 16-Bit Microprocessor
Am29C116-1	CMOS 16-Bit Microprocessor
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	Four-Port, Dual-Access Register File
Am29C334	CMOS Four-Port, Dual-Access Register File
Am29337	16-Bit Cascadable Bounds Checker

CONNECTION DIAGRAM
Bottom View

	A	B	C	D	E	F	G	H	J	K	L	M	N
1	Y16	Y17	$\overline{OE}$	Y21	TTL GND	PY3	Y27	Y28	TTL VCC	CNT2	TTL GND	CNT6	BDQ3
2	PY2	Y15	Y18	Y20	Y23	Y24	Y26	Y29	Y31	CNT1	CNT4	CNT5	BDQ2
3	TTL GND	Y14	Y13	Y19	Y22	ECL VCC	Y25	ECL GND	Y30	CNT0	CNT3	BDQ0	BDQ1
4	Y12	Y11	Y10								$\overline{DQEN}$	$\overline{RESET}$	$\overline{RXMIT}$
5	TTL VCC	Y9	Y8								$\overline{QEN}$	BSW1	DQCLK
6	Y7	PY1	TTL GND								QCLK	BQ1	BSW0
7	Y6	Y5	Y4								BQ0		D30
8	Y2	Y3	TTL VCC								D31	D28	D29
9	TTL GND	Y1	Y0								D27	D25	D26
10	PY0	PYERR	PDERR								D24	PD3	D23
11	TTL VCC	A_FULL	PD0	D2	ECL VCC	D6	D7	D12	ECL GND	D15	D22	D20	D21
12	FULL	POS1	POS0	D1	ECL VCC	D3	D8	D9	ECL GND	D14	PD2	D19	D18
13	A_EMPTY	EMPTY	D5	D0	ECL VCC	D4	PD1	D11	ECL GND	D13	D10	D16	D17

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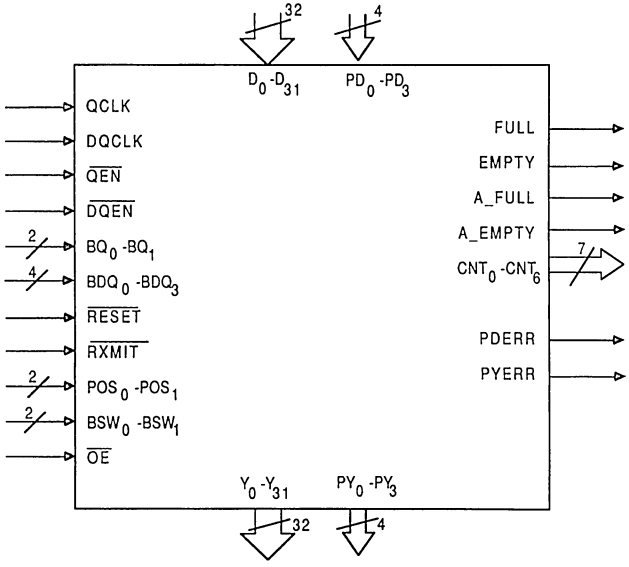
PIN DESIGNATIONS
(Sorted by Pin Number)

PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
1	**A1**	Y_{16}	115	**C5**	Y_8	40	**G11**	D_7	27	**L10**	D_{24}
120	**A2**	PY_2	113	**C6**	TTL GND	36	**G12**	D_8	88	**L11**	D_{22}
59	**A3**	TTL GND	52	**C7**	Y_4	96	**G13**	PD_1	32	**L12**	PD_2
58	**A4**	Y_{12}	53	**C8**	TTL V_{CC}	69	**H1**	Y_{28}	35	**L13**	D_{10}
56	**A5**	TTL V_{CC}	109	**C9**	Y_0	10	**H2**	Y_{29}	75	**M1**	CNT_6
114	**A6**	Y_7	48	**C10**	PDERR	68	**H3**	ECL GND	15	**M2**	CNT_5
54	**A7**	Y_6	44	**C11**	PD_0	34	**H11**	D_{12}	77	**M3**	BDQ_0
51	**A8**	Y_2	104	**C12**	POS_0	95	**H12**	D_9	78	**M4**	$\overline{RESET}$
50	**A9**	TTL GND	41	**C13**	D_5	94	**H13**	D_{11}	80	**M5**	BSW_1
49	**A10**	PY_0	4	**D1**	Y_{21}	11	**J1**	TTL V_{CC}	81	**M6**	BQ_1
47	**A11**	TTL V_{CC}	63	**D2**	Y_{20}	71	**J2**	Y_{31}	82	**M7**	NC
106	**A12**	FULL	3	**D3**	Y_{19}	70	**J3**	Y_{30}	25	**M8**	D_{28}
46	**A13**	A_EMPTY	102	**D11**	D_2	38	**J11**	ECL GND	86	**M9**	D_{25}
61	**B1**	Y_{17}	43	**D12**	D_1	38	**J12**	ECL GND	87	**M10**	PD_3
60	**B2**	Y_{15}	103	**D13**	D_0	38	**J13**	ECL GND	89	**M11**	D_{20}
119	**B3**	Y_{14}	5	**E1**	TTL GND	13	**K1**	CNT_2	30	**M12**	D_{19}
117	**B4**	Y_{11}	65	**E2**	Y_{23}	72	**K2**	CNT_1	91	**M13**	D_{16}
116	**B5**	Y_9	64	**E3**	Y_{22}	12	**K3**	CNT_0	16	**N1**	BDQ_3
55	**B6**	PY_1	98	**E11**	ECL V_{CC}	92	**K11**	D_{15}	76	**N2**	BDQ_2
112	**B7**	Y_5	98	**E12**	ECL V_{CC}	33	**K12**	D_{14}	17	**N3**	BDQ_1
111	**B8**	Y_3	98	**E13**	ECL V_{CC}	93	**K13**	D_{13}	19	**N4**	$\overline{RXMIT}$
110	**B9**	Y_1	6	**F1**	PY_3	14	**L1**	TTL GND	20	**N5**	DQCLK
108	**B10**	PYERR	66	**F2**	Y_{24}	74	**L2**	CNT_4	21	**N6**	BSW_0
107	**B11**	A_FULL	8	**F3**	ECL V_{CC}	73	**L3**	CNT_3	24	**N7**	D_{30}
45	**B12**	POS_1	100	**F11**	D_6	18	**L4**	$\overline{DQEN}$	84	**N8**	D_{29}
105	**B13**	EMPTY	42	**F12**	D_3	79	**L5**	$\overline{QEN}$	26	**N9**	D_{26}
2	**C1**	$\overline{OE}$	101	**F13**	D_4	23	**L6**	QCLK	28	**N10**	D_{23}
62	**C2**	Y_{18}	9	**G1**	Y_{27}	22	**L7**	BQ_0	29	**N11**	D_{21}
118	**C3**	Y_{13}	67	**G2**	Y_{26}	83	**L8**	D_{31}	90	**N12**	D_{18}
57	**C4**	Y_{10}	7	**G3**	Y_{25}	85	**L9**	D_{27}	31	**N13**	D_{17}

PIN DESIGNATIONS
(Sorted by Pin Name)

PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME	PAD NO.	PIN NO.	PIN NAME
82	M7	**NC**	34	H11	**D_{12}**	105	B13	**EMPTY**	51	A8	**Y_2**
46	A13	**A_EMPTY**	93	K13	**D_{13}**	106	A12	**FULL**	111	B8	**Y_3**
107	B11	**A_FULL**	33	K12	**D_{14}**	2	C1	**$\overline{OE}$**	52	C7	**Y_4**
77	M3	**BDQ_0**	92	K11	**D_{15}**	44	C11	**PD_0**	112	B7	**Y_5**
17	N3	**BDQ_1**	91	M13	**D_{16}**	96	G13	**PD_1**	54	A7	**Y_6**
76	N2	**BDQ_2**	31	N13	**D_{17}**	32	L12	**PD_2**	114	A6	**Y_7**
16	N1	**BDQ_3**	90	N12	**D_{18}**	87	M10	**PD_3**	115	C5	**Y_8**
22	L7	**BQ_0**	30	M12	**D_{19}**	48	C10	**PDERR**	116	B5	**Y_9**
81	M6	**BQ_1**	89	M11	**D_{20}**	104	C12	**POS_0**	57	C4	**Y_{10}**
21	N6	**BSW_0**	29	N11	**D_{21}**	45	B12	**POS_1**	117	B4	**Y_{11}**
80	M5	**BSW_1**	88	L11	**D_{22}**	49	A10	**PY_0**	58	A4	**Y_{12}**
12	K3	**CNT_0**	28	N10	**D_{23}**	55	B6	**PY_1**	118	C3	**Y_{13}**
72	K2	**CNT_1**	27	L10	**D_{24}**	120	A2	**PY_2**	119	B3	**Y_{14}**
13	K1	**CNT_2**	86	M9	**D_{25}**	6	F1	**PY_3**	60	B2	**Y_{15}**
73	L3	**CNT_3**	26	N9	**D_{26}**	108	B10	**PYERR**	1	A1	**Y_{16}**
74	L2	**CNT_4**	85	L9	**D_{27}**	23	L6	**QCLK**	61	B1	**Y_{17}**
15	M2	**CNT_5**	25	M8	**D_{28}**	79	L5	**$\overline{QEN}$**	62	C2	**Y_{18}**
75	M1	**CNT_6**	84	N8	**D_{29}**	78	M4	**$\overline{RESET}$**	3	D3	**Y_{19}**
103	D13	**D_0**	24	N7	**D_{30}**	19	N4	**$\overline{RXMIT}$**	63	D2	**Y_{20}**
43	D12	**D_1**	83	L8	**D_{31}**	113	C6	**TTL GND**	4	D1	**Y_{21}**
102	D11	**D_2**	20	N5	**DQCLK**	14	L1	**TTL GND**	64	E3	**Y_{22}**
42	F12	**D_3**	18	L4	**$\overline{DQEN}$**	59	A3	**TTL GND**	65	E2	**Y_{23}**
101	F13	**D_4**	38	J11	**ECL GND**	5	E1	**TTL GND**	66	F2	**Y_{24}**
41	C13	**D_5**	68	H3	**ECL GND**	50	A9	**TTL GND**	7	G3	**Y_{25}**
100	F11	**D_6**	38	J13	**ECL GND**	56	A5	**TTL V_{CC}**	67	G2	**Y_{26}**
40	G11	**D_7**	38	J12	**ECL GND**	53	C8	**TTL V_{CC}**	9	G1	**Y_{27}**
36	G12	**D_8**	98	E11	**ECL V_{CC}**	47	A11	**TTL V_{CC}**	69	H1	**Y_{28}**
95	H12	**D_9**	98	E12	**ECL V_{CC}**	11	J1	**TTL V_{CC}**	10	H2	**Y_{29}**
35	L13	**D_{10}**	8	F3	**ECL V_{CC}**	109	C9	**Y_0**	70	J3	**Y_{30}**
94	H13	**D_{11}**	98	E13	**ECL V_{CC}**	110	B9	**Y_1**	71	J2	**Y_{31}**

LOGIC SYMBOL



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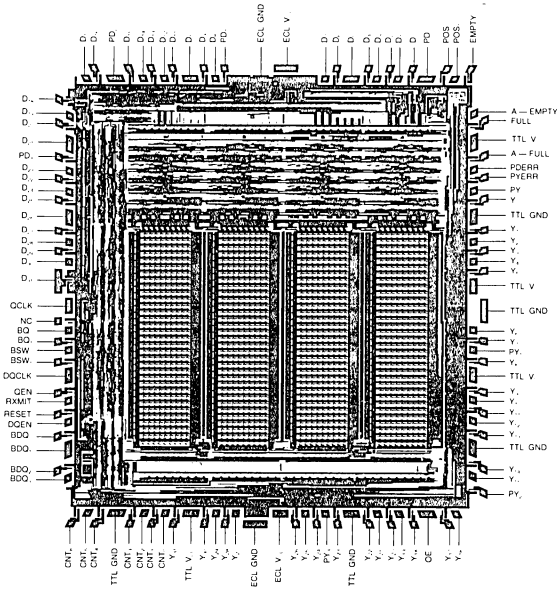
METALLIZATION AND PAD LAYOUT

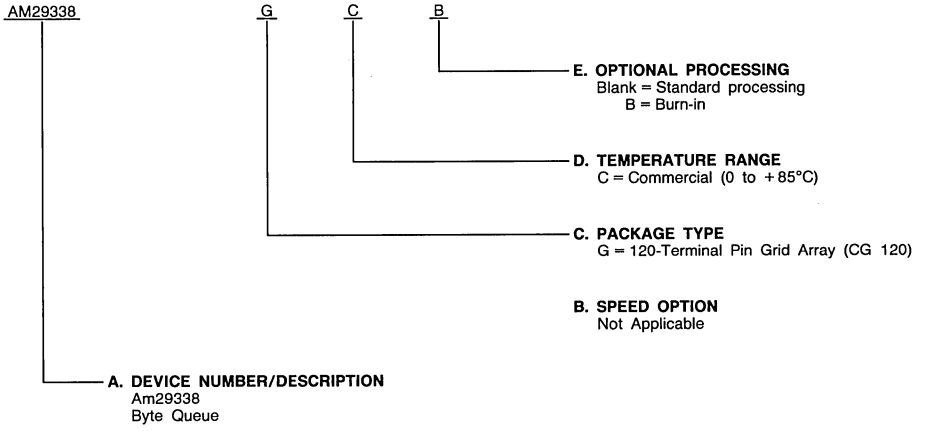


Die Size: 270 x 290 mils^2
Gate Count: 9000

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM29338	GC, GCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

A_EMPTY Almost Empty (Output; Active HIGH)
Indicates that there are less than four bytes of data in the queue. It is used in either synchronous or asynchronous operation.

A_FULL Almost Full (Output; Active HIGH)
Indicates that there are less than four bytes of space remaining. It is used in either synchronous or asynchronous operation.

$BDQ_0 - BDQ_3$ Bytes Dequeued (Input)
Selects the number of bytes to be dequeued (see Table 2). The byte queue must operate synchronously to be able to dequeue more than four bytes in a single cycle.

$BQ_0 - BQ_1$ Bytes Queued (Input)
Selects the number of bytes to be queued (see Table 1).

$BSW_0 - BSW_1$ Byte Swap (Input)
Allows the bytes on the output to be swapped (see Table 3).

$CNT_0 - CNT_6$ Byte Count (Output)
Gives the current number of bytes in the queue. These are used only in synchronous operation.

$D_0 - D_{31}$ Data Input (Input)
Data inputs to be queued.

DQCLK Dequeue Clock (Input)
Dequeues the number of bytes set up on the Y bus. A LOW-to-HIGH transition on this input adjusts the internal dequeue pointer by the number set up on the BDQ lines.

$\overline{DQEN}$ $\overline{Dequeue\ Enable}$ (Input; Active LOW)
While $\overline{DQEN}$ is LOW, dequeuing is performed normally. When $\overline{DQEN}$ is HIGH, DQCLK is disabled.

EMPTY Empty (Output; Active HIGH)
Indicates that the queue is empty. It is used in either synchronous or asynchronous operation.

FULL Full (Output; Active HIGH)
Indicates that the queue is full. It is used in either synchronous or asynchronous operation.

$\overline{OE}$ $\overline{Output\ Enable}$ (Input; Active LOW)
When $\overline{OE}$ is LOW, the four bytes following the current dequeue pointer and the corresponding parity bits are on Y and PY outputs. When $\overline{OE}$ is HIGH, Y and PY outputs are three stated.

$PD_0 - PD_3$ Data Input Parity (Input)
The input parity bits for the corresponding byte on the D inputs. Only the bytes to be queued and the corresponding PD lines are checked for possible parity error. The byte queue has the even parity.

PDERR Data Input Parity Error (Output; Active HIGH)
If any of the bytes to be queued have a parity error, PDERR is asserted.

$POS_0 - POS_1$ Position (Input)
These inputs are used to program the location of each byte queue in horizontally cascaded system upon $\overline{RESET}$ (see Table 4).

$PY_0 - PY_3$ Output Data Parity (Output; Three State)
The output parity bits for Y outputs. When $\overline{OE}$ is HIGH, the parity bits of the four bytes following the dequeue pointer appear on these outputs. The byte queue has the even parity.

PYERR Y Output Parity Error (Output; Active HIGH)
If any of the bytes on the output has a parity error, PYERR is asserted.

QCLK Queue Clock (Input)
When QCLK is LOW, the number of bytes set up on the BQ lines are written into the next free space in the queue from the data set up on the D inputs. On a LOW-to-HIGH transition of this input, the internal queue pointer is updated. If $\overline{QEN}$ is HIGH, QCLK has no effect.

$\overline{QEN}$ $\overline{Queue\ Enable}$ (Input; Active LOW)
When $\overline{QEN}$ is LOW, queuing is performed normally. When $\overline{QEN}$ is HIGH, QCLK is disabled.

$\overline{RESET}$ $\overline{Reset}$ (Input; Active LOW)
When $\overline{RESET}$ is LOW, both the internal queue pointer and the internal dequeue pointer are reset to the first RAM location and both EMPTY and A_EMPTY are asserted.

$\overline{RXMIT}$ $\overline{Retransmit}$ (Input; Active LOW)
When $\overline{RXMIT}$ is LOW, the internal dequeue pointer is reset to the first RAM location while the internal queue pointer remains unchanged. This allows the data contained between the current queue pointer and the first RAM location to be retransmitted.

$Y_0 - Y_{31}$ Data Output (Output; Three State)
The four bytes following the current dequeue pointer appear on these outputs when $\overline{OE}$ is LOW. When $\overline{OE}$ is HIGH, they are three stated.

FUNCTIONAL DESCRIPTION

Architecture

The Am29338 is a 32-bit high-performance byte queue that stores up to 128 bytes in the internal RAM slices and queues or dequeues up to four bytes in a single cycle. The byte queue is divided into five functional blocks: 1) four memory-slice logics, 2) byte rotators for input and output buses, 3) rotate-enable logic, 4) byte-count logic, and 5) full/empty-generate logic. The byte-oriented parity checking is provided on both the D-input bus and the Y-output bus. Figure 1 shows a detailed block diagram of the byte queue.

Memory-Slice Logic

Figure 2 shows a detail of the memory-slice logic. It consists of a 32 x 9 RAM, queue and dequeue pointers, adders for the pointers, and a full/empty detector. The RAM has independent 9-bit read and write ports. Both ports are accessible simultaneously if different RAM locations are operated on. A parity bit is stored along with its corresponding byte into the RAM.

The queue and dequeue pointers point to the next location available for dequeuing. The next locations are produced by the internal adders with BQ_{0-1} or BDQ_{0-3} and the current pointer values. When $\overline{RESET}$ is asserted, both pointers are set to zero and the RAM is flushed. These pointers are also used to indicate that the RAM is either empty or full for each memory slice. The slice-empty or slice-full signal is used to combinationally form FULL, A_FULL, EMPTY, and A_EMPTY signals.

Byte Rotator

There are two byte rotators in the byte queue. Each accepts 36-bit wide data and performs rotation of bytes according to the 2-bit rotate values fed from the rotate-enable logic. The

input byte rotator realigns and stores the bytes to be queued into the next free slice location. The output byte rotator realigns the bytes to be dequeued to the least significant byte of the Y-output bus.

Rotate-Enable Logic

The queue and dequeue rotate-enable logic keeps track of which slice holds the first byte of the next queue/dequeue operation. A modulo-4 counter is used to rotate the data in operation and enables the correct slices by the number of bytes specified by either BQ_{0-1} or BDQ_{0-3}.

The queue rotate-enable logic also performs byte and/or word swaps on the incoming data. The input bytes are swapped in one of four ways, according to Table 3, with BSW_{0-1} and the current modulo-4 byte count through the input byte rotator.

Byte-Count Logic

This logic consists of a queue count register and a dequeue count register. The registers are incremented during a queue/dequeue operation by the number of bytes in the operation. The combinational subtract logic outside of these registers determines the number of bytes stored in the byte queue.

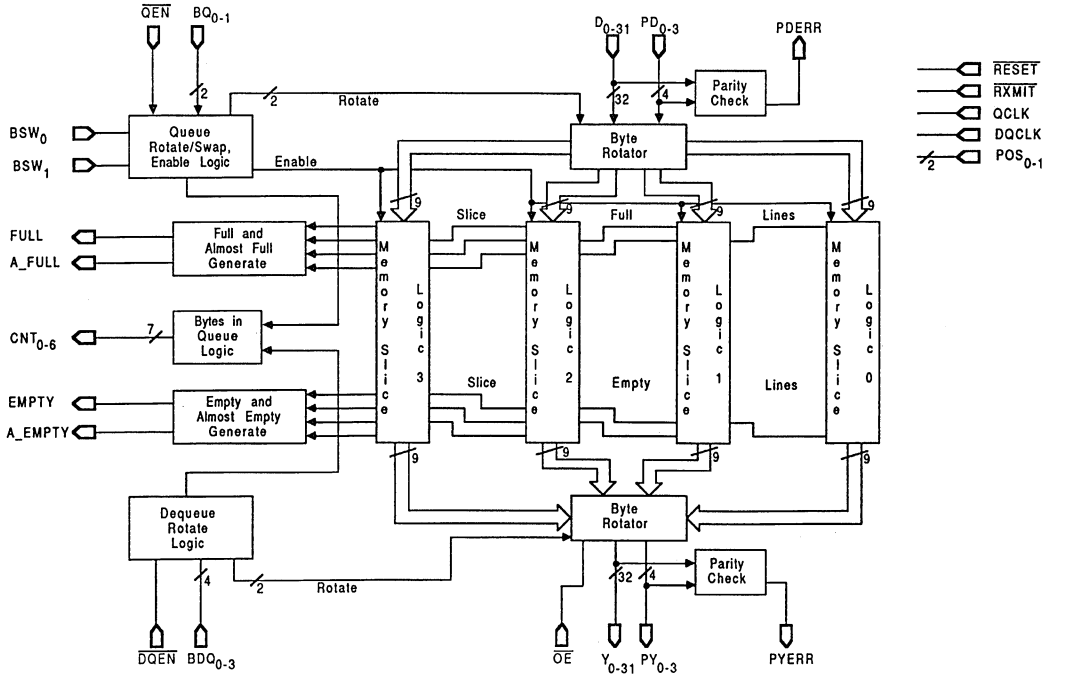


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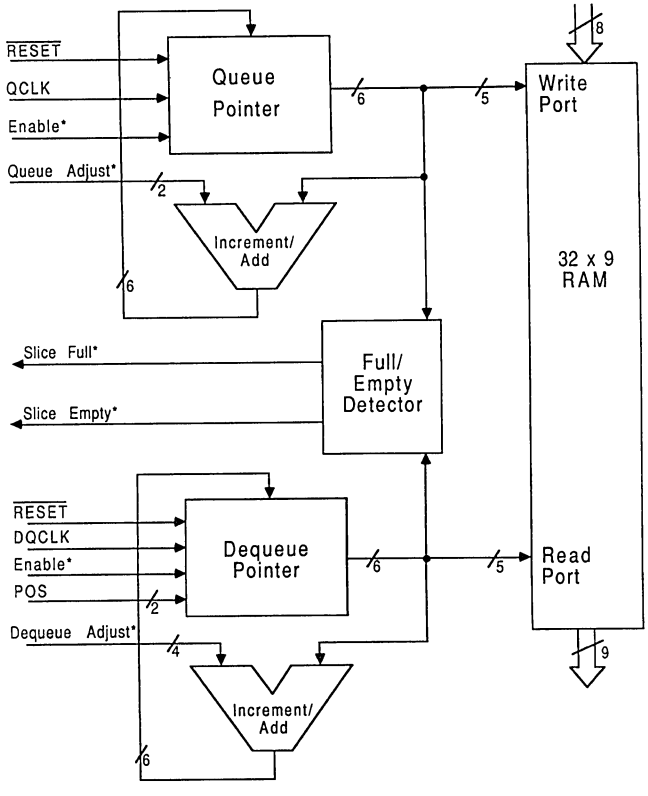
Figure 1. Am29338 Byte Queue Detailed Block Diagram



*Internally generated inputs.

Figure 2. Memory and Slice Logic

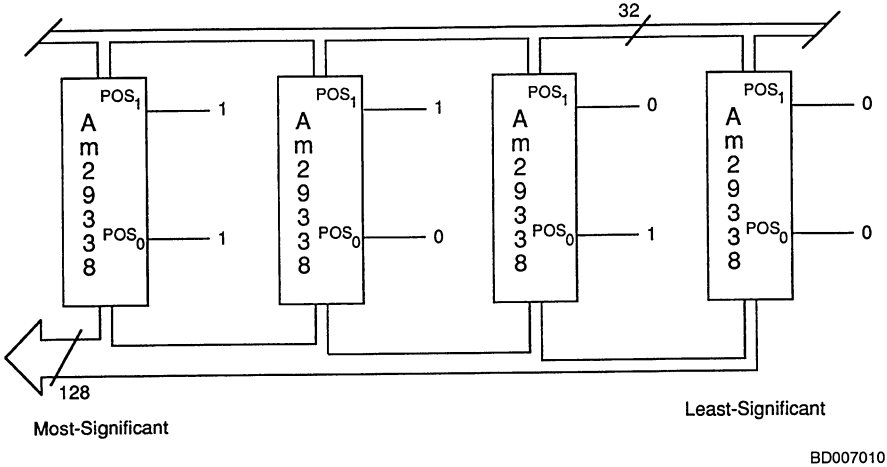


Figure 3. Position Line Values in Horizontally Cascaded System

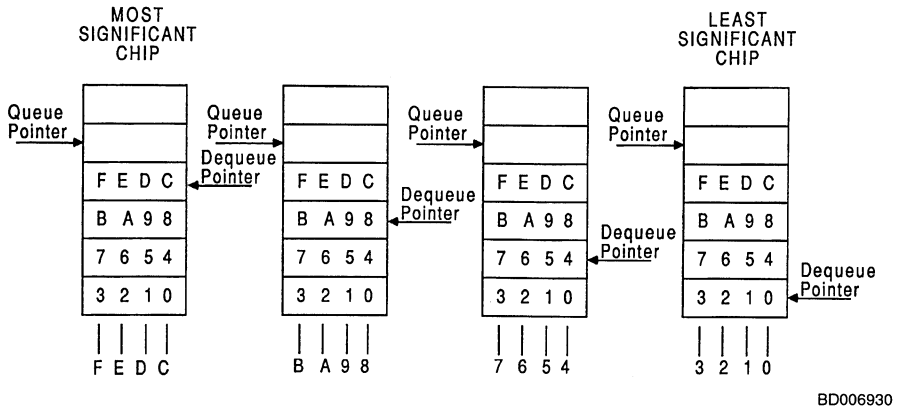


Figure 4. An Example of Horizontal Cascading

TABLE 1. SELECTING THE NUMBER OF BYTES TO BE QUEUED

BQ_1	BQ_0	Bytes To Be Queued
L	H	1
H	L	2
H	H	3
L	L	4

Key: L = LOW
H = HIGH

TABLE 2. SELECTING THE NUMBER OF BYTES TO BE DEQUEUED

BDQ_3	BDQ_2	BDQ_1	BDQ_0	Bytes To Be Dequeued
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5*
L	H	H	L	6*
L	H	H	H	7*
H	L	L	L	8*
H	L	L	H	9*
H	L	H	L	10*
H	L	H	H	11*
H	H	L	L	12*
H	H	L	H	13*
H	H	H	L	14*
H	H	H	H	15*
L	L	L	L	16*

Key: L = LOW
H = HIGH

* This is possible when four of the byte queues are cascaded together. The byte queue must be operated synchronously to select more than four bytes for dequeuing.

TABLE 3. ENCODING OF BSW INPUTS

Inputs		Outputs			
BSW_1	BSW_0				
L	L	A	B	C	D
L	H	B	A	D	C
H	L	C	D	A	B
H	H	D	C	B	A

Key: L = LOW
H = HIGH

Note: The assumption is made that the 32-bit data "A B C D" appears on the input bus.

TABLE 4. LOCATION IDENTIFICATION FOR HORIZONTAL CASCADING

POS_1	POS_0	Location
L	L	0
L	H	1
H	L	2
H	H	3

Key: L = LOW
H = HIGH

Note: "0" stands for the least significant chip and "3" the most significant chip.

Operational Modes

Synchronous Mode

Both synchronous and asynchronous operations are available for the byte queue. During synchronous operation, both QCLK and DQCLK must be asserted on the edge of a common clock within certain skew limits. The following signals can be used as valid status outputs for this mode: FULL, A_FULL, EMPTY, A_EMPTY, and CNT_{0-6}. Refer to the applications section for an example.

Asynchronous Mode

During asynchronous operation, QCLK and DQCLK clocks may be different. It is possible to execute queue and dequeue operations simultaneously if different locations are accessed. In this mode, CNT outputs are not guaranteed as valid and horizontal cascading is not possible. Refer to the applications section for an example.

Horizontal Cascading

In synchronous operation, four byte queues can be horizontally cascaded together. In this case, each of the four byte queues hold the same data and up to sixteen bytes may be dequeued in a single cycle, as shown in Table 2, and Figures 3 and 4. Each part has to be programmed with its position by the POS inputs, as shown in Table 4. In a normal operation, the internal dequeue pointer of each part is displaced according to the POS inputs. When $\overline{RESET}$ or $\overline{RXMIT}$ is asserted, the dequeue pointers are offset by the value programmed on the POS inputs.

Horizontal cascading is useful in instruction buffers designed for systems with large, variable instructions that can span many bytes.

APPLICATIONS

Using Am29338 as an Instruction-Prefetch Queue

Figure 5 shows the Am29338 used as an instruction-prefetch queue. Sequential 32-bit memory locations are fetched by the Instruction Fetch Unit (IFU) and are queued up in the byte queue. When the central processor needs the next instruction, it looks at the next four bytes from the byte queue. The central processor then determines the instruction length from the opcode and updates the dequeue pointer in the byte queue by setting up the instruction length on the BDQ lines and asserting DQCLK. When a jump occurs, the IFU flushes the queue by asserting the $\overline{RESET}$ input and begins from the new address. For this application, the byte queue must be in synchronous mode.

Using the $\overline{RXMIT}$ input, the byte queue can resend the block data through dequeuing rather than having to requeue it. This is useful for locking the loops into the byte queue and allows the processor to run faster than if it had to refetch instructions from memory or cache. Figure 6 illustrates how a loop can execute directly out of the byte queue.

Using Am29338 as a Hardware Mailbox in Multiprocessing System

A mailbox is a communication device between loosely coupled processes in a multi-programming system. Messages from one process to another are queued in the mailbox on a first-in, first-out (FIFO) basis. In a multiprocessing system, hardware mailboxes are required. This can be implemented using the Am29338 as shown in Figure 7.

When a process wishes to send a message to the mailbox, it calls a special operating-system routine. This routine first reads the status of the mailbox; if it is not FULL, the routine first writes the message to the mailbox and returns to the calling process. If the mailbox is FULL, the operating system

blocks the calling process on a special queue and enables interrupts from the mailbox. When a slot becomes available in the mailbox, the sending processor is interrupted. The interrupt routine sends the message to the mailbox, disables interrupts from the mailbox, and unblocks the blocked process. On the receiving side, the EMPTY status of the mailbox must be available to the receiving processor in order to allow the receiving process to be blocked if the mailbox is empty. When a mailbox slot becomes filled, a blocked process must be awakened by interrupting the receiving processor.

The mailbox can be extended to operate in a heterogeneous multiprocessing system. In this type of system, processors with varying data-path widths and clock frequencies are interconnected. For example, a 32-bit main processor may control 8- to 16-bit coprocessors. The ability of the Am29338 to match data-path widths and to queue and dequeue asynchronously allows processors of different widths and clock rates to communicate.

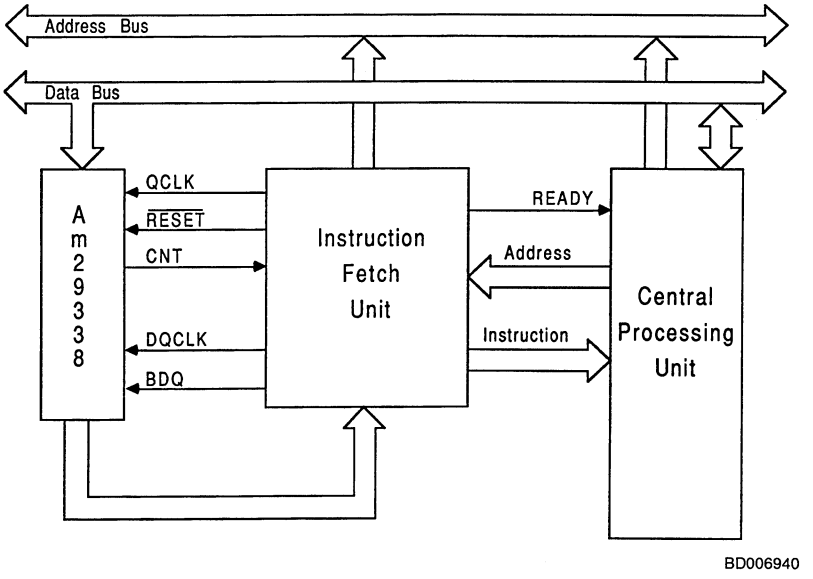
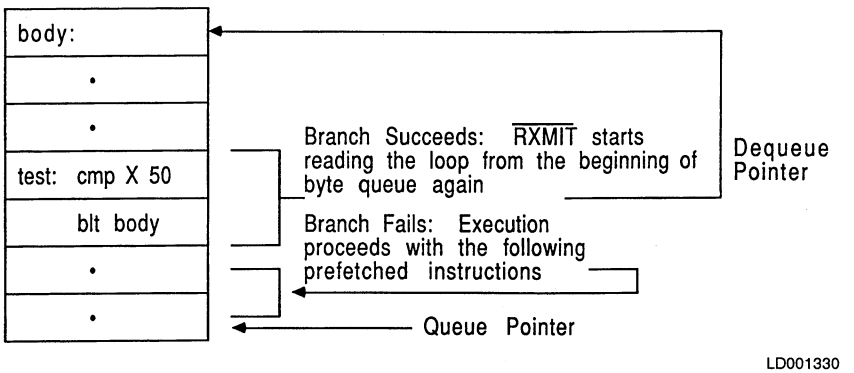


Figure 5. Instruction-Prefetch Queue



Note: This describes a block of macro instructions.

Figure 6. Loop Locking Using Am29338

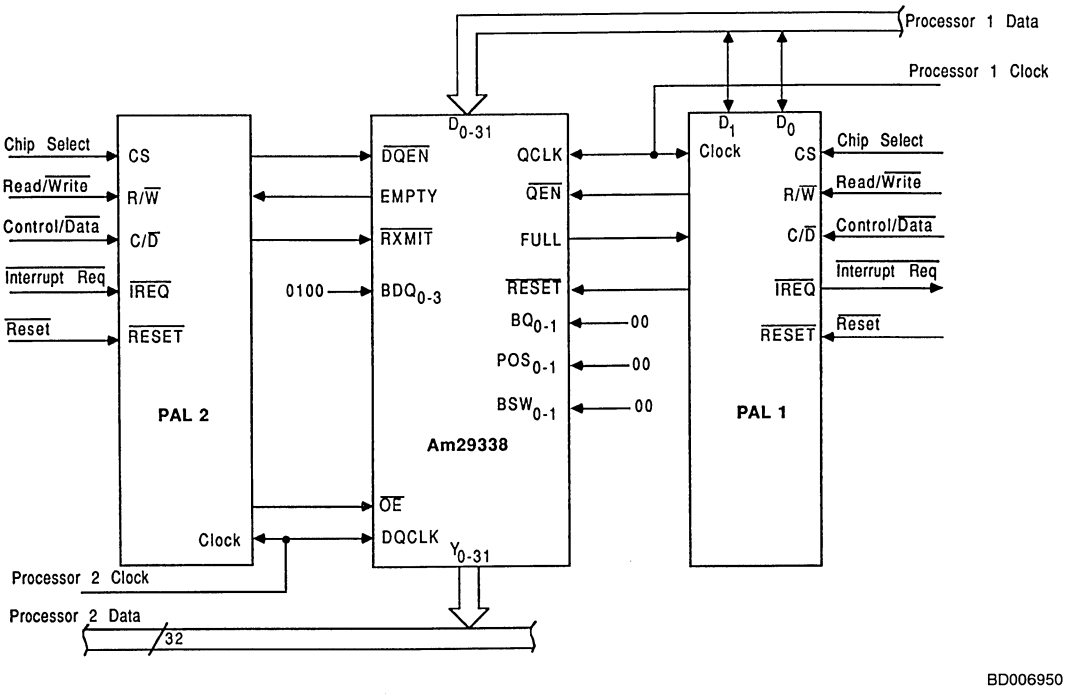
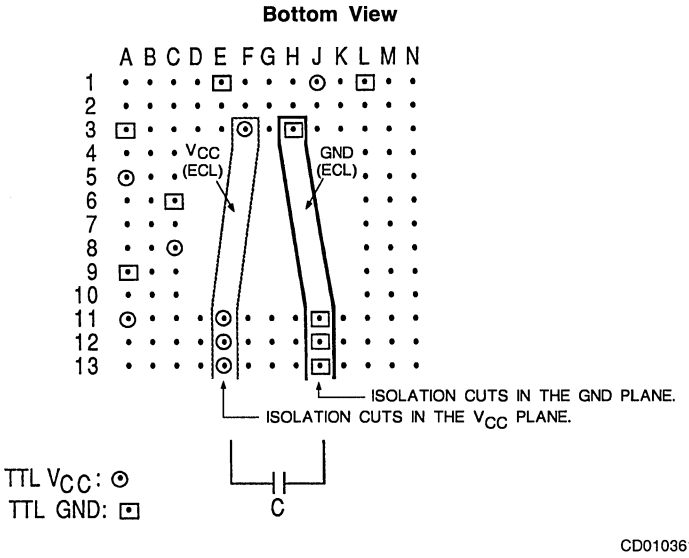


Figure 7. Implementation of a Hardware Mailbox



Notes: 1. The noise-generating TTL supply pins are connected directly to their respective power plane.
2. The noise-sensitive ECL supply pins are interconnected and decoupled as shown, then each connected to the respective power plane in one point only.
3. The heavy lines indicate cuts in the two supply planes that achieve this isolation.

Figure 8. Am29338 Suggested Printed-Circuit-Board Layout

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature
with Power Applied ..... −55 to +125°C
Supply Voltage
with Respect to Ground ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs
for HIGH State .....−0.5 V to +V_{CC} Max.
DC Input Voltage .....−0.5 V to +5.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_C) ..... 0 to +85°C
Supply Voltage (V_{CC}) .....+4.75 to +5.25 V
θ_{JA} ..... (under 200 lfm)

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note: Recommended operating air velocity is 200 linear feet per minute

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IL} or V_{IH} I_{OH} = −3 mA		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IL} or V_{IH} I_{OL} = 16 mA				0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = −18 mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = Max. V_{IN} = 0.5 V	QCLK, DQCLK			−1.0	mA
			Others			−0.5	
I_{IH}	Input HIGH Current	V_{CC} = Max. V_{IN} = 2.4 V				50	µA
I_I	Input HIGH Current	V_{CC} = Max. V_{IN} = 5.5 V				1.0	mA
I_{OZH} I_{OZL}	Off State (High-Impedance) Output Current	V_{CC} = Max.	V_O = 2.4 V			50	µA
			V_O = 0.5 V			−50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = Max. to +0.5 V V_O = 0.5 V		−20		−80	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = Max.	T_C = 0 to +85°C		800	900	mA
			T_C = +85°C			800	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. Typical values are for V_{CC} = +25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
4. Measured with all inputs HIGH.

ADVANCE INFORMATION

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Combinational Propagation Delays

No.	From	To	Delays	Unit
1	D	PDERR	50	ns
2	PD	PDERR	50	ns
3	DQCLK ↑	A_EMPTY or A_FULL	44	ns
4	DQCLK ↑	CNT	46	ns
5	DQCLK ↑	EMPTY or FULL	44	ns
6	DQCLK ↑	PYERR	60	ns
7	DQCLK ↑	Y	52	ns
8	$\overline{OE}$	PYERR	25	ns
9	$\overline{OE}$	Y	25	ns
10	QCLK ↑	A_EMPTY or EMPTY	44	ns
11	QCLK ↑	CNT	46	ns
12	QCLK ↑	A_FULL or FULL	44	ns
13	$\overline{RESET}$ ↓	A_FULL or FULL	44	ns
14	$\overline{RESET}$ ↓	CNT	46	ns
15	$\overline{RESET}$ ↓	EMPTY or A_EMPTY	44	ns
16	$\overline{RESET}$ ↓	PYERR	60	ns
17	$\overline{RESET}$ ↓	Y	52	ns
18	$\overline{RXMIT}$ ↓	A_FULL or FULL	44	ns
19	$\overline{RXMIT}$ ↓	CNT	46	ns
20	$\overline{RXMIT}$ ↓	A_EMPTY or EMPTY	44	ns
21	$\overline{RXMIT}$ ↓	PYERR	60	ns
22	$\overline{RXMIT}$ ↓	Y	52	ns

Setup and Hold Times

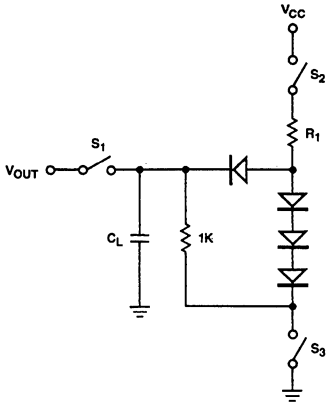
No.	Parameter	For	With Respect To	Delays	Unit
23	Bytes Dequeued Setup	BDQ	DQCLK ↑	20	ns
24	Bytes Dequeued Hold	BDQ	DQCLK ↑	0	ns
25	Bytes Queued Setup	BQ	QCLK ↓	12	ns
26	Bytes Queued Hold	BQ	QCLK ↑		ns
27	Byte Swap Setup	BSW	QCLK ↑	20	ns
28	Byte Swap Hold	BSW	QCLK ↓		ns
29	Data Setup	D	QCLK ↑	8	ns
30	Data Hold	D	QCLK ↑		ns
31	Data Parity Setup	PD	QCLK ↑	8	ns
32	Data Parity Hold	PD	QCLK ↑		ns
33	Dequeue Enable Setup	$\overline{DQEN}$	DQCLK ↑	8	ns
34	Dequeue Enable Hold	$\overline{DQEN}$	DQCLK ↑	0	ns
35	Queue Enable Setup	$\overline{QEN}$	QCLK ↓		ns
36	Queue Enable Hold	$\overline{QEN}$	QCLK ↑		ns

Minimum Clock Requirements

No.	Input	Description	Delays	Unit
37	DQCLK	Dequeue Min. Pulse Width LOW	10	ns
38		Dequeue Min. Pulse Width HIGH	10	
39		Dequeue Min. Cycle Time	80	
40	QCLK	Queue Min. Pulse Width LOW	10	ns
41		Queue Min. Pulse Width HIGH	10	
42		Queue Min. Cycle Time	80	

Advance Information

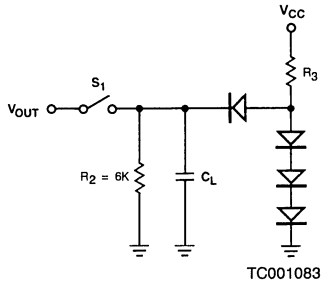
SWITCHING TEST CIRCUITS



TC001102

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{1K}}$$

A. Three-State Outputs



TC001083

$$R_2 = \frac{2.4\ V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + \frac{V_{OL}}{R_2}}$$

B. Normal Outputs

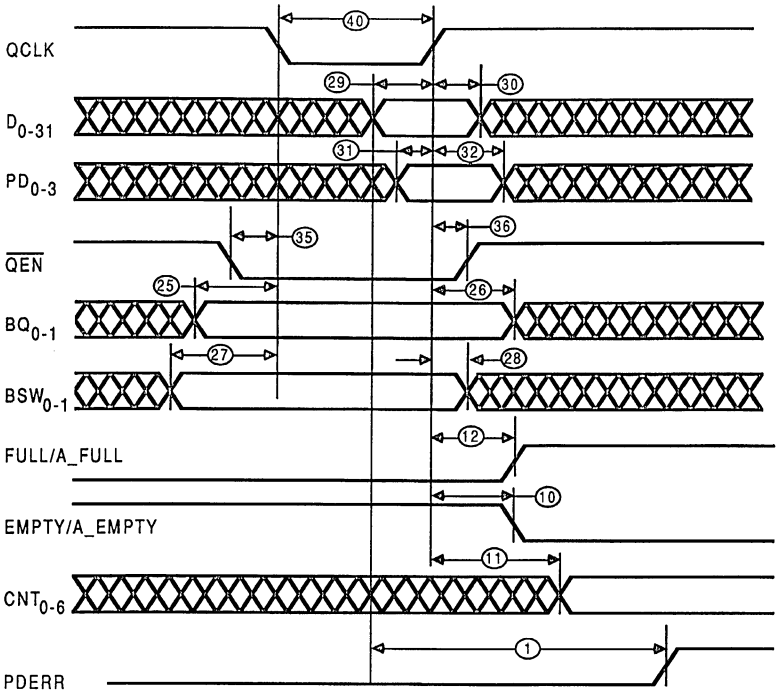
Notes: 1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

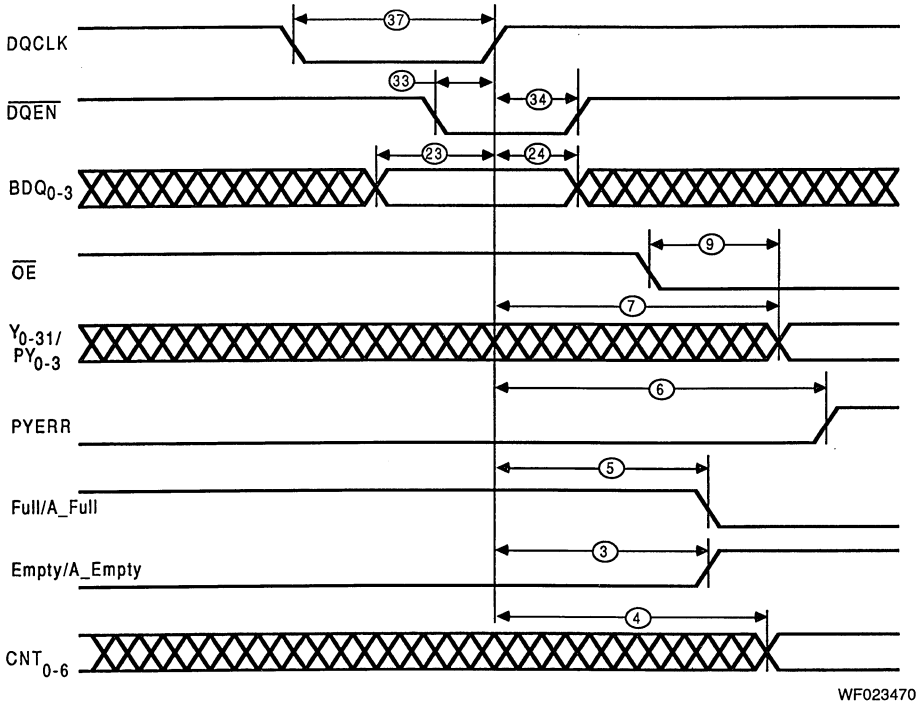
KS000010



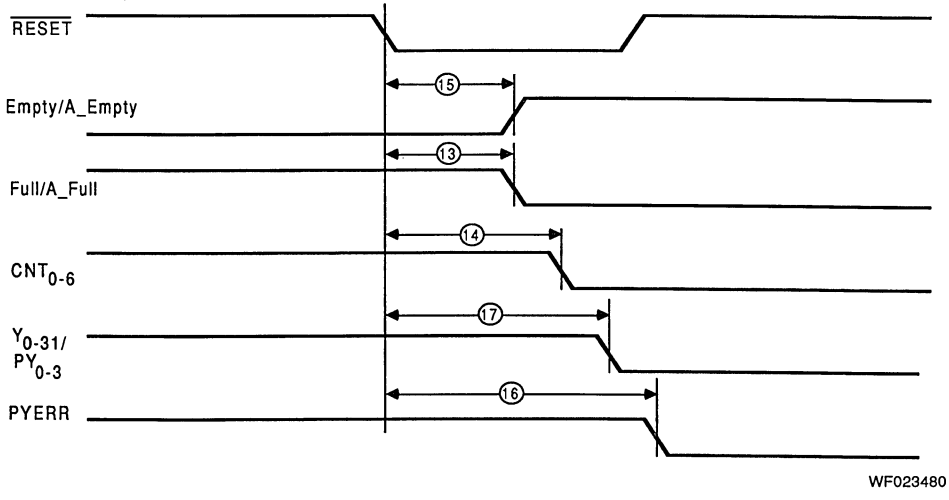
WF023460

Queue Cycle

SWITCHING WAVEFORMS (Cont'd.)



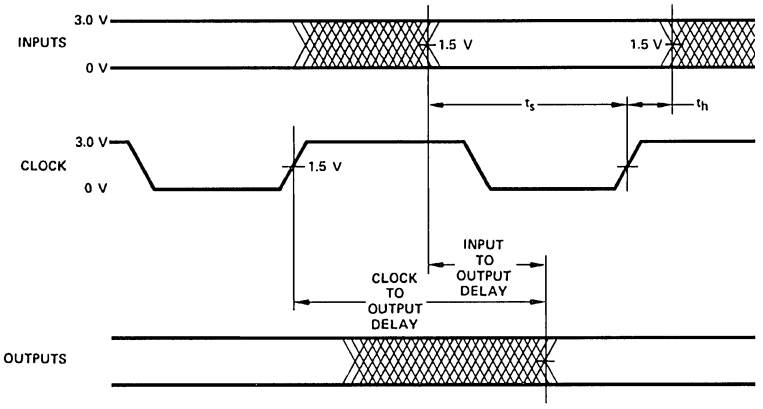
Dequeue Cycle



RESET Timing Diagram

Notes: 1. Minimum time $\overline{\text{RESET}}$ must be asserted.
2. This timing diagram is applicable to $\overline{\text{RXMIT}}$.

SWITCHING WAVEFORMS (Cont'd.)



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Notes on Test Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown.

1. Ensure the part is adequately decoupled at the test head. Large changes in supply current when the device switches may cause function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5 – 8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins which may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in most cases, can provide actual Sentry programs, under license from Sentry.
7. Capacitive Loading for A.C. Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another, but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" which measure the propagation delays into and out of the high impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench set up are used to predict the result at the lower capacitance.

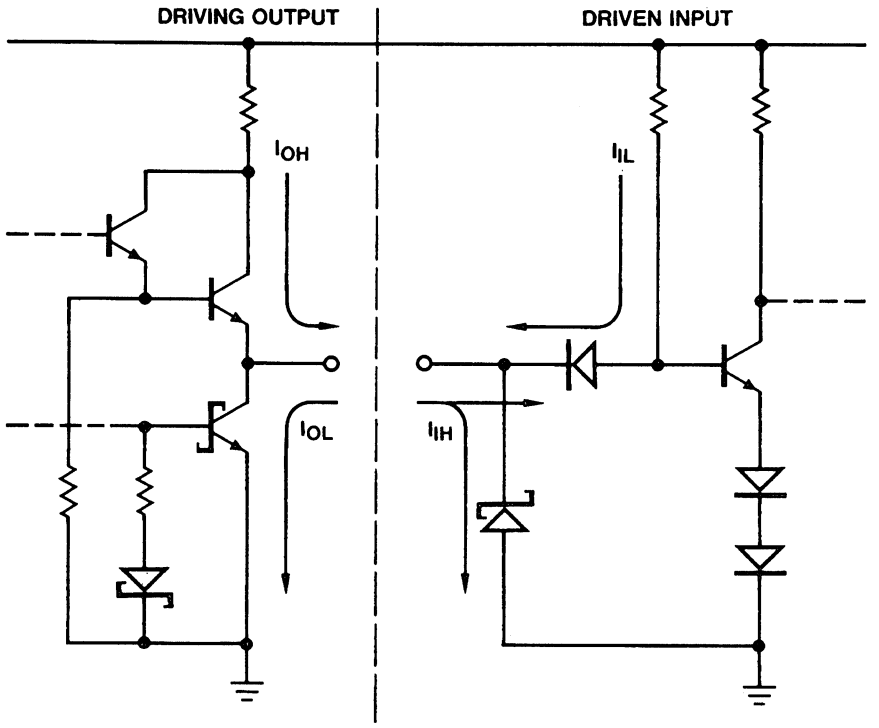
   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at both capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench set up and the knowledge that certain D.C. measurements (I_{OH}, I_{OL}, for example) have already been taken and are within specification. In some cases, special D.C. tests are performed in order to facilitate this correlation.
8. Threshold Testing

   The noise associated with automatic testing, the long, inductive cables, and the high gain of bipolar devices when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for each input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and A.C. testing are performed at "hard" input levels rather than at V_{IL} max and V_{IH} min.
9. A.C. Testing

   Occasionally, parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other A.C. tests that have been performed. These correlations are arrived at by the cognizant engineer by using data from precise bench measurements in conjunction with the knowledge that certain D.C. parameters have already been measured and are within specification.

   In some cases, certain A.C. tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.

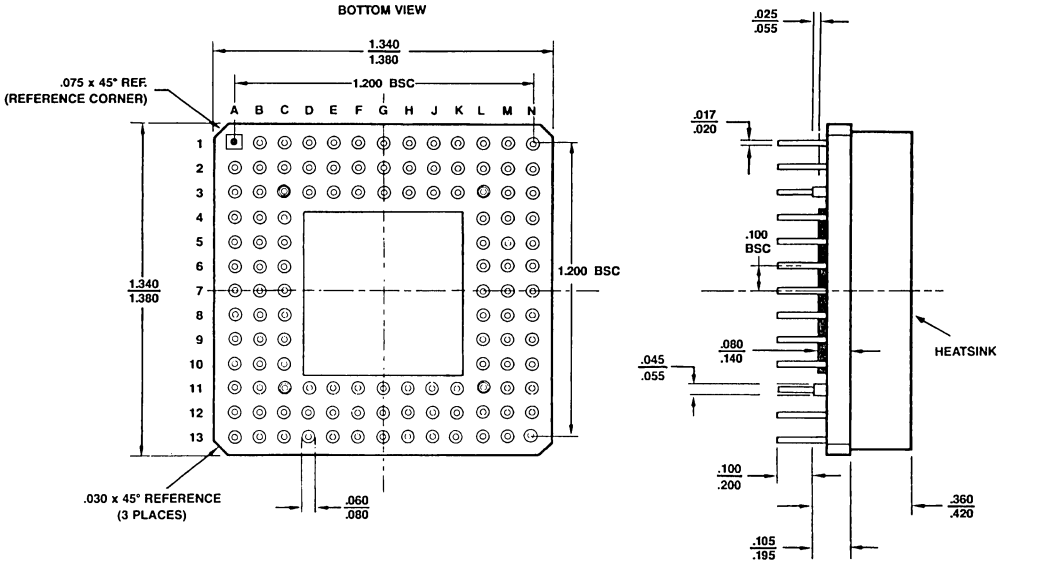
INPUT/OUTPUT CIRCUIT DIAGRAM



ICR00480

PHYSICAL DIMENSIONS*

CG 120



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