LIBERTY CHIP™ IC

Am29C01

Four-Bit CMOS Microprocessor Slice

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- **Low Power**
  The CMOS Am29C01 is a plug-in replacement for the bipolar Am2901B/C. The Am29C01 dissipates 10% of the power of the equivalent bipolar part.
- **Two-address architecture**
  Independent simultaneous access to two working registers saves machine cycles.
- **Eight-function ALU**
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- **Expandable**
  Connect any number of Am29C01s together for longer word lengths.
- **Four status flags**
  Carry, overflow, zero, and negative.
- **Flexible data source selection**
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.

GENERAL DESCRIPTION

The Am29C01 industry standard four-bit microprocessor slice is a high-speed cascadable ALU intended for use in CPUs, peripheral controllers, and programmable microprocessors. The microinstruction flexibility of the Am29C01 permits efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU.

The Am29C01 is a low power CMOS plug-in replacement for the Am2901B/Am2901C.

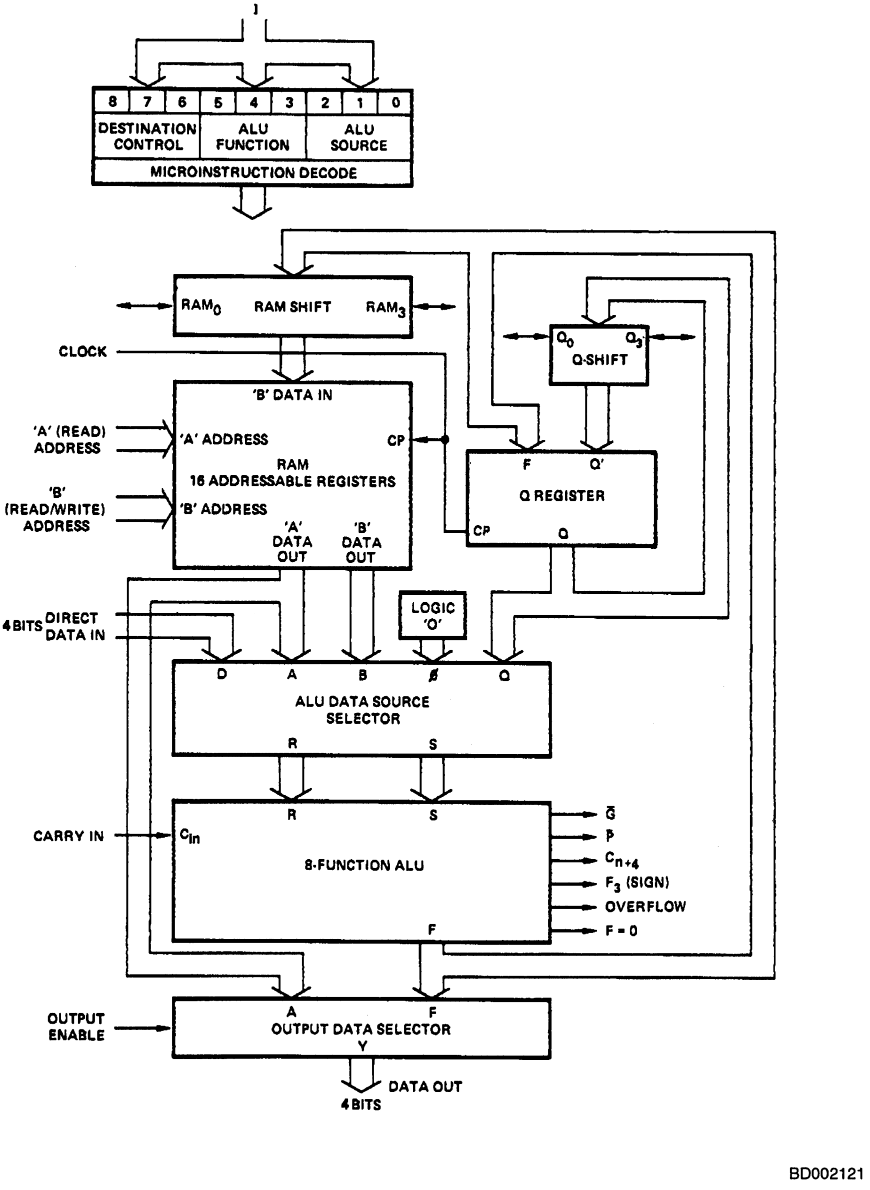
RELATED PRODUCTS

Part No.	Description
Am29C101	16-Bit CMOS Microprocessor Slice
Am29C10A	CMOS Microprogram Controller
Am2904	Status and Shift Control Unit
Am2914	Vectored Priority Interrupt Controller
Am29818	Pipeline Register with SSR Diagnostics
Am29800A	High-Performance Bus Interface Family
Am29C800	High-Performance CMOS Bus Interface Family
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952A	Bidirectional I/O Port
Am27S35A	Registered PROM

Publication #	Rev.	Amendment
07366	B	/0

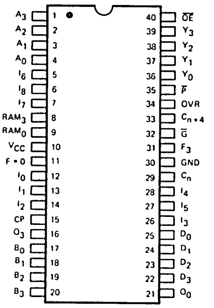
Issue Date: **March 1986**

BLOCK DIAGRAM



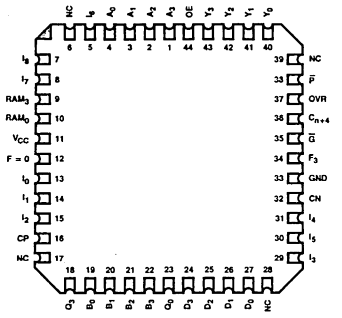
For applications information see Chapters III and IV of
Bit Slice Microprocessor Design,
by Mick and Brick, McGraw Hill Publishers.

CONNECTION DIAGRAMS
Top View



CD004110

LCC*

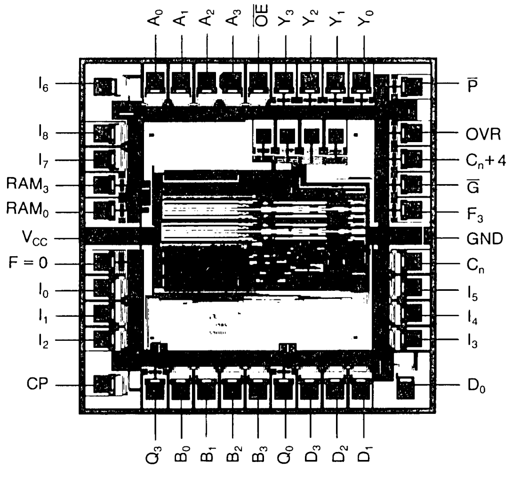


CD004120

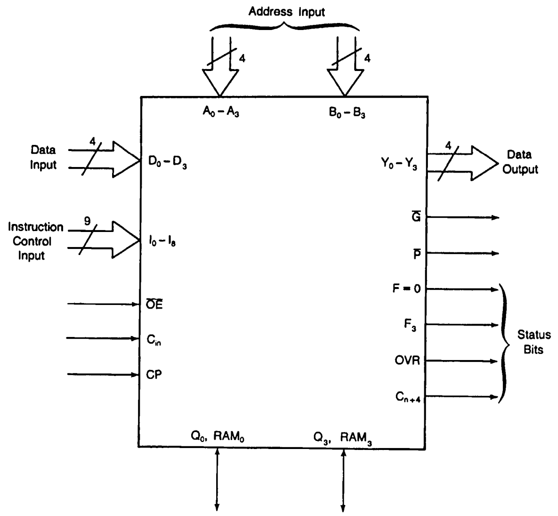
* Same pinouts apply for PLCC.

Note: Pin 1 is marked for orientation.

METALLIZATION AND PAD LAYOUT



LOGIC SYMBOL



LS002311

V_{CC} = Power Supply
GND = Ground

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing

AM29C01 -1 D C B

E. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

D. TEMPERATURE RANGE
C = Commercial (0 to + 70°C)

C. PACKAGE TYPE
P = 40-Pin Plastic DIP (PD 040)
D = 40-Pin Ceramic DIP (CD 040)
J = 44-Pin Plastic Leaded Chip Carrier (PL 044)
L = 44-Pin Ceramic Leadless Chip Carrier (CL 044)

B. SPEED OPTION
Blank = Am2901B Speed
−1 = Am2901C Speed

A. DEVICE NUMBER/DESCRIPTION
Am29C01
4-Bit CMOS Microprocessor Slice

Valid Combinations	
AM29C01	PC, PCB, DC, DCB, JC, LC
AM29C01-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

$A_0 - A_3$ Address Inputs — A Port (Input)

The four address inputs to the register stack used to select one register whose contents are displayed through the A Port.

$B_0 - B_3$ Address Inputs — B Port (Input)

The four address inputs to the register stack used to select one register whose contents are displayed through the B Port and into which new data can be written when the clock goes LOW.

$I_0 - I_8$ Instruction Control Lines (Input)

The nine instruction control lines used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q register or the register stack (I_{678}).

Q_3, RAM_3 Shift Lines (Input/Output)

A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7), the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are electrically OFF (high impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0, RAM_0 Shift Lines (Input/Output)

Shift lines like Q_3 and RAM_3, but at the LSB of the Q register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

$D_0 - D_3$ Direct Data Inputs (Input)

A 4-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

$Y_0 - Y_3$ Data Outputs (Output, Three-State)

The four data outputs. These are three-state output lines. When enabled they display either the four outputs of the ALU or the data on the A Port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ $\overline{\text{Output Enable}}$ (Input)

When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ $\overline{\text{Carry Generate}}$, $\overline{\text{Propagate}}$ Outputs (Output)

The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow Status Bit (Output)

This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's-complement operation has overflowed into the sign bit.

$F = 0$ Status Bit (Output, Open Drain)

This is an open-drain output which goes HIGH (OFF) if the data on the four ALU outputs ($F_0 - F_3$) are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 Status Bit (Output)

The most significant ALU output bit.

C_{in} Carry In (Output)

The carry-in to the internal ALU.

C_{n+4} Carry Out (Output)

The carry-out of the internal ALU.

CP Clock (Input)

The Q-register and register-stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable pulse width to the 16 x 4 RAM. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

FUNCTIONAL DESCRIPTION

A detailed block diagram of the CMOS microprogrammable microprocessor structure is shown in Figure 1. The circuit is a 4-bit slice cascadable to any number of bits. Therefore, all 4 data paths within the circuit are 4 bits wide. The two key elements in the Figure 1 diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random-Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A-address field input. Likewise, data in any of the 16 words of the RAM as defined by the B-address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A-select field and B-select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B-address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R-input field is driven from a 2-input multiplexer, while the S-input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am29C01 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Table 1. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the 4-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Table 2. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902A. A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, $F = 0$, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The $F = 0$ output is used for zero detect. It is an open-drain output and can be wire OR'ed between microprocessor slices. $F = 0$ is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Table 3.

The 4-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A 2-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Table 3 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a 3-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift-down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Table 3.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q-register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Table 3.

The clock input to the Am29C01 controls the RAM, the Q register, and the A- and B- data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B-address field when the clock input is LOW.

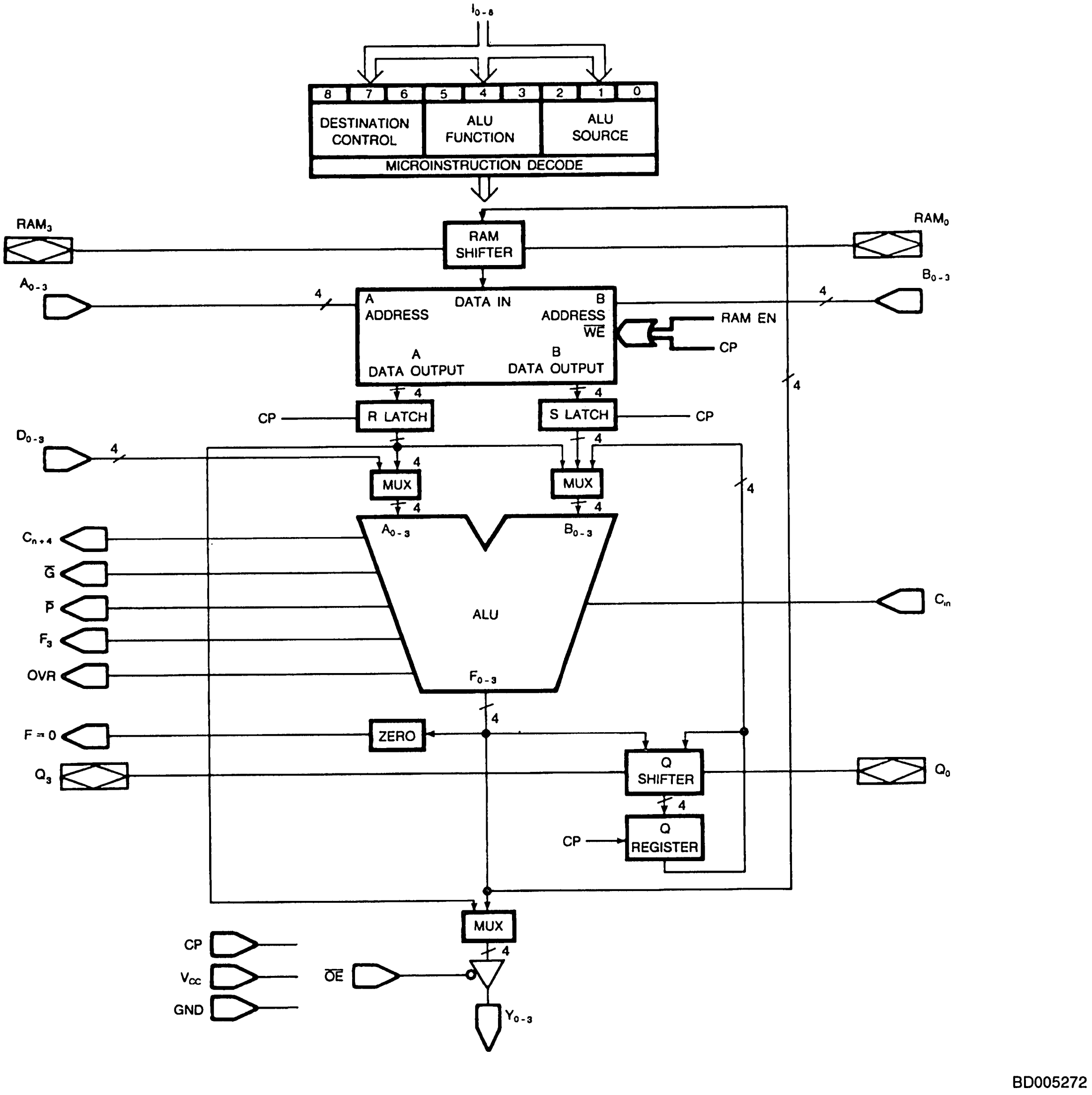


Figure 1. Detailed Block Diagram

FUNCTIONAL TABLES

TABLE 1. ALU SOURCE OPERAND CONTROL

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

TABLE 2. ALU FUNCTION CONTROL

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	$R+S$
SUBR	L	L	H	1	S Minus R	$S-R$
SUBS	L	H	L	2	R Minus S	$R-S$
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \forall S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

TABLE 3. ALU DESTINATION CONTROL

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL-equivalent input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

TABLE 4. SOURCE OPERAND and ALU FUNCTION MATRIX

		I_{210} OCTAL							
		0	1	2	3	4	5	6	7
OCTAL I_{543}	ALU Function	ALU Source							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	$C_n = L$ R Plus S $C_n = H$	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	$C_n = L$ S Minus R $C_n = H$	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	−D − 1 −D
2	$C_n = L$ R Minus S $C_n = H$	A − Q − 1 A − Q	A − B − 1 A − B	−Q − 1 −Q	−B − 1 −B	−A − 1 −A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \forall Q$	$A \forall B$	Q	B	A	$D \forall A$	$D \forall Q$	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus
− = Minus
$\vee$ = OR
$\wedge$ = AND
$\forall$ = EX-OR

TABLE 5. ALU LOGIC MODE FUNCTIONS

Octal I_{543}, I_{210}	Group	Function
4 0 4 1 4 5 4 6	AND	$A \wedge Q$ $A \wedge B$ $D \wedge A$ $D \wedge Q$
3 0 3 1 3 5 3 6	OR	$A \vee Q$ $A \vee B$ $D \vee A$ $D \vee Q$
6 0 6 1 6 5 6 6	EX-OR	$A \veebar Q$ $A \veebar B$ $D \veebar A$ $D \veebar Q$
7 0 7 1 7 5 7 6	EX-NOR	$\overline{A \veebar Q}$ $\overline{A \veebar B}$ $\overline{D \veebar A}$ $\overline{D \veebar Q}$
7 2 7 3 7 4 7 7	INVERT	$\overline{Q}$ $\overline{B}$ $\overline{A}$ $\overline{D}$
6 2 6 3 6 4 6 7	PASS	Q B A D
3 2 3 3 3 4 3 7	PASS	Q B A D
4 2 4 3 4 4 4 7	"ZERO"	0 0 0 0
5 0 5 1 5 5 5 6	MASK	$\overline{A} \wedge Q$ $\overline{A} \wedge B$ $\overline{D} \wedge A$ $\overline{D} \wedge Q$

TABLE 6. ALU ARITHMETIC MODE FUNCTIONS

Octal I_{543}, I_{210}	$C_{in} = L$		$C_{in} = H$	
	Group	Function	Group	Function
0 0 0 1 0 5 0 6	ADD	$A + Q$ $A + B$ $D + A$ $D + Q$	ADD plus one	$A + Q + 1$ $A + B + 1$ $D + A + 1$ $D + Q + 1$
0 2 0 3 0 4 0 7	PASS	Q B A D	Increment	$Q + 1$ $B + 1$ $A + 1$ $D + 1$
1 2 1 3 1 4 2 7	Decrement	$Q - 1$ $B - 1$ $A - 1$ $D - 1$	PASS	Q B A D
2 2 2 3 2 4 1 7	1's Comp.	$-Q - 1$ $-B - 1$ $-A - 1$ $-D - 1$	2's Comp. (Negate)	$-Q$ $-B$ $-A$ $-D$
1 0 1 1 1 5 1 6 2 0 2 1 2 5 2 6	Subtract (1's Comp)	$Q - A - 1$ $B - A - 1$ $A - D - 1$ $Q - D - 1$ $A - Q - 1$ $A - B - 1$ $D - A - 1$ $D - Q - 1$	Subtract (2's Comp)	$Q - A$ $B - A$ $A - D$ $Q - D$ $A - Q$ $A - B$ $D - A$ $D - Q$

Source Operands and ALU Functions

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_{in}, also affects the ALU results when in the arithmetic mode. The C_{in} input has no effect in the logic mode. When I_0 through I_5 and C_{in} are viewed together, the matrix of Table 4 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Table 5 defines the various logic operations that the Am29C01 can perform and Table 6 shows the arithmetic functions of the device. Both carry-in LOW ($C_{in} = 0$) and carry-in HIGH ($C_{in} = 1$) are defined in these operations.

Logic Functions for $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am29C01 is in the add or subtract mode. Table 7 indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

TABLE 7. LOGIC FUNCTIONS for CARRY and OVERFLOW CONDITIONS

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3 P_2 P_1 P_0}$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$	C_4	$C_3 \veebar C_4$
1	S − R	←Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions→			
2	R − S	←Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions→			
3	R ∨ S	LOW	$P_3 P_2 P_1 P_0$	$\overline{P_3 P_2 P_1 P_0} + C_n$	$\overline{P_3 P_2 P_1 P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	←Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions→		
6	$R \veebar S$	←Same as $R \veebar S$, but substitute $\overline{R_i}$ for R_i in definitions→			
7	$\overline{R \veebar S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0$	$\overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 P_0 (G_0 + C_n)}$	(See Note 1)

Definitions: **+ = OR**

$P_0 = R_0 + S_0$ $\quad G_0 = R_0 S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1 S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2 S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3 S_3$

$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_n$

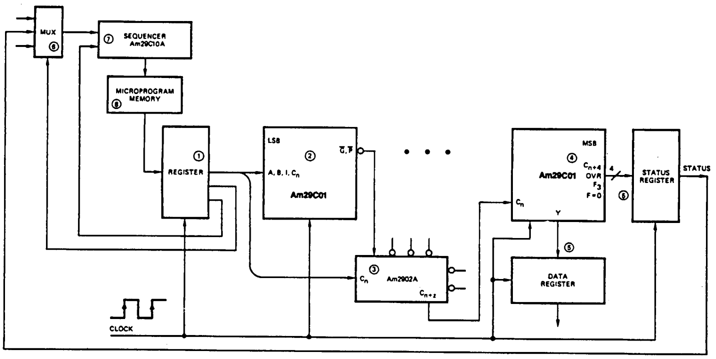
$C_3 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$

Notes: 1. $\left[\overline{P}_2 + \overline{G}_2 \overline{P}_1 + \overline{G}_2 \overline{G}_1 \overline{P}_0 + \overline{G}_2 \overline{G}_1 \overline{G}_0 C_n\right] \veebar \left[\overline{P}_3 + \overline{G}_3 \overline{P}_2 + \overline{G}_3 \overline{G}_2 \overline{P}_1 + \overline{G}_3 \overline{G}_2 \overline{G}_1 \overline{P}_0 + \overline{G}_3 \overline{G}_2 \overline{G}_1 \overline{G}_0 C_n\right]$

APPLICATIONS

Minimum Cycle Time Calculations for 16-Bit Systems

Speeds used in calculations for parts other than Am29C01 and Am29C10A-10 are representative for available MSI parts (see Figures 2 and 3).



AF001622

DATA LOOP

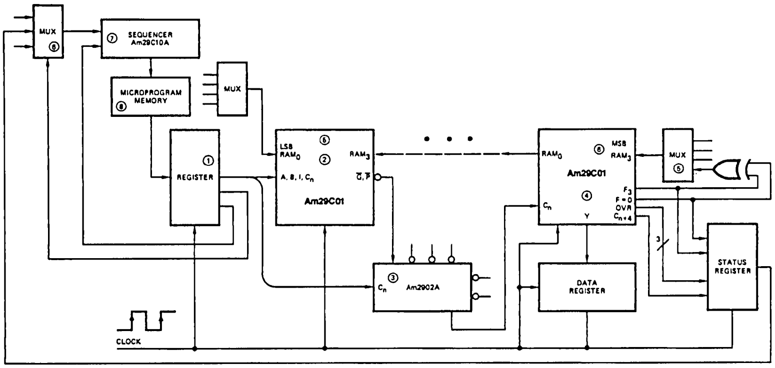
① Register	Clock to Output	11 ns
+② 29C01	A, B to $\overline{G}$, $\overline{P}$	50 ns
+③ 2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7 ns
+④ 29C01	C_n to C_{n+4}, OVR, F_3, F = 0, Y	37 ns
+⑤ Register	Setup Time	4 ns
		109 ns

CONTROL LOOP

① Register	Clock to Output	11 ns
+⑥ MUX	Select to Output	13 ns
+⑦ 29C10A	CC to Output	30 ns
+⑧ PROM	Access Time	30 ns
+① Register	Setup Time	4 ns
		88 ns

Minimum clock period = 109 ns

Figure 2. Pipelined System, Add without Simultaneous Shift



AF001632

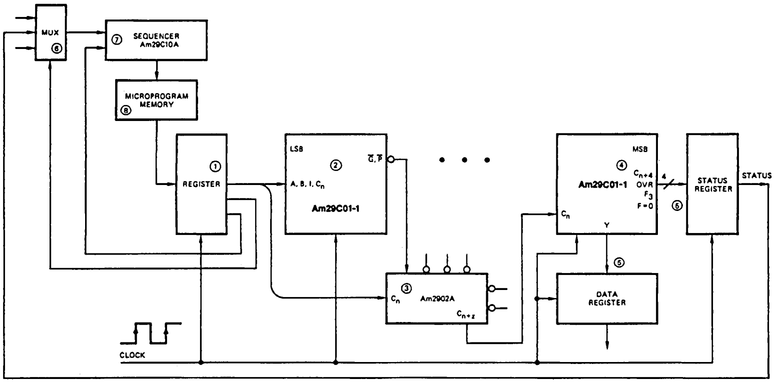
DATA LOOP		
① Register	Clock to Output	11 ns
+② 29C01	A, B to $\overline{G}$, $\overline{P}$	50 ns
+③ 2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7 ns
+④ 29C01	C_n to F_3, OVR	29 ns
+⑤ XOR and MUX		21 ns
+⑥ 29C01	RAM_3 Setup	18 ns
		136 ns

CONTROL LOOP		
① Register	Clock to Output	11 ns
+⑥ MUX	Select to Output	13 ns
+⑦ 29C10A	CC to Output	30 ns
+⑧ PROM	Access Time	30 ns
+① Register	Setup Time	4 ns
		88 ns

Minimum clock period = 136 ns

Figure 3. Pipelined System, Simultaneous Add and Shift Down

Speeds used in calculations for parts other than Am29C01-1 and Am29C10A-20 are representative for available MSI parts (see Figures 4 and 5).



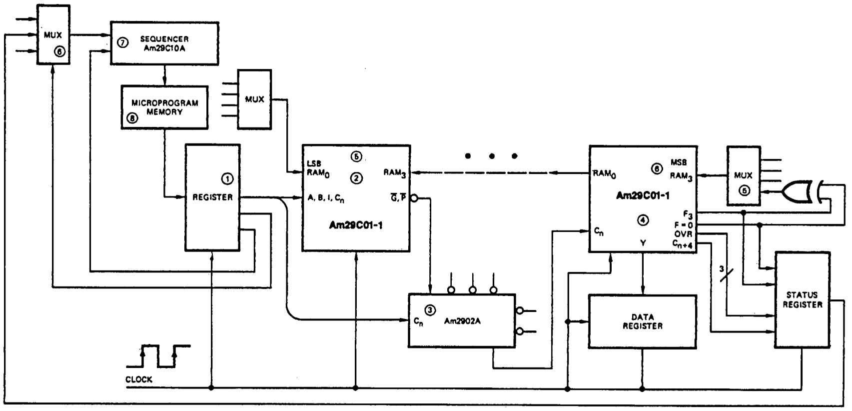
AF001623

DATA LOOP		
① Register	Clock to Output	11 ns
+② 29C01-1	A, B to $\overline{G}$, $\overline{P}$	37 ns
+③ 2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7 ns
+④ 29C01-1	C_n to C_{n+4}, OVR, F_3, F = 0, Y	25 ns
+⑤ Register	Setup Time	4 ns
		84 ns

CONTROL LOOP		
① Register	Clock to Output	11 ns
+⑥ MUX	Select to Output	13 ns
+⑦ 29C10A	CC to Output	30 ns
+⑧ PROM	Access Time	30 ns
+① Register	Setup Time	4 ns
		88 ns

Minimum clock period = 88 ns

Figure 4. Pipelined System, Add without Simultaneous Shift



AF001633

DATA LOOP

① Register	Clock to Output	11 ns
+② 29C01-1	A, B to $\overline{G}$, $\overline{P}$	37 ns
+③ 2902A	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	7 ns
+④ 29C01-1	C_n to F_3, OVR,	22 ns
+⑤ XOR and MUX		21 ns
+⑥ 29C01-1	RAM_3 Setup	12 ns
		110 ns

CONTROL LOOP

① Register	Clock to Output	11 ns
+⑥ MUX	Select to Output	13 ns
+⑦ 29C10A	CC to Output	30 ns
+⑧ PROM	Access Time	30 ns
+① Register	Setup Time	4 ns
		88 ns

Minimum clock period = 110 ns

Figure 5. Pipelined System, Simultaneous Add and Shift Down

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−55 to +125°C
Supply Voltage to Ground Potential Continuous	−0.3 to +7.0 V
DC Voltage Applied to Outputs For High Output State	−0.3 to $+V_{CC}+0.3$ V
DC Input Voltage	−0.3 to $+V_{CC}+0.3$ V
DC Output Current, Into LOW Outputs	30 mA
DC Input Current	−10 to +10 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Temperature (T_A)	0° to +70°C
Supply Voltage (V_{CC})	+4.75 to +5.25 V
Military (M) Devices	
Temperature (T_C)	−55 to +125°C
Supply Voltage (V_{CC})	+4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS* over operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Note 1)			Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min. $V_{IN} = V_{IH}$ or V_{IL}		I_{OH} = −1.6 mA All Others	2.4		V
				I_{OH} = −600 µA RAM_0, RAM_3, Q_0, Q_3	2.4		
I_{CEX}	Output Leakage Current For F = 0 Output	V_{CC} = Min., V_{OH} = 5.5 V $V_{IN} = V_{IH}$ or V_{IL}				10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min., $V_{IN} = V_{IH}$ or V_{IL}	All Others	I_{OL} = 20 mA (COM'L)		0.5	V
				I_{OL} = 16 mA (MIL)		0.5	
			RAM_0, RAM_3, Q_0, Q_3	I_{OL} = 6.0 mA		0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 2)			2.0		V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 2)				0.8	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V				−10	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.4 V				10	µA
I_I	Input HIGH Current	V_{CC} = Max., $V_{IN} = V_{CC}$ −0.5 V				100	µA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = Max.	Y_{0-3}	V_O = 2.4 V		50	µA
				V_O = 0.5 V		−50	
I_{CC}	Static Power Supply Current (Note 3)	V_{CC} = Max., $V_{IN} = V_{CC}$ or GND, I_O = 0 µA		T_A = 0° to +70°C (COM'L only)		40	mA
				T_C = −55° to +125°C (MIL only)			
C_{PD}	Power Dissipation Capacitance (Note 4)	V_{CC} = 5.0 V, T_A = 25°C, No Load			500 pF Typical		

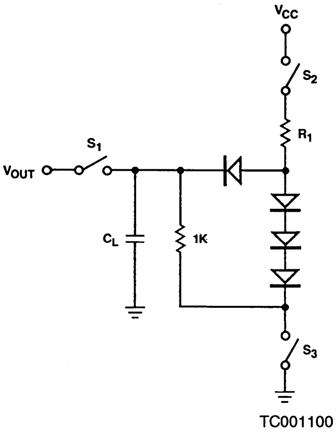
Notes:

1. V_{CC} conditions shown as Min or Max, refer to the military (±10%) or commercial (±5%) V_{CC} limits.
2. These input levels provide zero noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. Worst-case I_{CC} is measured at the lowest temperature in the specified operating range.
4. C_{PD} determines the no-load dynamic current consumption:
   I_{CC} (Total) = I_{CC} (Static) + C_{PD} V_{CC} f, where f is the switching frequency of the majority of the internal nodes, normally one-half of the clock frequency.

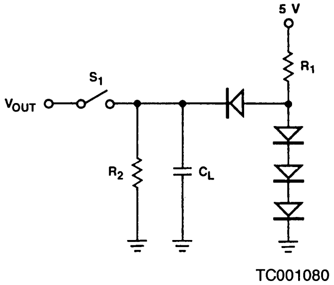
* Applies to both Am29C01 and Am29C01-1 devices.

SWITCHING TEST CIRCUITS

A. THREE-STATE OUTPUTS

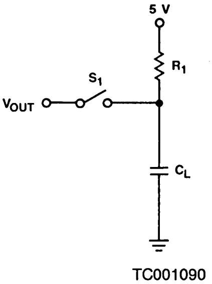


B. NORMAL OUTPUTS



$$R_2 = \frac{2.4\ \text{V}}{I_{OH}}$$

C. OPEN-DRAIN OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Notes:
1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.

SWITCHING CHARACTERISTICS

I. Am29C01 Switching Characteristics: Commercial Range

The following tables specify the guaranteed performance of the Am29C01 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75 V to 5.25 V. All data are in ns, with measurements made at 1.5 V. All outputs have maximum DC load, $C_L = 50$ pF

A. Cycle Time and Clock Characteristics

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	64 ns*
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	15 MHz*
Minimum Clock LOW Time	30 ns
Minimum Clock HIGH Time	30 ns
Minimum Clock Period	64 ns*

*These specs are not tested, but are derived from other specs.

B. Combinational Propagation Delays (Note 1)

	To Output							
From Input	**Y**	**F_3**	**C_{n+4}**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM_0 RAM_3**	**Q_0 Q_3**
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
C_{in}	30	29	20	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	51	52	52	45	60	49	53	–
I678	28	–	–	–	–	–	35	35
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↑	49	48	47	37	58	55	59	29

C. Setup and Hold Times Relative to Clock (CP) Input (Note 1)

Input	**CP:**  **Setup Time Before H →L**	**Hold Time After H →L**	**Setup Time Before L →H**	**Hold Time After L →H**
A, B Source Address	30	4 (Note 3)	60, 30 + T_{PWL} (Note 4)	–
B Destination Address	15	Do Not Change (Note 2)		4
D	–	–	40	0
C_{in}	–	–	40	0
I012	–	–	45	0
I345	–	–	45	0
I678	14	Do Not Change (Note 2)		5
$RAM_{0,3}$, $Q_{0,3}$	–	–	18	7

D. Output Enable/Disable Times (Note 5)

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

Notes: See page 19 for notes.

II. Am29C01 Switching Characteristics: Military Range

The following tables specify the guaranteed performance of the Am29C01 over the military operating range of −55°C to +125°C, with V_{CC} from 4.5 V to 5.5 V. All data are in ns, with measurements made at 1.5 V. All outputs have maximum DC load, $C_L = 50$ pF

A. Cycle Time and Clock Characteristics

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	
Minimum Clock LOW Time	
Minimum Clock HIGH Time	
Minimum Clock Period	

B. Combinational Propagation Delays (Note 1)

	To Output							
From Input	**Y**	**F_3**	**C_{n+4}**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM_0 RAM_3**	**Q_0 Q_3**
A, B Address								–
D								–
C_{in}				–				–
I012								–
I345								–
I678		–	–	–	–	–		
A Bypass ALU (I = 2XX)		–	–	–	–	–	–	–
Clock ↑								

C. Setup and Hold Times Relative to Clock (CP) Input (Note 1)

Input	**CP:**  **Setup Time Before H →L**	**Hold Time After H →L**	**Setup Time Before L →H**	**Hold Time After L →H**
A, B Source Address		(Note 3)	(Note 4)	
B Destination Address		Do Not Change (Note 2)		
D	–	–		
C_{in}	–	–		
I012	–	–		
I345	–	–		
I678		Do Not Change (Note 2)		
$RAM_{0,\ 3}$, $Q_{0,\ 3}$	–	–		

D. Output Enable/Disable Times (Note 5)

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y		

Notes: See page 19 for notes.

SWITCHING CHARACTERISTICS

I. Am29C01-1 Switching Characteristics: Commercial Range

The following tables specify the guaranteed performance of the Am29C01-1 over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75 V to 5.25 V. All data are in ns, with measurements made at 1.5 V. All outputs have maximum DC load, $C_L = 50$ pF

A. Cycle Time and Clock Characteristics

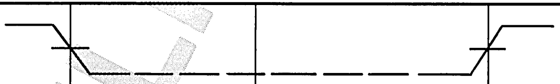
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	34 ns*
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	29 MHz*
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	15 ns
Minimum Clock Period	34 ns*

*These specs are not tested, but are derived from other specs.

B. Combinational Propagation Delays (Note 1)

	To Output							
From Input	**Y**	**F_3**	**C_{n+4}**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM_0 RAM_3**	**Q_0 Q_3**
A, B Address	40	40	40	37	40	40	40	–
D	30	30	30	30	38	30	30	–
C_{in}	22	22	20	–	25	22	25	–
I012	35	35	35	37	37	35	35	–
I345	35	35	35	35	38	35	35	–
I678	25	–	–	–	–	–	26	26
A Bypass ALU (I = 2XX)	35	–	–	–	–	–	–	–
Clock ↑	35	35	35	35	35	35	35	28

C. Setup and Hold Times Relative to Clock (CP) Input (Note 1)

Input	**CP:**  **Setup Time Before H →L**	**Hold Time After H →L**	**Setup Time Before L →H**	**Hold Time After L →H**
A, B Source Address	15	4 (Note 3)	30, 15 + T_{PWL} (Note 4)	–
B Destination Address	15	Do Not Change (Note 2)		4
D	–	–	25	0
C_{in}	–	–	25	0
I012	–	–	30	0
I345	–	–	30	0
I678	10	Do Not Change (Note 2)		5
$RAM_{0,\ 3}$, $Q_{0,\ 3}$	–	–	12	7

D. Output Enable/Disable Times (Note 5)

Input	Output	Enable	Disable
$\overline{OE}$	Y	23	23

Notes: See page 19 for notes.

II. Am29C01-1 Switching Characteristics: Military Range

The following tables specify the guaranteed performance of the Am29C01-1 over the military operating range of −55°C to +125°C, with V_{CC} from 4.5 V to 5.5 V. All data are in ns, with measurements made at 1.5 V. All outputs have maximum DC load, $C_L = 50$ pF

A. Cycle Time and Clock Characteristics

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	
Minimum Clock LOW Time	
Minimum Clock HIGH Time	
Minimum Clock Period	

B. Combinational Propagation Delays (Note 1)

	To Output							
From Input	**Y**	**F_{15}**	**C_{n+16}**	**$\overline{G}$, $\overline{P}$**	**F = 0**	**OVR**	**RAM_0 RAM_{15}**	**Q_0 Q_{15}**
A, B Address								–
D								–
C_{in}				–				–
I012								–
I345								–
I678		–	–	–	–	–		
A Bypass ALU (I = 2XX)		–	–	–	–	–	–	–
Clock ↑								

C. Setup and Hold Times Relative to Clock (CP) Input (Note 1)

Input	CP:  **Setup Time Before H →L**	**Hold Time After H →L**	**Setup Time Before L →H**	**Hold Time After L →H**
A, B Source Address		(Note 3)	(Note 4)	
B Destination Address	Do Not Change (Note 2)			
D	–	–		
C_{in}	–	–		
I012	–	–		
I345	–	–		
I678		Do Not Change (Note 2)		
$RAM_{0,15}$, $Q_{0,15}$	–	–		

D. Output Enable/Disable Times (Note 5)

Input	**Output**	**Enable**	**Disable**
$\overline{OE}$	Y		

Notes: See page 19 for notes.

SWITCHING CHARACTERISTICS NOTES:

1. A dash indicates a propagation delay path or setup time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The setup time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.
5. Output disable times are specified with $C_L = 5$ pF and measured to 0.5 V change of output-voltage level. Enable times are specified with $C_L = 50$ pF and measured at 1.5 V output-voltage level.

Notes on Test Methods

The following points give the general philosophy which we apply to tests which must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown in the data sheet.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. To assist in testing, AMD offers complete documentation on our test procedures and, in some cases, can provide Fairchild Sentry programs, under license.
7. Capacitive Loading for A.C. Testing

   Automatic testers and their associated hardware have stray capacitance which varies from one type of tester to another but is generally around 50 pF. This, of course, makes it impossible to make direct measurements of parameters which call for smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays" which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF) and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at <u>both</u> capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench set up and the knowledge that certain D.C. measurements (I_{OH}, I_{OL}, for example) have already been taken and are within spec. In some cases, special D.C. tests are performed in order to facilitate this correlation.
8. Threshold Testing

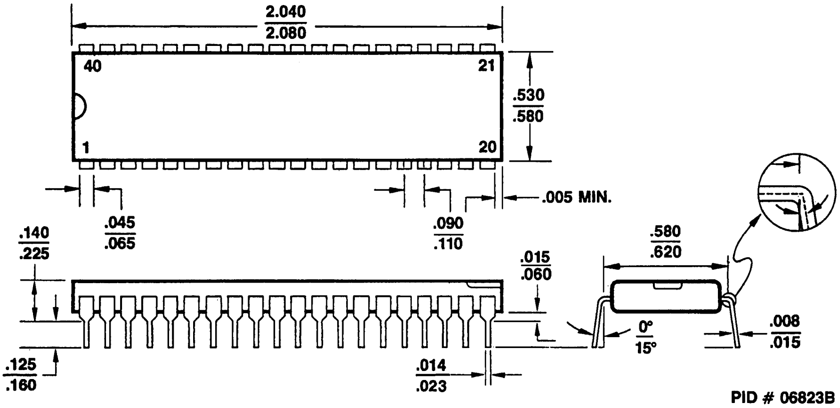
   The noise associated with automatic testing (due to the long, inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for <u>each</u> input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and A.C. testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
9. A.C. Testing

   Occasionally, parameters are specified which cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other A.C. tests which have been performed. These correlations are arrived at by the cognizant engineer by using data from precise bench measurements in conjunction with the knowledge that certain D.C. parameters have already been measured and are within spec.

   In some cases, certain A.C. tests are redundant since they can be shown to be predicted by other tests which have already been performed. In these cases, the redundant tests are not performed.

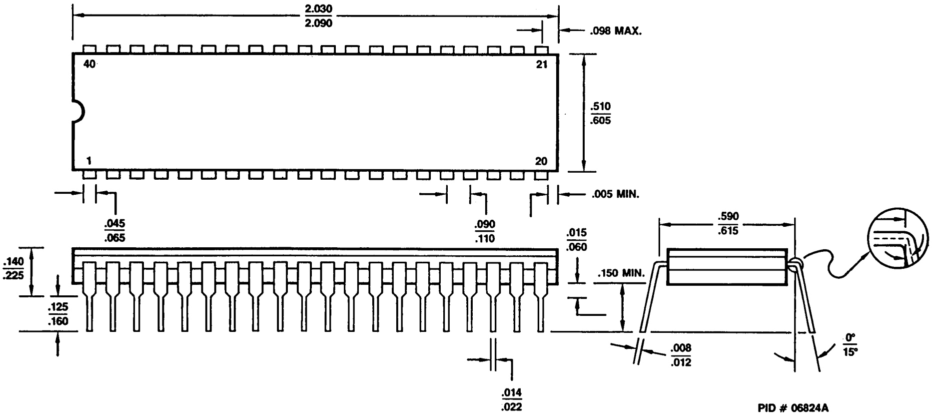
PHYSICAL DIMENSIONS (Cont'd.)

PD 040



PID # 06823B

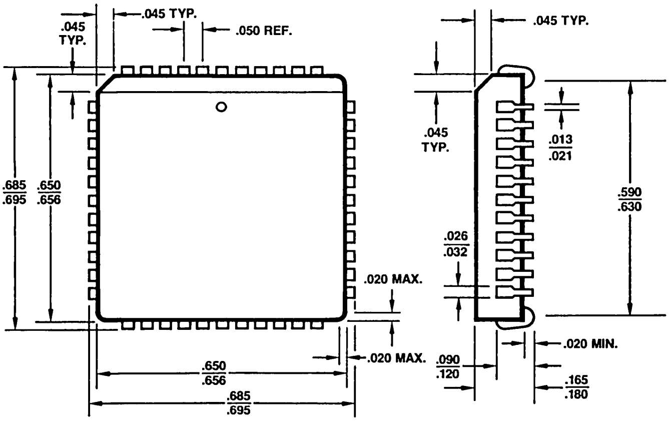
CD 040



PID # 06824A

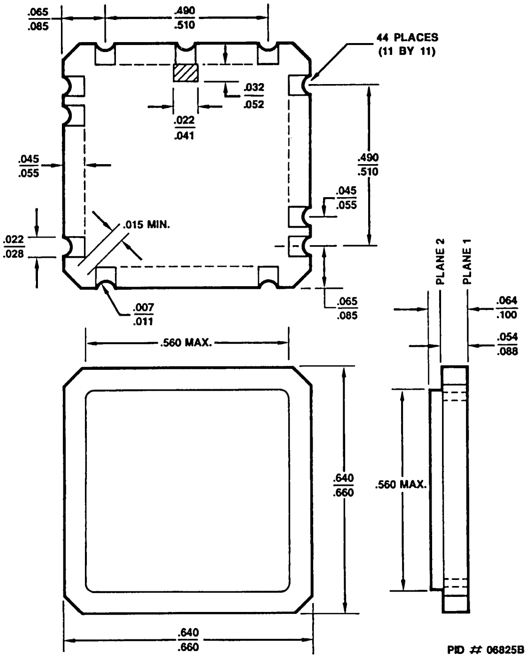
PHYSICAL DIMENSIONS

PL 044



PID # 06752B

CL 044



PID # 06825B

The International Standard of Quality guarantees a 0.05% AQL on all electrical parameters, AC and DC, over the entire operating range.

INT·STD·500

ADVANCED MICRO DEVICES DOMESTIC SALES OFFICES

ALABAMA	(205) 882-9122
ARIZONA,	
Tempe	(602) 242-4400
Tucson	(602) 792-1200
CALIFORNIA,	
El Segundo	(213) 640-3210
Newport Beach	(714) 752-6262
San Diego	(619) 560-7030
Sunnyvale	(408) 720-8811
Woodland Hills	(818) 992-4155
COLORADO	(303) 741-2900
CONNECTICUT,	
Southbury	(203) 264-7800
FLORIDA,	
Altamonte Springs	(305) 339-5022
Clearwater	(813) 530-9971
Ft. Lauderdale	(305) 484-8600
Melbourne	(305) 254-2915
GEORGIA	(404) 449-7920
ILLINOIS	(312) 773-4422
INDIANA	(317) 244-7207
KANSAS	(913) 451-3115
MARYLAND	(301) 796-9310
MASSACHUSETTS	(617) 273-3970
MINNESOTA	(612) 938-0001
NEW JERSEY	(201) 299-0002
NEW YORK,	
Liverpool	(315) 457-5400
Poughkeepsie (IBM only)	(914) 471-8180
Woodbury	(516) 364-8020
NORTH CAROLINA,	
Raleigh	(919) 847-8471
OREGON	(503) 245-0080
OHIO,	
Columbus	(614) 891-6455
PENNSYLVANIA,	
Allentown (AT&T only)	(215) 398-8006
Willow Grove	(215) 657-3101
TEXAS,	
Austin	(512) 346-7830
Dallas	(214) 934-9099
Houston	(713) 785-9001
WASHINGTON	(206) 455-3600
WISCONSIN	(414) 782-7748

INTERNATIONAL SALES OFFICES

BELGIUM,		
Bruxelles	TEL:	(02) 771 99 93
	FAX:	762-3716
	TLX:	61028
CANADA, Ontario,		
Kanata	TEL:	(613) 592-0090
Willowdale	TEL:	(416) 224-5193
	FAX:	(416) 224-0056
FRANCE,		
Paris	TEL:	(01) 46 87 36 66
	FAX:	(01) 46 86 21 85
	TLX:	202053F
GERMANY,		
Hannover area	TEL:	(05143) 50 55
	FAX:	5553
	TLX:	925287
München	TEL:	(089) 41 14-0
	FAX:	406490
	TLX:	523883
Stuttgart	TEL:	(0711) 62 33 77
	FAX:	625187
	TLX:	721882
HONG KONG,		
Kowloon	TEL:	3-695377
	FAX:	1234276
	TLX:	50426
ITALY, Milano	TEL:	(02) 3390541
	FAX:	3498000
	TLX:	315286
JAPAN, Tokyo	TEL:	(03) 345-8241
	FAX:	3425196
	TLX:	J24064 AMDTKOJ
LATIN AMERICA,		
Ft. Lauderdale,	TEL:	(305) 484-8600
	FAX:	(305) 485-9736
	TLX:	5109554261 AMDFTL
SWEDEN, Stockholm	TEL:	(08) 733 03 50
	FAX:	7332285
	TLX:	11602
UNITED KINGDOM,		
Manchester area	TEL:	(0925) 828008
	FAX:	827693
	TLX:	628524
London area	TEL:	(04862) 22121
	FAX:	22179
	TLX:	859103

NORTH AMERICAN REPRESENTATIVES

CALIFORNIA	
I^2 INC	OEM (408) 988-3400
	DISTI (408) 496-6868
IDAHO	
INTERMOUNTAIN TECH MKGT	(208) 322-5022
INDIANA	
SAI MARKETING CORP	(317) 241-9276
IOWA	
LORENZ SALES	(319) 377-4666
MICHIGAN	
SAI MARKETING CORP	(313) 227-1786
NEBRASKA	
LORENZ SALES	(402) 475-4660
NEW JERSEY	
TAI CORPORATION	(609) 933-2600
NEW MEXICO	
THORSON DESERT STATES	(505) 293-8555
NEW YORK	
NYCOM, INC	(315) 437-8343
OHIO	
Dayton	
DOLFUSS ROOT & CO	(513) 433-6776
Strongsville	
DOLFUSS ROOT & CO	(216) 238-0300
PENNSYLVANIA	
DOLFUSS ROOT & CO	(412) 221-4420
UTAH	
R^2 MARKETING	(801) 595-0631

ADVANCED MICRO DEVICES 901 Thompson Pl., P.O. Box 3453, Sunnyvale, CA 94088, USA
TEL: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450

PRINTED IN U.S.A. AIS-WCP-15M-4/86-0