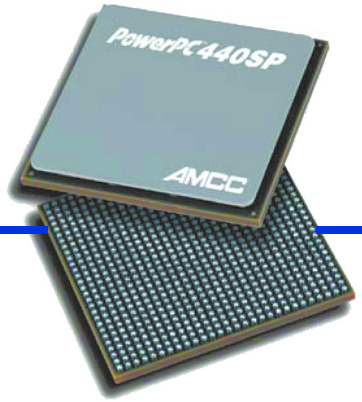
AMCC



PowerPC 440SP

Embedded Processor

With speeds of up to 667 MHz, the PowerPC 440SP embedded processor provides high bandwidth, design flexibility and robust features to demanding storage and networking applications. With three PCI-X version 2.0 interfaces, an on-chip double data rate (DDR I/DDR II) SDRAM controller, I2O messaging unit, RAID 5/RAID 6 acceleration hardware, and a rich peripheral mix, the PowerPC 440SP embedded processor is ideally suited for RAID controllers and storage area networking (SAN) equipment.

PowerPC™

Benefits

- Delivers 533-MHz to 667-MHz performance for embedded I/O processor designs
- 32-Kbyte-I/32-Kbyte D L1 caches
- 256-Kbyte L2 cache with parity protection may also be used as on-chip SRAM
- High-speed processor local bus (PLB) with 2-way crossbar, supports 10.4-Gbytes/s peak bandwidth
- PCI-X v2.0 DDR compatible (266 MHz) bridge with one 32-bit and two 64-bit PCI-X interfaces
- Dual-ported 32/64-bit SDRAM memory controller, interfaced to both PLB slave segments, supporting 166/333-MHz DDR I and 333/667-MHz DDR II
- On-chip RAID 5 and RAID 6 acceleration hardware
- Integrated I2O messaging with two-channel DMA controller
- On-chip peripherals including 10/100/1000 Ethernet MAC, UARTs, IIC
- Offers low power dissipation and small form factor for high-density and power-conscious applications

The PowerPC 440 Core

To enhance overall throughput, the PowerPC 440 superscalar core incorporates a 7-stage pipeline and executes up to two instructions per cycle. Its large 32-Kbyte data cache and 32-Kbyte instruction cache are 64-way set-associative. For additional system performance, the PowerPC 440 core includes dynamic branch prediction and 24 digital signal processing (DSP) instructions, as well as non-blocking caches that can be managed in either write-through or write-back mode.

High-Bandwidth Bus Architecture

For RAID applications, the ability to move large volumes of data is the key to performance. The PowerPC 440SP processor employs a unique two-way cross-bar Processor Local Bus (PLB) to provide a high-bandwidth data pathway between the processor core, the PCI bus and the memory controller. In addition to the separate 128-bit read and write data buses found in other PowerPC processors, the 440SP doubles the number of data paths to achieve more than 10 Gbytes/s of peak bandwidth.

High Performance Memory Support

Attached to the PLB is a DDR/DDR2 SDRAM memory controller. The memory controller connects to all four data paths, taking advantage of the PLB's generous bandwidth. It supports up to 4 Gbytes of DDR667-compliant memory, and offers ECC for enhanced data integrity.

PCI-X 3.3V Multiport Bridge

Three PCI-X Revision 2.0 double data rate (DDR) interfaces provide a variety of options for interfacing with both peripheral devices and other PowerPC 440SP processors. The DDR interfaces latch data on both edges of the clock, for an effective DDR266 throughput. The primary bus is a 64-bit interface with a maximum bandwidth of 2.13 Gbytes/s. The secondary buses include one 64-bit interface and one 32-bit interface. All three are compatible with PCI-X v 1.0a and PCI v 2.3 specifications, include internal arbiters, and can be configured in Host or Adapter mode. These PCI-X interfaces can function as an opaque PCI-X to PCI-X bridge, allowing data to be transferred directly between the buses through the PLB.

Ethernet Interface

For simplified management, the 440SP offers an on-chip 10/100/1000-Mbits/s Ethernet port.

RAID Hardware and I2O Accelerate Storage Applications

The 440SP offers on-chip acceleration hardware for RAID 5 and RAID 6 parity generation and checking. This hardware, along with an internal high efficiency DMA engine, implements XOR and Galois Field P and Q operations at a high throughput rate.

I/O processing and applications using multiple processors can benefit from the integrated messaging unit. Designed to meet I2O specifications, this messaging unit can utilize I2O message frames to provide communication between the 440SP processor and a host system using the host-side PCI-X v 2.0 (DDR) bus. It also allows the 440SP to work as an intelligent I/O adapter controller.

The 440SP features DMA capability by means of two DMA hardware controller functions.

Standard Peripherals

The PowerPC 440SP offers three 16750-compliant UARTs, support for up to 32 general- purpose I/O (GPIO) and two IIC controllers.

PowerPC 440SP

PowerPC Partners Ecosystem

AMCC's embedded PowerPC processors are supported by an extensive ecosystem of products and services from a wide range of leading suppliers. AMCC's PowerPC Partners program includes industry-standard providers of:

- Embedded operating systems
- Hardware and software development tools
- Embedded software products and services
- Board-level products
- System design services
- Technical training

For full details of the products and services available through the PowerPC Partners program, or to browse support available for a specific processor, visit:***http://www.amcc.com/Embedded/Partners.***

AMCC also provides an evaluation kit for this PowerPC processor, including an optimized evaluation board as well as sample applications and other software.

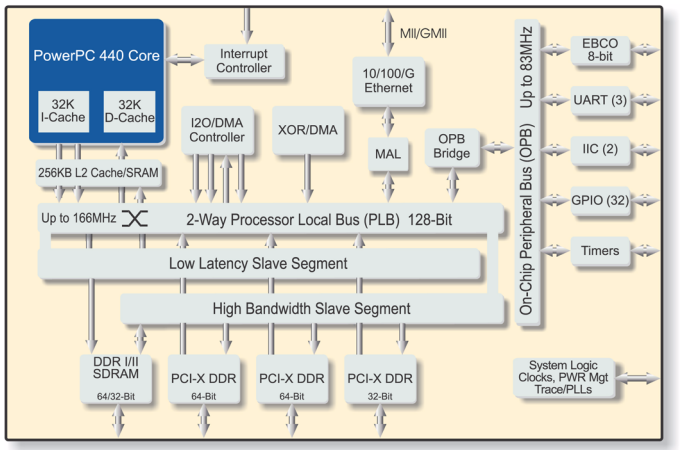
Features

- Speed (frequency): 533 MHz to 667 MHz
- Performance: 2.0 DMIPS/MHz (1,334 DMIPS @ 667 MHz peak)
- 32-Kbyte-I/32-Kbyte D L1 caches and 256-Kbyte L2/SRAM with parity protection
- 32/64-bit DDR I/DDR II SDRAM controller, for DDR166/333 and DDR333/667 operation
- PCI-X 3.3-V multiport bridge
- Three PCI-X version 2.0 interfaces, up to 133 MHz / DDR266
- Opaque PCI-X to PCI-X bridge functionality
- Ability to boot from the primary PCI-X bus memory
- RAID 5 and RAID 6 acceleration hardware for parity generation and check functions
- Intelligent messaging unit (I2O specification)
- Two-channel DMA included with I2O, one-channel DMA included with XOR
- External bus control (EBC) Interface (up to 83 MHz) supporting up to three ROM, RAM, or EPROM peripheral devices
- One 10/100/1000-Mbits/s Ethernet MAC, full-duplex GMII/MII interface with DMA capability by means of memory access layer (MAL)
- Three serial ports (16750-compliant UARTs) with 64-byte FIFOs
- Two IIC controllers
- Up to 32 general-purpose I/Os (GPIO)
- General-purpose timers
- Universal programmable interrupt controller supporting six external interrupt sources and 56 internal sources.
- Support for JTAG board testing, JTAG debuggers, and 4XX instruction trace interface

For more information, please visit ***http://www.amcc.com.***

Specifications

Technology
• 0.13 µm CMOS
Performance (estimated)
• 1,334 Dhrystone MIPS @ 667 MHz,
Frequency
• CPU: 533 to 667 MHz
• Memory: 32-bit width: up to 1.3 Gbytes/s (DDR333) 64-bit width: up to 5.3 Gbytes/s (DDR667)
• PCI-X: primary side: 64-bit width @ 133 MHz, DDR266, 2.1-Gbyte/s peak throughput PCI-X secondary side: 64-bit width @ 133 MHz, DDR266, 2.1-Gbyte/s peak throughput PCI-X secondary side: 32-bit width @ 133 MHz, DDR266, 1.1-Gbytes/s peak throughput
Typical Power Dissipation
• < 6.0 W @ 533 MHz
Case Temperature Range
• -40° C to +100° C
Power Supply
• 1.5 V (logic), 2.5 V/1.8 V (SDRAM), 3.3 V/1.5 V (x3 PCI-X), 3.3 V (Ethernet, other I/O) signal I/Os
Signal I/Os
• 524
Packaging
• 783 FC-PBGA, 29 mm x 29 mm with 1.0-mm pad pitch



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