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(12) # EUROPEAN PATENT APPLICATION

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(54) **Personal computer interface.**

(57) Disclosed is an apparatus for interfacing a personal-computer to a 3274/6 compatible cluster controller of a 3270 type system, the apparatus employing a special high-speed processor.
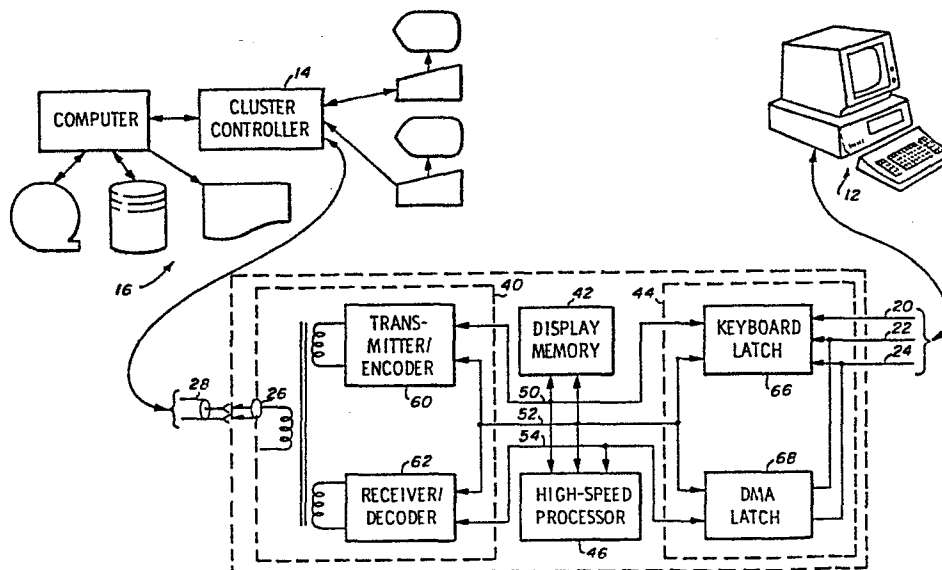
Fig_1

EP 0 135 127 A2

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to personal-computers generally and more specifically to an apparatus for interfacing a personal-computer to an IBM 3274/6 compatible cluster controller of a 3270 system.

Description of the Prior Art

It is common practice to couple a number of terminals to a computer (host) to permit resource sharing. In what is commonly referred to as a 3270-type system, a main frame computer of the type that is commonly designated 370, 30XX or 43XX by the International Business Machines (IBM) Corporation is connected to one, or more, IBM 3274/6-type cluster controllers (control units) each of which is connected to a number of IBM 3278/9-type terminals (display stations). In such a system, controller-terminal communication is over a single-wire coaxial cable by means of a serial by bit, dipulse (biphase) format at a relatively high (2.3587 Megahertz bit) rate. (The protocols for controller-terminal interconnection and communication are discussed in the IBM document entitled "IBM 3274, 3276 Control Unit to Device Product Attachment Information".) Unfortunately, IBM 3278/9-type terminals (and terminals compatible therewith) are relatively expensive.

Personal-computers, such as, for example, those of the IBM-type (IBM PC), are gaining popularity as an alternative to the use of a terminal connected to a system of the above-mentioned type. Although providing considerable computing power, absent a connection to such a system, personal-computers are disadvantageous in that they are unable to provide many of the resources of such a system including the computing power of

1 a main frame computer, the data base of the main frame computer

2 and/or the system and the networking power of the system.

3 (For a technical discussion of the IBM personal-computer the

4 reader is referred to the IBM user manuals generally and par-

5 ticularly to the manual designated "Hardware Design and Interface

6 Information 6025008.")

7 SUMMARY OF THE PRESENT INVENTION

8 It is therefore an object of the present invention to

9 provide a relatively inexpensive apparatus for interfacing a

10 personal computer to an IBM 3274/6 compatible cluster controller.

11 Another object of the present invention is to provide a

12 processor of sufficient speed and economy to be suitable for use

13 in interfacing a personal-computer to an IBM 3274/6 compatible

14 cluster controller.

15 Briefly, the preferred embodiment of an apparatus for

16 interfacing a personal-computer to an IBM 3274/6 compatible

17 cluster controller employs a cluster-controller interface (40),

18 a display memory (42), a personal-computer interface (44), and a

19 high-speed processor (46), all interconnected by a destination

20 bus (50), a control bus (52), and a source bus (54). The

21 processor (46) has a multiplexer (100) for developing a jump

22 address from source bus data, for developing another jump address

23 from data on a B bus (150) and for selecting one of the jump

24 addresses; a program counter (102) for developing an instruction

25 address by incrementing the previous address or loading the

26 selected jump address; a program store (104) for retrieving an

27 instruction addressed by the program counter; an immediate

28 buffer (108) for placing as data the immediate portion of each

29 instruction (if any) on the source bus; circuitry (114) for

30 decoding each instruction; circuitry (116) for developing machine

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1 cycle timing signals; an F register (stack) (122) for storing data

2 placed on the destination bus and for placing stored data on the

3 source bus; a B register (accumulator)(124) for storing (temporary

4 and working result) data placed on the destination bus and for

5 placing stored data on the B bus; an arithmetic logic unit (ALU)

6 (128) for performing the operation specified by the instruction

7 on the source bus data (operand) and on the B bus data (operand)

8 to develop data (results) on the destination bus; circuitry (136)

9 for testing a (processor external)(hardware) condition for

10 (direct) jump on condition (to an indirect address) instructions;

11 a destination bus control register (138); a source bus control

12 register (140); and an output (processor external hardware

13 control) register (142).

14   The present invention is advantageous in that it permits

15 a personal-computer to be economically interfaced to an

16 IBM 3274/6 compatible cluster controller.

17   Another advantage of the present invention is that it

18 permits the construction of economical high-speed processors.

19   These and other objects and advantages of the present

20 invention will no doubt become apparent to those skilled in

21 the art after reading the following detailed description of the

22 preferred embodiment which is illustrated in the several figures

23 of the drawing.

24   IN THE DRAWING

25   FIGURE 1 is a combined block diagram and perspective

26 view of a personal-computer to IBM 3274/6 compatible cluster

27 controller interfacing apparatus in accordance with the present

28 invention; and

29   FIGURES 2A-2D are block diagrams further illustrating

30 the high-speed processor shown in FIGURE 1.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Illustrated in FIGURE 1 of the drawing generally designated by the number 10 is the preferred embodiment in accordance with the present invention of an apparatus for interfacing a personal-computer, such as, for example, the IBM-type personal-computer illustrated at 12, to an IBM 3274/6 compatible cluster controller of a 3270 system, the cluster controller being designated 14 and the system being generally designated 16. Preferably, the components of apparatus 10 are interconnected by means of a printed circuit board of suitable configuration for disposition within the personal-computer, computer 12, within an expansion slot (connector) to access the computer's address, data and control buses, respectively designated 20, 22 and 24. Additionally, apparatus 10 has a connector 26 for connection by a coaxial cable 28 to cluster controller 14.

Apparatus 10 includes as principal components a cluster controller interface 40, a display memory 42, a personal-computer interface 44 and a high-speed processor 46 all interconnected by an 8-line destination bus 50, a control bus 52 and an 8-line source bus 54.

Interface 40 has a portion 60 which is responsive to signals developed on control bus 52 and operative to encode in IBM 3270 serial-bit format the byte of data represented by signals developed in parallel format on the eight lines of destination bus 50 and to develop a signal representing the encoded bits for transmission over coaxial cable 28 to cluster controller 14. Additionally, interface 40 has a portion 62 for receiving from cluster controller 14 by way of coaxial cable 28 a signal representing bits encoded in IBM 3270 serial-bit format, the portion being operative to decode the bit signal to develop corresponding

1 data bytes, and, responsive to signals developed on control bus

2 54, operative to develop on the eight lines of source bus 54,

3 signals representing in parallel format the current data byte.

4 Preferably, interface 40 employs a pulse transformer

5 and three devices, respectively designated DP8340, DP8341 and

6 DS3487 by the National Semiconductor Corporation, all configured

7 substantially as suggested in the data sheets published by the

8 National Semiconductor Corporation for the DP8340 and DP8341

9 devices. Additionally, interface 40 employs an inverter (circuit)

10 of the type that forms one circuit of the several circuits

11 integrated in a device of the type which is commonly designated

12 74LS04 of the 7400 low-power Schottky TTL series. The inverter is

13 employed to develop an (active-high) signal for enabling the data

14 output of the DP8341 device from an (active-low) signal developed

15 on a line of control bus 52 for reading the device register.

16 Further, interface 40 employs a pair of D-type flip-flop

17 (circuits) of the type that are collectively integrated in a

18 device of the type commonly designated 74LS74. Each of the

19 flip-flops is employed to latch the (binary) state of the signal

20 developed at a respective one of the D10 and D11 DP8341 device

21 outputs to develop a (latched) signal for driving a respective

22 one of two lines of control bus 52, the flip-flops being latched

23 responsive to the signal used for reading the DP8341 register.

24 An 18.87 Megahertz signal developed by the DP8340 device is used

25 to drive a line of control bus 52 to serve as an apparatus 10

26 master clocking signal.

27 Display memory 42 provides a repository (double buffer)

28 for data (characters) transmitted by cluster controller 14 for

29 updating the visual display generated by the personal-computer,

30 computer 12, to permit the task of receiving the data from the

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cluster controller to be separated from the task of updating the

personal-computer display memory. Additionally, memory 12 pro-

vides processor 46 convenient access to the data used in gene-

rating the visual display.

Preferably, for this purpose, memory 42 employs

(three or) four random access memory (RAM) devices of the type

commonly designated 6116. Each of the 11 address inputs of each

of the four RAM devices is connected to a respective one of the

11 lowest order lines of a 13-line, memory 12 internal, address

bus; and, each of the eight data inputs/outputs of each of the

four RAM devices is connected to a respective one of the lines

of an 8-line, memory 12 internal, data bus.

A pair of devices of the type commonly designated

74LS273 (octal latch) are employed for latching the (binary) state

of the signals developed on destination bus 50 to develop signals

for driving the memory 12 internal address bus. Each of the

eight data inputs of one of the 74LS273 devices (a device

referred to as the low (L) address register) is connected to a

respective one of the eight lines of destination bus 50; and, the

eight data outputs of the device are connected each to a respec-

tive one of the eight lowest order lines of the memory 12

internal, address bus. Five of the data inputs of the other

74LS273 device (a device referred to as the high (H) address

register) are connected each to a respective one (orderwise) of

the five lowest order lines of destination bus 50; and, the

corresponding five data outputs of the device are connected each

to a respective one (orderwise) of the five highest order lines

of the memory 12 internal, address bus. The (active-low) reset

input of each of the 74LS273 devices is connected to a line of

control bus 52 on which an (active-low) apparatus 12 master

1 resetting signal is developed. The latch (clock) input of each

2 of the 74LS273 devices is driven responsive to a signal developed

3 on a respective one of two lines of control bus 52, each of the

4 lines being coupled to the respective input by a respective one

5 of two inverter (circuits) of the type which (with other in-

6 verter circuits) are integrated in a device of the type commonly

7 designated 74LS04. Each of the two lowest order lines of the

8 memory 42 internal, address bus is connected to a respective

9 one of the two inputs of a 74LS32 2-input OR gate (circuit), the

10 output of which is connected to a line of control bus 52.

11 A device of the type commonly designated 74LS139

12 (2-to-4 line decoder/demultiplexer) is employed for RAM device

13 selection. The two decode/multiplex inputs of the 74LS139

14 device are each connected to a respective (orderwise) one of the

15 two highest order lines of the memory 12 internal, address bus;

16 and, each of the four device (active-low) outputs is connected to

17 the (active-low) chip select input of a respective one of the

18 four RAM devices. The (active-low) enable input of the 74LS139

19 device is connected to a low logic level potential (circuit

20 ground). The (active-low) output-enable input of each of the

21 RAM devices is connected to a (single) line of control bus 52.

22 A 74LS74 type flip-flop (circuit) is employed for

23 developing an (active-low) RAM device writing signal. The

24 (active-low) set input of the flip-flop is connected to a high

25 logic level potential (+5 volts); and, the flip-flop (active-low)

26 reset and (active-high) data inputs are connected to the control

27 bus 50 line on which the apparatus 10 master resetting signal is

28 developed. The clock input of the flip-flop is connected to the

29 control bus 50 line on which the apparatus 10 master clocking

30 signal is developed; and, the flip-flop inverted data output is

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1 connected to the (active-low) write input of each of the four RAM
2 devices.

3 Finally, a pair of devices of the type commonly designa-
4 ted 74LS244 (octal tri-state drivers) are employed, one being
5 connected to selectively develop on each of the eight lines of
6 the memory 42 internal, data bus a signal which corresponds in
7 (binary) state with that of a signal developed on a respective one
8 of the eight lines of destination bus 50 and the other being
9 connected to selectively develop on each of the eight lines of
10 source bus 50 a signal which corresponds in state with that of a
11 signal developed on a respective one of the eight lines of the
12 internal data bus. The two output-enable inputs of the former
13 74LS244 device are connected to the memory 42 flip-flop inverted
14 data output; and, the two output-enable inputs of the latter
15 74LS244 device are connected to a line of control bus 52.

16 Personal-computer interface 44 has a portion 66 for
17 receiving from the personal-computer, computer 12, a byte of data
18 identifying a computer keyboard key closure, the portion being
19 operative to latch the state of signals developed by the computer
20 on computer data bus 22 at each of the times identified by com-
21 puter control bus 24 signals and, responsive to signals developed
22 on apparatus 10 control bus 52, being operative to develop on the
23 eight lines of source bus 54 signals representing the current
24 latched signal states. Additionally, interface 44 has a por-
25 tion 68 for providing the personal-computer, computer 12, a
26 byte of data for use by the computer in updating its visual dis-
27 play memory, the portion being operative to latch the state of
28 each of the signals developed on the eight lines of destination
29 bus 50 at each of the times identified by an apparatus 10 control
30 bus 52 line signal and, responsive to signals developed by the
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1 personal-computer on computer control bus 24, being operative to

2 develop on computer data bus 22 signals representing the current

3 latched signal states.

4   Preferably, keyboard data byte latching portion 66

5 employs a device of the type commonly designated 74LS244 (octal

6 driver), a device of the type commonly designated 74LS273 (octal

7 latch) for latching the state of signals representing a nibble

8 (4-bits) of personal-computer, computer 12, developed control

9 data, a device of the type commonly designated 74LS374 (octal

10 tri-state latch)(K register) for latching signals representing

11 the byte of keyboard data developed by the computer and circuitry

12 for address decoding. The 74LS244 device develops on a portion

13 66 internal, data bus buffered signals representing those

14 developed on the personal-computer, computer 12, data bus (bus

15 22). For this purpose, each of the eight data inputs of the

16 74LS244 device is connected to a respective one of the eight

17 lines forming bus 22; and, each of the eight data outputs of the

18 device is connected to a respective one of eight lines forming

19 the portion 66 internal, data bus. The two (active-low) enable

20 inputs of the 74LS244 device are connected to a low logic level

21 potential (circuit ground).

22   Four of the data inputs of the 74LS273 device are con-

23 nected each to a respective one of the four lowest order lines of

24 the portion 66 internal, data bus; and, the three highest order

25 data outputs of the four corresponding data outputs of the device

26 are connected each to a respective one of three lines of control

27 bus 52. The other data output of the 74LS273 device is connected

28 to one input of a 74LS00 type 2-input NAND gate (circuit). The

29 other input of the NAND gate is connected to the reset input of

30 the 74LS273 device; and, the output of the NAND gate is connected

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1 to a 74LS04 type inverter (circuit) which develops the apparatus

2 10 resetting signal used to drive the respective line of control

3 bus 52. A signal for driving the (active-low) reset input of the

4 74LS273 device is developed by a 74LS04 type inverter (circuit)

5 from a reset signal developed on personal-computer, computer 12,

6 control bus 24.

7 Each of the eight data inputs of the 74LS374 device is

8 connected to a respective one of the portion 66 internal, data

9 bus; and, each of the eight data outputs of the device is

10 connected to a respective one of the eight lines of source bus

11 54. The output-enable input of the 74LS374 device is connected

12 to a line of control bus 52.

13 The address decoding circuitry of interface 44 portion

14 66 is responsive to signals developed by the personal-computer,

15 computer 12, to develop signals for latching (clocking) the

16 74LS273 and 74LS374 devices. When employed with a personal-

17 computer of the IBM type (IBM PC), portion 66 is, preferably,

18 responsive to signals developed by the personal-computer, com-

19 puter 12, when the computer executes an output instruction

20 which specifies a preselected one of the two (control) ports

21 commonly designated 2EE and 3EE and operative to develop the

22 74LS273 device latching signal. Further, the circuitry is re-

23 sponsive to the signals developed when an output instruction

24 which specifies a pre-selected one of the two (keyboard) ports

25 commonly designated 2EF and 3EF is executed and is operative to

26 develop a signal for latching the 74LS374 device.

27 Specifically, the latch (clock) input of the 74LS273

28 device is connected to the output of a first 74LS00 type 2-input

29 NAND gate (circuit) a first input of which is coupled by a

30 74LS04 type inverter to the lowest order address line (the line

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1 commonly designated A0) of personal-computer, computer 12, address

2 bus 20. The second input of the first NAND gate is coupled by

3 a 74LS04 type inverter to the output of a first 74LS32 type

4 2-input OR gate one input of which is connected to the output of

5 a second 74LS32 type 2-input OR gate the inputs of which are

6 connected each to a respective one of the (active-high and

7 active-low) lines of the personal-computer control bus 24 that

8 are commonly designated address enable and input/output write.

9 The other input of the first NOR gate is connected to the output

10 of a third 74LS32 type 2-input OR gate one input of which is

11 connected to the personal-computer address bus (bus 20) line

12 commonly designated A4. The other input of the third OR gate is

13 connected to the output of a 74LS30 type 8-input NAND gate seven

14 of the eight inputs of which are connected each to a respective

15 one of the personal computer address bus (bus 20) lines commonly

16 designated A1, A2, A3, A5, A6, A7 and A9. The eighth input of the

17 74LS30 type NAND gate is connected to the output of a preselected

18 (by jumper) one of a pair of 74LS04 type inverters which are

19 connected in series and which are driven by the signal developed

20 on the personal-computer address bus (bus 20) line commonly

21 designated A8. The latch (clock) input of the 74LS374 device is

22 connected to the output of a second 74LS00 type 2-input NAND

23 gate. The first input of the second NAND gate is coupled to the

24 first input of the first NAND gate by a 74LS04 type inverter;

25 and, the second input of the second NAND gate is connected to the

26 second input of the first NAND gate. Finally, a 74LS74 type

27 flip-flop is employed, the data and (active-low) set inputs of

28 which are connected to a high logic level potential; the clock

29 input of which is connected to the output of the second NAND gate;

30 the data output of which is connected to a line of control bus

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1 52; and, the (active-low) reset input of which is coupled by a

2 74LS04 type inverter to the output of a 74LS00 type 2-input

3 NAND gate having one input connected to the output/enable input

4 of the 74LS374 device and having the other input connected to the

5 line of control bus 52 on which the apparatus 10 master

6 resetting signal is developed.

7 Preferably, DMA latching portion 68 (of interface 44)

8 employs a device of the type commonly designated 74LS374 for

9 latching the signals representing the data byte. Additionally,

10 portion 68 employs control circuitry that includes a first and a

11 second 74LS32 type 2-input OR gate, a 74LS04 type inverter and a

12 first and a second 74LS109 type J-K flip-flop. Each of the eight

13 data inputs of the 74LS374 device is connected to a respective

14 one of the eight lines of designation bus 50; and, the eight

15 data outputs of the device are connected each to a respective one

16 of the eight lines forming personal-computer, computer 12, data

17 bus 22. The latch (clock) input of the 74LS374 device is con-

18 nected to the output of the inverter the input of which is

19 connected to a line of control bus 24; and, the (active-low)

20 output-enable input of the 74LS374 device is connected to the

21 output of the first OR gate. The two inputs of the first OR gate

22 are connected one to the (active-low) line of personal-computer,

23 computer 12, control bus 24 commonly designated input/output

24 request and the second to a pre-selected one (by jumper) of the

25 two computer control lines commonly designated data acknowledge

26 one and data acknowledge two.

27 The J, (active-low) K and (active-low) set inputs of the

28 first flip-flop are connected to a high logic level potential.

29 The clock input of the first flip-flop is connected to the output

30 of the inverter; and, the inverted data output and (active-low)

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1 reset input of the flip-flop are connected to the (active-low) set

2 input of the second flip-flop. The J and (active-low) K inputs

3 of the second flip-flop are connected to a low logic level

4 potential (circuit ground); and, the (active-low) reset input of

5 the flip-flop is connected to the line of control bus 52 upon

6 which the apparatus 10 master resetting signal is developed. The

7 data output of the second flip-flop is connected both to a line

8 of control bus 52 and a pre-selected one (by jumper) of

9 personal-computer, computer 12, control bus 24 lines commonly

10 designated data request one and data request three. Finally,

11 the clock input of the flip-flop is connected to the output of

12 the second OR gate one input of which is connected to the second

13 input of the first OR gate and the other input of which is con-

14 nected to the (active-low) line of personal-computer, computer

15 12, control bus 24 commonly designated memory write.

16 The operation of the various components of apparatus

17 10 is controlled by high-speed processor 46 which is illustrated

18 in detail in FIGURES 2A-2D of the drawing. Processor 46 is

19 shown to include as principal components a jump address multi-

20 plexer, illustrated in FIGURE 2A generally designated 100, a

21 program counter, generally designated 102, a (micro-code)

22 program instruction store, generally designated 104, an instruc-

23 tion register, generally designated 106, an immediate instruction

24 buffer 108, instruction decoding circuitry, illustrated in FIGURE

25 2B generally designated 114, machine cycle generating circuitry,

26 generally designated 116, an (F) register (stack), illustrated

27 in FIGURE 2C generally designated 122, a working (B) register

28 (accumulator) 124, an arithmetic logic unit (ALU), generally

29 designated 128, a temporary (T) register 130, condition testing

30 circuitry, illustrated in FIGURE 2D, generally designated 136,

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1 a destination-bus-control register, generally designated 138, a

2 source-bus-control register, generally designated 140, and an

3 output register, generally designated 142, the components being

4 interconnected by destination bus 50, control bus 52, source bus

5 54, an 8-line B bus 150, and a 16-line instruction bus 152.

6   Multiplexer 100, illustrated in FIGURE 2A, develops

7 two 11-bit jump addresses. The 11 bits of one of the addresses

8 are represented each by the (binary) state of the signal

9 developed on a corresponding ond of 11 lines which include, for

10 lower order bits, the eight lines of source bus 50 and, for

11 higher order bits, three lines collectively designated 202.

12 The other 11 bit address is, preferably, derived from the five

13 bits represented each by the (binary) state of the signal

14 developed on a corresponding one of five of the eight lines of B

15 bus 150. Responsive to a signal developed on a line 200,

16 multiplexer 100 is operative to select one of the two jump

17 addresses.

18   Preferably, for this purpose, multiplexer 100 has three

19 74LS157 type devices (quad 2-to-1 line selectors/multiplexers),

20 respectively designated herein 206, 208 and 210. The select input

21 of each of devices 206, 208 and 210 is connected to line 200;

22 and, the (active-low) enable (strobe) input of each of the

23 devices is connected to a low logic potential (circuit ground).

24 The four data (Y) outputs of device 206 are connected each to a

25 respective one of four lines collectively designated 214. The

26 two highest order data inputs of the four inputs of device 214

27 which are selected when a low logic level potential is

28 developed on line 200 (A inputs) are connected each to a

29 respective one of the two lowest order lines of B bus 150, the

30 other two device 206 selected inputs being connected to a low

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1   logic potential. The other four data inputs of device 206 (B

2   inputs) are connected each to a respective one of the four

3   lowest order lines of source bus 54. The four outputs of device

4   208 are connected each to a respective one of four lines col-

5   lectively designated 216. The three lowest order inputs of the

6   four inputs of device 206 that are selected when a low logic level

7   potential is developed on line 200 are connected to a respective

8   one (orderwise) of the three highest order lines of the five

9   lowest order lines of B bus 150, the remaining device 206 selected

10 input being connected to a high logic level potential. The other

11 four data inputs of device 208 are connected each to a respective

12 one (orderwise) of the four highest order lines of source bus

13 54. Finally, three of the four outputs of device 210 are

14 connected each to a respective one of three lines collectively

15 designated 218; the corresponding three data inputs of the device

16 which are selected when a low logic level potential is developed

17 on line 200 are connected to a low logic level potential; and, the

18 three corresponding data inputs which are not selected by such a

19 potential are each connected to a respective one of the three

20 lines collectively designated 202.

21   Program counter 102 develops a series of (micro-code)

22 program instruction addresses, each by incrementing the previous

23 address or by setting the address to the multiplexer 100

24 selected jump address. Preferably, program counter 102 has

25 three 74LS161 type devices (synchronoush counters), designated

26 therein 122, 124 and 126, connected in cascade to form an 11-bit

27 (12-bit) counter for developing 11 bit instructior addresses.

28 The carry output of device 122 is connected by a line 128 to an

29 enable input of device 124 the carry output of which is connected

30 by a line 130 to an enable input of device 126. The other

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1   enable inputs of devices 122, 124 and 126 are connected to a high

2   logic level potential; and, the (active-low) reset input of each

3   of the devices is connected to the line of control bus 52 upon

4   which the apparatus 10 master resetting signal is developed, the

5   line being designated 232. For incrementing the previous instruc-

6   tion address, the clock input of each of the devices (222, 224

7   and 226) is connected to a line 234; and, for setting the address

8   to the selected jump address, the (active-low) parallel load input

9   of each of the devices is connected to a line 236. The four data

10 inputs of device 222, the four data inputs of device 224 and

11 the three data inputs of device 226 are connected each to a res-

12 pective one of the 11 lines collectively designated 214, 216

13 and 218; and, the corresponding 11 data outputs of the device are

14 connected each to a respective one of 11 lines collectively

15 designated 240.

16   Program store 140 stores a plurality of (micro-code)

17 program instructions, retrieving the addressed one of the instruc-

18 tions. Preferably, program store 140 has two programmable

19 read-only memory (PROM) devices of the type which are commonly

20 designated TBP28S166 and which are designated herein 244 and 246.

21 Each of the address inputs of each of devices 244 and 246 is

22 connected to a respective one of the 11 lines collectively

23 designated 240. The data output lines of device 244 are con-

24 nected each to a respective one of eight lines collectively

25 designated 250; and, those of device 246 are connected each to a

26 respective one of eight lines collectively designated 252.

27   Preferably, instruction register 106 has a pair of

28 74LS273 type devices, designated herein 256 and 258, connected to

29 latch the state of each of the signals developed on the lines

30 collectively designated 250 and 252, responsive to a latching

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1 (clocking) signal developed on a line 260, and to develop on each

2 of the 16 lines of instruction bus 152 a signal having a

3 respective one of the latched states. The 16 lines of instructions

4 bus 152 are designated, in ascending order, 170-185.

5 Buffer 108, which, preferably, has a device of the type

6 generally designated 74LS244, develops on each of the eight

7 lines of source bus 54 a signal which has a state that corres-

8 ponds to the state of the signal developed on a corresponding one

9 of the eight lowest order lines of instruction bus 152 respon-

10 sive to an (active-low) output enabling signal developed on a line

11 264.

12 Preferably, instruction decoding circuitry 114, illus-

13 trated in FIGURE 2B, has a pair of 74LS139 type devices (2-to-4

14 line decoders/demultiplexers), designated herein 300 and 302.

15 The two select inputs of device 300 are connected each to a

16 respective one of the two highest order lines of instruction bus

17 152 (lines designated 174 and 175); and, the two select inputs

18 of device 302 are connected each to a respective one of the next

19 two higher order lines of the instruction bus (lines which are

20 designated 172 and 173). The enable input of device 300 is

21 connected to a low logic level potential; and, the enable input

22 of device 302 is connected to a line 304. Device 300 is operative

23 to develop a low logic level potential on a line 306 when the

24 respective potential levels developed on lines 176 and 175 are

25 both low (00), as is the case for jump instructions; on a line

26 308 when the levels are low and high (01) for ALU instructions;

27 on a line 310 when the levels are high and low (10) for immediate

28 instructions; and on line 304 when the levels are both high (11)

29 for register instructions. When a low logic level potential is

30 developed on line 304, for register instructions, device 302 is

31 operative to develop a low logic level potential on a line 312

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1 when the respective potential levels developed on line 174 and

2 173 are both low (00) for T register to a designated register

3 instructions; on a line 314 when the levels are low and high (01)

4 for bit register instructions; on a line 316 when the levels are

5 high and low (10) for vectored return instructions; and on a

6 line 318 when the levels are both high (11) for conditional

7 vectored jump instructions.

8   Additionally, instruction decoding circuitry 114 has a

9 pair of flip-flops and a number of inverters and gates all of the

10 7400 low-power Schottky TTL type connected to develop processor

11 46 controlling signals including: an (active-low) F register 122

12 output enabling signal on a line 330; a T register 130 latching

13 signal on a line 332; an (active-low) immediate buffer 208 output

14 enabling signal on line 264; an (active-low) destination register

15 control enabling signal on a line 334; an (active-low) S register

16 122 write enabling signal on a line 336; an (active-low) program

17 counter 102 (jump) loading (setting) signal on line 236; a

18 multiplexer 100 jump address selecting signal on line 200, an

19 output bit register 142 loading signal on a line 338, and a

20 program counter 102 clocking signal on line 234.

21   Preferably, machine cycle generating circuitry 116

22 has a pair of 74LS109 type flip-flops, designated herein 350 and

23 352, and a 74LS109 type device (2-to-4 line decoder/demultiplexer),

24 designated herein 354. Flip-flops 350 and 352 and device 354

25 are connected to respond to the apparatus 10 master clocking signal

26 developed by interface 10 on the respective line, designated

27 360, of control bus 52, to develop on four lines of the control

28 bus (active-low) signals defining the four machine cycles which

29 comprise each instruction period of processor 46 including a T0

30 "bar" signal on a line 362, a T1 "bar" signal on a line 364, a

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1 T2 "bar" signal on a line 366, and a T3 "bar" signal on a line

2 368.

3   Preferably, F register (stack) 122, illustrated in

4 FIGURE 2C, has a pair of devices of the type commonly designated

5 74LS189, designated herein 400 and 402, and a device of the

6 74LS240 type, designated herein 404. Devices 400, 402 and 404 are

7 connected to latch in a stack register addressed by the signals

8 developed on the four lowest order lines of instruction bus 152

9 the state of each of the signals developed on the eight lines of

10 destination bus 50 at the time designated by the (active-low)

11 F register latching (write enabling) signal developed on line 336

12 and to develop on the eight lines of source bus 54 signals each

13 having a respective one of the states latched in the stack

14 register addressed by the bus 152 signals when enabled by the

15 (active-low) output enabling signal developed on line 330.

16   B register (accumulator) 124, preferably, has a 74LS374

17 type device connected to latch the state of each of the signals

18 developed on the eight lines of destination bus 50 at the time

19 designated by the latching signal developed on a line 410 and to

20 develop on the eight lines of B bus 150 signals each having a

21 resepctive one of the latched states.

22   Arithmetic logic unit (ALU) 128 performs the arithmetic

23 or logic operation: selected by the signals developed on instruc-

24 tion bus 152 on the byte of data (A operand) represented by

25 signals developed on source bus 152 and on the byte of data (B

26 operand) represented by signals developed on B bus 150 to

27 develop as a result a byte of data represented by signals

28 developed on destination bus 50 and a signal on a line 414

29 representing a resultant inverse carry.

30   Preferably, ALU 128 has a pair of 74LS181 type devices,

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designated herein 416 and 418, and a 74LS373 type device, desig-
nated herein 420. The inputs commonly designated S0, S1, S2
and S3 (function select) of both devices 416 and 418 are con-
nected to the respective (orderwise) four most significant lines
of the 12 least significant lines of instruction bus 152 (lines
designated 178-181). The input commonly designated M (mode
control) of both devices 416 and 418 is connected to the thirteen-
th least significant line (182) of instruction bus 152; and, the
input commonly designated inverse carry of device 418 is connected
to the fourteenth least significant line (183) of the instruction
bus. The inverse carry output of device 418 is connected by a
line 422 to the inverse carry input of device 416; and, the
inverse carry output of device 416 is connected to line 414.

The inputs of device 418 commonly designated A0-A3
are connected each to a respective one of the four lowest order
lines of source bus 54; and, those of device 416 are connected
each to a respective one (orderwise) of the four highest order
lines of the source bus. Similarly, inputs of device 418
commonly designated B0-B3 are connected each to a respective one
of the four lowest order lines of B bus 152; and, those of
device 416 are connected each to a respective one (orderwise) of
the four highest order lines of the B bus. The device outputs
commonly designated F0-F3 are connected to device 420, those of
device 418 each by a respective one of four lines collectively
designated 424 and those of device 416 each by a respective one
of four lines collectively designated 426.

Device 420 is connected to latch the state of each of
the signals developed on the lines collectively designated 424
and 426 at the time designated by the latching signal developed
on line 332 and to develop on the eight lines of bus 50 signals

-20-

1 each having a respective one of the latched states, signals

2 corresponding to those developed by device 418 are developed each

3 on the respective one of the four lowest order lines of bus

4 50; and, signals corresponding to those developed by device 416

5 are developed each on the respective (orderwise) one of the

6 four highest order lines of the bus.

7   It should be noted that device 420 is not required in

8 embodiments employed in applications in which the resultant loss

9 in processor 46 speed is not significant. In these embodiments,

10 the F0-F3 outputs of devices 418 and 416 are directly connected

11 to the corresponding lines of destination bus 50.

12   Condition testing circuitry 136, illustrated in FIGURE

13 20, ascertains the (binary) state of a selected one of a number

14 of apparatus 10 component (hardware) conditions each of which is

15 evidenced by a logic level potential developed by a component on

16 a respective line (generally of control bus 50). Circuitry 136

17 is operative to develop on a line 500 a logic level potential

18 the state of which corresponds to that developed on the selected

19 condition line.

20   Preferably, circuitry 136 has a 74LS74 type flip-flop,

21 designated herein 504, and a 74LS04 type inverter, designated

22 herein 506, connected to develop a signal on line 508 by latching

23 and inverting the inverse carry signal developed on line 414.

24 Additionally, circuitry 136 has a pair of 74LS23 type 4-input NOR

25 gates, designated herein 512 and 514, and a 74LS00 type 2-input

26 NAND gate, designated herein 516, connected to develop on a

27 line 518 a signal having a low logic level only when a low logic

28 level potential is developed on each of the eight lines of des-

29 tination bus 50. Further, circuitry 136 has a pair of 74LS151

30 type devices (data selector/multiplexer), designated herein 522

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-21-

1 and 524, a 74LS04 type inverter, designated herein 526, and a

2 74LS32 type 2-input OR gate, designated herein 528. The three

3 select inputs of both devices 522 and 524 are connected to the

4 three highest order lines of the twelve lowest order lines of

5 instruction bus 152 (lines designated 178-180). The enable input

6 of device 524 is connected to the next higher order line (line

7 181) of instruction bus 152; and, the enable input of device 522

8 is coupled to the line by inverter 526. The data output of each

9 of devices 522 and 524 is connected to a respective one of the

10 two inputs of OR gate 528 the output of which is connected to

11 line 500.

12 The five lowest order data inputs of device 522 are

13 connected (in ascending order) to the lines of control bus 52 on

14 which: the (cluster controller interface 40, portion 60) DP8340

15 device develops a transmitter register full signal; the DP8340

16 device develops a transmitter active signal; the (personal-

17 computer interface 44, keyboard data byte latching) portion 66

18 flip-flop develops a signal indicating that a keyboard data byte

19 is available; the second (interface 44, DMA latching) portion 68

20 flip-flop develops the data request signal; and the display

21 memory 42 OR gate develops a signal indicating that a low logic

22 potential is being developed on both of the two lowest order lines

23 of the memory 12 internal address bus. The next higher order

24 data input of device 522 is connected to line 518.

25 The two lowest order data inputs of device 524 are

26 connected, respectively, to a high logic level potential and to

27 line 508. The remaining six data inputs of device 524 are

28 connected (in ascending order) to the lines of control bus 52 on

29 which (cluster controller interface 40) portion 60 develops: the

30 latched D10 signal; the latched D11 signal; a (EP8341 device

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1 generated) receiver error signal; a (DP8341 device generated)

2 receiver data available signal; and a (DP8341 device generated)

3 receiver active signal.

4 Source bus control register 140 designates (enables)

5 the source of signals driving source bus 54. Preferably, register

6 140 has a 74LS04 type inverter, designated herein 540, a 74LS10

7 type 3-input NAND gate, designated herein 542, and a 74LS139

8 type device (2-to-4 line decoder/demultiplexer), designated herein

9 544. Device 544 is connected to develop a source bus 54 access

10 (output) enabling signal on a line of control bus 52 selected by

11 signals developed on the two lowest order lines of instruction bus

12 152 (the lines being designated 170 and 172), when enabled by a

13 signal developed on a line 546 by the inverter and NAND gates

14 (540 and 542). The three highest order outputs of the four data

15 outputs of device 544 are connected (in ascending order) to

16 lines of control bus 52 to develop: a signal to enable the output

17 of the 74LS374 device of (personal computer interface 44, keyboard

18 data byte latching) portion 66; the (cluster controller interface

19 40) portion 60, signal for reading the DP8341 register; and a

20 signal to enable the outputs of the 74LS244 device of display

21 memory 42.

22 Destination bus control register 138 designates the

23 destination of signals driving destination bus 50. Preferably,

24 register 138 has a 74LS138 type device (3-to-8 line decoder/-

25 demultiplexer), designated herein 550, and a 74LS04 type inverter,

26 designated herein 552. Device 550 is connected to develop a

27 destination bus 50 latching signal on a line of control bus 52

28 selected by signals developed on the three highest order lines of

29 the eight lowest order lines of instruction bus 152 (lines 175-

30 177) when enabled by a (high logic level potential) signal

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1 developed on (the active-low reset) line 232 and a (active-low)

2 signal developed on line 334. The seven lowest order outputs of

3 device 550 are connected (in ascending order) to lines of control

4 bus 52 to develop: a personal computer, computer 12, interrupt

5 request signal; a (cluster controller interface 40, portion 60)

6 DP8340 device idle response signal; a (personal computer interface

7 44 DMA latching) portion 66, inverted driving signal (74LS374

8 device clocking signal); a DP8340 device register (transmit)

9 loading signal; the B register latching (clocking) signal; a

10 display memory 42 driving (L register clocking) signal; and

11 another display memory 42 driving (H register clocking) signal.

12   · Output register 140 is operative to develop (simul-

13 taneously) on each of a number of lines of control bus 52 (and

14 the lines collectively designated 202) a logic level potential the

15 (binary) state of which is (individually) controllable.

16 Preferably, register 140 has a pair of devices of the type

17 commonly designated DM9334 (bit registers), designated herein 570

18 and 572, a pair of 74LS00 type 2-input NAND gates, designated

19 herein 574 and 576, and a 74LS04 type inverter, designated

20 herein 578. The three address inputs of devices 570 and 572

21 are connected each to respective ones of the three lowest order

22 lines of instruction bus 152 (lines designated 170-172); and,

23 the data input of each of the devices is connected to the twelfth

24 lowest order line of the bus (designated 181). The NAND gates and

25 inverters (574, 576 and 578) are connected to develop signals for

26 enabling a one of devices 570 and 572 selected by the state

27 of the signal developed on (line 173) the fourth lowest order line

28 of instruction bus 152. The three lowest order outputs of device

29 570 are connected each to a respective one of the three lines

30 collectively designated 202 to develop signals forming a bank

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1 selecting portion of the signals used by multiplexer 100 when

2 developing one of the two jump addresses, The remaining five

3 device 570 outputs are connected to respective lines of control

4 bus 52, the three lower order outputs for controlling (driving),

5 respectively, the (cluster interface 40, portion 60) DP8340 device

6 D10, D11 and parity inputs. The eight data outputs of device 570

7 are connected to respective lines of control bus 52, the first,

8 third and fifth lowest order outputs for controlling (driving):

9 the (cluster interface 40, portion 60) DP8340 device parity

10 (even/odd "bar") input; DP8341 device (data/status "bar") output

11 input; and (display memory 42) RAM device write input.

12   Following is the preferred processor 46 instruction

13 format.

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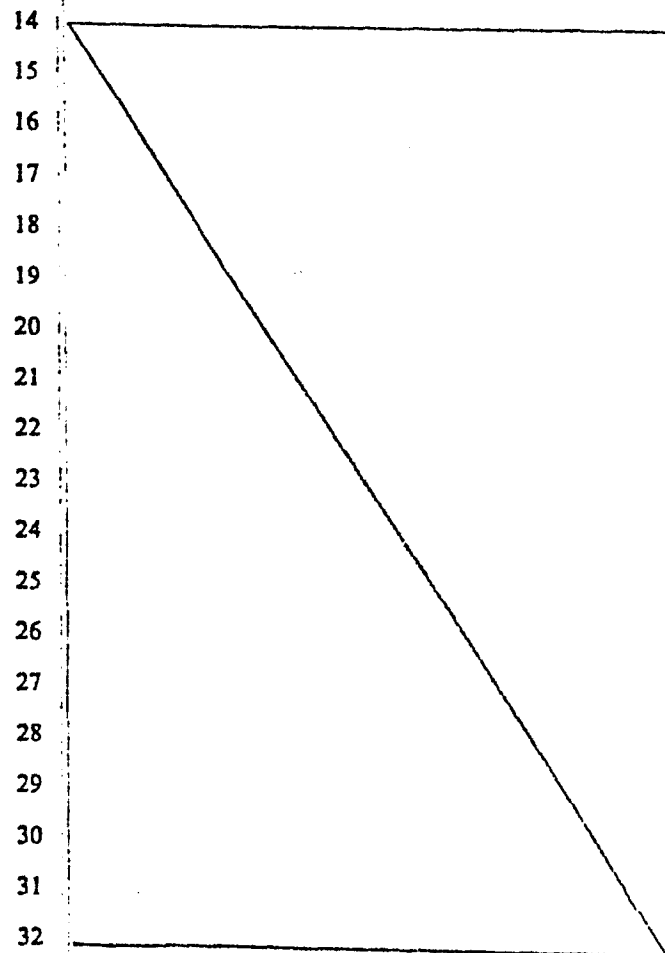
```
              PROCESSOR 46   INSTRUCTION FORMAT

15                8 7             0
X X X XIX X X XIX X X XIX X X X

NOTE: * = DON'T CARE

JMP INSTRUCTION:

OP   NOT COND        ADDR
---  - --------  ----------------
0 0 * XIX X X XIX X X XIX X X X

ALU INSTRUCTION:

OP     ALU OP   DEST   SOURCE
---  ------------ ----- ----------
0 1 X XIX X X XIX X X XIX X X X

     ALU OP CODE BITS 8 -> 13

           BIT  8 = S0      BIT 11 = S4

           BIT  9 = S1      BIT 12 = M

           BIT 10 = S3      BIT 13 = Cn

IMMEDIATE INSTRUCTION:

OP     ALU OP       DATA
---  ------------ ----------------
1 0 X XIX X X XIX X X XIX X X X

REGISTER INSTRUCTION: ( T REG TRANSFER TO REG INSTRUCTION )

   OP          DEST REG # IN REG FILE
--------              --------
1 1 0 0I* * * *I* * * 1IX X X X

   OP          DEST  REG
--------          -----
1 1 0 0I* * * *IX X X 0I* * * *

BIT REGISTER INSTRUCTION:

   OP  VALUE            BIT #
-------- -            -------
1 1 0 1IX * * *I* * * *IX X X X

RETURN REG FILE:

   OP                     REG #
--------                -------
1 1 1 0I* * * *I* * * *IX X X X

JMP RECEIVER VECTOR:

   OP
--------
1 1 1 1I* * * *I* * * *I* * * *

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```

BIT REGISTER DEFINITIONS

BITS 765	REGISTER
000	T REGISTER ONLY (RESULT ALWAYS IN T REG)
001	H DISPLAY ADDRESS, 3 BITS * * * *I* X X X
010	L DISPLAY ADDRESS, 8 BITS
011	B REGISTER (ACCUMULATOR)
100	X REGISTER (XMT REG)
101	D REGISTER, DMA DATA INPUT REGISTER. WHEN USED AS DESTINATION IT INITIATES A SINGLE BYTE DMA TRANSFER. IT SHOULD NOT BE USED MORE OFTEN THAN EVERY 4 uSEC.
110	WHEN USED AS DESTINATION IT INITIATES AN INTERRUPT ON LEVEL 6

ALU SOURCE REGISTER DEFINITIONS

BITS 4 3210	USE
0 0000 ^ I v 0 1111	REGISTER FILE 0 - 15
1 0000	DISPLAY RAM
1 0001	R REGISTER (RECEIVER REGISTER)
1 0010	K REGISTER (KEYBOARD INPUT)
1 0011	NOT USED

BIT REGISTER DEFINITIONS

BITS 3210	VALUE	FUNCTION
0000	X	BANK SELECT BIT 0 (LSB)
0001	X	BANK SELECT BIT 1
0010	X	BANK SELECT BIT 2 (MSB)
0011	X	TRANSMIT DATA BIT 10
0100	X	TRANSMIT DATA BIT 11
0101	0	TRANSMIT DATA BIT 10 = PARITY
0110		NOT USED
0111		NOT USED

0135127

1000	0	TRANSMIT ODD PARITY
1000	1	TRANSMIT EVEN PARITY
1001		NOT USED
1010	0	RECEIVER DATA = ERROR CODES
1010	1	RECEIVER DATA = DATA
1011		NOT USED (OLD DMA)
1100	X	DISPLAY RAM WRITE, T REGISTER IS WRITTEN WHILE 1 AND MUST BE RESET BY THE PROCESSOR IN THE NEXT INSTRUCTION.
1101		NOT USED
1110		NOT USED
1111		NOT USED

JUMP INSTRUCTION CONDITION CODES

TRUE CONDITION: BIT 12 = 0

NOT TRUE CONDITION: BIT 12 = 1

BITS 11-8	TRUE CONDITION
0000	UNCONDITIONAL JUMP
0001	A = B
0010	CARRY = 1
0011	RECEIVER BIT 10 = 1
0100	RECEIVER BIT 11 = 1
0101	RECEIVER ERROR
0110	RECEIVER DATA AVAILABLE
0111	RECEIVER ACTIVE
1000	TRANSMIT REGISTER FULL
1001	TRANSMITTER ACTIVE
1010	KEYBOARD HAD INPUT
1011	DMA REQUESTED = 1, MAY BE IN SERVICE
1100	AO AND A1 DISPLAY RAM ADDRESS = 0

1	1101	T REGISTER = 0 (NOT EQUAL TRUE)
2	1110	NOT USED
3	1111	NOT USED
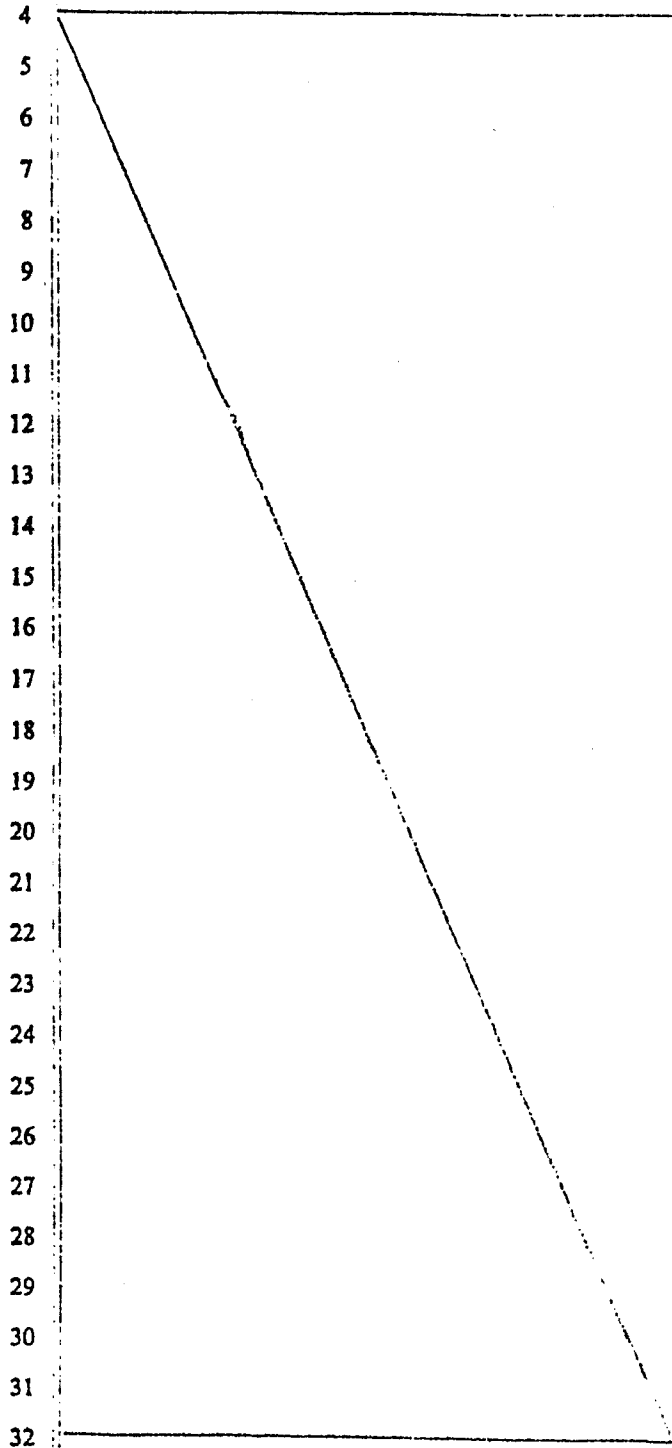
Processor 46 executes each instruction in four machine
cycles (periods) defined by signals developed by machine cycle
generating circuitry 116. During the first machine cycle,
designated T0 "bar", the previous address is incremented or the
jump address loaded into program counter 100 to develop (on
the lines collectively designated 240 signals representing) the
next instruction address. Responsive to the instruction address
(signals) program store 104 retrieves the addressed instruction
and develops representative signals the states of which are
latched by instruction register 106 which develops signals
having the latched states on instruction bus 152. Instruction
decoding circuitry 114 decodes the instruction (signals) and
develops signals enabling the source specified in the instruction
to drive source bus 54. B bus 150 is always driven by B
register 124. Arithmetic logic unit (ALU) 128 performs the
arithmetic or logic operation specified by the signals developed
on instruction bus 152 on the operands represented by signals
developed on source bus 54 and B bus 150 and develops signals
representing the result for driving T register 130. After the
signals have settled, during the third machine cycle, designated
T2 "bar", T register 130 latches the states of the signals
developed by ALU 128 and develops signals on destination bus 50
having the latched states. Finally, during the fourth machine
cycle, designated T3 "bar", the states of the signals developed
on destination bus 50 are latched by the destination register
specified by the instruction.

Immediate buffer 108 develops the source bus 54 driving
signals from the (lower order byte (8-bits) of the) instruction
(signals) during the execution of immediate instructions and
jump (on condition) instructions. For jump instructions, the

1 immediate data byte is coupled (unaltered) by ALU 128, T register

2 130 and B register 124 onto B bus 150 to drive jump address

3 multiplexer 100.   Condition testing circuitry 136 and instruction

4 decoding circuitry 114 ascertain the state of the (external

5 hardware) condition specified by the instruction.   Depending

6 thereon, the jump is taken (the jump address is loaded into

7 program counter 100) or not (the program counter is incremented).

8 As a result, processor 46 executes a hardware indirect jump

9 instruction.

10   After having read the preceding disclosure certain

11 alterations and modifications of the present invention will no

12 doubt become apparent to those skilled in the art.   It is there-

13 fore intended that the following claims be interpreted to cover

14 all such alterations and modifications as fall within the true

15 spirit and scope of the invention.

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IN THE CLAIMS

1. A processor comprising in combination:

an instruction bus;

a source bus;

a B bus;

a destination bus;

a program counter for developing signals representing an instruction address, said counter being responsive to a clocking signal and operative to increment said instruction address;

a program store storing a plurality of instructions, said store being responsive to said address signals and operative to develop signals representing the addressed one of said instructions;

an instruction register responsive to a signal and operative to latch the state of each of said instruction signals and to-develop on said instruction bus signals each having a respective one of said latched instruction signal states;

an arithmetic logic unit for performing the one of a plurality of operations specified by at least some of said instruction bus signals on signals developed on said source bus as a first operand and on signals developed on said B bus as a second operand to develop signals representing a result;

means for developing signals representing said result on said destination bus;

a B register responsive to a signal and operative to latch the state of each of said destination bus signals and to develop said B bus signals so each has a respective one of said latched destination bus signal states;

a register stack including a plurality of stack registers, said stack being responsive to a signal and operative to

1 latch the state of each of said destination bus signals in the

2 one of said stack registers addressed by at least some of said

3 instruction bus signals and said stack being responsive to an

4 output enabling signal and operative to develop said source bus

5 signals so each has a respective one of said destination bus

6 signal states latched in the one of said stack registers

7 addressed by said some of said instruction bus signals;

8 circuitry for developing timing signals; and

9 instruction decoding circuitry responsive to at least

10 some of said instruction bus signals and operative to develop said

11 program counter clocking signal, said instruction register latch-

12 ing signal, said B register latching signal, said stack latching

13 signal, and said stack output enabling signal, each at a time

14 designated by said timing signal developing circuitry.

15 2. A processor as recited in claim 1 further comprising a multi-

16 plexer for developing a first jump address from at least some of

17 said B bus signals and for developing a second jump address from

18 at least some of said source bus signals, said multiplexer being

19 responsive to a signal and operative to select one of said

20 first and said second jump addresses and wherein said program

21 counter is further responsive to a loading signal and operative

22 to set said instruction address to said selected jump address

23 and wherein said instruction decoding circuitry is further

24 responsive to said some of said instruction bus signals and

25 operative to develop said multiplexer selecting signal and said

26 program counter loading signal.

27 3. A processor as recited in claim 1 further comprising an

28 immediate buffer responsive to an output enabling signal and

29 operative to develop said source bus signals so each corresponds

30 in state to that of a respective one of a like number of said

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1 instruction bus signals and wherein said instruction decoding

2 circuitry is further responsive to said some of said instruction

3 bus signals and operative to develop said immediate buffer

4 output enabling signal.

5 4. A processor as recited in claim 1 further comprising a con-

6 trol bus including a plurality of lines and an output register

7 for developing a plurality of signals each on a respective one

8 of said control bus lines for controlling external circuitry,

9 said output register being responsive to at least some of said

10 instruction bus signals and operative to set the signal

11 developed on the one of said control bus lines addressed by at

12 least some of said instruction bus signals to a state indicated

13 by at least one of said some of said instruction bus signals.

14 5. A processor as recited in claim 1 further comprising a con-

15 trol bus including a plurality of lines, means for developing a

16 jump address from at least some of said B bus signals, and means

17 for testing a plurality of external conditions each evidenced

18 by the state of a signal externally developed on a respective

19 one of said control bus lines, said testing means being respon-

20 sive to the state of the signal developed on the one of said

21 control bus lines addressed by at least some of said instruction

22 bus signals and operative to develop a condition state signal

23 and wherein said program counter is further responsive to a

24 loading signal and operative to set said instruction address

25 to said jump address and wherein said instruction decoding cir-

26 cuitry is further responsive to said some of said instruction

27 bus signals and said condition state signal and operative to

28 develop said program counter loading signal.

29 6. A processor as recited in claim 1 further comprising a con-

30 trol bus including a plurality of lines, a multiplexer for

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1 developing a first jump address from at least some of said B bus

2 signals and for developing a second jump address from at least

3 some of said source bus signals, said multiplexer being respon-

4 sive to a signal and operative to select one of said first

5 and said second jump addresses, and means for testing a plurality

6 of external conditions each evidenced by the state of a signal

7 externally developed on a respective one of said control bus lines

8 said testing means being responsive to the state of the signal

9 developed on the one of the control bus lines addressed by at

10 least some of said instruction bus signals and operative to

11 develop a condition state signal and wherein said program counter

12 is further responsive to a loading signal and operative to set

13 said instruction address to said selected jump address, wherein

14 said instruction decoding circuitry is further responsive to

15 said some of said instruction bus signals and operative to

16 develop said multiplexer selecting signal, and wherein said ins-

17 truction decoding circuitry is further responsive to said some

18 of said instruction bus signals and said condition state signal

19 and operative to develop said program counter loading signal.

20 7. A processor as recited in claim 6 further comprising an

21 immediate buffer responsive to an output enabling signal and

22 operative to develop said source bus signals so each corresponds

23 in state to that of a respective one of a like number of said

24 instruction bus signals and wherein said instruction decoding

25 circuitry is further responsive to said some of said instruction

26 bus signals and operative to develop said immediate buffer output

27 enabling signal.

28 8. A processor as recited in claim 7 further comprising an output

29 register for developing a plurality of signals each on a

30 respective one of said control bus lines for controlling external

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circuitry, said output register being responsive to at least some

of said instruction bus signals and operative to set the signal

developed on the one of said control bus lines addressed by at

least some of said instruction bus signals

to a state indicated by at least one of said some of said instruc-

tion bus signals.

9.   An apparatus for interfacing a personal-computer to a 3270

compatible system, the apparatus comprising in combination:

       a control bus including a plurality of lines;

       a destination bus;

       a source bus;

       a system interface responsive to signals developed on

said control bus and operative to develop a signal for trans-

mission to the system representing encoded in 3270 serial-bit

format a byte of data represented by signals developed in parallel

format on said destination bus, to develop in parallel format

on said source bus signals representing a byte of data encoded

in said serial bit format and transmitted by said system, and to

develop at least one system interface condition indicating

signal on a respective one of said control bus lines;

       a personal-computer interface responsive to signals

developed on said control bus and operative to latch the state of

signals developed on said destination bus for use by the

personal-computer, to develop on said source bus signals

developed by said personal-computer, and to develop at least one

personal-computer interface condition indicating signal on a

respective one of said control bus lines; and

       a processor including,

          an instruction bus,

          a B bus,

means for developing a jump address from at some
signals developed on said B bus,

a program counter for developing signals represent-
ing an instruction address, said counter being respon-
sive to a clocking signal and operative to increment
said instruction address and said couter being respon-
sive to a loading signal and operative to set said
instruction address to said jump address;

a program store storing a plurality of instructions,
said store being responsive to said address signals
and operative to develop signals representing the
addressed one of said instructions,

an instruction register responsive to a signal
and operative to latch the state of each of said instruc-
tion signals and to develop on said instruction bus
signals each having a respective one of said latched
instruction signal states,

an arithmetic logic unit for performing the one of
a plurality of operations specified by at least some of
said instruction bus signals on said source bus
.signals as a first operand and on signals developed on
said B bus as a second operand to develop signals
representing a result,

means for developing said destination bus signals
so as to represent said result,

a B register responsive to a signal and operative
to latch the state of each of said destination bus
signals and to develop said B bus signals so each has a
respective one of said latched destination bus signal
states,

a register stack having a plurality of stack
registers, said stack being responsive to a signal
and operative to latch the state of each of said
destination bus signals in the one of said stack regi-
sters addressed by at least some of said instruction
bus signals and said stack being responsive to an output
enabling signal and operative to develop said source
bus signals so each has a respective one of said
destination bus signal states latched in the one of said
stack registers addressed by said some of said instruc-
tion bus signals,

an output register for developing said system
interface and said personal-computer interface
controlling control bus signals, said output register
being responsive to at least some of said instruction
bus signals and operative to set the signal developed
on the one of said control bus lines addressed by at
least some of said some of said instruction bus signals
to a state indicated by at least one of said some of
said instruction bus signals,

testing means responsive to the state of the
signal developed on the one of said control bus lines
addressed by at least some of said instruction bus
signals and operative to develop a condition state
signal,

circuitry for developing timing signals, and

instruction decoding circuitry responsive to at
least some of said instruction bus signals and said
condition state signal and operative to develop said
program counter clocking signal, said program counter

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loading signal, said instruction register latching

signal, said B register latching signal, said stack

latching signal, and said stack output enabling signal,

each at a time designated by said timing signal

developing circuitry.

10. An apparatus as recited in claim 9 wherein said processor

further includes an immediate buffer responsive to an output

enabling signal and operative to develop said source bus signals

so each corresponds in state to that of a respective one of a like

number of said instruction bus signals and wherein said instruction

decoding circuitry is further responsive to said some of said

instruction bus signals and operative to develop said immediate

buffer output enabling signal.

Fig_1

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Fig_2A

Fig.2B

Fig_2C

Fig_2D