



**V9000/S1**

**OPTIONS MANUAL**

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**V9000/S1 OPTIONS**  
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\*denotes "not available"



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8087



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**SECTION I**  
**THEORY OF OPERATION**

The Victor 8087 Option Board will allow greater, faster, and more reliable numeric processing on the Victor 9000 computer system. The 8087 numeric processor shares the local bus with the 8088 CPU and simultaneously reads instructions with the 8088. The 8087 can process instructions concurrently with the 8088 to allow for greater system throughput.

The 8087 is a coprocessor that performs numerous arithmetic and logical functions on a variety of data types. The 8087 is used in conjunction with a MAXIMUM mode 8088 CPU. The 8087 extends the register and instruction sets of the 8088 and adds several new data types as well.

The 8087 data types and principle instructions are listed in the tables below.

TABLE I (DATA TYPES)

DATA TYPE	# OF BITS
Word integer	16
Short integer	32
Long integer	64
Packed decimal	80
Short real	32
Long real	64
Temporary real	80

TABLE II (PRINCIPLE INSTRUCTIONS)

CLASS	PRINCIPLE INSTRUCTIONS
Data transfer	load, store, exchange
Arithmetic	add, subtract, multiply, divide, subtract reversed, divide reversed, square root, scale, remainder, integer part, change sign, absolute value, extract
Transcendental	tangent, arctangent, $2^X-1$ , $Y \cdot \log_2(X+1)$ , $Y \cdot \log_2(X)$
Comparison	compare, examine, test
Constant	0, 1, $\pi$ , $\log_{10} 2$ , $\log_e 2$ , $\log_{10} e$ , $\log_2 e$
Processor control	load control word, store control word, load environment, save, restore, enable interrupts, clear exceptions, initialize

The 8087 can internally be divided into two processing areas, the CONTROL UNIT (CU) and the NUMERIC EXECUTION UNIT (NEU). THE CU reads and writes memory operands, fetches instructions, and executes processor control instructions. The NEU executes all numeric instructions. The CU and the NEU operate independently of one another, thus allowing the CU to maintain synchronization with the 8088 while the NEU executes instructions.

The CU keeps the 8087 synchronized with the 8088. 8087 and 8088 instructions are fetched in a single stream of intermixed 8088 and 8087 instructions. The 8087, by monitoring the status lines, can determine when an instruction is being fetched. When that instruction is available to the local bus, the 8087 reads that instruction along with the 8088.

The CU instruction queue is identical to the 8088 instruction queue. The 8087 uses the queue status lines to obtain and decode instructions in synchronization with the 8088.

The 8088 and 8087 process instructions differently. The first five bits of all 8087 instructions are the same. These five bits designate the coprocessor escape class of instruction. The 8087 CU ignores all instructions that do not contain this bit pattern. When the CU decodes an escape instruction, it either executes the instruction itself or passes it onto the NEU for processing.

The NEU processes all arithmetic, comparison, transcendental, constant, and data transfer instructions that reference the register stack. The data path in the NEU is 68 bits wide, thus allowing for fast data transfer.

The 8087, being a coprocessor to the 8088, is wired directly to the 8088. The 8088 queue status lines (QS0, QS1) allow the 8087 to obtain and decode instructions in synchronization with the 8088. The 8087 busy signal informs the 8088 that the 8087 is processing. The 8087 uses the request/grant (RQ/GT) line to gain control of the local bus for data transfer (loads and stores).

Sheet 2 of schematic 101911 shows the 8088 and 8087 coprocessor. The 8088 is set in the maximum mode by tying pin 33 on the 8088 to a logic level 0. The maximum mode 8088 does not generate any bus control or command output signals. These signals must be generated by other support circuitry.

Vcc for the 8087 is supplied at pin 40. The address/data lines (AD0-AD7, A8-A19) are supplied through connector P1 and are common to the 8088 and the 8087 processors. The ready line (active high) and the non maskable interrupt line (NMI) are also supplied directly through connector P1 and are common to both processors. The clock frequency for both is 5 MHz. The 5 MHz clocking signal (MPU CLOCK) is generated on sheet 3 of schematic 100471.

The RESET signal is supplied directly through connector P1 and is common to both processors. The RESET signal is generated on sheet 3 of schematic 100471.

The 8087 monitors the 8088 instruction queue status lines. The two queue status lines (QS0, QS1) help keep the 8087's instruction queue synchronized with the 8088's instruction queue. The two status lines encode one of four possible states.

QS0	QS1	
0	0	no operation
0	1	first byte of instruction taken from queue
1	0	queue was reinitialized
1	1	subsequent byte of instruction taken

Pin 34 BHE/S7 is a status line monitored by the 8087. The S7 status line is used to synchronize the queue length of the 8087 with the queue length of the CPU (8088).

Whenever the 8087 writes or reads more than one word of data from memory, the 8087 forces the 8088 to relinquish control of the local bus. This is done through the use of the request/grant line. The 8087's request/grant line (RQ/GT0) pin 31 is connected to the 8088's RQ/GT1 (pin 30). The 8087 gains control of the local bus by pulsing its RQ/GT0 line for one clock period. The 8087 waits for the grant pulse (1 clock period), when it is received the 8087 will initiate bus transfer activity in the next clock cycle. The 8087 will generate a release pulse one clock period after completion of the last 8087 bus cycle.

The busy line (pin 23) of the 8087 is high when the 8087 is executing an instruction. The BUSY signal is nor'ed with the TEST/ signal at location 4D (pins 5 and 6). The output is inverted at 4D (pins 8 and 9) and input to the 8088. The busy line on the 8087 must be low (logic 0) in order for the 8088 TEST/ line to be active (logic level 0). The TEST/ input is used in conjunction with the (wait for test) instruction. The TEST/ line is used to synchronize the 8088 to some external event. The TEST/ line is used to synchronize processor activity with disk action. When the 8087 is processing an instruction, the busy line will be held high. The active (HIGH) busy signal will hold the TEST/ line going to the 8088 high until the 8088 completes processing. The 8088 will remain in a (wait for test) loop until the test line becomes active (LOW), thus preventing any further disk access. This action assures that the 8088 and 8087 will be ready to read instructions concurrently.

The 8087 can generate an interrupt when necessary. The interrupt line pin 32 on the 8087 is nor'ed at 4D pin 2 with the interrupt request line from the programable interruptcontroller (PIC). The signal is then inverted by nand gate 3B (pins 4 and 5). The inverted output is applied to the interrupt request line (pin 18) on the 8088. The 8088 determines where the interrupt is from and updates the status lines S0/, S1/ and S2/ to the proper states.

The 8087 uses the status lines S0/, S1/, and S2/ to generate bus cycle information. The 8087 uses only three of the eight possible status states.

S2	S1	S0	
1	0	1	READ MEMORY
1	1	0	WRITE MEMORY
1	1	1	PASSIVE

The 8088 in maximum mode generates no bus control signals. Instead the status lines S0/, S1/ and S2/ are used in conjunction with support circuitry to control bus cycles.

S2	S1	S0	
0	0	0	INTERRUPT ACKNOWLEDGE
0	0	1	READ I/O
0	1	0	WRITE I/O
0	1	1	HALT
1	0	0	INSTRUCTION FETCH
1	0	1	READ MEMORY
1	1	0	WRITE MEMORY
1	1	1	PASSIVE (NO BUS CYCLE)

Once the status lines S2/, S1/, and S0/ are set for the particular bus cycle, the proper MIMIMUM mode bus control signals must be generated. These control signals are RD/, WR/, IO/ $\bar{M}$ , DT/ $\bar{R}$ , SS0/, DEN/, INTA/, and ALE.

IO/ $\bar{M}$  is directly controlled by status line S2/.

DT/ $\bar{R}$  is directly controlled by status line S1/.

SS0/ is directly controlled by status line S0/.

The bus control signals IO/ $\bar{M}$ , DT/ $\bar{R}$  and SS0/ are gated through latch 3A and output to the CPU logic board through connector P1. The latch at location 3A is gated by the ALE signal.

RD/ is generated whenever a memory read is required. The status setting for a MEMORY READ is S2/=1, S1/=0, and S0/=1. The status signals are gated through latch 3A. The RD/signal is decoded by the AND-OR-INVERT gate at location 1A and input to the CPU logic board through connector P1.

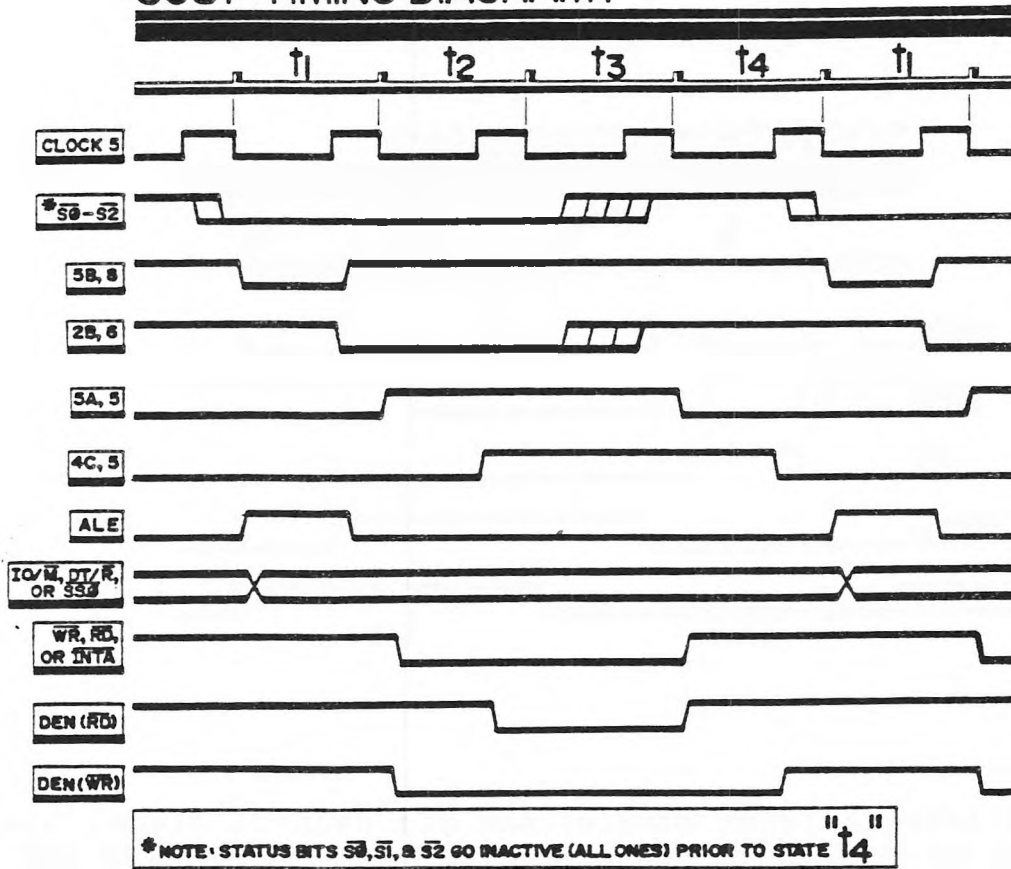
WR/ is generated whenever a memory write is required. The status line setting for MEMORY WRITE is S2/=1, S1/=1, and S0/=0. The status signals are gated through latch 3A by the ALE signal. The WR/ signal is decoded by the quad input nand gate at location 2A (pins 1,2,4, and 5). The WR/ signal is input to the CPU logic board through connector P1.

INTA/ is a read strobe for interrupt acknowledge cycles. The status line setting for INTA/ is S2/=0, S1/=0, and S0/=0. The status signals are gated through latch 3A by the ALE signal. The INTA signal is decoded by the quad input nand gate at location 2A (pins 9,10,12, and 13). The INTA/ signal is input to the CPU logic board through connector P1.

DEN/ is supplied as an enable for the bus transeivers. DEN/ is active (LOW) during Read, Write, and Interrupt Acknowledge cycles. The DEN/ signal will be active from the middle of state T2 until the start of state T4 for RD/ and INTA/ cycles. The DEN/ signal will be active from the start of state T2 until the middle of state T4 for WR/ cycles.

The minimum mode control timing is provided by the timing circuit composed of 74LS74 (5A) and 74LS112 (4C). This circuit provides a "timing enable" for the signals RD/, WR/, INTA/, and DEN/.

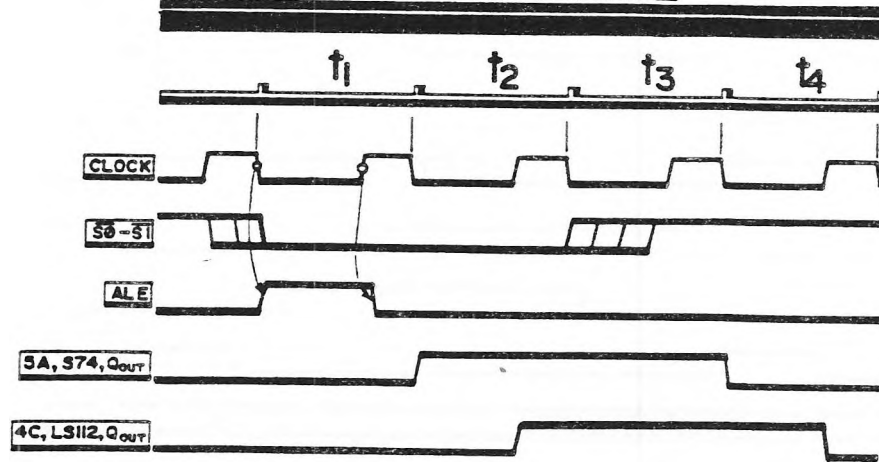
### 8087-TIMING DIAGRAM I



The DEN/ signal is generated by the AND-OR-INVERT gate (74LS51 2B). The DEN/ signal is input to the CPU logic board through connector P1.

ALE (Address Latch Enable) is generated by the AND-OR-INVERT gates at locations 2B and 5B during each bus cycle. Gate 5B is clocked by clk/ signal, and gate 2B is clocked by the clk signal. The ALE signal is high during T1 and low for T2-T4. 5B and 2B work together to hold the ALE signal low for states T2-T4.

### 8087-TIMING DIAGRAM 2



ALE ( address latch enable) and all control signal timing is controlled by the timing circuit which consists of AND -OR - INVERT gates 5B (pins 1,9,10,11,12, and 13), 2B (pins 2,3,4, and) and the two J-K flip flops at locations 5A and 4C.



The clock frequency for the timing circuit is 5 MHz. The reset for the 8087 board is controlled by the reset line from the CPU logic board.

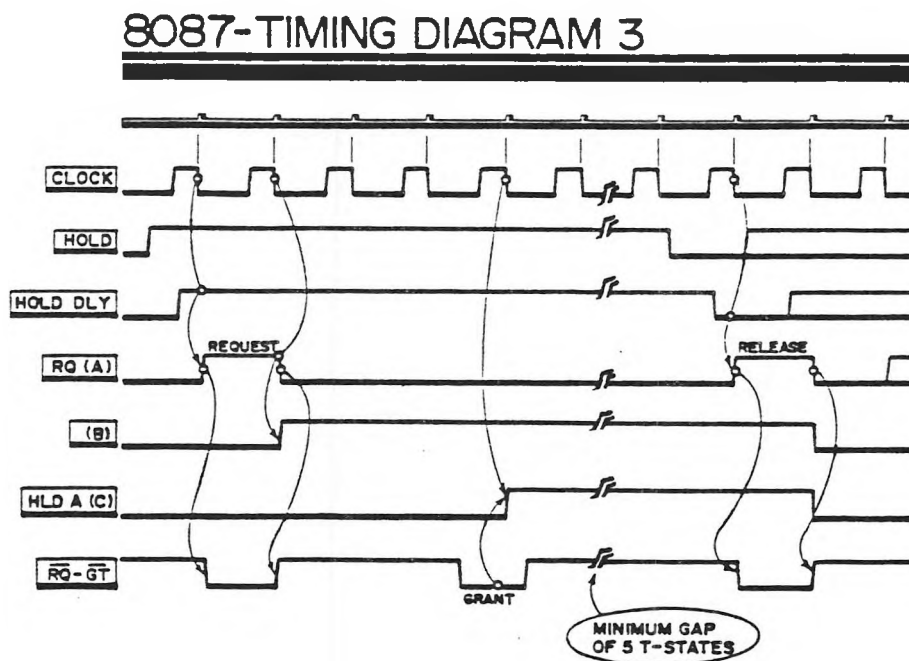
The HOLD signal is used by another processor to gain control of the bus in the MINIMUM mode. The 8088 CPU on the 8087 board is strapped in the maximum mode, thus support circuitry must be used to generate the minimum signals.

In the maximum mode the request/grant line is used in place of HOLD and HLDA. The request/grant (RQ/GT) line is a bi-directional signal line.

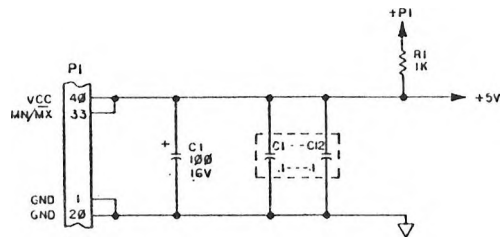
When an external processor request the bus, the hold signal is asserted. The hold signal is input through connector p1 (pin 31) and applied to the D input (pin 12) on the d flip flop at location 5A. The hold sequence timing is provided by the 5 MHz clock and associated circuitry consisting of D flip-flop (5A), AND-OR-INVERT gate (5B), inverter 4B, and and J-K flip flops 4C and 5C. The HOLD signal is gated from 5C pin 9 and input to inverter 5D pin 1. The output of 5D pin 2 is input to the RQ/GT0 pin 31 line. The 8088 releases the bus after completing its present bus cycle. The 8088 pulses the RQ/GT0 line to acknowledge the hold.

The acknowledging pulse is applied as an input to nand gate 4D pin 11. The output of 4D pin 13 is applied to the inputs of the J-K flip flop at location 4C.

The Q output pin 9 of the J-K flip flop at 4C issues the hold acknowledge signal to the external processor.



**SECTION II  
SCHEMATICS**



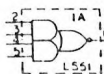
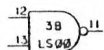
NOTES UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICRODIARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE 1/4W, 5%.
3. ALL IC'S ARE SN74 SERIES.
4. IC PINS ARE GND=7 +5V=14 EXCEPT FOR

DEVICE	GND	+5V
LS112	8	16
LS375	8	16
8000	20	40
8007	20	40

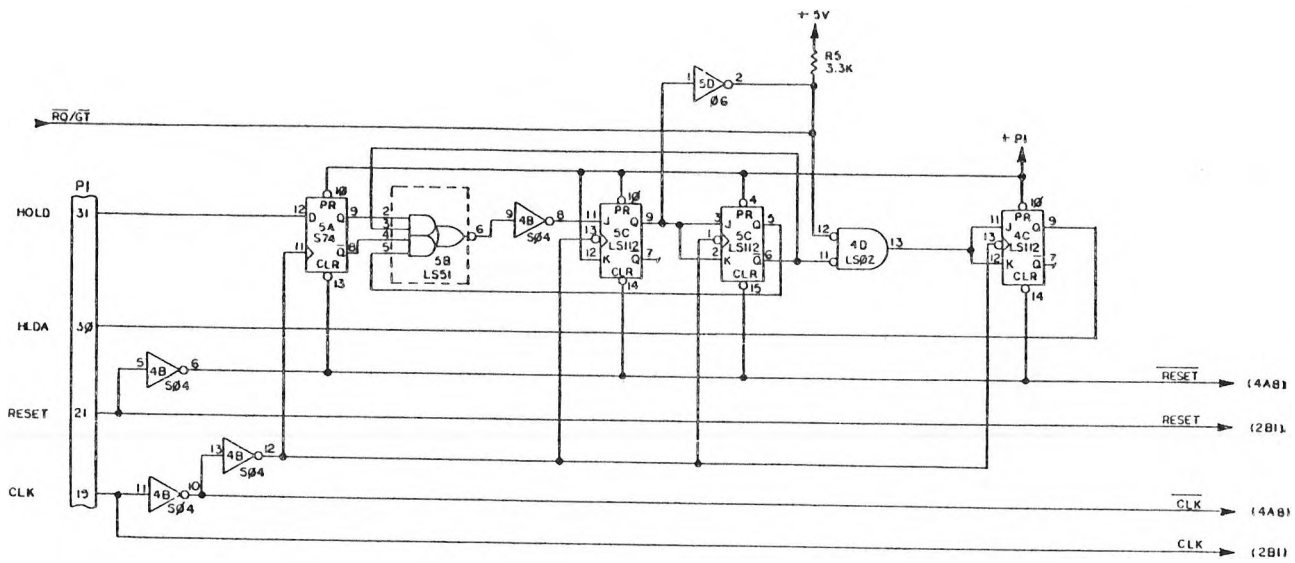
5. IC 8000 MUST BE INTEL COPYRIGHT ©'81.

SPARE GATES



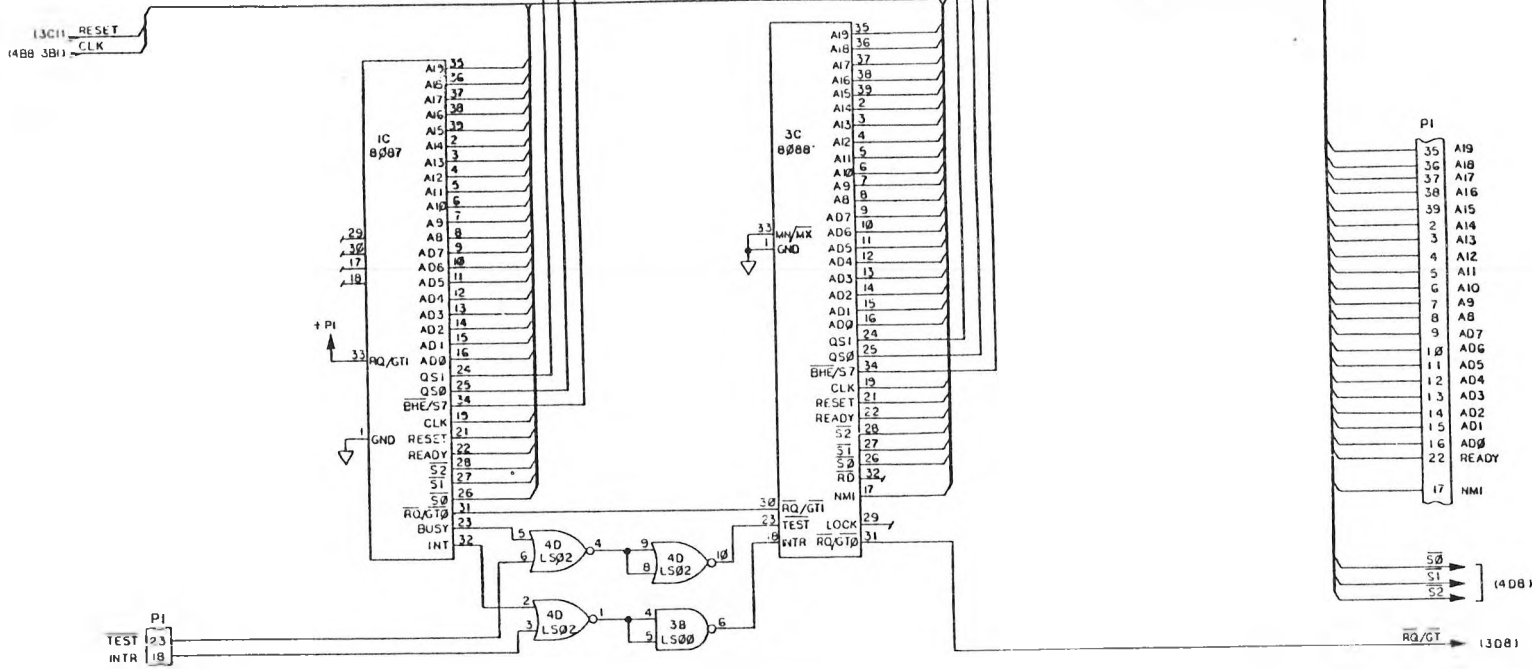
SHT 4 OF 4 | REV A  
DWG NO 101911

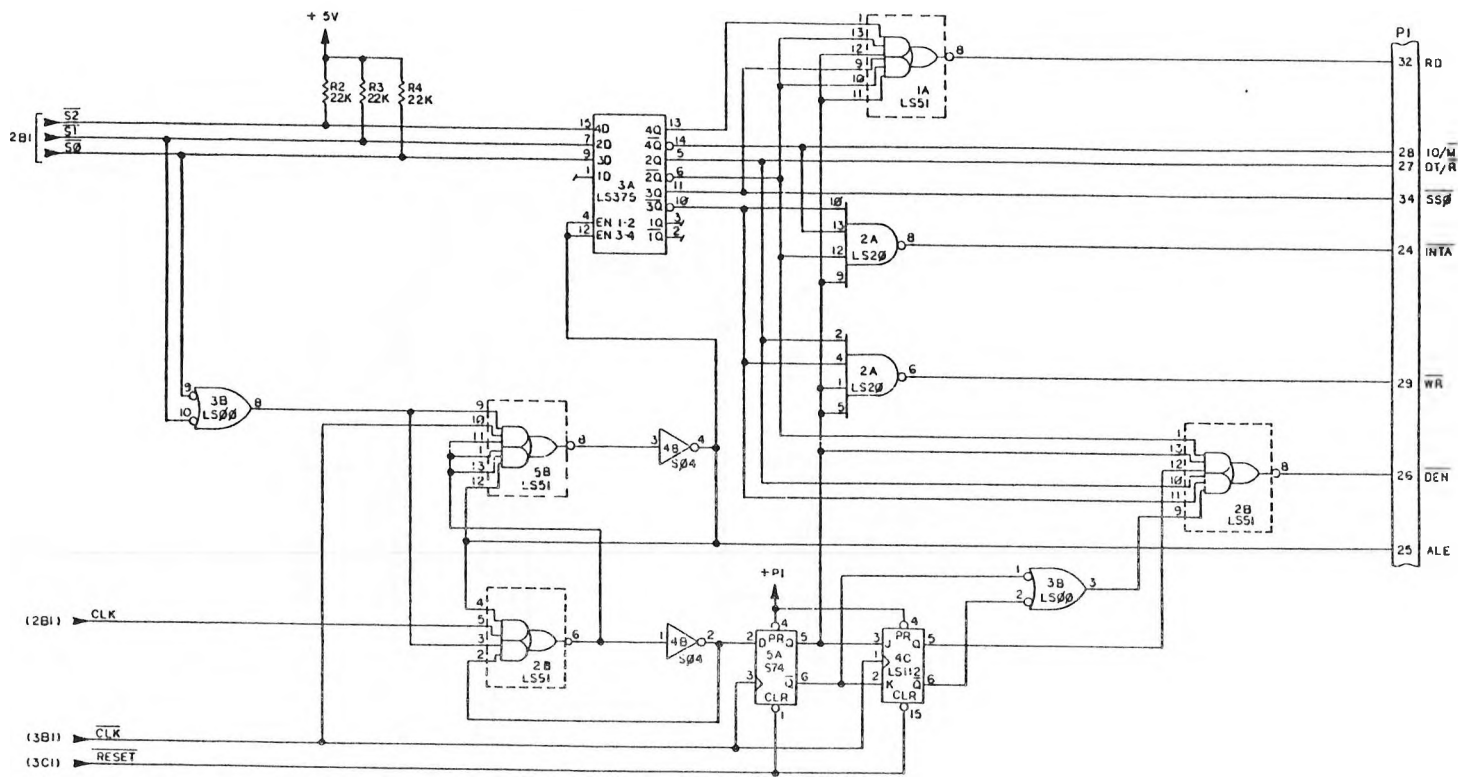
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SHT 3 OF 4 REV. A  
 DWG. NO. 101911

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SHT 1 OF 4 REV A  
DWG NO 101911

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CPM/80





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SECTION I  
THEORY OF OPERATION

The Z80 CPU board was designed to accommodate software written to run under the CP/M 80 operating system. The Z80 card allows users to run existing Z80 software while utilizing all the advantages of the Victor 9000 computer system. The Z80 board contains a Z80 microprocessor running at 6 MHz, 64k of dynamic RAM memory, and a Corvus hard disk interface.

The Z80 board utilizes the Victor 9000 for all I/O including graphics capabilities, disk storage, and access to I/O ports. The Corvus hard disk interface allows the user to connect a Corvus 5, 10, or 20 megabyte hard disk to the Victor 9000. Up to four 20 megabyte drives may be on line at one time and up to 64 Victor 9000 computers may be networked together using the Corvus constellation multiplexer board. High speed backup onto standard video tape is available from Corvus by ordering the Corvus mirror option.

CP/M 80 is a disk operating system that manages program and data files. CP/M 80 programs will run on a Z80 system provided sufficient memory is available (64k bytes max).

The Z80 card occupies one of the available I/O port addresses. The Z80 board comes factory set for I/O port address 0. This address may be changed if necessary. The two 10 position dip switch banks set the I/O port address for the Z80 card. (NOTE: When the Z80 card hardware port address is changed, the user must also change the CP/M 80 software I/O port address for the Z80 board by using the NEWSYS program).

The table below describes the I/O port address switch banks.

SWITCH 1 (NEAR CENTER OF CARD)

PIN #	I/O ADDRESS BIT #
1	0
2	1
3	2
4	3
5	4
6	5
7	6
8	7
9	8
10	9

PIN #	I/O ADDRESS BIT #
1	10
2	11
3	12
4	13
5	14
6	15
7	RESERVED
8	RESERVED
9	RESERVED
10	RESERVED

By typing a command, the 9000 user can switch between CP/M 80 and CP/M 86 operating systems. (NOTE: CP/M operating system disk must be loaded to access CP/M 80 operating system.)

TO LOAD CP/M 80, FROM FROM CP/M 86 :  
TYPE 80 (CR)

TO RETURN TO CP/M 86 FROM CP/M 80:  
TYPE 86 (CR)

Refer to the CP/M 80 #101882 users guide for further software information.

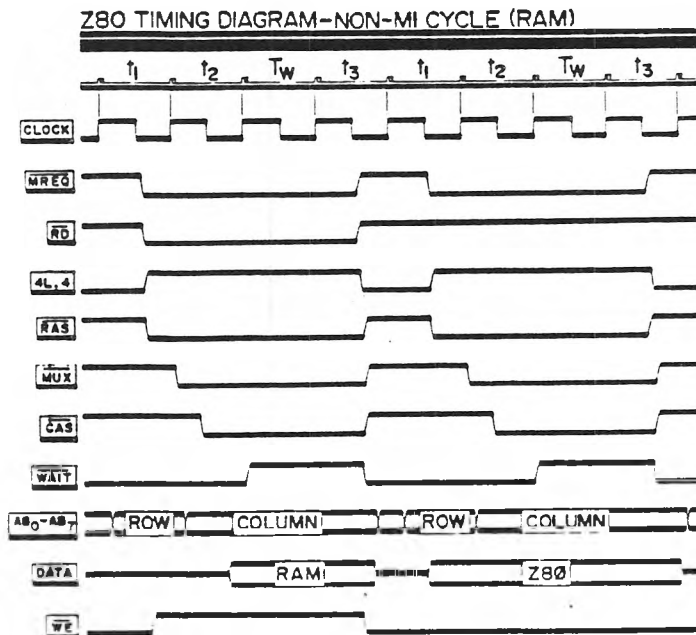
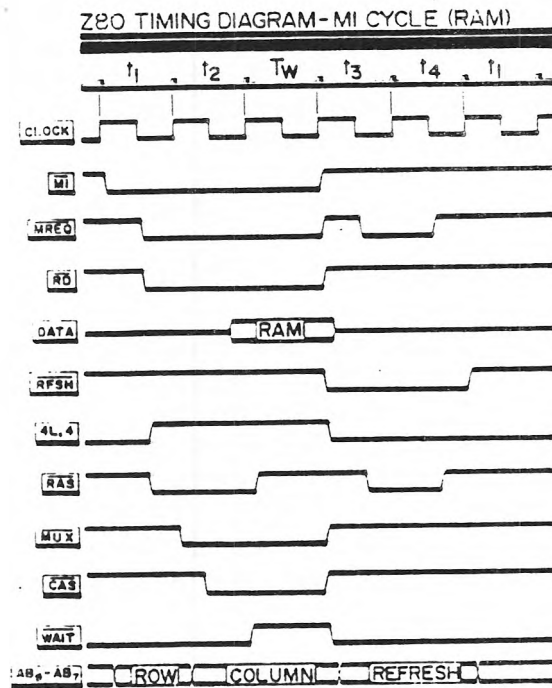
Use for the Victor 9000 schematics document # 101311 to follow the Z80 board description.

The clock frequency for the Z80 CPU is 6 MHz. The base frequency is supplied by the 12 MHz crystal at location Y1, inverter 4L and feedback resistors R10 and R11. Capacitors C3 and C5 ensure that the clock circuit will oscillate on initial power up. The J-K flip flop at location 4M is configured as a T flip flop, thus doubling the clock period which develops the 6 MHz system clock.

Reset for the Z80 microprocessor is accomplished by inverting the RESET signal from the Victor 9000 expansion bus. The RESET signal is input to inverter 4L (Pin 13) and fed to the Z80 reset input pin 26. The inverted reset signal also presets the flip flop at location 4M which allows PROM access at address 0 on power up. This causes the the Z80 to execute a jump to location FCxx - FFCx hex depending upon the jumper settings at location 2N. The address space occupied by the PROM is unusable space to the systems programmer. The inverted RESET signal also clears flip flop (3J) which turns LED DS1 off, indicating that the Z80 board is deselected.

The INTR and NMI inputs to the Z80 are tied high disabling all interrupts. The interrupts are not used because the Victor 9000 handles the crt, keyboard, ports, and disk drives. The Busreq and Busack signals are held high disabling their function.

The Z80 board executes one wait state for every (M) machine cycle. A (M) cycle is composed of three or more (T) timing cycles plus one wait state on the Z80 board. The Z80 can execute two types of (M) cycles, M1 and non M1. The M1 cycle is used to fetch the op code of the next instruction to be executed. The M1 cycle for the Z80 board is 5 (T) cycles long (T1, T2, Tw, T3, T4). The non M1 cycle can be used for memory read, memory write, I/O read or I/O write.



The Z80 board circuitry inserts a Tw (wait) state after every T2 cycle during a memory read, memory write, or fetch cycle (M1). D flip flops 3H and 3J are used to generate the one Tw (wait) state. The Tw state is inserted after T2 by pulsing the WAIT state input (pin 20) on the Z80 microprocessor low during T2. The Tw state is inserted in the next T cycle.

The following discussion describes the Z80 memory cycle. The Z80 memory cycle is generated whenever dynamic RAM or PROM access is required. During the memory cycle several control signals are generated in order to access dynamic RAM or PROM memory. These signals are RAS, CAS, MUX, and PROM.

The EPROM can be 2716 (16k) or 2732 (32k) PROM. The type of EPROM selected can be set by jumpers E1, E2 and E3. When the jumper is set from E2 to E3, the PROM address space is setup for a 2716 PROM. When the jumper is set from E1 to E3, the PROM address space is setup for a 2732 PROM.

E1-----E3	2732 EPROM
E2-----E3	2716 EPROM

The EPROM at location 1N is always chip enabled by grounding the CE/ input (pin 18). The EPROM output enable (OE/ ,pin 20) is driven by the signal PROM/, which can be initiated by one of two sources. Either the J-K flip flop at 4M or the 13 input NAND gate at 3L will initiate the EPROM access via the 'OR' function of the NAND gate at 3K (pins 10,9,& 8). This output at 3K pin 8 is then qualified with signal RFSH/ at device 3K (pins 1,2,& 3) and the timing of signal PROM/ is set by signal MREQ/ at device 3D (pins 4,5,& 6).

After system reset, the J-K flip flop at 4M will preset, allowing the Z80 to read the EPROM. The Q output is fed back to the J input (pin 3) and the flip flop will remain set until the address A1 goes high at the K input (pin 2). When address A1 goes high, the flip flop will toggle low and remain low until the system reset is asserted again. This allows the Z80 to read the first 3 bytes of code from the EPROM and then the EPROM is mapped to upper memory.

The default address for the EPROM in upper memory is OFFCx hex. This address is decoded by the 13 input NAND gate at 3L. This default address can be changed by the cut & jump selection area at 2N. The range of addresses that can be set up is from OFCxx hex to OFFCx hex.

To access dynamic RAM four control signals are needed, RAS, CAS, MUX, and WE. RAS, CAS, and WE are common to all the dynamic ram chips. The MUX signal is used to select between the row and column addresses. When MUX is high, the "B" inputs are selected on the 74LS257 decoders (2M, 3M) and the row addresses are presented onto the ABO-AB7 bus. When the MUX signal is low, the "A" inputs are selected and the column addresses are presented to the ABO-AB7 bus. The signal WE/ (write enable) is the inverted ZRD/ signal from device 3F (pin 4).

The generation of RAS/ is qualified by the PROM signal being false and when MREQ/ is true, through the OR gate (74LS32, 3D). The PROM signal is locked out when a refresh cycle is started, therefore a RAS/ can be generated. RAS/ normally follows MREQ/ except on an M1 cycle. M1 is generated by the Z80 when the current machine cycle is the OP code fetch (machine cycle one). RAS has to be cut off earlier to meet its precharge time for the second RAS generated for the refresh. RAS/ is cut off by the Q/ output of the D flip flop at 3J (pin 6).

The two D flip flops at 3H (74LS74) set up the timing requirements for signals MUX/ and CAS/. Both flip flops are preset, when MREQ/ is false and RSFH/ is false, through nand gate 3K (74LS00). When MREQ/ goes true (falling edge of uP clock in T1), the rising edge of the uP clock in T2 resets the MUX/ signal low and the Q/ output clocks the second D flip flop (resetting the Q output low, signal CAS/). To make sure there is no race condition between MUX/ setting up the address and CAS/, CAS/ has an R-C network to delay the leading edge. The second flip flop (3H, pin 8) no longer holds the third flip flop (3J) preset, so the rising edge of the uP clock in T3 will generate a high pulse on Q/. The Q/ output on 3J is the signal that cuts off RAS/ on the M1 cycle and also is the signal WAIT/ which holds the Z80 in a wait state until the third uP clock of the current access. CAS/ is removed when either the RFSH/ signal is true or the MREQ/ signal is false.

The refresh of the dynamic RAM's is handled by the Z80 itself, which generates RFSH/ when it has a valid refresh address on the lower 7 bits of the address BUS (128 bit refresh). RFSH/ locks out PROM, CAS/, and MUX/, and also makes sure RAS/ will meet its set up time.

The Corvus hard disk interface consist of 11 total lines; 8 data lines, one strobe line (STR/) going to the hard disk to latch in valid data, and two status lines (CREADY and DIFAC/) coming from the hard disk which dictates when the Z80 can write or read data.

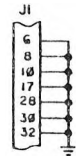
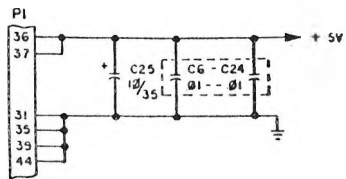
When the Z80 does an I/O instruction (IN or OUT) IORQ/ goes true (low) and enables the 3-to-8 line decoder (74LS138, 3B). The port specified by the I/O instruction is output on the lower 8-bits of the Z80 address lines and qualified by IORQ/. The 3 least significant bits decode which output is selected (0-7). In the case of a Corvus access the port you want to read and write from is port 01 hex. The output of the decoder directs the signals ZRD/ and ZWR/ through the OR gates at 3D to produce the CREAD/ and CWRITE/. CREAD/ and CWRITE/ are Ored together and inverted through the nand gate at 4J (74LS00) to create signal (STR/), a strobe pulse that will enable the output of the Corvus hardware when reading or latch the valid data when writing to the Corvus hardware. The CWRITE/ has to be delayed through an RC network to ensure the data is valid when the STR/ signal is true (low). The Corvus' status signals are read back through the buffer at 1L when polled by the software at I/O port address 00. CREADY indicates the drive is ready and DIFAC/ indicates the disk interface active.

The interface between the 8088 and the Z80 use 21 lines (excluding power) on the expansion BUS slot of the Victor 9000 computer. Sixteen lines are used for address, with the lower 8 address lines being multiplexed with data bits D0 - D7, and 5 control lines; RD/, WR/, IO/M, ALE, and RESET.

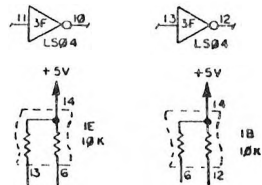
The I/O address of the Z80 board can be adjusted by changing the switch settings at 1C and 1D. Currently the 80.CMD program uses the address at 00 hex. The upper address lines from the 8088 are compared to the switch settings of 1C through the 74LS688 at 1A. The comparator (74LS688, 1A) checks the addresses A8 - A15 when the IO/M signal from the 8088 is high. Signal ALE latches in the lower address lines into the 74LS373 at 1H. If the upper address bits match, the P=Q (pin 19--74LS688, 1A) enables the second comparator (74LS688, 1F), which compares addresses A0 - A7 to the switch settings of 1D. If the lower address bits match, it enables the NOR gates at 3C. This allows the 8088 read and write (RD/ & WR/) signals to enable the latches at 1K (read Z80 data) or 1J (write Z80 data). The Z80 control signals to read or write to the latches at 1K or 1J are SREAD/ and SWRITE. The Z80 writes data to the system through the latch at 1K and reads data from the system through the latch at 1J. The two signals SWRITE and SREAD/ are generated by the same I/O decoder (74LS138, 3B) as described in the previous section. Writing to I/O port 02 hex will enable the NOR gate and generate SWRITE. In a similar fashion, a SREAD/ is generated when reading from I/O port 03 hex.



SECTION II  
CPM 80 SCHEMATICS



SPARE GATES :

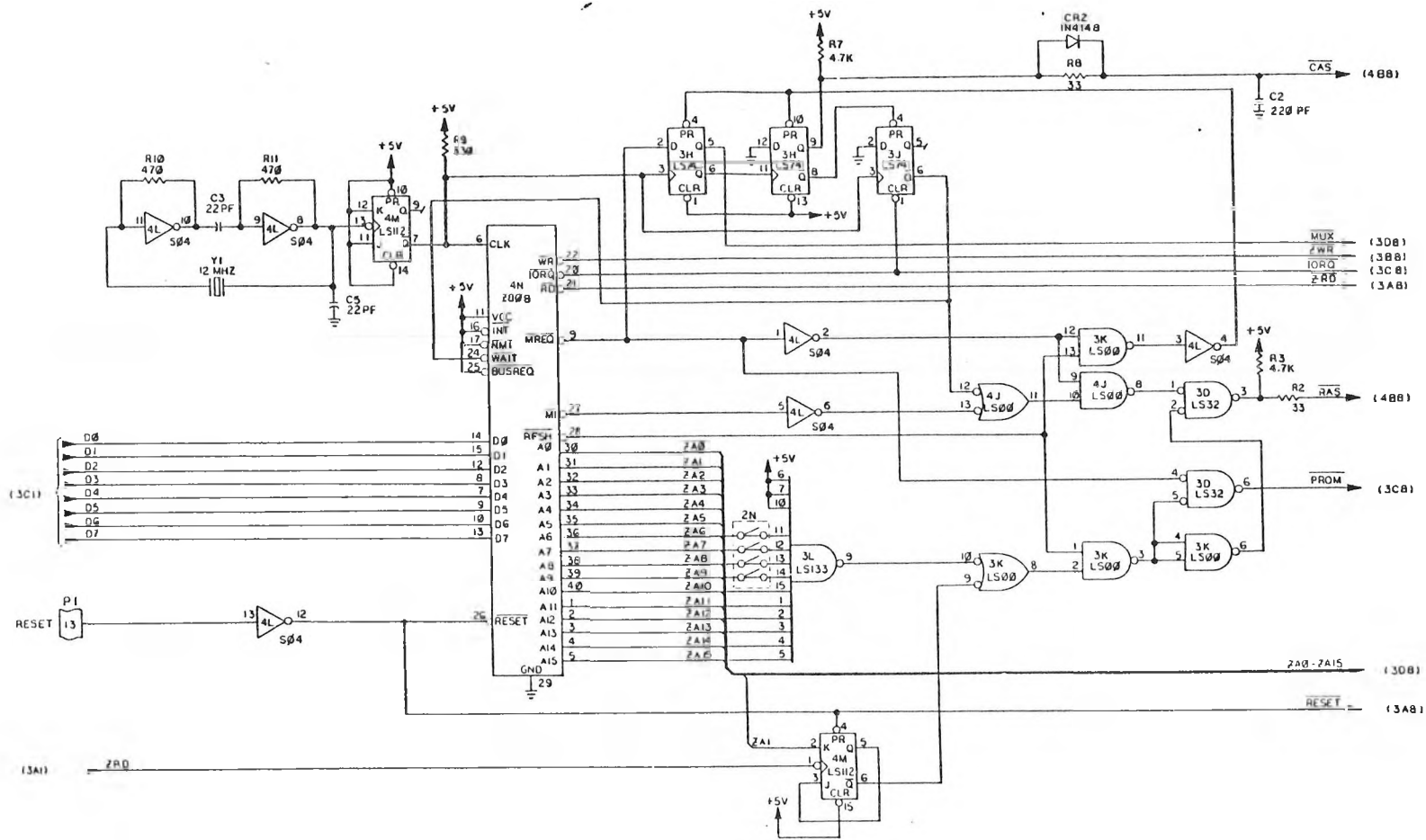


NOTES - UNLESS OTHERWISE SPECIFIED :

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE  $\pm 5\%$ , 1/4W.
3. ALL IC S ARE SN74 SERIES.
4. IC PINS ARE GND=7, +5=14 EXCEPT FOR:

IC TYPE	GND	+5V	(REF)
780A	29	11	
-164	9	16	
LS244	10	20	
LS373	10	20	
LS680	10	20	
LS138	8	16	
LS133	8	15	
S257	8	16	
LS365	8	16	
2716	12	24	

CR2		
Y1	J1	
C25	E1	
DS1	RI:	CR
LAST USED		NOT USED
REFERENCE	DESIGNATORS	



(3C1) D0  
D1  
D2  
D3  
D4  
D5  
D6  
D7

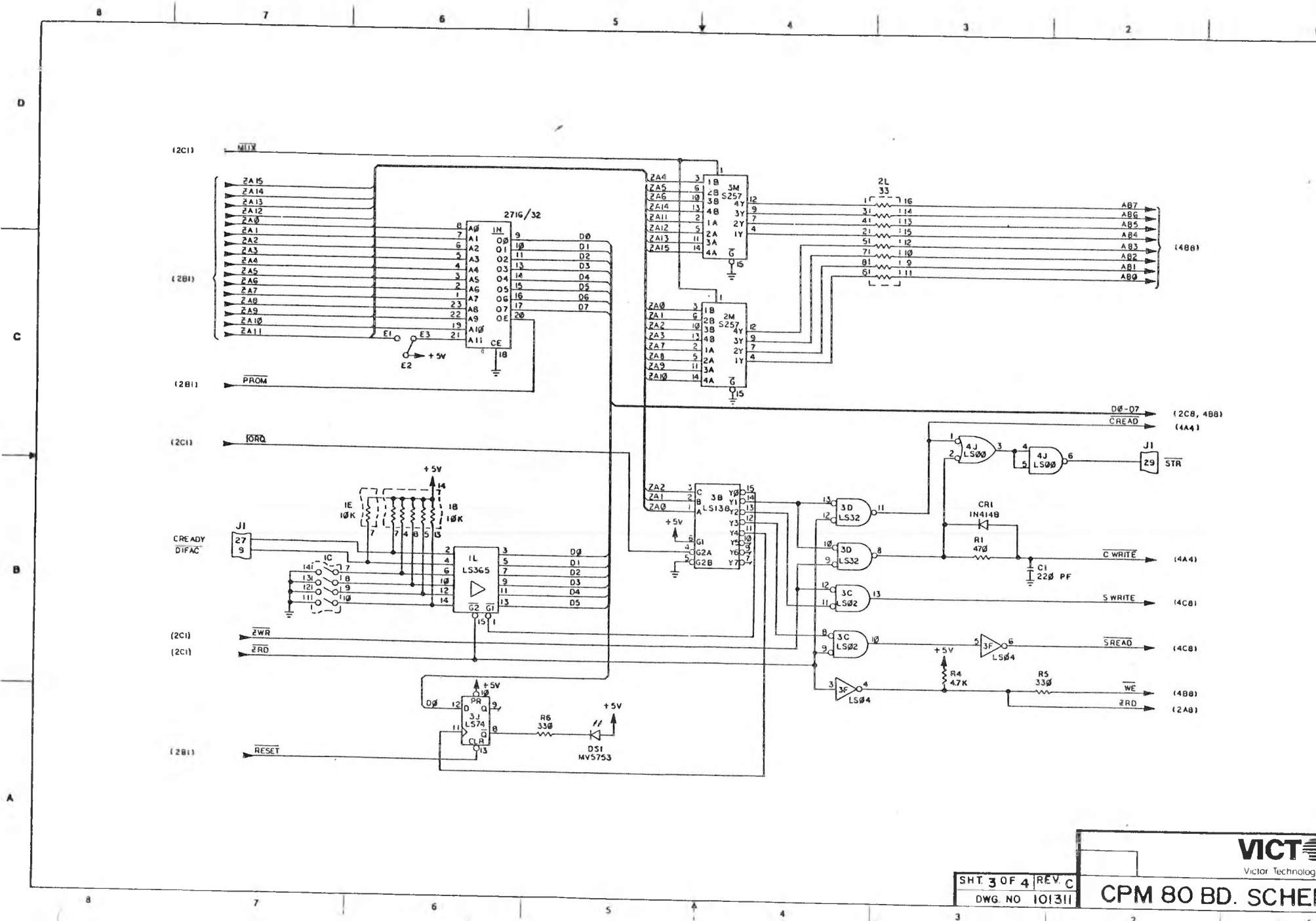
RESET P1 13

(3A1) ZR0

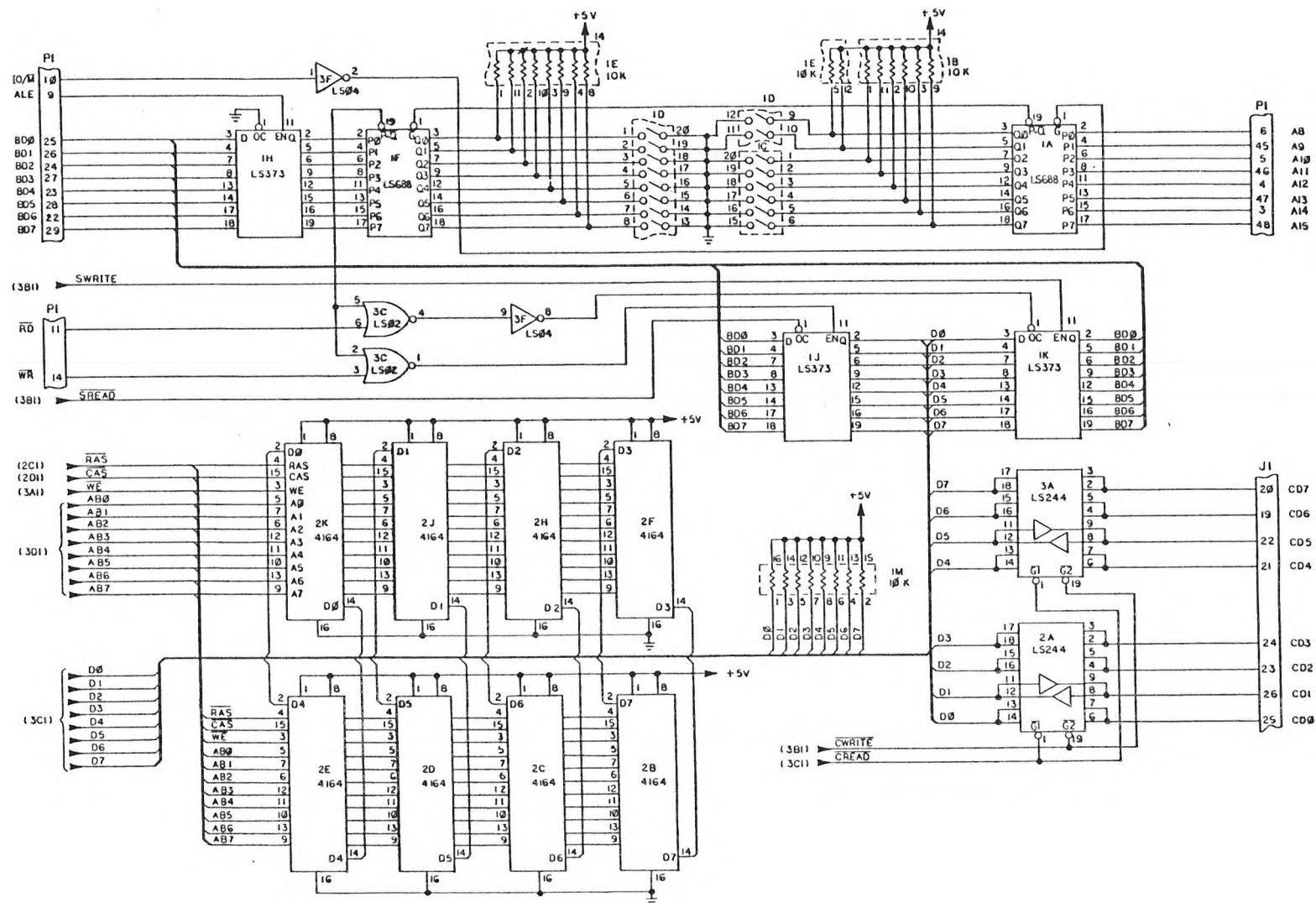
**VICTOR**  
Victor Technologies, Inc.

SHT 2 OF 4 REV. C  
DWG NO 101311

**CPM 80 BD. SCHEM.**



SHT 3 OF 4 REV. C  
 DWG NO 101311



SHT. 4 OF 4 REV C  
 DWG NO 101311

**VICTOR**  
 Victor Technologies, Inc.  
**CPM 80 BD. SCHEM.**



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4

NETWORK

## CONTENTS

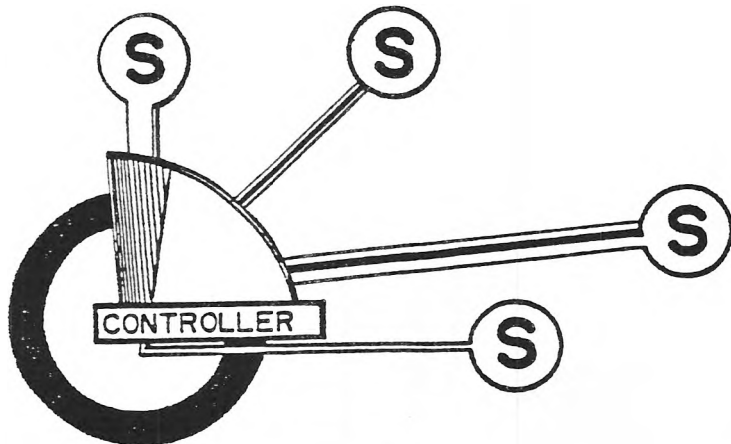
<b>SECTION I</b>	Introduction: Local Area Networking .....	4-1
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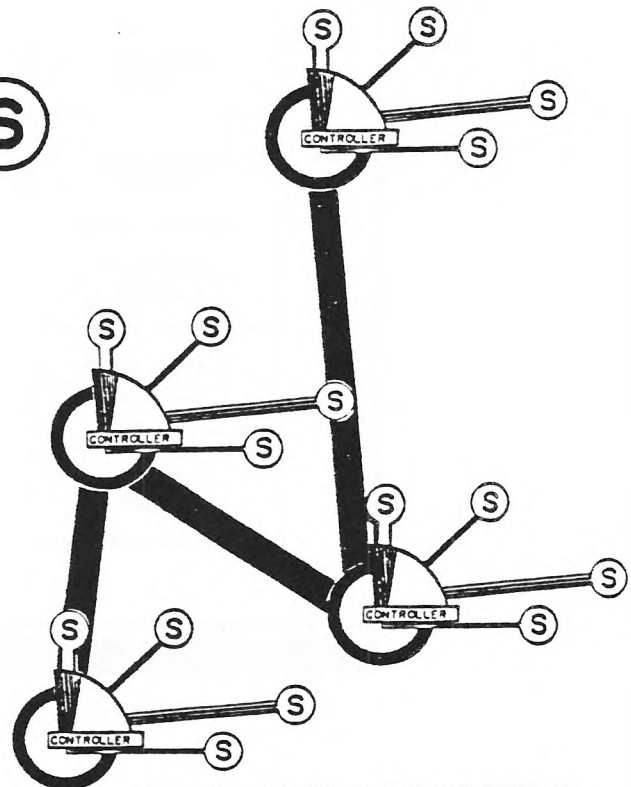
# SECTION I INTRODUCTION

Today's businesses require a computer system capable of multiple inputs and processing. These capabilities have been available in minicomputer systems for many years. In recent years the microcomputer has been replacing the minicomputer in office environments. This has forced micro systems to have the same multi input and processing features as minicomputer systems. Microcomputer systems are now being used in multi-terminal configurations to form local area networks ( LAN ).

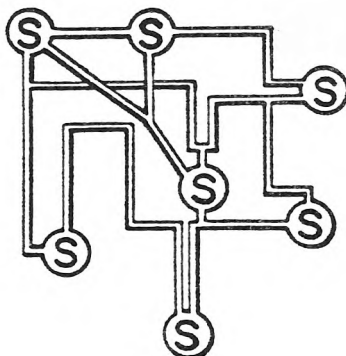
LAN's are distributed processing systems that incorporate multiple user stations, mass data storage, and background printing facilities. There are basically three types of networks; centralized, decentralized, and distributed. A centralized network has a "master" system controller controlling network operation. A decentralized network is basically a group of interconnected centralized networks. A distributed network has no main controller and each node on the system shares in the network control process.



CENTRALIZED



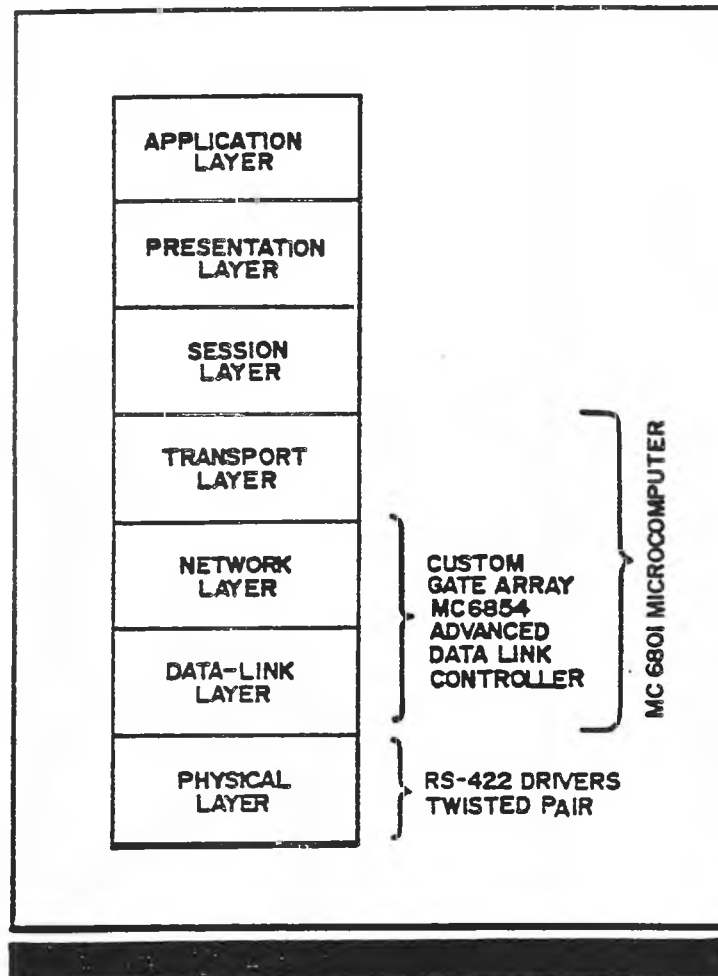
DECENTRALIZED



DISTRIBUTED

hardware allows the user multiple station input (multi-user) and concurrent processing (multi-tasking). The Victor LAN will be initially offered in a multi-user, single tasking configuration. The network software for this configuration will be MS-DOS version 2.0 (SERVERS) and MS-DOS version 1.25 for network stations. The network will (at a later date) be offered in a multi-user, multi-tasking configuration. The multi tasking operating system will be based on the BELL LABS UNIX III operating system. Multi-tasking will allow concurrent processing of data, thus increasing system throughput.

The International Standards Organization (ISO) and the American National Standards Institute have developed a seven layer hierarchical network model. The Victor LAN network board will implement the four lower levels.



## ISO SEVEN LAYER NETWORK MODEL

### LAYER 1. Physical Layer

The unit of exchange is the bit; considerations are voltage or current levels, signal timing, and connector pin assignments.

### LAYER 2. Data Link Layer

The unit of exchange is the frame, independent of any data content; considerations are error detection, frame acknowledgment, retransmission on errors, and duplicate frame detection.

### LAYER 3. Network Layer

The unit of exchange is the packet; considerations are message/packet conversion, verification of receipt, etc.

### LAYER 4. Transport Layer

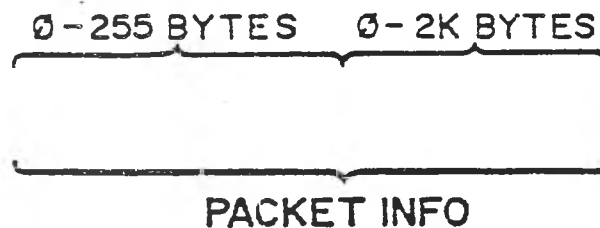
The unit of exchange is the message; considerations are message ordering, host to host communication, etc.

### LAYER 5-7. Session, Presentation, and Application Layers

The unit of exchange is the message; considerations are applications oriented, such as billing, encryption, code compression, etc.

The Victor network software and applications software will implement the upper three layers.

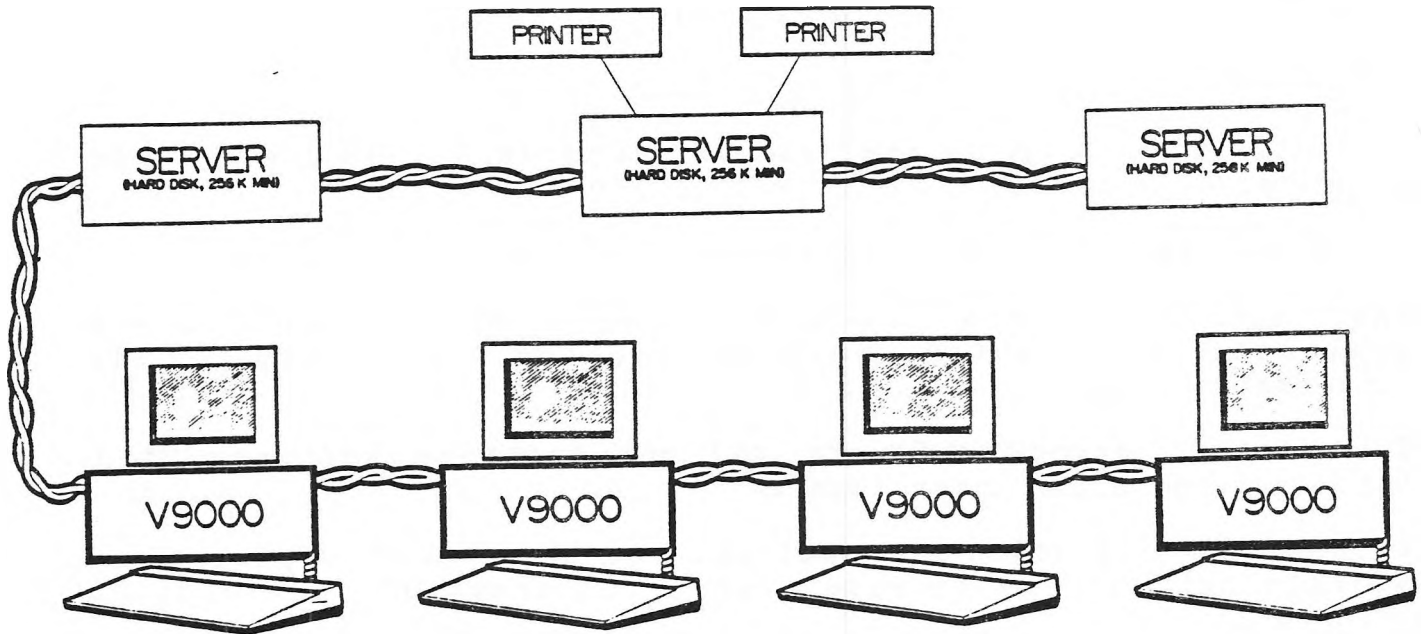
Network communication protocol will be the packet. A packet may contain data, node addresses, error information, and control information.



Each station on the network will need some method of accessing the network communications channel. The technique used will be carrier sense multiple access (CSMA). CSMA is a technique where a node requiring access to the channel will sense the channel for the presence of a carrier (activity), if no carrier is sensed for a predetermined amount of time, the node accesses the channel. If activity is sensed, the node will calculate a "waiting" period before trying to access the channel again. The "wait for retry" period is initiated only when no carrier is sensed to prevent nodes from queueing up to the channel.

The Victor LAN system uses Positive message acknowledgment to ensure proper message reception. Positive message acknowledgment is a system in which all packet(s) transmitted MUST be acknowledged by the receiving station. If the packet is not acknowledged the host retransmits the packet until it is acknowledged or the packet retry limit is reached. CSMA along with positive message acknowledgment should effectively eliminate collisions.

Mass data storage is an important feature of a LAN. The Victor LAN mass storage units will be hard disk units with expanded memory (256K min.). These units will be called network servers. The network servers will also handle background printing of user files (SPOOLING).



## SECTION II HARDWARE OVERVIEW

The Victor LAN is based on the Corvus OMNI-NET network system. The network supports 64 users (10 servers, 54 stations). The communications channel is a twisted pair cable with a maximum end to end length of 1500 feet. The network data transfer rate approaches 1 mega-bit per second.

Each node on the network will contain a transporter board (network card). The network card is directly connected to the network communications channel and the host (node) computers data bus. The network card will handle all network functions thus freeing the host processor from the duty of controlling the network. The network board communicates with the host system data bus. The network board contains a DMA (direct memory access) controller that allows the network card direct access to its own on-board memory without host CPU intervention.

The network card will perform functions such as packet transmission and reception, packet formatting, error detection, and DMA transfers.

Each node on the network has a unique address. The address is switch selectable on the network card. The eight position DIP switch at location 1A is used to select the board address segment and set the interrupt priority level.

The network board default setting is at E810h (hexadecimal segment address). Switches 1-6 on switch 1A select the board segment address.

Switch #	Address bit #
1	A9
2	A10
3	A11
4	A12
5	A13
6	A14

**\*EXAMPLE: SW. 1-6 "ON" SELECTS ADDRESS SEGMENT E810h \***

Switches 7 and 8 are for selecting interrupt priority levels.

Switch #	Interrupt level
7 (ON)	4
8 (ON)	5
7,8 (OFF)	Disable interrupts

The eight position DIP switch at location 3M is used to select the user node address (0-9 servers, 10-63 stations). The switches are used to set a binary value from 0 to 63. A switch in the "ON" position represents a binary 0.

Switch #	Value
1	1
2	2
3	4
4	8
5	16
6	32
7,8	NOT USED

Example: switches 1,3,5 "ON" all others "OFF" selects node address 42.

The network card can be functionally broken down into four parts:

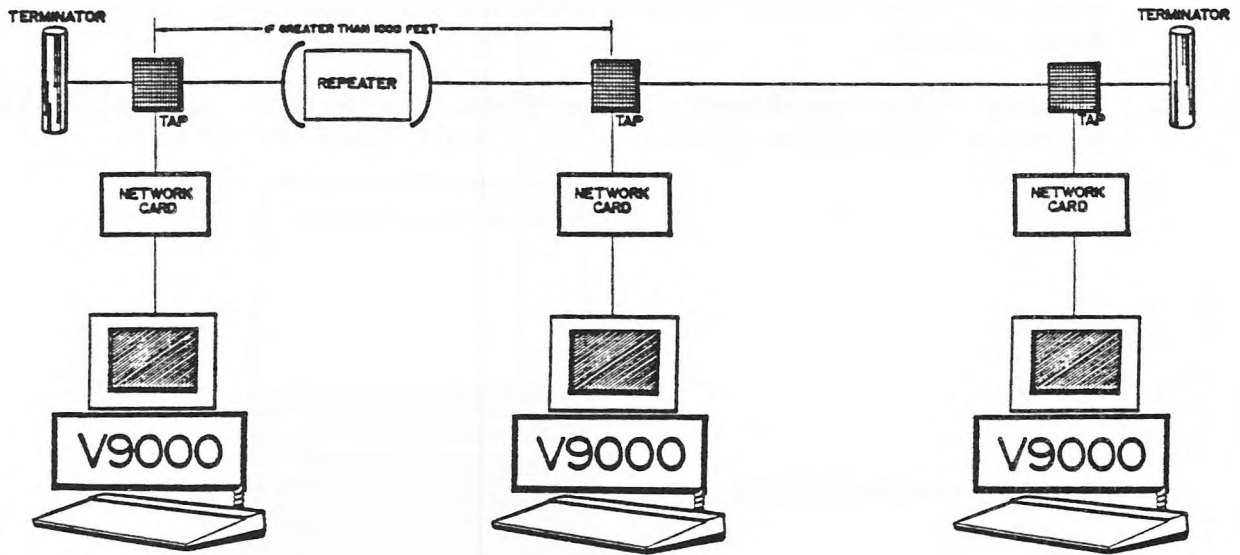
1. DMA controller
2. MC6854 advanced data link controller
3. 6801 microprocessor
4. RS-422 transceivers SN74174/SN74175

The DMA controller chip is a custom gate array chip designed to control the interface between the Victor computer bus and the Network card. Each DMA cycle is explicitly invoked by the 6801 microprocessor allowing the network software complete control of the DMA transfer between the Victor computer and the network card.

The MC6854 advanced data link controller (ADLC) controls many of the functions specified in the ISO data link and network layers. The ADLC performs such functions as data serialization, error code detection (CRC) and generation, packet framing, bit protocol implementation (NRZI non return to zero inverted) and zero insertion.

The 6801 microprocessor oversees the operation of the DMA controller and the ADLC. The 6801 controls the transfer of data and control information between the Victor computer and the Network card.

The SN75174/75175 chips form the RS-422 transceiver. The 75174 is a differential line driver, and the 75175 is a differential line receiver. Because the driver and receiver use differential circuits, they offer high noise immunity characteristics. The twisted wire pair was chosen as the communications medium because of its ease of installation and RFI (radio frequency interference) immunity level.



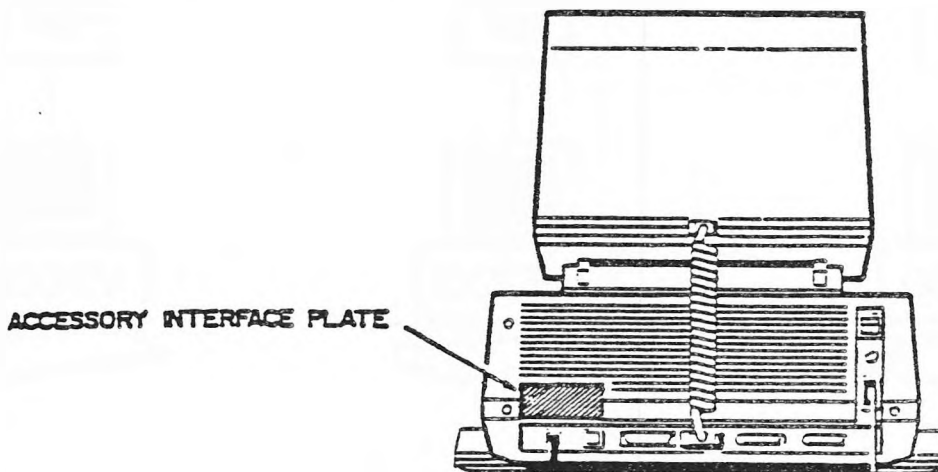
**SECTION III**  
**HARDWARE INSTALLATION PROCEDURES**

The network hardware procedure can be broken down into two areas:

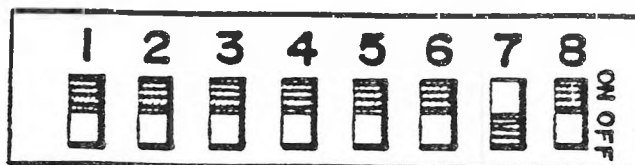
1. Transporter Installation
2. Trunk Cable Installation

**TRANSPORTER INSTALLATION**

- Step 1. Remove back panel from V9000/S1 by removing the four back screws.
- Step 2. Remove the accessory interface plate and install the network interface plate #104168-01 (see diagram).



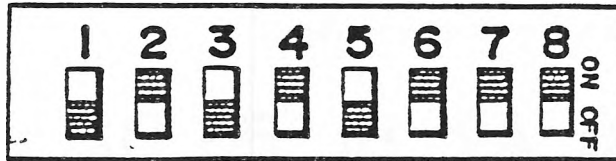
- Step 3. Remove top cover by sliding cover back.
- Step 4. Set transporter board DIP switch 1A (sw.# 1-6) to the ON position (Address Space E810H).



- SW.# 7,8 Set interrupt levels (int. 4 or 5)  
SW.# 7 Interrupt level 4  
SW.# 8 Interrupt level 5 (for all units)



- Step 5. Set transporter station address' 0-9 Servers, 10-63 stations. (SW.#1=LSB,SW.#6=MSB)



- Step 6. Install interface wire from accessory interface plate to connector J4 (upper right side of board)
- Step 7. Install transporter board in V9000/S1 expansion slot. (\* component side facing away from disk assembly \*)
- Step 8. Replace top cover and rear bezel (\* be sure to plug reset switch cable into cpu board connector J11, if applicable \*)

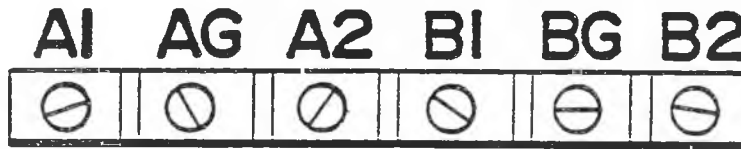
#### TRUNK CABLE INSTALLATION

The trunk cable is a braid shielded twisted pair cable,( Columbia #C1642-21-10 or Belden # ST9272). The trunk cable is terminated at each end by 100 ohm resistors (inside the end junction boxes). The distance between junction boxes should not exceed 1000 feet.

- Step 1. Place all workstations and servers in their assigned locations.
- Step 2. Lay the trunk cable so that it passes within 5 feet of each server or station. (see service loop diagram)
- Step 3. Install the junction boxes for each station and server . (see junction box installation)

## JUNCTION BOX INSTALLATION

Open the junction box by prying off the lid with a screwdriver. Inside the box is a terminal block (T1) and connector (J1) along with some passive components.



### Terminal Strip Description

A1-INCOMING TRUNK CONDUCTOR HOOKUP

A2-INCOMING TRUNK CONDUCTOR HOOKUP

AG-INCOMING TRUNK SHIELD HOOKUP

B1-OUTGOING TRUNK CONDUCTOR HOOKUP OR TERMINATOR

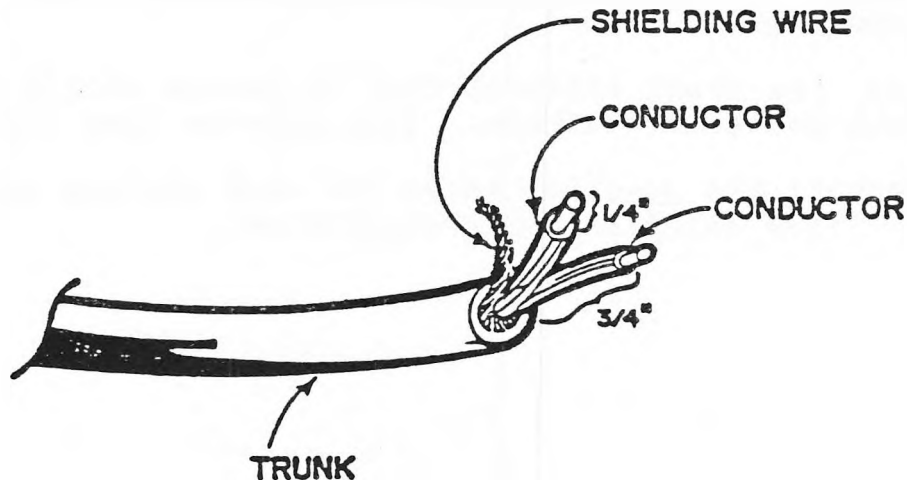
B2-OUTGOING TRUNK CONDUCTOR HOOKUP OR TERMINATOR

BG-OUTGOING TRUNK SHIELD HOOKUP

\* The end station/server junction boxes will leave the 100 ohm resistor in the B1-B2 position, these resistors are used to terminate the trunk cable \*

Cut the trunk wire and install the junction boxes as follows:

- A. Strip approx. 3/4 inch of insulation from the trunk cable, then strip approx. 1/4 inch of wire from the conductors.  
(see diagram below)



- B. Unravel the shielding wire and twist it into a single multi-stranded wire, tin the end of the shield wire.

- C. Take one side of the trunk cable and insert the conductors into A1 and A2 on the terminal strip. Insert the shield wire into AG. Tighten the terminal screws for AG,A1 and A2.
- D. Remove the resistor across B1-B2 junction. Take the other side of the cable and insert the conductor into B1-B2 on the terminal strip. Insert the shield wire into BG. Tighten the terminal screws for B1,B2 and BG.
- E. If the junction box is connected to the end station or server, then a 100 ohm resistor will be inserted across B1-B2 junction.

#### HARDWARE CHECK PROCEDURE

The field engineer should check the network system hardware before installing the network software.

- . Workstation/Server Units.  
The WS/Server unit should be checked out by using the Victor Diagnostic Diskette HDFIELD #104030 (for hard disk, single, and double sided units).
- B. The printer(s) should be checked by using the printer's selftest mode.
- C. The Transporter Board- Computer Interface can be checked out by booting up the workstation software #104764-01 (NETUP.EXE). If the software "sees" the board it will return the node address.

#### SOFTWARE INSTALLATION OVERVIEW

**Before any Server Network Installation is attempted the Victor FE MUST carefully read the Server Network Users Guide.**

1. The FE must make copies of the Master Server Software Diskette (1 for each Server + 1 extra).
2. The server system hard disk must be configured using the NETSETUP.EXE program. \*\* When diskless workstations become available their boot programs must be stored on the servers hard disk. \*\*
3. The FE must create a network station diskette for each workstation by using the MAKESTN.bat program. **The distribution of the INSTALL program should be controlled by the systems operator to control the installation/deletion of system users.**

4. Each workstation must be installed on the network system by running the INSTALL program on each workstation.
5. The users on the system that have been installed can be checked by using the NETUSERS program which will display all users installed on the system.

## SECTION IV FILE SERVER OVERVIEW

The Server Network product supports a local network of Victor work stations with one or more network servers providing mass storage and printer access for network users. The network servers are dedicated to providing services for network users and cannot be used as work stations. The network can include diskless network stations that boot from the network and have all their mass-storage on the network server(s). Each network server supports a ten megabyte hard disk and double-sided floppy disk drive, but does not need a screen or keyboard.

The network servers run network software under the MS-DOS 2.0 operating system while the network stations run a network interface in conjunction with MS-DOS 1.25. The appearance of the file system on a network server is transparent to programs running on the work station, with the network server's hierarchical file system being used to provide each user with private directories. Except for the private directories, all directories on a network server are treated as common storage and can be shared by one or more network users.

The Server Network product satisfies the following requirements:

- (1) The product supports diskless network stations.
- (2) The product supports multiple network servers.
- (3) The product supports MS-DOS based applications consistently.
- (4) Each network station user can keep private files on the servers.
- (5) Network stations can have common access to public files on network servers.
- (6) The product does not require a "super user" or system administrator. Configuration of the system and addition of network stations requires only basic MS-DOS 1.25 operation and usage familiarity.
- (7) Network server and station failures do not bring down the network, as long as at least one network server and station are operative.
- (8) The product supports background printing of files on the network servers.

An INSTALL program adds users to the network by taking an eleven-character user name, optional password, and assigning drive designators to link the user to disk volumes on the network servers. The INSTALL program takes the available drive designators (those not used for local work station storage) and sequentially assigns them to network server volumes with private and common directories being assigned in a ratio of one to two. The assignments are displayed, and can be changed if desired. Choosing the default assignments ensures that all users have consistent links to all network server volumes. Network installation is simplified by the use of standard AUTOSET files to configure network server hard disk volumes.

Common directory assignments can be made to a subset of network users allowing groups that work on common data to share files that, by installation conventions, are unavailable to other users of the network. Login to the network can be performed automatically if the network station is not shared among several people, or a user can be required to login by giving his or her name and password (if required). Utilities can be run to check the status of the network, list the network users, print files on the network server, or reserve files for exclusive access.

The network server supports three protection schemes for basic file sharing in common directories:

- (1) Files on a network server can be set to read/only using the PROTECT command. Any writes to a read/only file fail with a "write protect" error.
- (2) For read/write files, an automatic mechanism prevents concurrent access to a file that is being written or updated. Writes to the file succeed only if no one else has opened the file, and effectively lock the file so that no one else can open or modify it until the writing process closes the file. Attempts to write to a file opened by two or more users generates a write protect error, while attempts to open a file that is write-locked generate a "file locked or reserved" error. This mechanism can be turned off for applications capable of managing their own concurrent access to a file or files.
- (3) A user can reserve a set of files that are located on a network server using the RESERVE command. The reserve command ensures that no other network station will be able to open or modify the files until they are released by the user with the RELEASE command. This facility allows a set of files to be updated without the danger of con-current access by another user or an unexpected error from the automatic mechanism described above. Attempts to open a file reserved by another user result in a "file locked or reserved" error. A RESERVE-KEY option allows a process to reserve an arbitrary semaphore for applications that provide their own concurrent access management.

To facilitate sharing of up to three printers connected to a network server the network station interface can redirect list output at the network station to a specified file on a network server for later printing.

Network server volume organization is determined by choosing an AUTOSET file or using HDSETUP with the server machine configured as a local work station (keyboard and screen connected). AUTOSET configuration can be performed by creating a special configuration disk, keyed to the server number, that automatically formats the server when booted. This alleviates the need to have a screen and keyboard connected to the server.

Each server's hard disk can be configured as a number of logical disk volumes, but must have at least two. These are assigned to A: and C: (B: is used for the floppy). The hard disk is optimized for the smallest possible allocation unit sized without regard for memory usage (this is why 256K RAM is required in network servers). Small allocation unit sizes have the effect of increasing the effective size of the disk and allow more files to be stored for the network users.

A network server appears as a set of remote volumes to programs running on the network stations, with the server's hierarchical directories providing private directories for each user. A user's private directory is a sub-directory on a network server volume named with the user's eleven character login name. Each volume's root directory contains the common files for that volume. No change directory command is provided, so that network users do not have to understand hierarchical directories, and, they cannot access any sub-directories that have not been assigned to them by INSTALL. This ensures that other user's sub-directories are not accessible, and remain private to their owners.

The network station accesses remote volumes on the network by using standard MS-DOS drive designators (A: thru O:). If a network station has local disk drives, the remote volumes should use different drive designators than the local drives, although the INSTALL program does not prohibit this.

The file system is composed of all network servers on the network. Each network server has its hard disk volumes partitioned into multiple directories. The private directories of each user are only accessible by that user. MS-DOS 2.0 will enforce "read-only" or "read-write" protection on all files in both regular and private directories. These file attributes can be set by anyone able to access that file (only the user for private directories, and anyone with a drive assignment for common directories).

A network server may have attached printers, or other output devices which may be in demand by multiple network users. The devices may be connected to the server through the parallel interface or through Serial A or Serial B RS-232 ports. In order

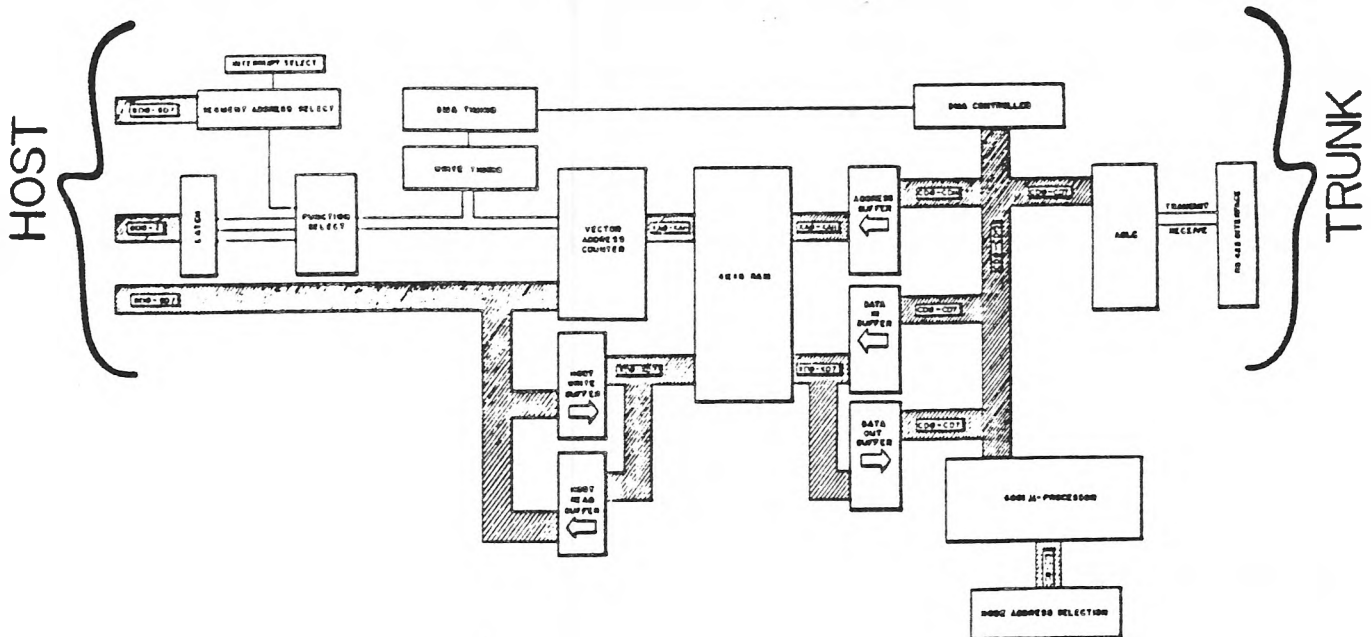
to share these devices, ~~operating system~~.  
The names of the spool files and the user names are placed into a  
queue maintained by the network server for each printer attached  
to the server.



## SECTION V NETWORK BOARD DESCRIPTION

The network card provides the intelligent interface between the host computer and the network system. The network card block diagram is shown below.

### NETWORK PCB ASS'Y BLOCK DIAGRAM



The network card can functionally be broken down into seven logical areas:

1. Board Addressing
2. Function Select
3. Ram Address Counters
4. RAM Memory
5. DMA & Write Timing
6. Omni-net Chip Set
7. RS-422 Transceivers

The network card is seen by the host (IE.V9000) as a memory mapped group of registers. The host reads and/or writes information to the network card's internal memory. The 4K internal memory is dual ported, it can be read or written by the host system or the 6801 microprocessor.

The Corvus chipset is the "heart" of the network card. The chipset consists of:

1. 6801 microprocessor
2. Gate array DMA controller
3. 68A54 advanced data link controller (ADLC)

The 6801 is an 8 bit microprocessor. The 6801 has 2K bytes of internal ROM (read only memory) which stores the board level network operating software. The 6801 controls all network card functions.

The 68A54 ADLC provides the interface between the RS-422 transceivers and the network board. The main functions of the ADLC are bit serialization, zero insertion, packet framing, CRC generation, and data byte buffering.

The DMA controller provides the timing and control for all data transfers occurring outside of the 6801. The DMA controller provides for six possible directions of data flow. The six data flow directions are:

1. 6801 to ADLC
2. ADLC to 6801
3. RAM\* to 6801
4. 6801 to RAM\*
5. RAM\* to ADLC
6. ADLC to RAM\*

\* denotes on board

## NETWORK BOARD-HOST INTERFACE

The host-transporter board (network board) interface allows two types of information exchange. The host computer can command the transporter card to perform one of several functions or part of a particular function. The host can send the message data to the transporter, or the transporter can send data that it has received to the host.

The host computer issues a command to the transporter by first writing a command vector in memory (4K RAM on network card) and then sending the address of that command vector to the 6801 microprocessor. The command vector address is stored in the 6801's 128 byte internal RAM memory.

The command vector tells the 6801 what it is supposed to do. The command vector will always contain the address of the result record in memory. The result record contains command status information as well as other types of information that will be updated by the host.

A transporter will transmit one message at a time, but may be activated to receive up to four messages in succession before receiving another command. Normally the 6801 will generate an interrupt after the command vector address has been validated. When the command has been completed the 6801 will generate another interrupt.

#### COMMAND MECHANISM

Commands are initiated from the host to the transporter by the host sending a 12 bit address to the 6801 microprocessor on the transporter board. This 12 bit address is the command vector address. This address points to some location within the 4K of on board RAM. The command vector contains a command code, a result record address, and other command information.

Before issuing a command, the host must write the value FF (hex) to the status byte of the return record. When the command is completed, the transporter will signal the host by changing the status byte to some other value and generating an interrupt to the host.

Command vector addresses are sent to the 6801, one byte at a time, by using a polling method to determine when the 6801 is ready to accept another byte.

The X-READY line is used to indicate the transporters ability to accept a byte of information. The polling process is implemented by using a two signal handshake. When the transporter is ready to accept a vector address byte from the host, the 6801 asserts the X-READY line high. When the host is ready to send a byte to the transporter, it sets the X-STROBE line low and asserts the data byte on the BDO-BD7 bus lines. When the X-STROBE line is asserted low, the X-READY line is also asserted low to prevent the host from transferring another byte of data before the previous byte has been accepted. The transfer is complete when the host asserts the X-STROBE line high. The host must wait for the X-READY line to go high before it can transfer another byte.

(insert ready-strobe timing diagram)  
p.27 omninet tech.ref. man.

The transporter board does DMA (direct memory access) transfers to the on board 4K RAM. DMA transfers are controlled by the gate array DMA controller chip.

The DMA cycle is initiated by the 6801 which outputs the 12 bit DMA address along with address bits 13,14, and 15. Address bits 14 and 15 are used to inform the DMA controller that a DMA transfer is being requested. When the 6801 asserts the code 01 on bits 14 and 15 the DMA chip knows a DMA transfer is being requested. Address bit 13 is the carry bit. When the DMA controller reads the code 01 on address lines 14 and 15, it drives the HACLK signal high. The low to high transition latches the DMA address into the address latches (sh.3 schematics 102991, 1N and 2K) and marks the beginning of the DMA cycle.

At this point the DMA controller takes over the responsibility for synchronizing the data transfer between RAM and the 6801 or the ADLC. Because the ADLC receives data over the network serially, it handles data slower than the 6801 which handles data in byte format. The 6801 must be halted until the ADLC is ready to receive or transmit a byte of data.

The DMA controller halts 6801 operation by freezing the clock (XTAL2) that it normally supplies to the 6801. This causes the EIN signal to stop from the 6801 which the DMA controller normally routes to the ADLC as signal EOUT. The ADLC would cease to function if it were not for the fact that the DMA controller chip takes over and provides the EOUT clock to the ADLC. The controller continues in this mode until the ADLC asserts the signals TDSR (transmit data service request) or RDSR (receive data service request) indicating that ADLC readiness to transmit or receive an entire byte of data. When this occurs the DMA controller unfreezes the 6801 by restoring the XTAL2 clock to the 6801 and asserting either the HDOUTS or the HDINC lines low on the falling edge of the current EOUT pulse.

When HDINC transitions from low to high, data from the 6801 bus is latch into the Data In Buffer (2L). When HDOUTS transitions from low to high, data to the 6801 bus is latched into the Data Out Buffer (2M).

HACLK is asserted low approximately 400ns after the rising edge of the last EOUT signal from the DMA controller. EIN is asserted low approximately 400ns before the DMA controller takes over producing the EOUT signal. At this point HDINC and HDOUTS return high and the data is latched into the buffers. The part of the DMA cycle that involves the 6801 data bus is completé.

When the DMA controller needs to transfer data to memory (on board 4K) it asserts XMAREQ high along with HDINC or HDOUTS. When XDMAREQ is asserted high the DMA timing circuit checks to see if the host is writing to memory, if the host is not it asserts the

XDMAGO signal and the XHAENA signal low. This tells the DMA controller that it is clear to begin the DMA transfer. When the DMA controller sees the DMAGO signal, it asserts XDMAREQ low and either HDOUTS or HDINC low depending on the direction of the transfer. XDMAGO transitioning from low to high signals the end of the DMA cycle.

BOARD ADDRESSING - \*Use schematics 102991 (network)

The network board is enabled when the segment address (selected by DIP switch 1A) is placed on the address bus. DIP switch 1A can select segment address spaces E810-EFF0 (on odd segment boundaries IE. E830, E850, etc.).

Address bits A8-A14 along with the CSEN signal are input through connector J1 to 74LS85 comparators (1B & 2B). The comparators compare the address bits A9-A14 to the switch settings on DIP switch 1A. Address bit A8 and signal CSEN must be high to match their inputs to comparator 2B. When the address asserted on the bus matches the selected segment address, CSEN and address bit A8 are high, the XBEN (board enable) signal is asserted low. The XEXTIO signal is also asserted (low) through connector J1 to the CPU board.

The XBEN signal is used to enable the function select register (sheet 2, loc. 2D). Address bits A0-A2 are latched into 74LS373 (sheet 4, loc. 1C) on the falling edge of the signal ALE. These latched address bits form the signals BSEL0, BSEL1 (board selects) and LA2 (latched address bit 2). These signals are used to select one of the nine board enable functions.

## INTERRUPTS

The 6801 microprocessor on the network card generates an interrupt to the host (IE.V9000) whenever a command is accepted or completed. The interrupt is generated by the 6801 to tell the host to examine the return code value for the instruction. The interrupt levels are set on DIP switch 1A as follows:

Switch 7 ON, switch 8 OFF	level 4
Switch 8 ON, switch 7 OFF	level 5

The network card provides for cascading of interrupts from additional local host based network cards. Connectors J2 and J3 on the network card are used to chain network card interrupts together.

The host "sees" the network card as a memory mapped set of registers. The host can select nine address spaces. Each address space is setup to perform a different function. The default board segment address is E810.

### Network Board Function Offsets

Read at offset 0	Read with increment
Write at offset 0	Write with increment
Read at offset 1	Read (no increment)
Write at offset 1	Write X-STROBE
Read at offset 2	Read low (byte) counter
Write at offset 2	Load low (byte) counter
Read at offset 3	Read high (nibble) counter
Write at offset 3	Load high (nibble) counter
Read at offset 7	Read X-READY status at bit 08 (HEX)

The 74LS138 (2D) is the function selection decoder chip. BSEL0, BSEL1 and BRD/ serve as the inputs to the decoder. The decoder (2D) is enabled by the BEN/ (board enable) signal. The following discussion describes the decoder functions.

Read with increment

Default(E810:0)

When address space E810:0 is read from, the host reads data from the transporters RAM. The decoder (2D) asserts output 0 low. The low signal is input to the negative logic AND gate (2E) pins 2 & 5. The output pin 6 (2E) enables the output control of the 74LS374 latch at 1H (Host Read Buffer). The output pin 3 (2E) is asserted to the clk (clock) input pin 14 on the address counters (1E, 2H, and 2F). When the clock input transitions from low to high, the address counter is incremented by 1.

Read (no increment)

Default(E810:1)

When address space E810:1 is read from, the host reads one byte of data from transporter RAM through the host read buffer. The decoder (2D) asserts output 1 low. This low is input to negative logic AND gate 2E (pin 4), this causes the output pin 6 to assert a low to pin 1 of the Host Read Buffer (1H). This enables the output of the buffer.

Read low counter address

Default(E810:2)

When the host reads from address space E810:2, the host can read the low (byte) of the address counter through the BD0-BD7 data bus. The decoder asserts output 2 low. This is the signal RDLOW/. The RDLOW/ signal enables the buffer at 1F, allowing the counter address (low byte) to pass from the C0-C7 bus (counter address bus) to the BD0-BD7 bus.

Read high counter address

Default(E810:3)

When the host reads from address space E810:3, the host can read the high (nibble) of the counter address. The decoder asserts output 3 low. This output enables the buffer at 1D, enabling the counter address bits C8-C11 onto the BD0-BD7 bus.

Read X-READY status

Default(E810:7)

When the host reads from the E810:7 address space, the X-READY signal status can be read from bit BD3 (08 Hex) on the buffered data bus. The status is ready by selecting function 3 (read high counter nibble) and substituting X-READY for address bit C11. The LA2 signal is used to determine whether address or status is read at bit 08 Hex of the high counter address. When LA2 is low, AND gate 3A (pin 11) is enabled passing counter address bit C11 to buffer 1D (pin 4). When LA2 is high, AND gate 3A (pin 3) is enabled passing X-READY through to buffer 1D pin 4.

Write

Default(E810:0)

When the host writes to the E810:0 address space, the write function is enabled. When the decoder asserts the output number 4 low, this causes the S-R flip flop composed of AND gate 3D (pins 1,2,12,13) to set asserting the output at pin 3 high. The output from pin 3 is input to pin 9 (3D). The output from 3D pin 8 is input to 2E pin 1. The output of 2E pin 3 is input to the clk (clock) input of the address counters. When the clk inputs transition from low to high the address counters are incremented. The output from gate 3D pin 8 is also input to gate 4E (pin 1). The output from gate 4E pin 3 is input to 4E pin 12. The output from 4E pin 11 is the write signal to the RAM memory chips(1L,1K). The low asserted from the decoder (2D) is input to gate 2E pin 10 also. The output of 2E pin 8 is input to the host write buffer (1J) pin 11, latching data from the BD0-BD7 bus into 1J. The output from 2E pin 8 is also input to 4B pin 3. The low to high transition on 4B pin 3 starts the write timing generator (4B,4A).

Write X-STROBE

Default(E810:1)

When the host writes to address space E810:1, the X-STROBE signal is issued to the DMA controller chip. The decoder asserts output 5 low, this resets the S-R flip flop (3D) disabling the write signal to the RAM chips. The write timing generator is started and the X-STROBE signal is asserted from 3D pin 6 to the DMA controller.

Load low (byte) to address counter      Default(E810:2)

When the host writes to address space E810:2, the low address counter is loaded with a byte of data from BD0-BD7 bus. This data is the low byte of the RAM address. The decoder asserts the output 6 low, this signal is input to the LD (load) inputs on counters (2H,2F).

Load high (nibble) to address counter      Default(E810:3)

When the host writes to address space E810:3, the high address counter is loaded with a byte of data from BD0-BD3. This data is the high byte of the RAM address. The decoder asserts the output 7 low, this signal is input to the LD (load) input on counter 1E.

## CHIPSET

The central logic of every transporter is contained in three integrated circuits, an MC6801 microprocessor, an MC68A54 advanced data link controller, and a custom gate array. Together these three circuits comprise the CHIPSET. They provide control and intelligence for all transporter operations.

## MC6801-1 PROCESSOR

The MC6801 is an 8-bit single chip microcomputer unit (MCU) and the heart of the CHIPSET. Contained within the 6801 is 2048 bytes of ROM which store the transporter operating program, and 128 bytes of RAM which are utilized for temporary storage by the program. The program itself runs on the 6801 and controls all transporter functions from the moment of power up. Command information is interpreted and acted upon by the program and line transmissions are responded to appropriately.



For proper operation the MC6801 must be operated in the Expanded Multiplexed Mode 6. A description of this mode plus a complete list of MC6801 specifications can be found in the Motorola 6801 data sheet.

Port 4 (Pins 22-29) When a transporter reset occurs, either because the host issued the Initialize command or because a power-up occurred, this port is configured as all inputs, and the network node address is read in from the transporter board dip switches. Pins 24-29 receive the six bit node address. After the node address is read, the port is reconfigured as outputs for address bits 8-15 on pins 22-29. The port remains in output mode for the duration until another reset occurs.

Pins 10-8 On the rising edge of RESET (Pin 6), these three pins are inputs which select which mode the MC6801 is to operate in. External hardware insures that mode six is always selected as mode 6 is the only mode in which the network program will run.

At all other times, pins 9-20 are unused while pin 8 receives the input capture interrupt (IRG2) on any low transition of FD (flag detect) from the ADLC.

Pin 11 On the rising edge of RESET, this pin is not used. At all other times, this pin is an output, active low, used to drive the indicator LED whenever the transporter is actively transmitting.

Pin 12 Pin 12 is not used...

<u>PIN</u>	<u>NAME</u>	<u>FUNCTION</u>
13	AUTO	Output, active high, used by the DMA chip to decode which DMA mode is selected.
14	IN/OUT	Output, used by the DMA chip to decode which DMA mode is selected. High indicates IN, low indicates OUT.
15	RSO	Output, used by the ADLC to find which of its internal registers has been selected for DMA.
16	READY	Input, active high. This signal travels to the host as well as to the 6801 and indicates to the host that the transporter

- 16      READY cont'd      is ready to receive another command vector address byte into the CAR (Function Select Decoder). This signal is generated by the DMA controller.
- 18      HDINT      This is the interrupt signal to the host. It is active low. The 6801 pulses HDINT after modifying the command return code to let the host know that command status has changed.
- 19      IRQ1      This is an input used to detect the collision avoidance condition during a transmit attempt. IRQ1 is an open collector and can be generated by either the DMA chip or the ADLC. However, it is the DMA chip that sets IRQ low to indicate a collision avoidance.
- 20      NADDRS      This signal is an output, active high, which gates the node address from the dip switches onto port 4 after a reset.

#### MC68A54 - ADVANCE DATA LINK CONTROLLER (ADLC)

The ADLC provides the interface between the RS-422 transceivers and the rest of the transporter. The main functions of the ADLC during transmission operations are bit serialization, zero-insertion, packet framing, CRC generation, and data byte buffering. The ADLC performs these functions in reverse when receiving information.

Because the ADLC has no special transporter defined signals, all references to the ADLC signal descriptions or timing characteristics should be traced to the Motorola data sheet, ADLC and other transporter circuits. First, pin 12 (R/W) of the ADLC should be connected to the IN/OUT output, pin 14, of the MC6801. This note is important because the 6801 also has a signal named R/W.

#### DMA CONTROLLER

The DMA controller also known as the Custom Gate Array, provides the timing and control for all data transfers occurring outside of the 6801 microcomputer. There are six possible directions of data flow via DMA. In addition the DMA chip performs such functions as decoding the intended actions of the 6801, generating DMA address bits 15-13, and providing the host interface for DMA cycles. To understand how the DMA chip accomplishes all of this, we provide a description of each DMA chip connection and its function, as follows.

<u>NAME</u>	<u>PIN</u>	<u>FUNCTION</u>
CLK	24	Input. Symmetric 10 Mhz clock.
EXTAL2	23	5 Mhz clock output to the MCU. This clock is halted (frozen) during DMA cycles shortly after the DMA chip generates the HACLK signal. The clock remains frozen (thus freezing the 6801) until the DMA chip receives one of the signals TDSR or RDSR from the ADLC.
EIN	6	1.25 Mhz clock received from the 6801. The DMA chip uses this signal for the timing of internal events (e.g. loading the 3-bit address register, freezing EXTAL2). This signal freezes when EXTAL2 freezes.
EOUT	7	1.25 Mhz clock output to the ADLC which uses it for internal timing. EOUT does not freeze during DMA's.
BITCLK	27	1 Mhz clock output to the ADLC for timing of bit transmission and reception. During transmission it is free running. During reception it is resynchronized to the source station every time a zero bit (line transition) is received.
RXD	26	Input from RS-422 receiver. RXD receives the data sampled during packet reception and detects zero bits for resynchronizing BITCLK. RXD is also used to trigger the collision avoidance circuit before packet transmission.
RTS	28	Request to send from the ADLC. On the leading edge of RTS the DMA chip decides to either assert TXENA (no collision) or IRQ (collision).
CS	37	Chip select output, active low. CS selects the ADLC when the 6801 is either reading or writing to ADLC registers.
TDSR	1	Transmitter data service request from the ADLC indicates that the transmit FIFO of the ADLC is empty and ready for the next byte of data during message sends. TDSR is active high.
RDSR	2	Receive data service request from the ADLC indicates that the receive FIFO of the ADLC is full and ready to transfer the byte to

RDSR	2 cont'd	the 6801 or host via DMA. RDSR is active high.
TXENA	29	Transmit enable, active high. If the collision avoidance circuit has not been triggered by RXD then the DMA chip will assert TXENA high on the leading edge of RTS. This enables the RS-422 driver to gate data onto the twisted pair.
A15	10	A15-A13 are sampled on each high to low transition of AS from the 6801. When A15 is low and A14 is high HACLK will go high indicating the beginning of a DMA cycle. If A15, A14, and A13 are all high, this indicates that the 6801 is attempting to load the high order DMA address bits into external latches and into the DMA chip. The DMA chip will then generated the HALOAD signal.
A14	9	See A15.
A13	8	A13 has one of two different functions during a DMA cycle depending on which DMA mode has started. If the cycle involves the host memory, A13 is the carry bit from the low order 13 DMA address bits and is added to the contents of the three bit internal register of the DMA chip to generate host address bits 15-13. If the DMA mode does not involve host memory, A13 selects the ADLC mode for the DMA transfer. The 6801 may read or write to ADLC status and control registers as well as to the receive and transmit data FIFO's.
D0	11	D2-D0 are inputs from the 6801. On HALOAD these bits are latched into an internal register as DMA address bits 15-13 respectively.
D1	12	See D0.
D2	13	See D0.
IRQ	30	The DMA chip generates IRQ to interrupt the 6801 when the collision avoidance circuit triggers. At other times the ADLC may generate IRQ. IRQ is active low.
RESET	25	Active low input which resets internal logic to initial state.

COUT	15	Active high output: COUT is the carry bit from DMA address bits 15-13. COUT is only important where DMA addresses are longer than 16 bits. In this case it should be connected to CIN of the four bit adder for address bits 19-16.
STROBE	32	Active low input from the host which has the effect of loading the Command Address Register. When the DMA chip receives STROBE, it generates HDOUTC which clocks a command vector address byte from the host data bus into the HOST DATA OUT LATCH.
READY	31	Status signal output to the host. High indicates that the CAR is ready to receive a new command vector address byte.
HACLK	21	Active high output which externally latches DMA address bits 15-0 and indicates that a DMA cycle has begun. This signal stays high while the 6801 is frozen.
HDOUTS	38	Active low output. Gates data from the HOST DATA OUT LATCH onto the 6801 data bus during DMA's.
HDOUTC	33	Active low output. Clocks data from the host memory data bus into the HOST DATA OUT LATCH. When IN/OUT is low, this signal will follow STROBE, or DMAGO.
HDINS	36	Active low output. Gates data from the HOST DATA IN LATCH onto the host memory data bus. When IN/OUT is high, this signal will follow DMAGO.
HDINC	39	Active low output. Clocks data from the 6801 data bus into the HOST DATA IN LATCH.
DMARQ	34	Active high output. Indicates that the transporter is requesting a DMA transfer with host memory.
IN/OUT	4	Input from the 6801 used to determine in which direction a DMA transfer with host memory is to be. High indicates that the transfer is into host memory. Low indicates a transfer out of host memory.
DMAGO	35	Active low input. This is the expected response to DMARQ. It indicates the host's readiness to proceed with a DMA transfer.

DMAGO	35 cont'd	Upon reception of DMAGO, the DMA chip will send either HDOUTC or HDINS depending on the direction of data transfer.
HAENA	22	Active low input from the host. Gates DMA address bits 15-0 onto the memory address bus and should be used to gate the other address bits onto the bus as well.
AS	19	The high to low transition of this input from the 6801 is used to sample bits A15-A13 of the 6801 address bus to determine whether a DMA cycle is to begin or if the 6801 wishes to load the high order DMA address bits into external latches and into the DMA chip. AS is pulsed at the beginning of every DMA cycle.
AUTO	3	Active high input from the 6801. Used to decode which DMA mode is to begin. See MODE chart below.
R/W	5	Same as AUTO. See MODE CHART below.

## DMA MODES

As was mentioned at the beginning of this chapter, there are six possible directions of DMA data flow. These six directions correspond to the six source/destination combinations possible between the host, the 8601, and the ADLC. In addition, the 6801 may write to the control registers or read the status registers of the ADLC. These two operations constitute two additional DMA flows as normal 6801/ADLC interchanges involve data being sent or received over the OMNINET trunk. The DMA chip makes this selection as well as the selection of the basic DMA flow direction according to information it receives from the 6801. This information is interpreted according to the Mode Chart below.

### TRANSPORTER MODE CHART

MODE	MC6801 OUTPUTS				DIRECTION OF DMA FLOW	
	AUTO	IN/OUT	R/W	A13	SOURCE	DESTINATION
A	0	0	0	0	6801	ADLC
A1	0	0	0	1	6801	ADLC (C)
B	0	0	1	X	HOST	6801
C	0	1	0	X	6801	HOST
D	0	1	1	0	ADLC	6801
D1	0	1	1	1	ADLC (S)	6801
E	1	0	1	X	HOST	ADLC
F	1	1	1	X	ADLC	HOST

Mode A1 represents a write operation from the 6801 to a control register of the ADLC. Mode D1 represents a read by the 6801 from a status register of the ADLC. During modes B, C, E, and F which involve the host, the value of A13, represented by an "X" in the chart above, is added to the 3-bit register of the DMA chip to get DMA address bits 15-13.

When the flow of DMA is between the host and either a control or status register of the ADLC, additional signals are required to inform the ADLC as to which of its four control registers or two status registers has been selected. These signals are RSO and RS1 from the 6801 and have already been mentioned briefly in our discussion of 6801 pin connections.

As a final note, it should be clear that it is not always necessary to freeze the 6801 during DMA cycles. This need only occur when the ADLC is involved in DMA transfers and then, only when the data being transferred is data which is intended for transmission over the trunk cable or which is being received over the trunk. In these two situations the ADLC has the responsibility for converting the data either into or out of a serial form and as a result, the ADLC processes each byte of data more slowly than does its DMA partner. Neither the 6801 nor the host processor need operate on the individual bits of a particular data byte and so these two processors function more quickly than can the ADLC.

In order to resolve the timing problem resulting from this discrepancy in operational speeds, the 6801 must be prevented from continuing on with its next programmed instruction until the ADLC is ready to begin a new operation. The DMA chip manages this by halting the clock to the 6801 and so freezing the 6801 dead in it's tracks. The 6801 is only allowed to continue operation after a signal from the ADLC (either TDSR or RDSR) indicates to the DMA chip that the ADLC is ready to proceed.

#### ADDRESS COUNTERS

The address counters are composed of 74LS191 binary counters (1E,2H,2F). These UP counters provide the address to the RAM chips for host read or write operations. The base address is loaded into the counters from the host. While there is no DMA transfer or request from the DMA controller, counter addresses are passed through drivers 1D and 2J to RAM on the XA0-XA11 bus. When the DMA chip requests a DMA transfer to RAM, the drivers (1D,2J) are disabled.

#### RAM MEMORY

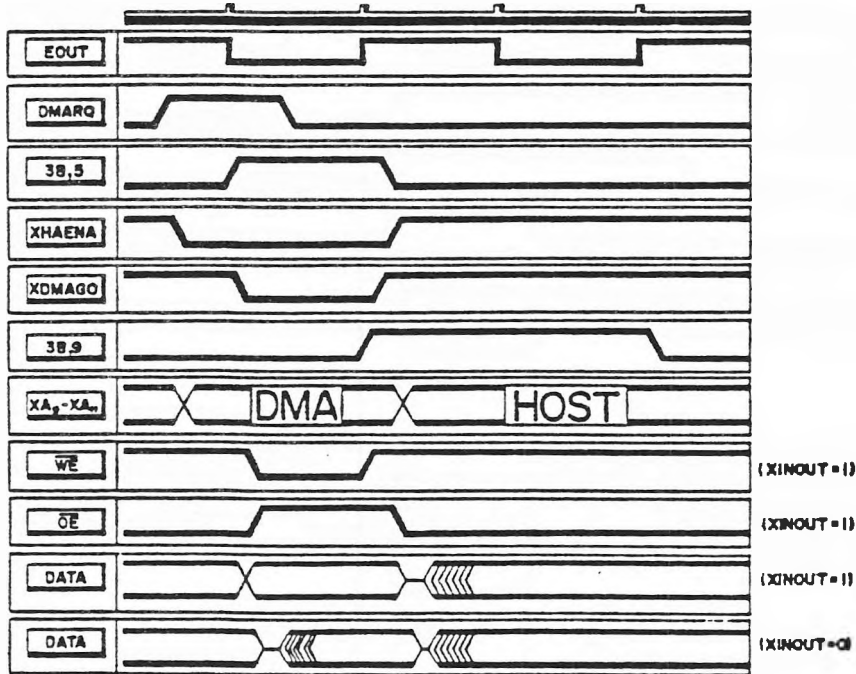
The 4K of transporter RAM is composed of (2) 2Kx8 RAM chips (1L,1K). The RAMS are addressed by an 11 bit address XA0-XA10. Address bit XA11 is used to select either the lower (000-07FF) or the upper (0800-0FFF) banks. The WE/ (write enable) can be generated by the host or the DMA controller. The write enables are synced to the EOUT 1.25 MHz clock. The OE/ output enable is enabled when X-HINS is high and 4B pin 9 of the write timing generator is low.



## DMA REQUEST/GRANT TIMING GENERATOR

The 74LS74 flip flops compose the DMA timing generator. This circuit generates the timing needed for DMA transfers to/from RAM. These transfers are synchronous. The timing diagram below describes the action of the timing circuit.

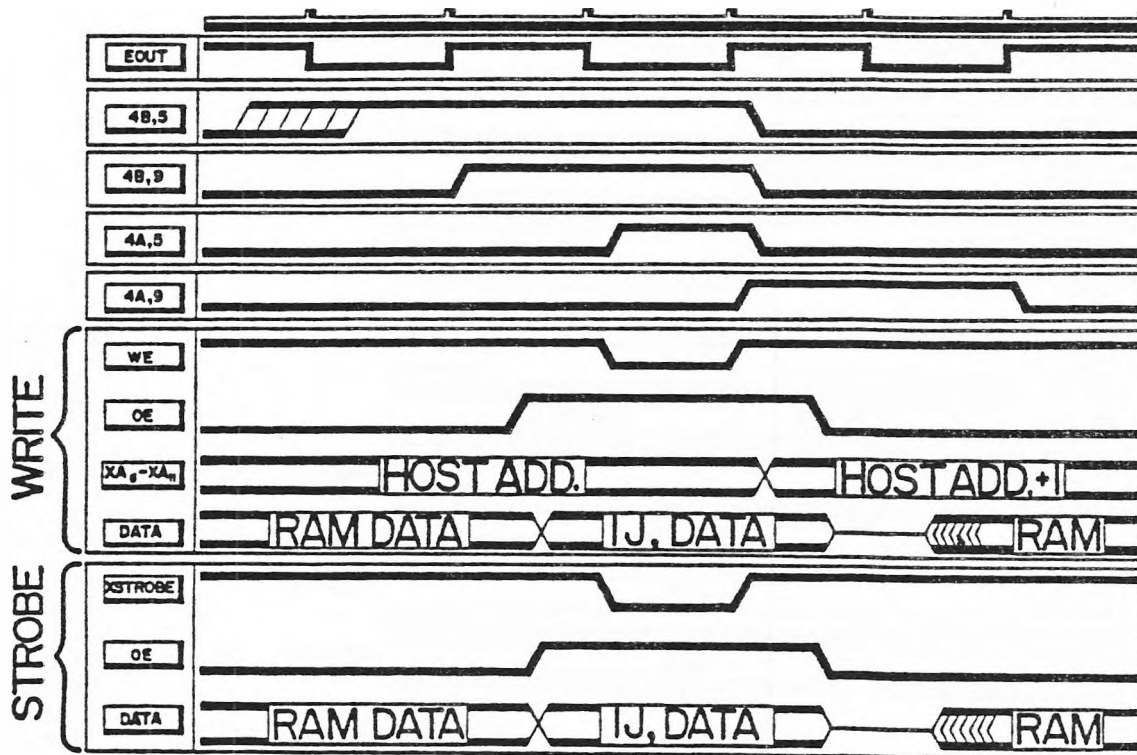
## DMA REQUEST/GRANT TIMING



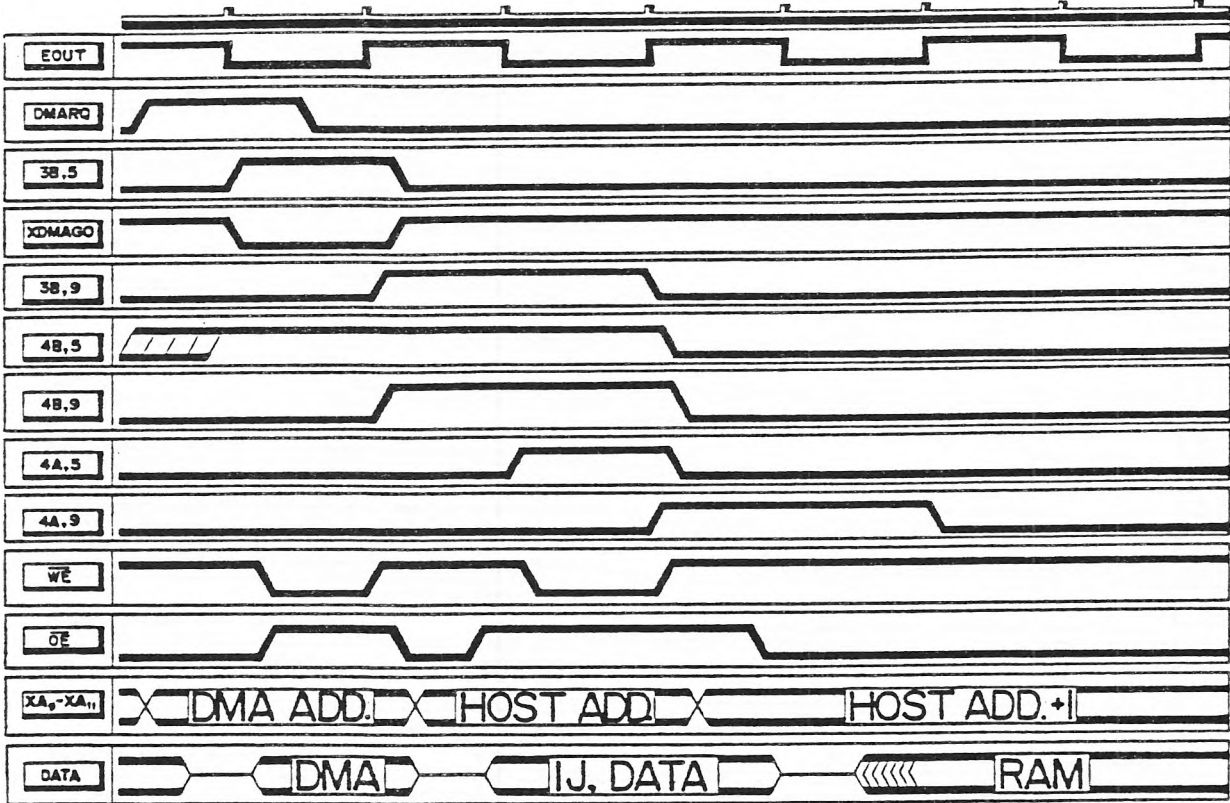
# WRITE TIMING GENERATOR

The Write timing generator is composed of 74LS74 flip flops 4A and 4B. These flip flops generate the timing needed to write data to RAM. These transfers are asynchronous. The timing chart below shows the timing function of the write timing generator.

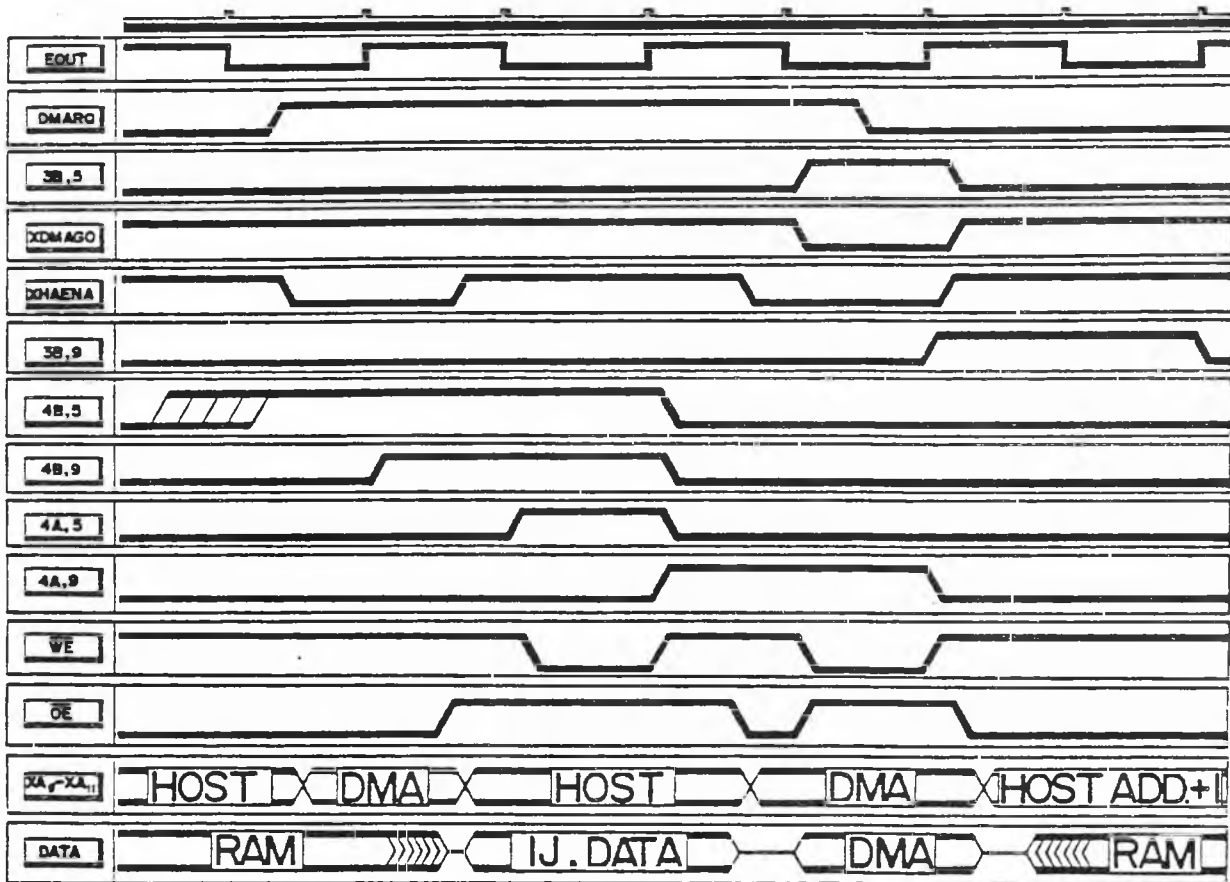
## HOST WRITE/STROBE REQUEST



# OVERLAPPED DMA/HOST REQUEST WITH DMA IN PROGRESS

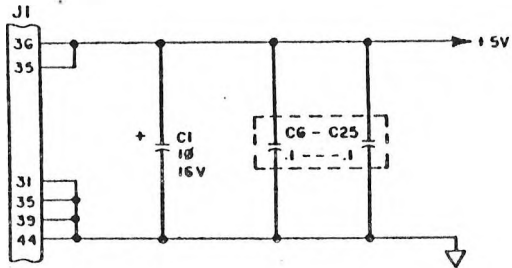


# OVERLAPPED DMA/HOST REQUEST WITH DMA HELD OFF



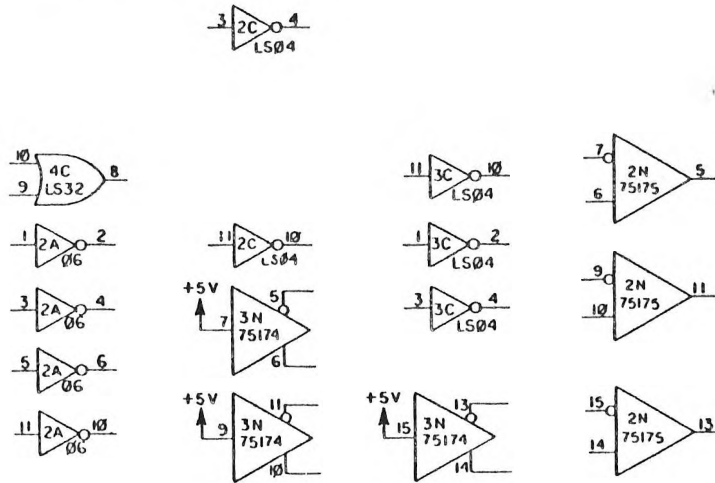
**SECTION VII**  
**SCHEMATICS**

REV	NO	DESCRIPTION	DATE
1	1	RELEASED FOR EVALUATION	8/22/77
2	1	RELEASED FOR EC 11206	11/15/77



DEVICE	GND	+5V
74LS74	7	14
LS32	7	14
LS132	7	14
LS00	7	14
LS00	7	14
LS05	8	16
LS373	10	20
LS244	10	20
LS191	8	16
LS374	10	20
LS138	8	16
7406	7	14
75174	8	16
75175	8	16
6116P	12	24
MCG8A54	1	14
DMA CONTROLLER	20	40
6801	1	21

SPARE GATES:

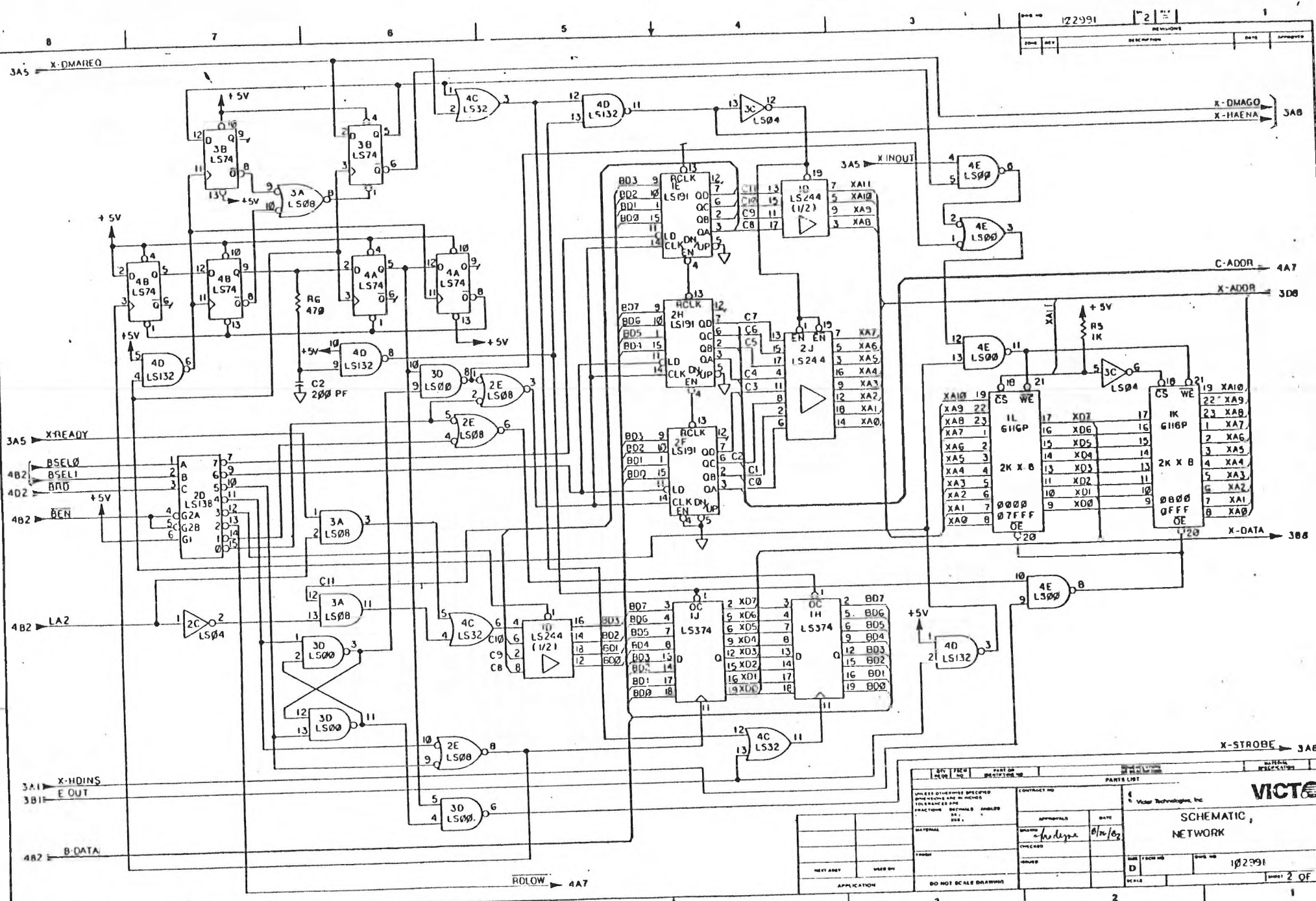


NOTES - UNLESS OTHERWISE SPECIFIED:

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE  $\pm 5\%$ , 1/4W.
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES, EXCEPT AS NOTED.

REFERENCE DESIGNATORS	APPLICATION
1.1, L2	RN 1
	L2
	J4, C29
	Y1, Q1
C5	DS1, R9
NOT USED	LAST USED

DATE: 11/15/77	REV: 1	DESCRIPTION: SCHEMATIC NETWORK	PROJECT: VICT
DESIGNED BY: [Signature]	CHECKED BY: [Signature]	DATE: 11/15/77	SCALE: AS SHOWN
DO NOT SCALE DRAWING		DATE: 11/15/77	SCALE: AS SHOWN



2% TOLERANCE UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES ARE . . . . .		CONTRACT NO. PARTS LIST Victor Technologies, Inc.	
APPROVALS DRAWN: <i>ah/djpa</i> CHECKED: <i>blm/ez</i>		DATE:	
TITLE:		SHEET NO. 15 OF 15	
DATE:		102991	
APPLICATION:		SHEET 2 OF 4	

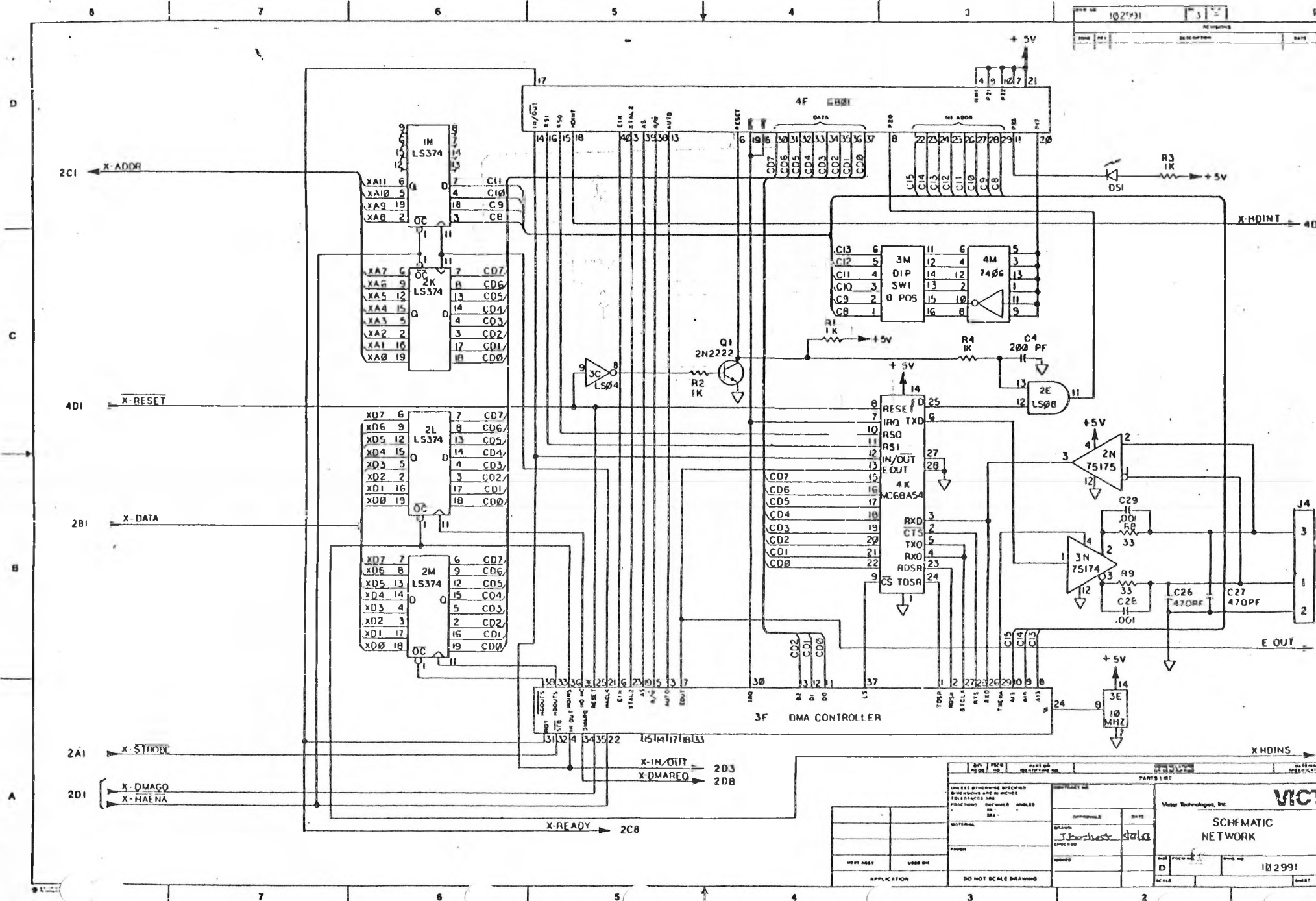
**VICTOR**

SCHEMATIC,  
NETWORK

102991

15

2 OF 4



PARTS LIST		DATE	
Q1	2N2222	DATE	
R1	1K	DATE	
R2	1K	DATE	
R3	1K	DATE	
R4	1K	DATE	
R9	33	DATE	
C1	100	DATE	
C2	100	DATE	
C3	100	DATE	
C4	200 PF	DATE	
C5	100	DATE	
C6	100	DATE	
C7	100	DATE	
C8	100	DATE	
C9	100	DATE	
C10	100	DATE	
C11	100	DATE	
C12	100	DATE	
C13	100	DATE	
C14	100	DATE	
C15	100	DATE	
C26	470PF	DATE	
C27	470PF	DATE	
C29	100	DATE	
U1	3N 75174	DATE	
U2	2N 75175	DATE	
U3	3F DMA CONTROLLER	DATE	
U4	4F 8081	DATE	
U5	3E 10 MHZ	DATE	
U6	7406	DATE	
U7	LS04	DATE	
U8	LS374	DATE	
U9	LS374	DATE	
U10	LS374	DATE	
U11	LS374	DATE	
U12	LS374	DATE	
U13	LS374	DATE	
U14	LS374	DATE	
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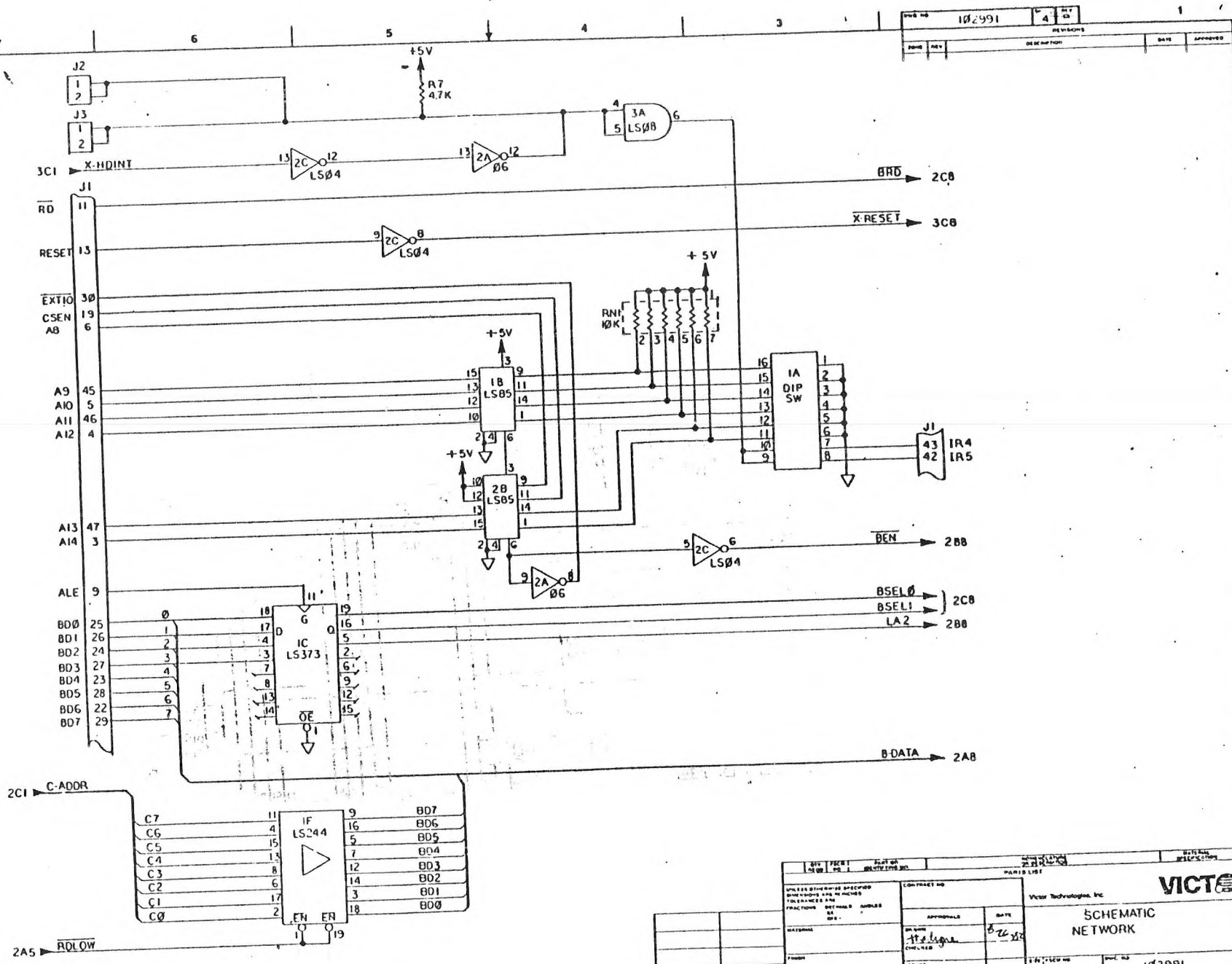
VICT

SCHEMATIC NETWORK

102991

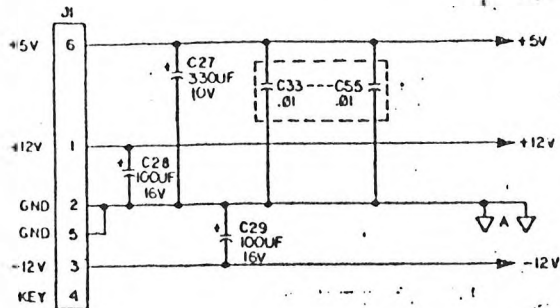
DO NOT SCALE DRAWING





REV NO	102991	REV	4
DESCRIPTION		DATE	APPROVED

DIVISION PROJECT NO. DRAWING NO. DATE		CONTRACT NO. Victor Technologies, Inc. SCHEMATIC NETWORK	
DESIGNED CHECKED DRAWN APPROVED	DATE 11/2/80 11/2/80	VICTOR SCHEMATIC NETWORK	
PART ASSY USED ON APPLICATION	DO NOT SCALE DRAWING	REV. NO. D	REV. NO. 102991 SHEET 4 OF 4



NOTES: UNLESS OTHERWISE SPECIFIED.

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.

2. ALL RESISTORS ARE 1/4W.

3. P.S. IS FACTORY SELECT COMPONENTS TO ADJUST PULSE WIDTH TO 10.5  $\mu$ S MAX - 1.15  $\mu$ S MIN.

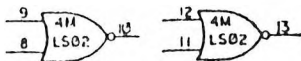
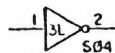
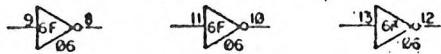
4. Q1, Q2 ARE MOUNTED ON HEATSINK.

5. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.

6. I.C. PINS ARE GND-7, +5V-14 EXCEPT FOR:

TYPE	GND	+5V
74LS123	8	16
74LS133	8	16
74LS139	8	16
74LS157	11	16
74LS165	8	16
74LS180	6	16
74LS191	8	16
74LS373	10	20
2316	12	24
75462	4	8

7. ALL DIODE ARE 1N4148.



SPARE GATES

REV	DESCRIPTION	DATE	BY
1	UPD PER EC 10229	10/30/81	W
2	UPD PER EC 10229	10/30/81	W
3	UPD PER EC 10229	10/30/81	W
4	UPD PER EC 10229	10/30/81	W
5	UPD PER EC 10229	10/30/81	W
6	UPD PER EC 10229	10/30/81	W
7	UPD PER EC 10229	10/30/81	W
8	UPD PER EC 10229	10/30/81	W
9	UPD PER EC 10229	10/30/81	W
10	UPD PER EC 10229	10/30/81	W
11	UPD PER EC 10229	10/30/81	W
12	UPD PER EC 10229	10/30/81	W
13	UPD PER EC 10229	10/30/81	W
14	UPD PER EC 10229	10/30/81	W
15	UPD PER EC 10229	10/30/81	W
16	UPD PER EC 10229	10/30/81	W
17	UPD PER EC 10229	10/30/81	W
18	UPD PER EC 10229	10/30/81	W
19	UPD PER EC 10229	10/30/81	W
20	UPD PER EC 10229	10/30/81	W
21	UPD PER EC 10229	10/30/81	W

SHEET	DESCRIPTION
1	POWER & SPARES
2	CPC INTERFACE (L122)
3	MOTOR (REF) (73) & DAC
4	PLL
5	RD/WR HEAD INTERFACE
6	DRIVE SELECT (L122) DECODE
7	GCR EN/DE CODER
8	DISK CONNECT (REF)
9	STPPER CONTROL

REVISION	REV PER EC	DATE	BY
1	10229	10/30/81	W
2	10229	10/30/81	W
3	10229	10/30/81	W
4	10229	10/30/81	W
5	10229	10/30/81	W
6	10229	10/30/81	W
7	10229	10/30/81	W
8	10229	10/30/81	W
9	10229	10/30/81	W

POWER & SPARES

J15	
TP9	
L9	
CR2C	
Q3	Chp
C55	CAC
W7	REF
LAST USED	DATE USED
REFERENCE	DESCRIPTION

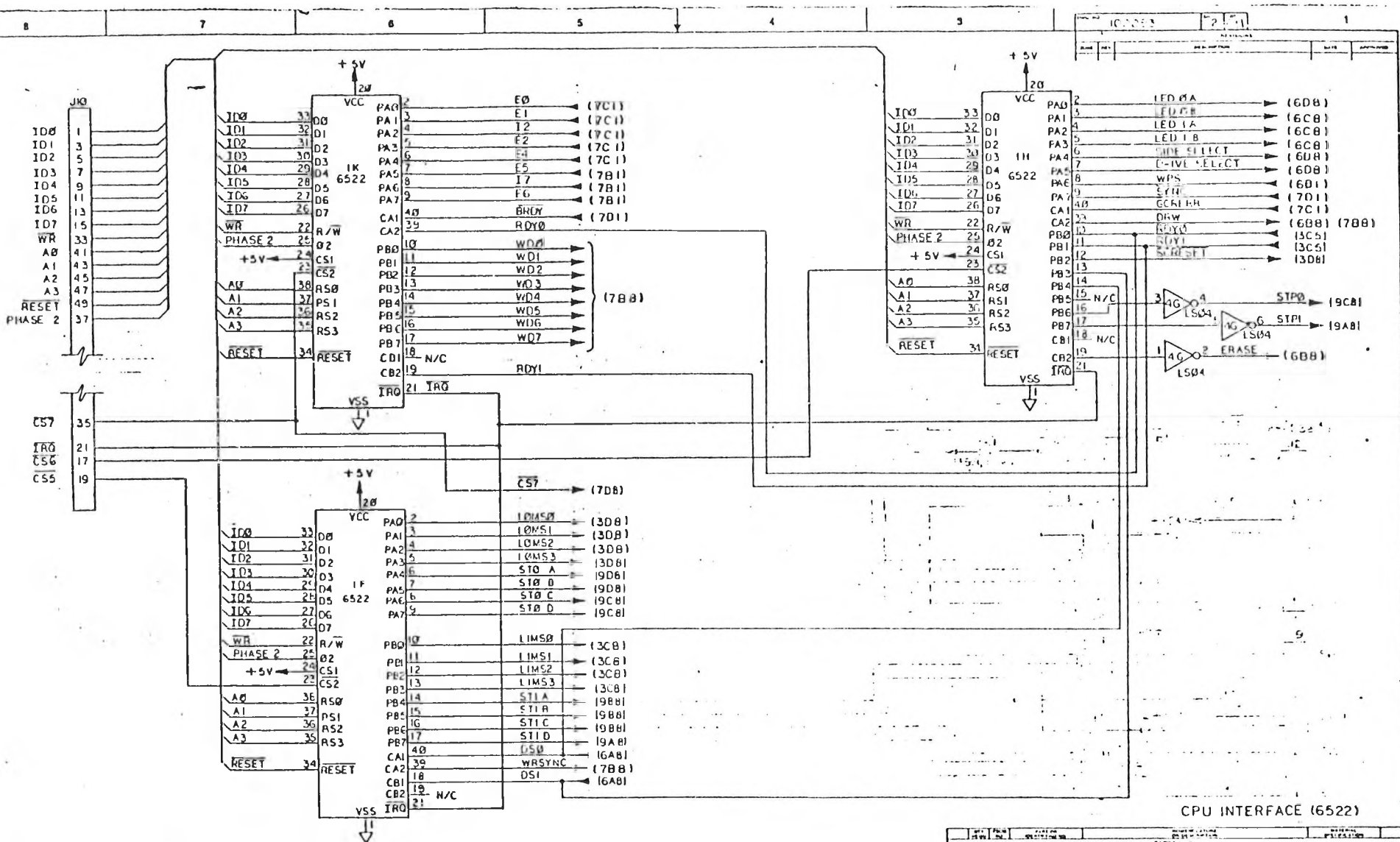
Victor Technologies, Inc.

W TAYLOR (729-B)

DISK DRIVE SCHEMATIC

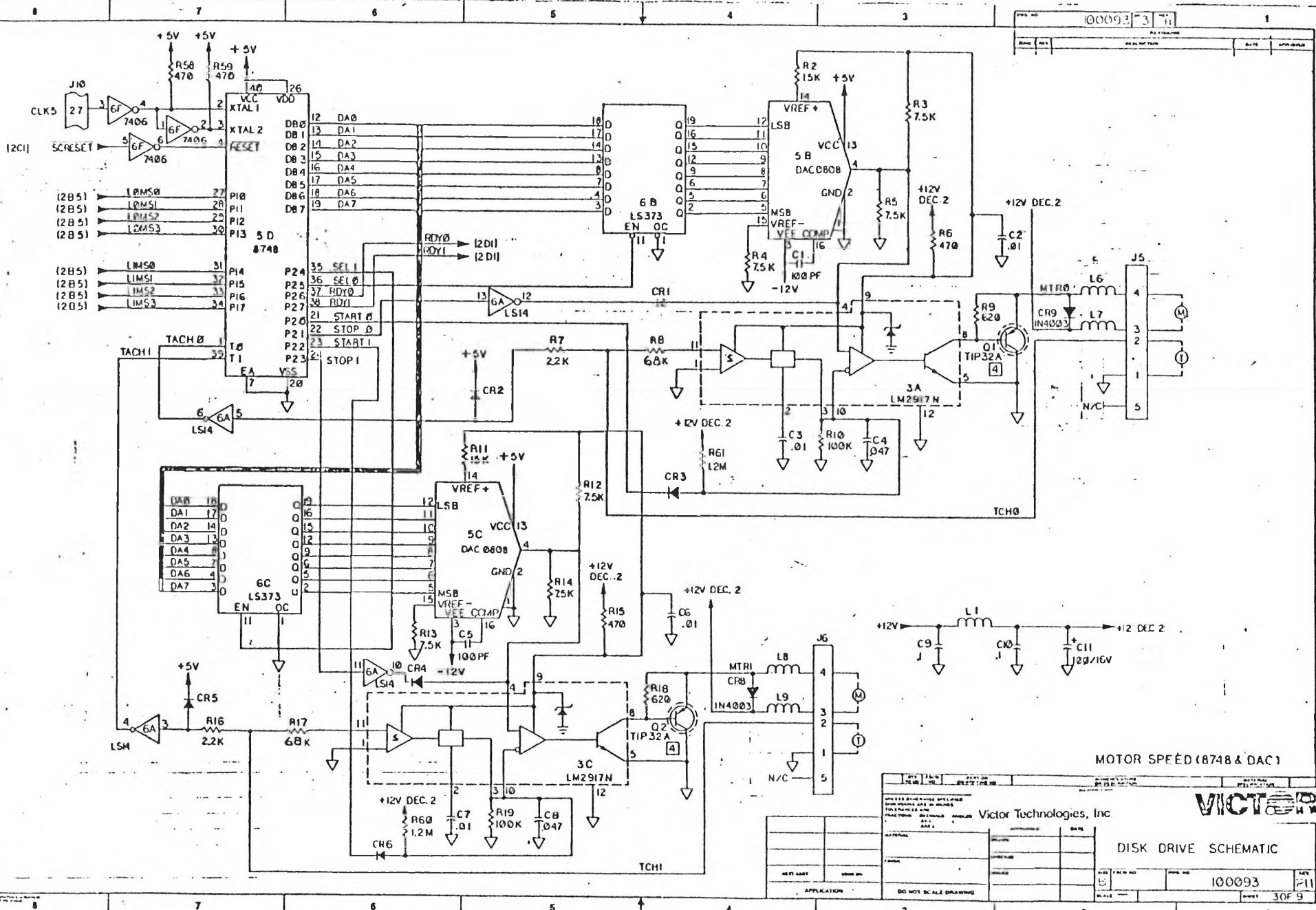
100093

1 OF 3



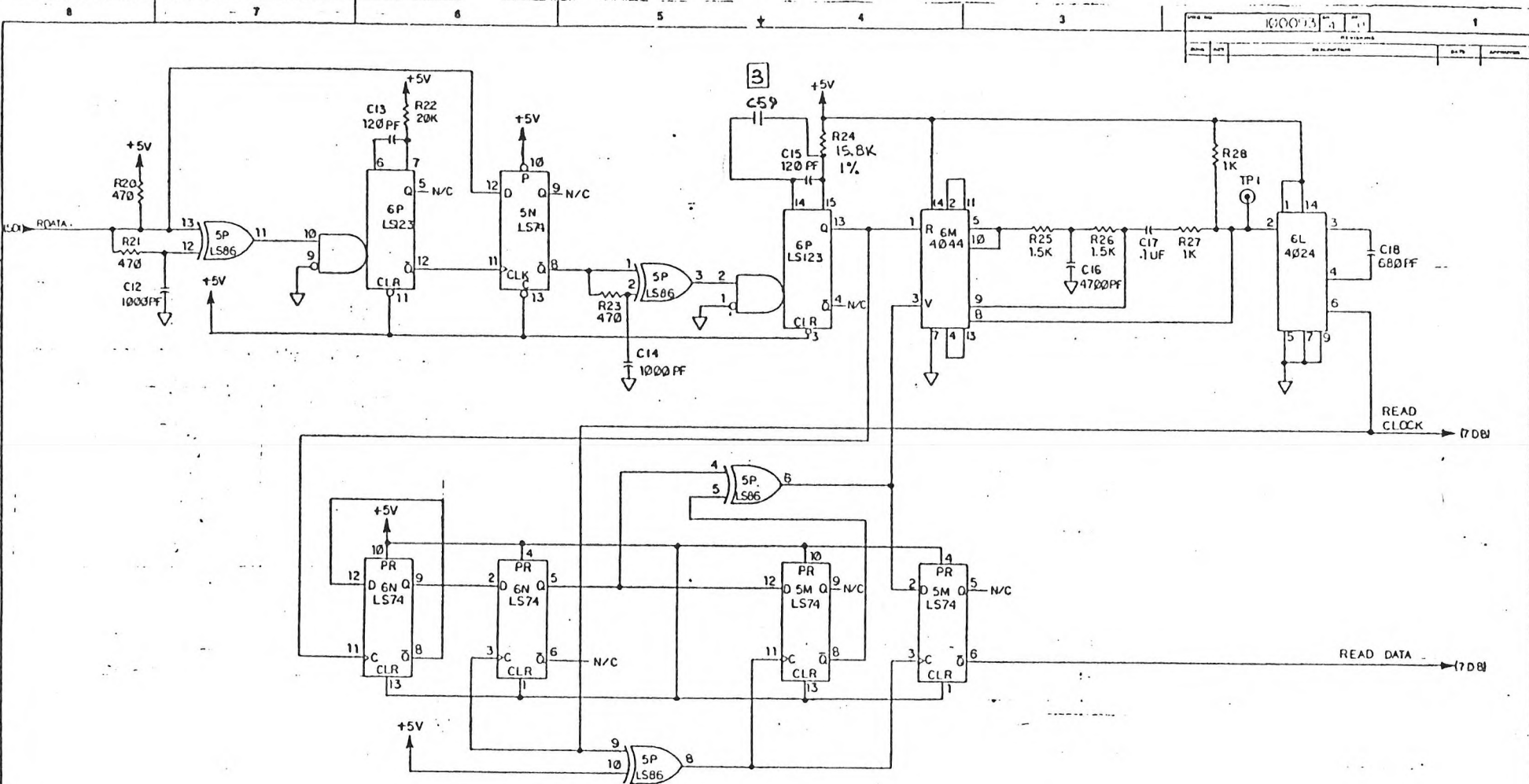
CPU INTERFACE (6522)

Victor Technologies, Inc.		<b>VICTOR</b>	
DISK DRIVE SCHEMATIC			
PART NO. 100093	REV. 1	DATE	1
DRAWN BY	CHECKED BY	APPROVED BY	DATE
APPLICATION	DO NOT SCALE DRAWING	MADE IN	SHEET 2 OF 4



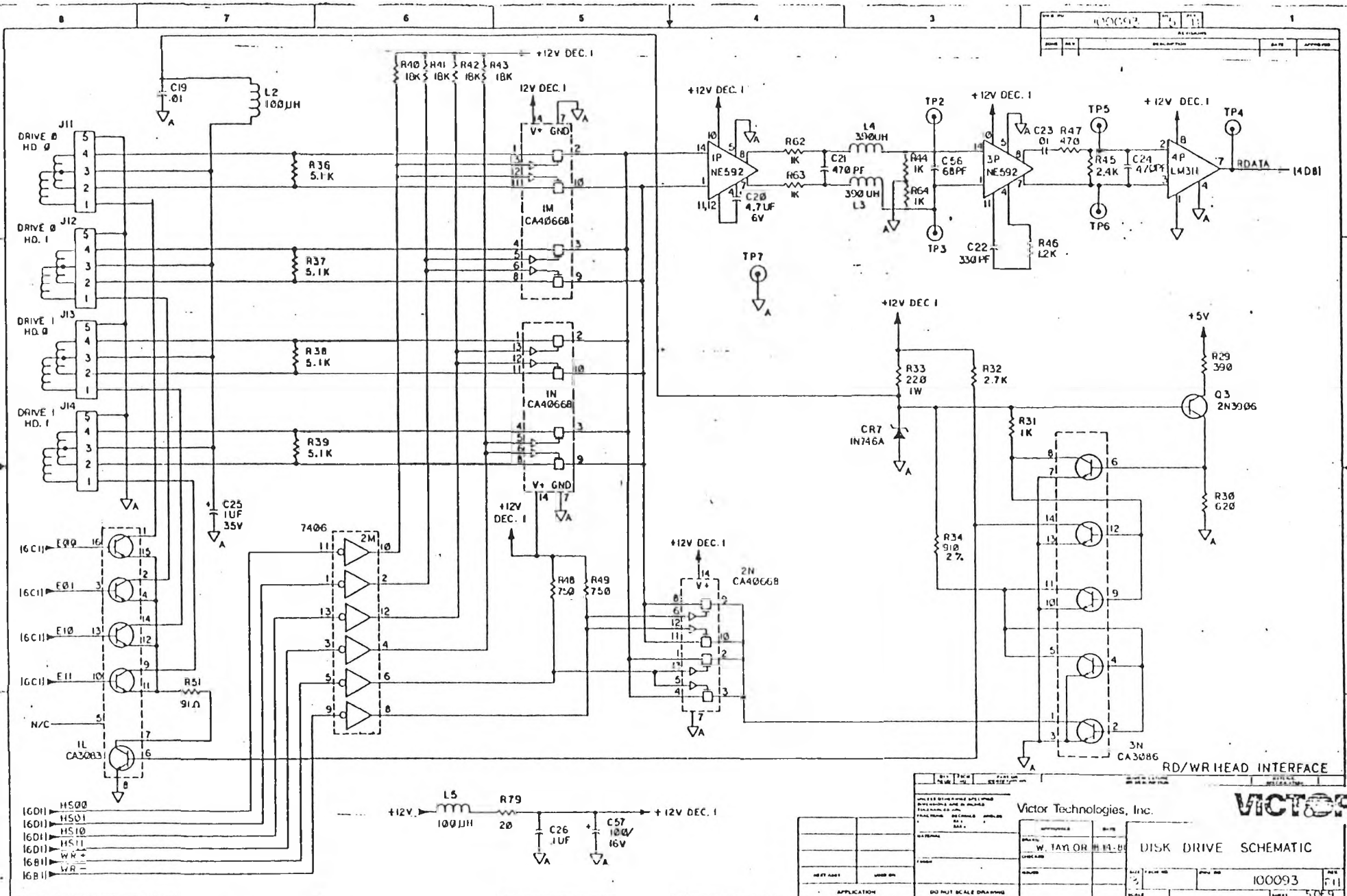
MOTOR SPEED (8748 & DAC)

<b>VICTOR</b> Victor Technologies, Inc.	
<b>DISK DRIVE SCHEMATIC</b>	
PART NO. 100093 REV. 11	DATE 3/91 PAGE 3 OF 9



PLL

Victor Technologies, Inc.		<b>VICTOR</b>	
DISK DRIVE SCHEMATIC		100093 11	
APPROVALS		DATE	
DESIGNER		7-19-81	
CHECKER		ES	
SCALE		1 OF 9	



NO.	REV.	DESCRIPTION	DATE	APPROVED

RD/WR HEAD INTERFACE

Victor Technologies, Inc.

**VICTOR**

DESIGNED BY W. TAYLOR		DATE 11-85	
CHECKED BY		SCALE	
APPLICATION		DO NOT SCALE DRAWING	

PROJECT NO.	100093
REV.	1
DATE	5-8-9

(2D1) SIDE SELECT  
 (2D1) DRIVE SELECT

(2D1) LED 0A

(2D1) LED 0B

(2D1) LED 1A

(2D1) LED 1B

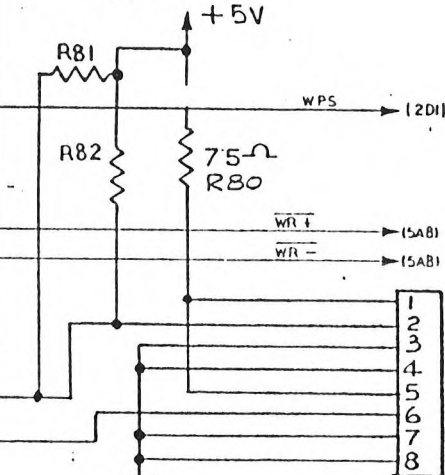
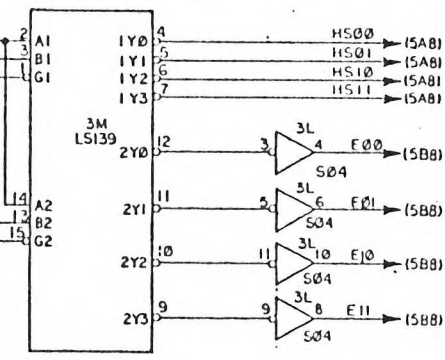
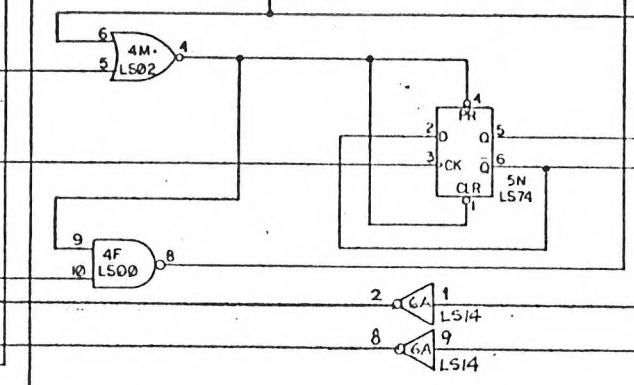
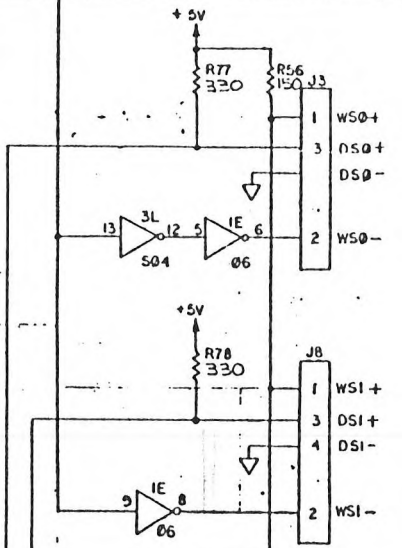
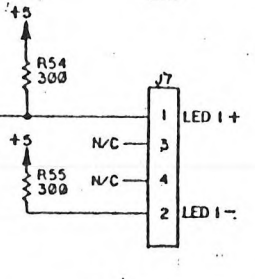
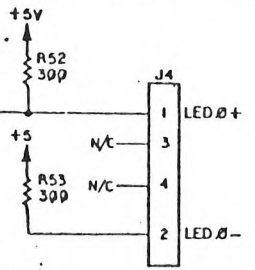
(2D1) DRW

(7C1) GCR DATA

(2C1) ERASE

(2A5) DS0

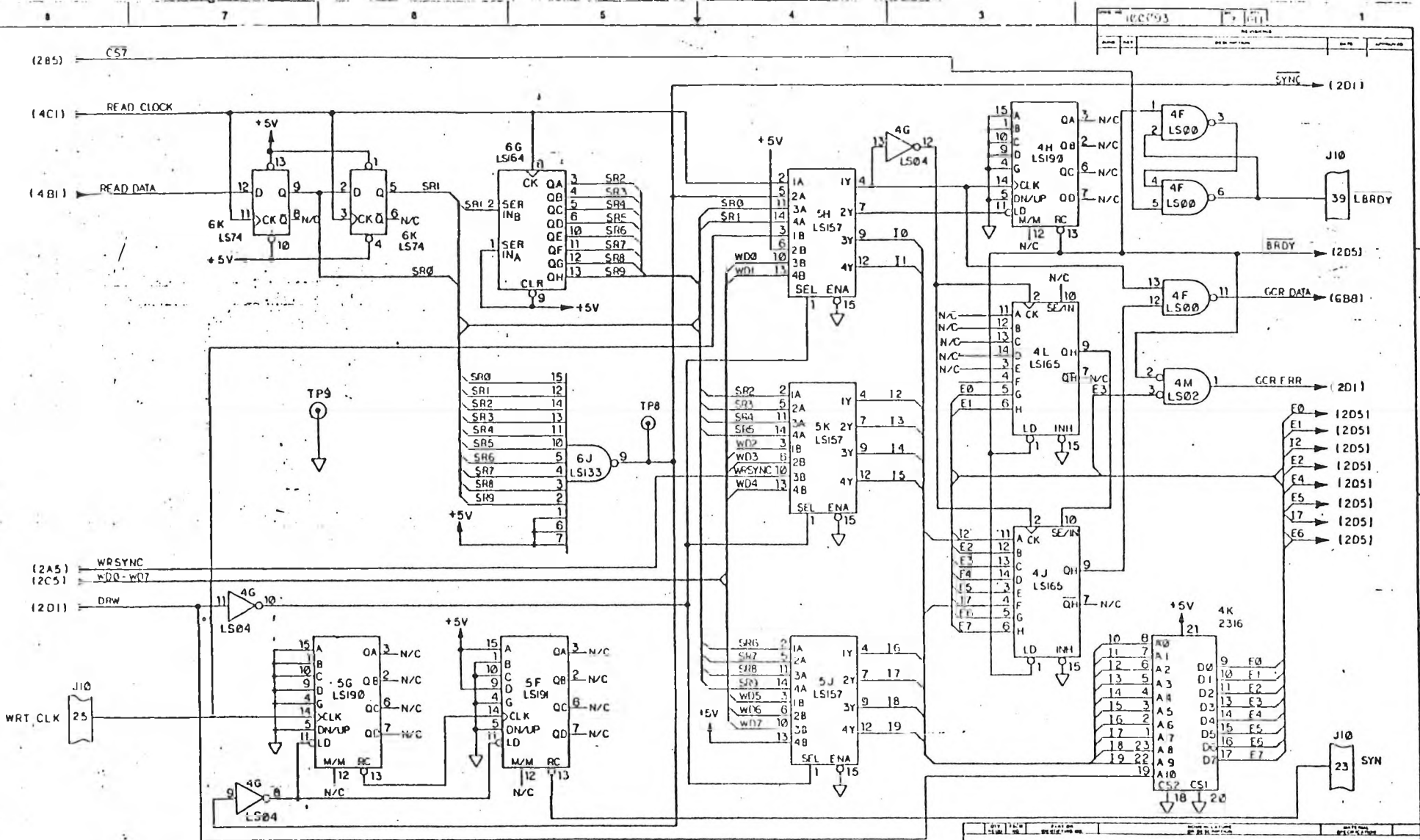
(2A5) DS1



DRIVE SELECT, LED, DECODE

J-15

PART NO. 100093		REV. 1	
DATE		APPROVALS	
DESIGNED BY		CHECKED BY	
DRAWN BY		DATE	
APPLICATION		DO NOT SCALE DRAWING	
VICTOR Technologies, Inc.		DISK DRIVE SCHEMATIC	
PART NO. 100093		REV. 1	
PAGE 6 OF 9			



GCR EN/DE-CODER

Victor Technologies, Inc.

**VICTOR**

DISK DRIVE SCHEMATIC

100093 P11

DATE: 7-23-81

WILL TAYLOR

APPROVAL: \_\_\_\_\_

DATE: \_\_\_\_\_

DESIGNED BY: \_\_\_\_\_

DATE: \_\_\_\_\_

CHECKED BY: \_\_\_\_\_

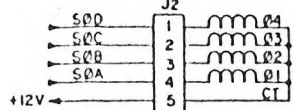
DATE: \_\_\_\_\_

APPLICATION: \_\_\_\_\_

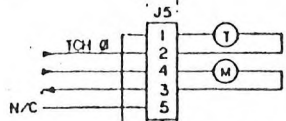
DO NOT SCALE DRAWING



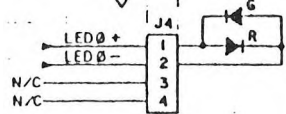
100093



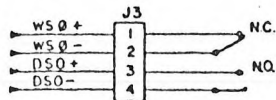
**STEPPER A**  
(SHT 9)



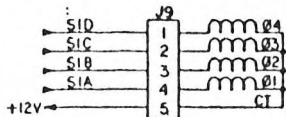
**MOTOR A** (8748, DAC, DISCRETE)  
(SHT 3)



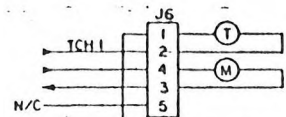
**ACTIVITY LED A**  
(SHT 6)



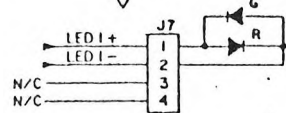
**WRITE PROTECT A**  
**DOOR SWITCH A**  
(SHT 6)



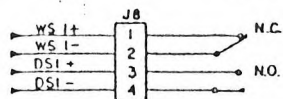
**STEPPER B**  
(SHT 9)



**MOTOR B**  
(SHT 3)

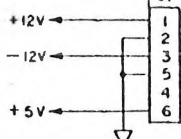
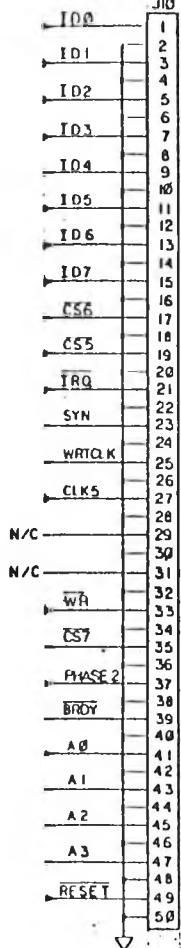


**ACTIVITY LED B**  
(SHT 6)



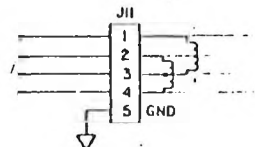
**WRITE PROTECT B**  
**DOOR SWITCH B**  
(SHT 6)

**CPU INTERFACE (6522)**  
(SHT 2)

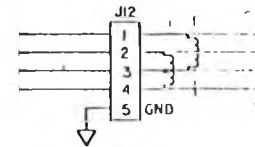


**POWER CONNECTOR**  
(SHT 1)

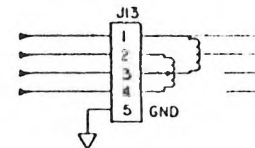
**DRIVE A HEAD 0**  
(SHT 5)



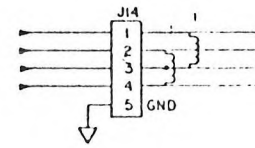
**DRIVE A HEAD 1**  
(SHT 5)



**DRIVE B HEAD 0**  
(SHT 5)



**DRIVE B HEAD 1**  
(SHT 5)



DISK CONNECTORS (REF)

Victor Technologies, Inc.

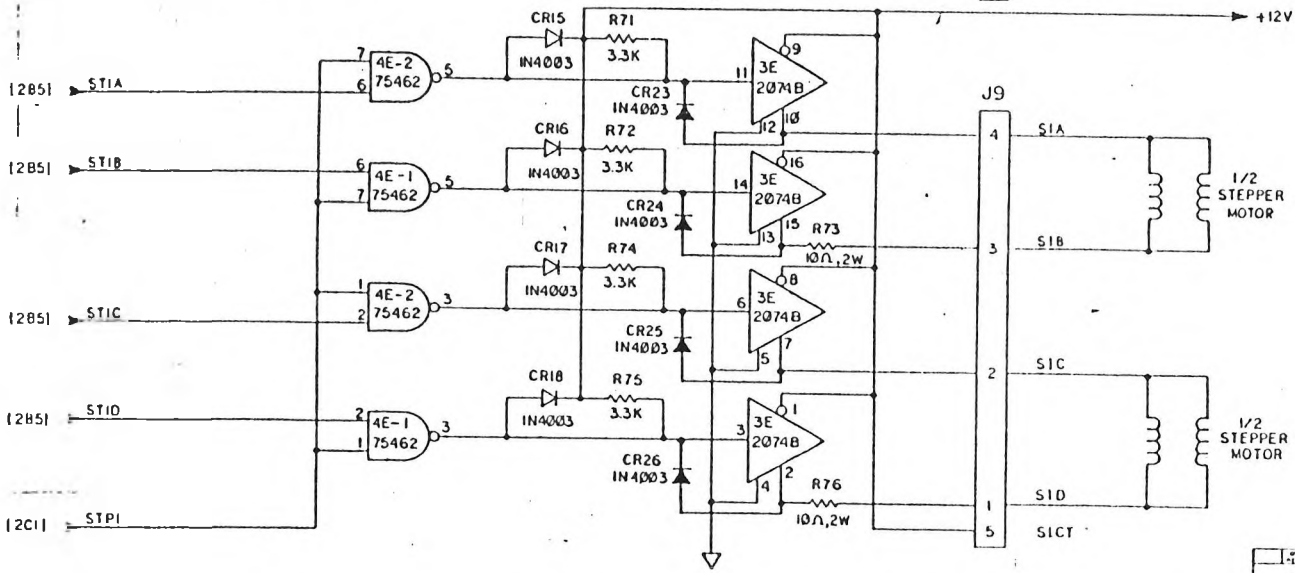
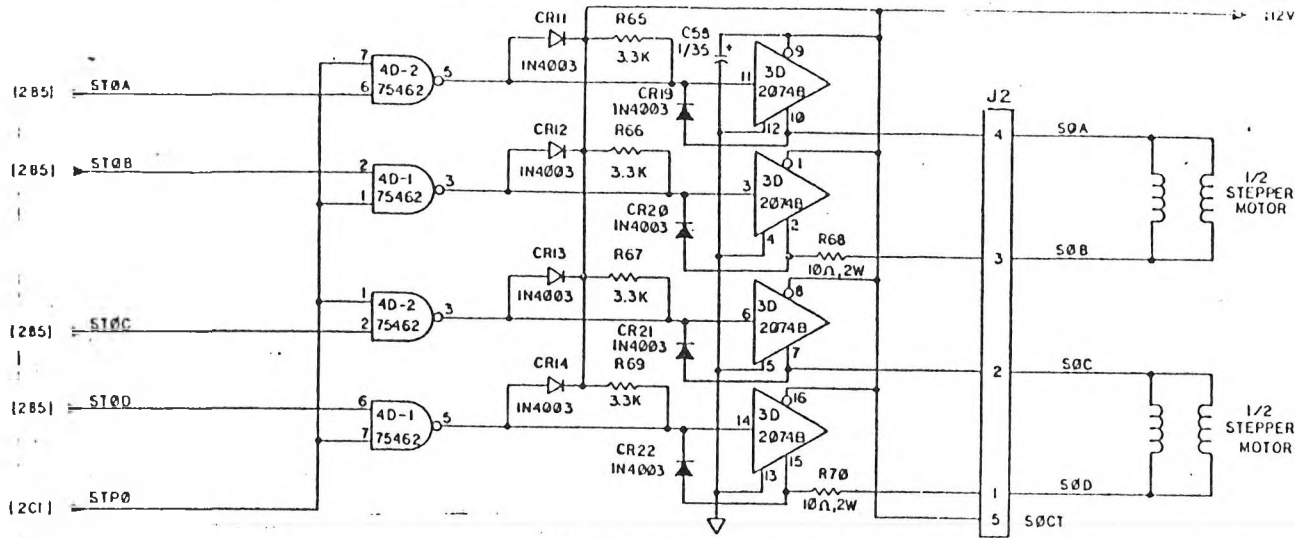
**VICTOR**

W. R. TAYLOR / Z. COBI

DISK DRIVE SCHEMATIC

100093

PAGE 1 OF 9

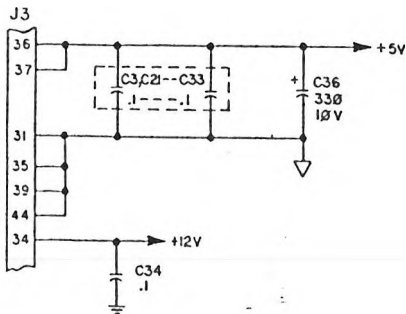


STEPPER CONTROL

Victor Technologies, Inc.	
<b>VICTOR</b>	
DISK DRIVE SCHEMATIC	
DATE: 8-14-88	DESIGNED BY: W. TAYLOR
CHECKED BY:	DRAWN BY:
MATERIAL:	PART NO: 100093
APPLICATION:	REV: 1/11
DO NOT SCALE DRAWING	9 OF 9



PART NO		REV		DATE	
100981		1		E	
REVISED					
REV	DATE	BY	APP'D	DATE	BY
A	RELEASE PER EC # 10522	12-1-62			
E	REVISED PER EC # 10911	10-15			



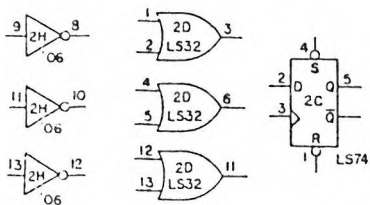
NOTES-UNLESS OTHERWISE SPECIFIED:

- 1 ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
- 2 ALL RESISTORS ARE  $\pm 5\%$ , 1/4 W.
- 3 ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
- 4 IC PINS ARE: GND=7, 5V=14

IC TYPE	GND	+5V
ADC0802	10	20
74LS373	10	20
74LS374	10	20
74LS138	8	16
74LS133	8	16
74LS157	8	16

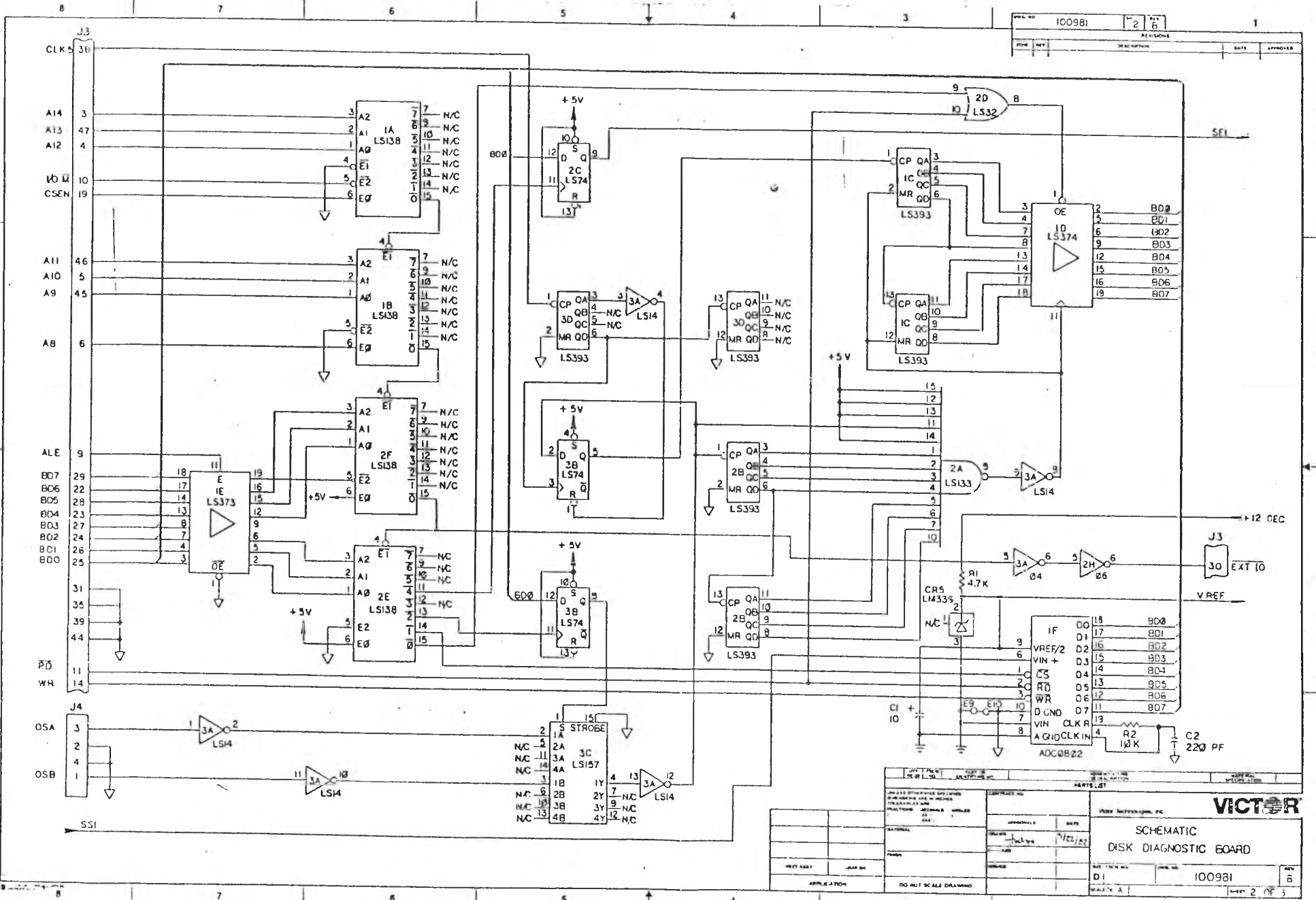
Company Control  
VICTOR TECHNOLOGICALS  
Not To Be Copied

SPARE GATES



E10			
J4			
L1			
CP5			
R36	R10		
C36	R17		
LAST USED	NOT USED	REF. DESIG.	APP. DESIG.

PART NO		REV		DATE	
100981		1		E	
REVISED					
REV	DATE	BY	APP'D	DATE	BY
A	RELEASE PER EC # 10522	12-1-62			
E	REVISED PER EC # 10911	10-15			
PARTS LIST					
USE ALL OTHERS UNLESS OTHERWISE SPECIFIED AND AS SHOWN FOR EXAMPLES USE PRACTICE DESIGN NUMBER 0011			<b>VICTOR</b> SCHEMATIC, DISK DIAGNOSTIC BOARD		
DO NOT SCALE DRAWING			100981		

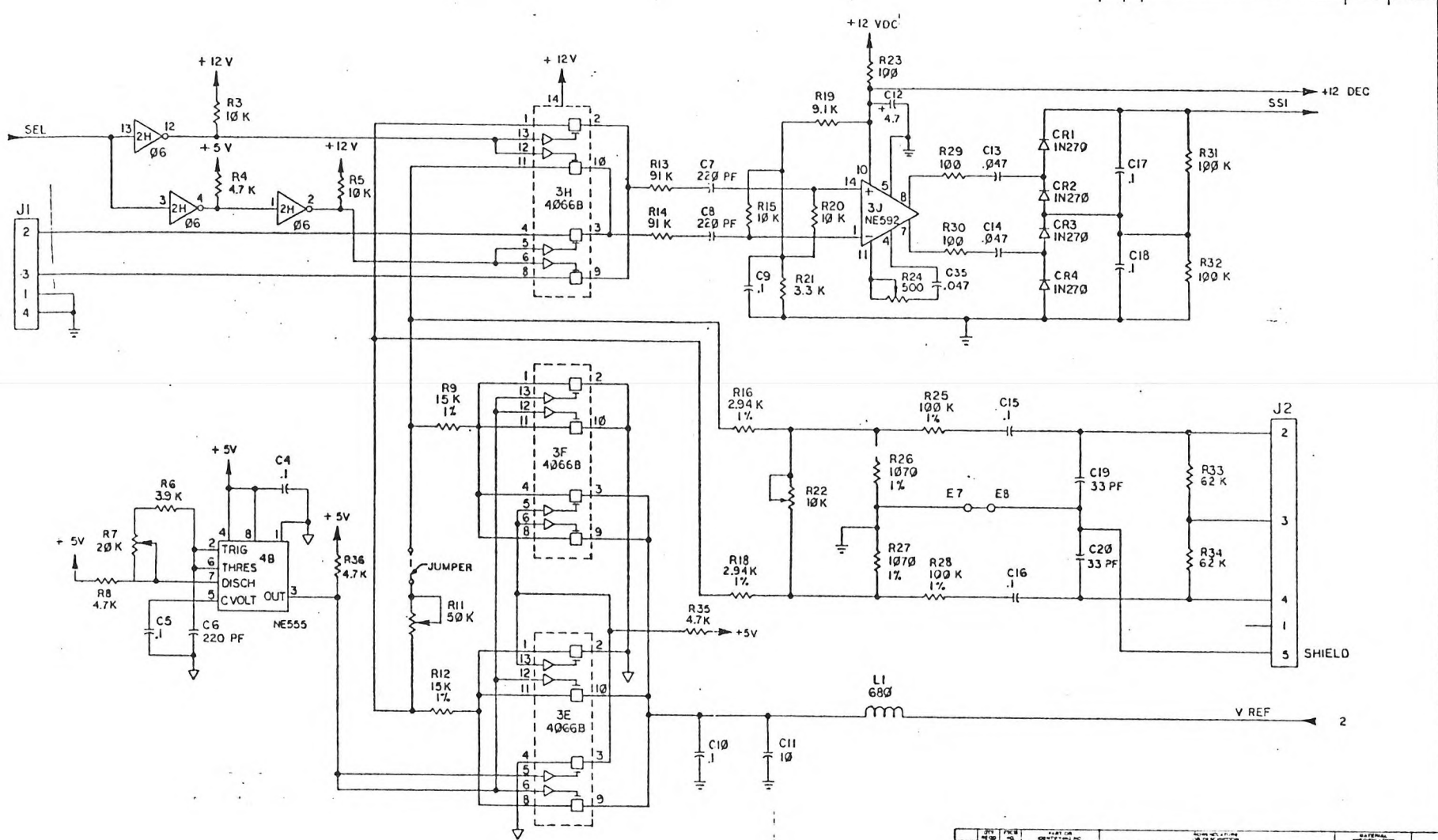


REV	REV	DESCRIPTION	DATE	APPROVED
1	2			

PARTS LIST		VICTOR	
1F 00 18 9D0 01 17 8D1 02 16 8D2 03 15 8D3 04 14 8D4 05 13 8D5 06 12 8D6 07 11 8D7 08 10 8D8 09 09 8D9 10 08 8D10 11 07 8D11 12 06 8D12 13 05 8D13 14 04 8D14 15 03 8D15 16 02 8D16 17 01 8D17 18 00 8D18		VREF/2 VIN + 1 CS 2 RD 3 WR 4 D GND 5 VIN CLK R 6 A GND CLK IN 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	
1F 00 18 9D0 01 17 8D1 02 16 8D2 03 15 8D3 04 14 8D4 05 13 8D5 06 12 8D6 07 11 8D7 08 10 8D8 09 09 8D9 10 08 8D10 11 07 8D11 12 06 8D12 13 05 8D13 14 04 8D14 15 03 8D15 16 02 8D16 17 01 8D17 18 00 8D18		VREF/2 VIN + 1 CS 2 RD 3 WR 4 D GND 5 VIN CLK R 6 A GND CLK IN 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	
1F 00 18 9D0 01 17 8D1 02 16 8D2 03 15 8D3 04 14 8D4 05 13 8D5 06 12 8D6 07 11 8D7 08 10 8D8 09 09 8D9 10 08 8D10 11 07 8D11 12 06 8D12 13 05 8D13 14 04 8D14 15 03 8D15 16 02 8D16 17 01 8D17 18 00 8D18		VREF/2 VIN + 1 CS 2 RD 3 WR 4 D GND 5 VIN CLK R 6 A GND CLK IN 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50	

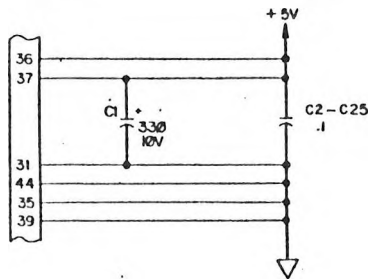
SCHEMATIC  
DISK DIAGNOSTIC BOARD  
100981  
REV 2 OF 3

REV	NO	DATE	APPROVED
3	100981		



PARTS LIST		APPROVALS	
QTY	PN#	DATE	BY
MATERIAL		DRAWN BY	
CHECKED BY		DATE	
NEXT ASSY		USED ON	
APPLICATION		DO NOT SCALE DRAWING	

**VICTOR**  
 SCHEMATIC,  
 DISK DIAGNOSTIC BOARD  
 100981  
 SHEET 3 OF 3



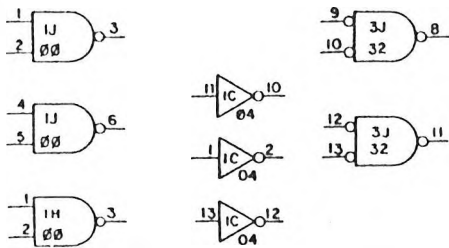
NOTES: UNLESS OTHERWISE SPECIFIED

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
2. ALL RESISTORS ARE  $\pm 5\%$ , 1/4W.
3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
4. IC PINS ARE , GND = 7, +5V = 14.

IC TYPE	GND	+5V
LS138	8	16
LS245	10	20
LS373	10	20
6116	12	24
2732A OR/4764	12	24

5. TO USE TWO 4764 DEVICES INSTEAD OF FOUR 2732A DEVICES, SEE TABLE 'A' BELOW.

SPARE GATES



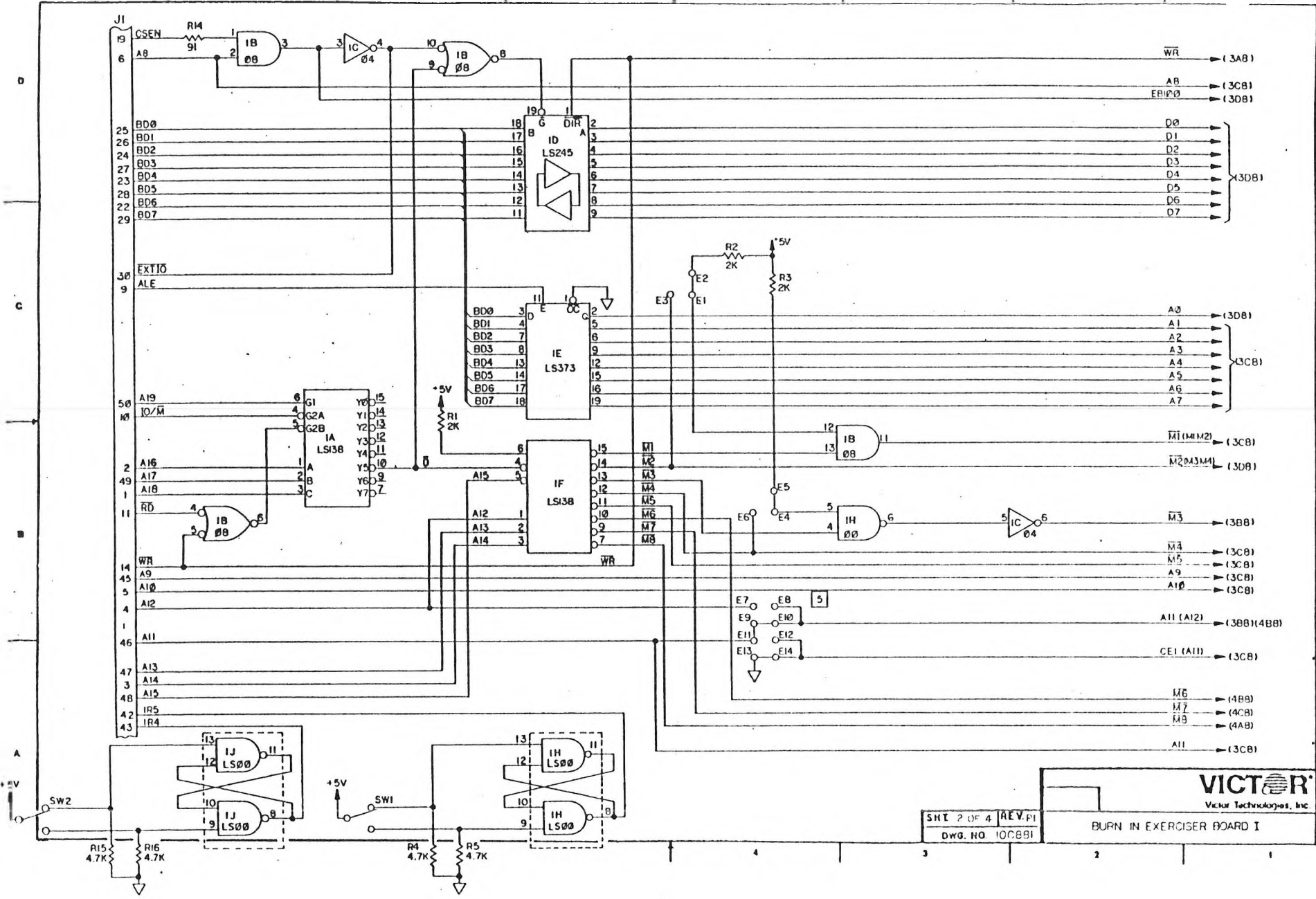
5

CUT	JOIN
E1 - E2	E1 - E3
E4 - E5	E4 - E6
E9 - E10	E7 - E8
E13 - E14	E11 - E12
E17 - E18	E15 - E16
E21 - E22	E19 - E20

SHEET 1 OF 4 | REV. P1  
Dwg. NO. 100281

**VICTOR**  
Victor Technologies, Inc.

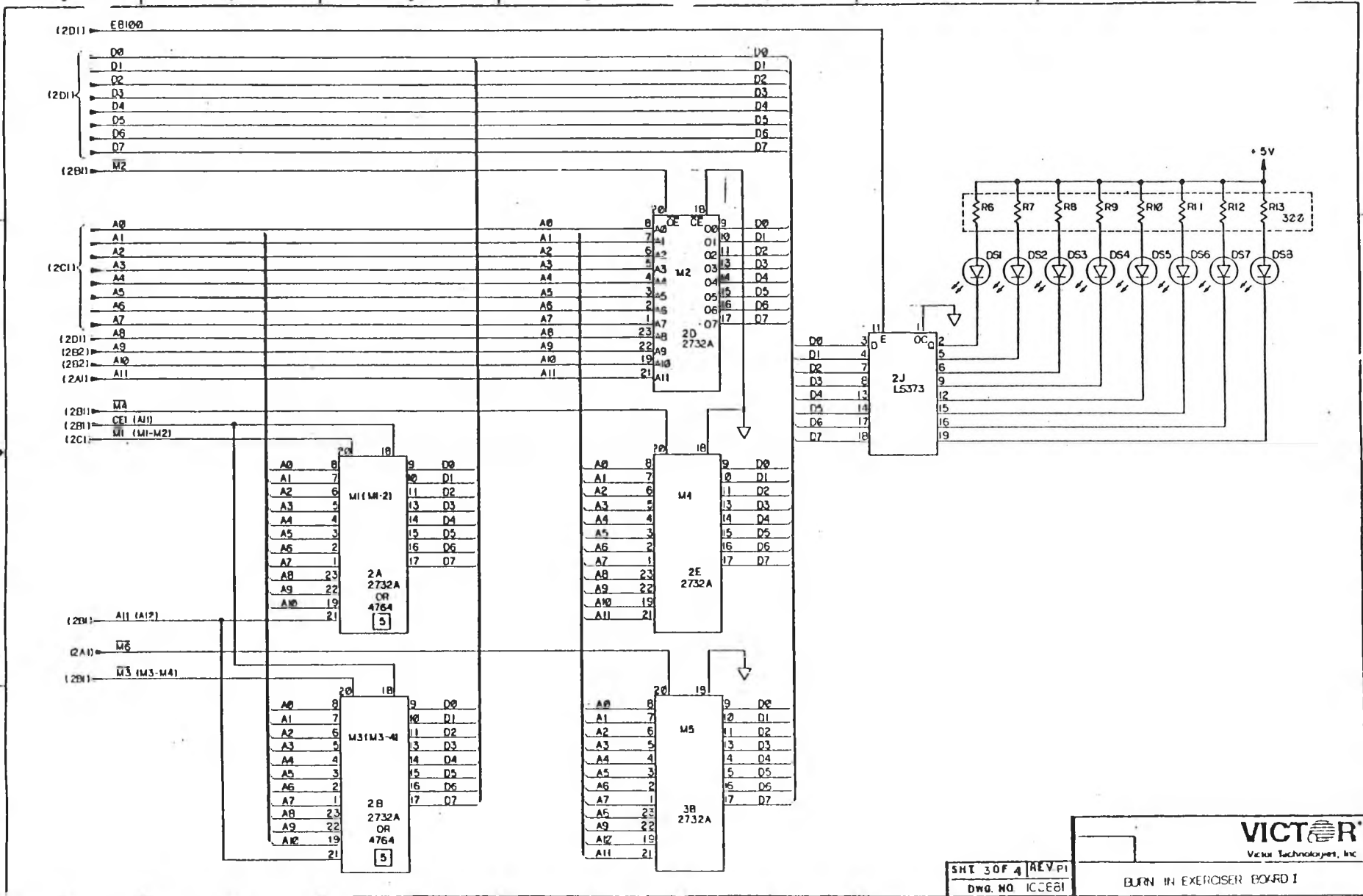
BURN IN EXERCISER BOARD I



SHEET 2 OF 4 REV. P1  
DWG. NO. 100881

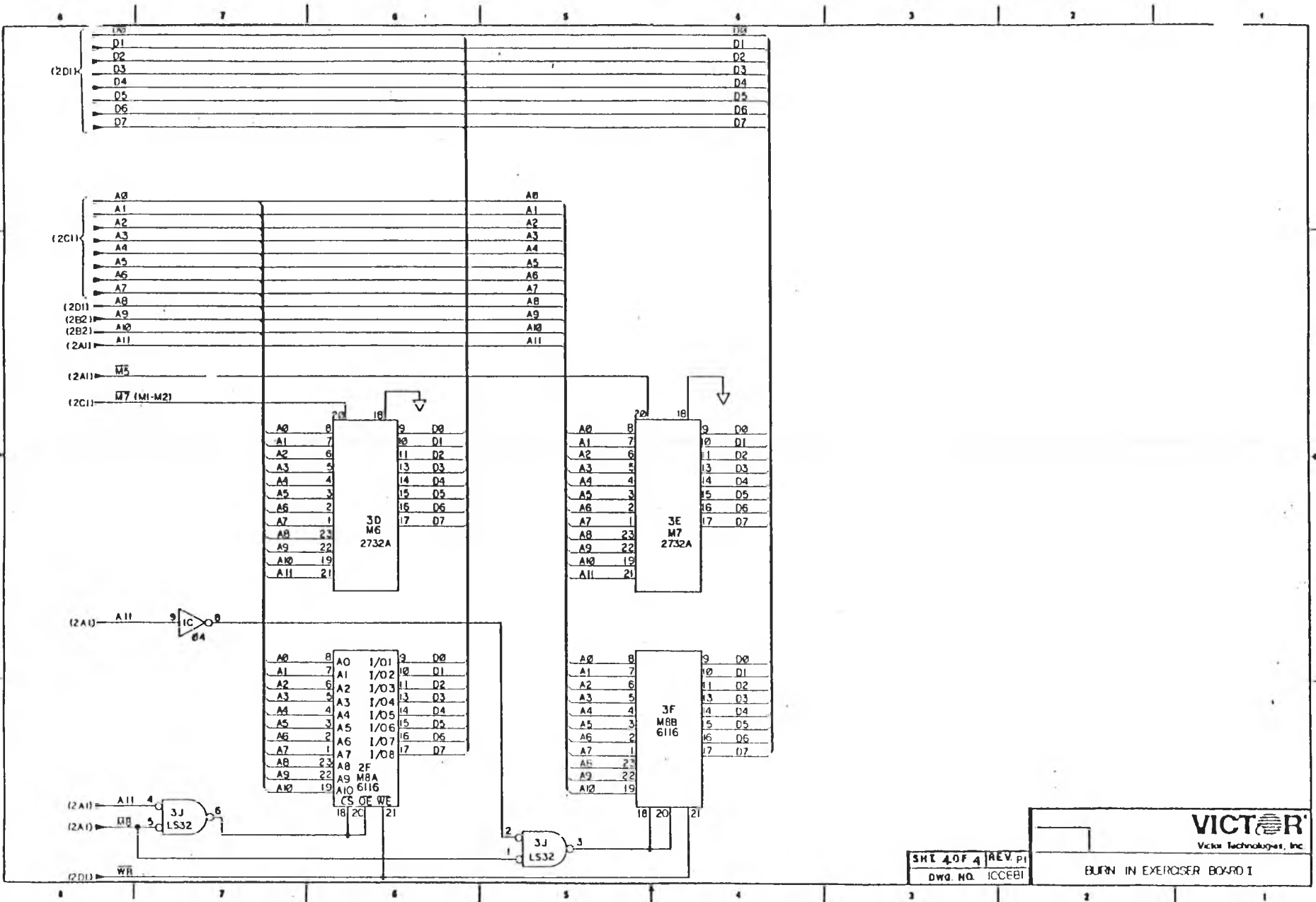
**VICTOR**  
Vector Technologies, Inc.  
BURN IN EXERCISER BOARD I





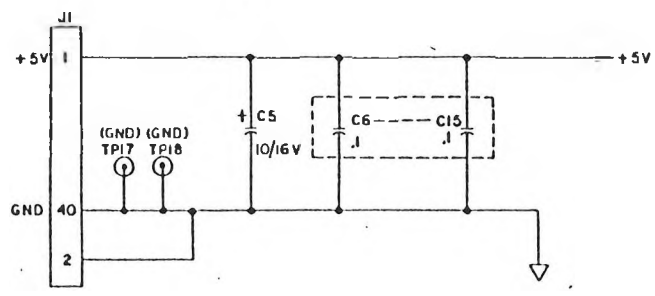
SHE 30F 4 REV P1  
 DWG. NO. ICCE81

**VICTOR**  
 Victor Technologies, Inc.  
 BURN IN EXERCISER BOARD I



SHEET 4 OF 4 REV. P1  
 DWG. NO. ICCEBI

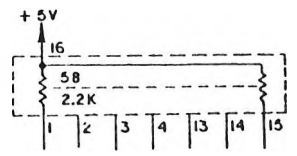
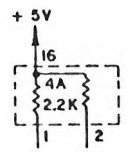
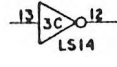
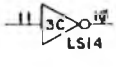
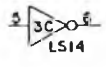
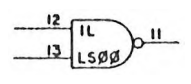
**VICTOR**  
 Victor Technologies, Inc.  
 BURN IN EXERCISER BOARD I



- NOTES; UNLESS OTHERWISE SPECIFIED.
1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS AND MICROHENRIES.
  2. ALL RESISTORS ARE  $\pm 5\%$ ,  $\sqrt{4W}$ .
  3. ALL INTEGRATED CIRCUITS ARE SN74 SERIES.
  4. I.C. PINS ARE GND = 7, +5V = 14 EXCEPT FOR:

TYPE	GND	+5V
74LS157	8	16
74LS244	10	20
8088	20	40

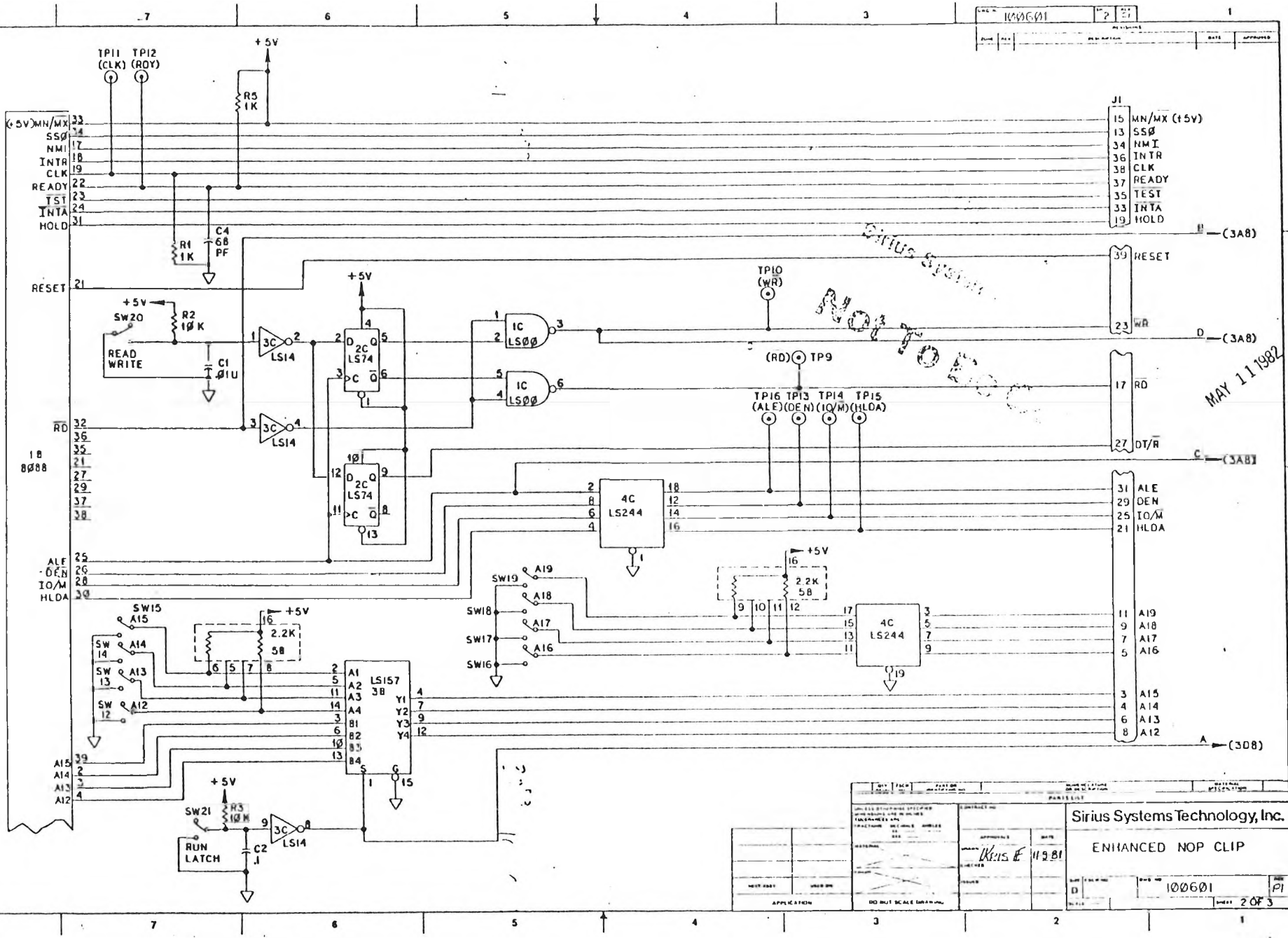
MAY 11 1982



SPARE GATES

REFERENCE	DESIGNATION	APPLICATION
J2		
TPI8		
SW0-SW22		
C15		
R5		
LAST USED	NOT USED	

PART NAME		PART NUMBER		DATE	
DESCRIPTION		REV		DATE	
MATERIAL		APPROVALS		DATE	
FABRICATION		CHECKED		DATE	
DO NOT SCALE DRAWING		ISSUED		DATE	
SIRIUS SYSTEMS TECHNOLOGY, INC.		SCHEMATIC, ENHANCED		NOP CLIP	
DRAWN BY: [Signature]		DATE: 11-11-81		REV: 1	
CHECKED BY: [Signature]		DATE: 12-22-82		REV: 2	
ISSUED BY: [Signature]		DATE: 12-22-82		REV: 3	
PART NUMBER: 100601		REV: P1		PAGE 1 OF 3	



REV	100601	1	2	21
DATE				
APPROVED				

MAY 11 1982

Not To Be Copied

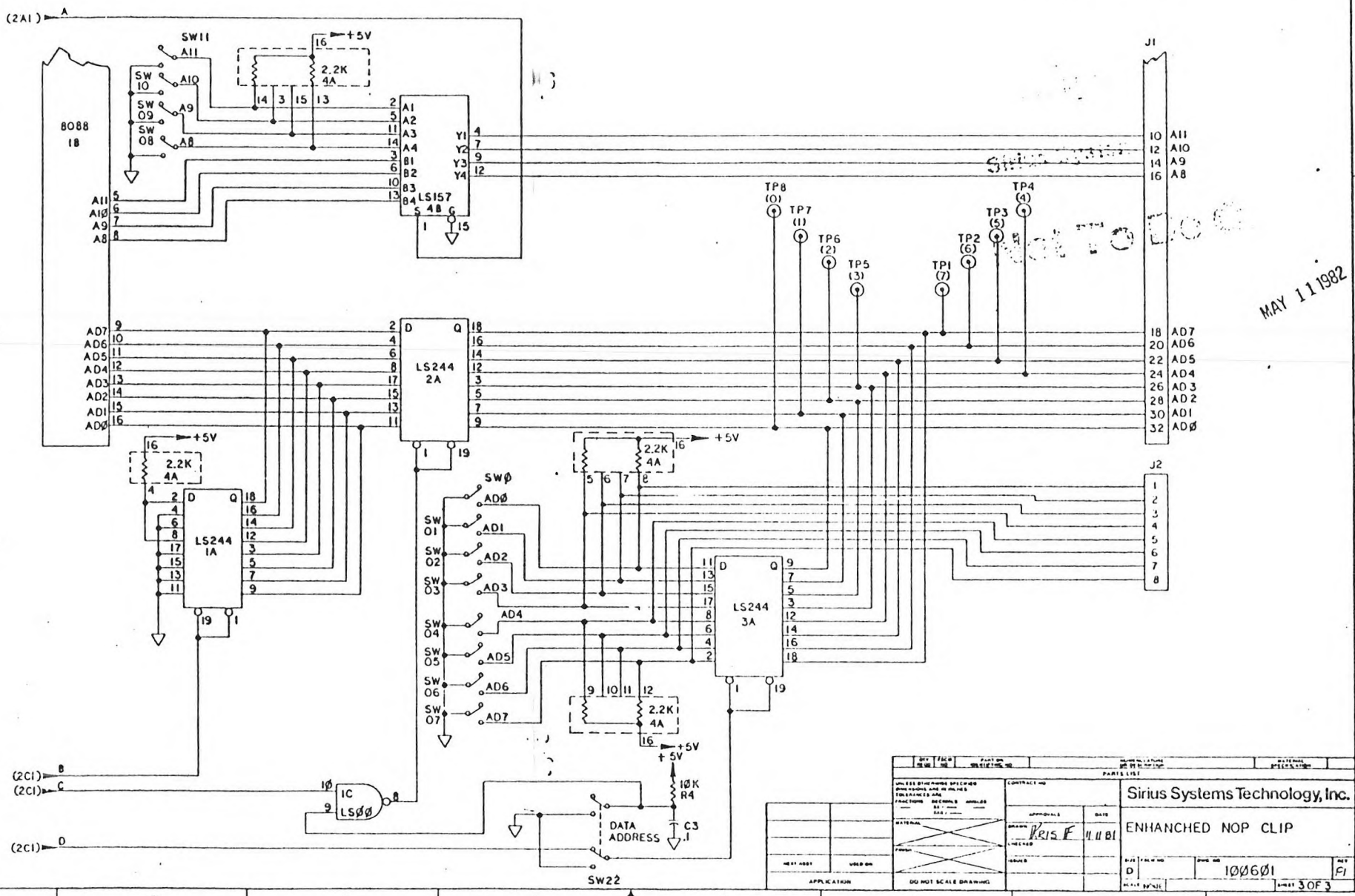
Sirius Systems Technology, Inc.

ENHANCED NOP CLIP

DATE: 11/2/81

REV: D    PART NO: 100601    SHEET: P1

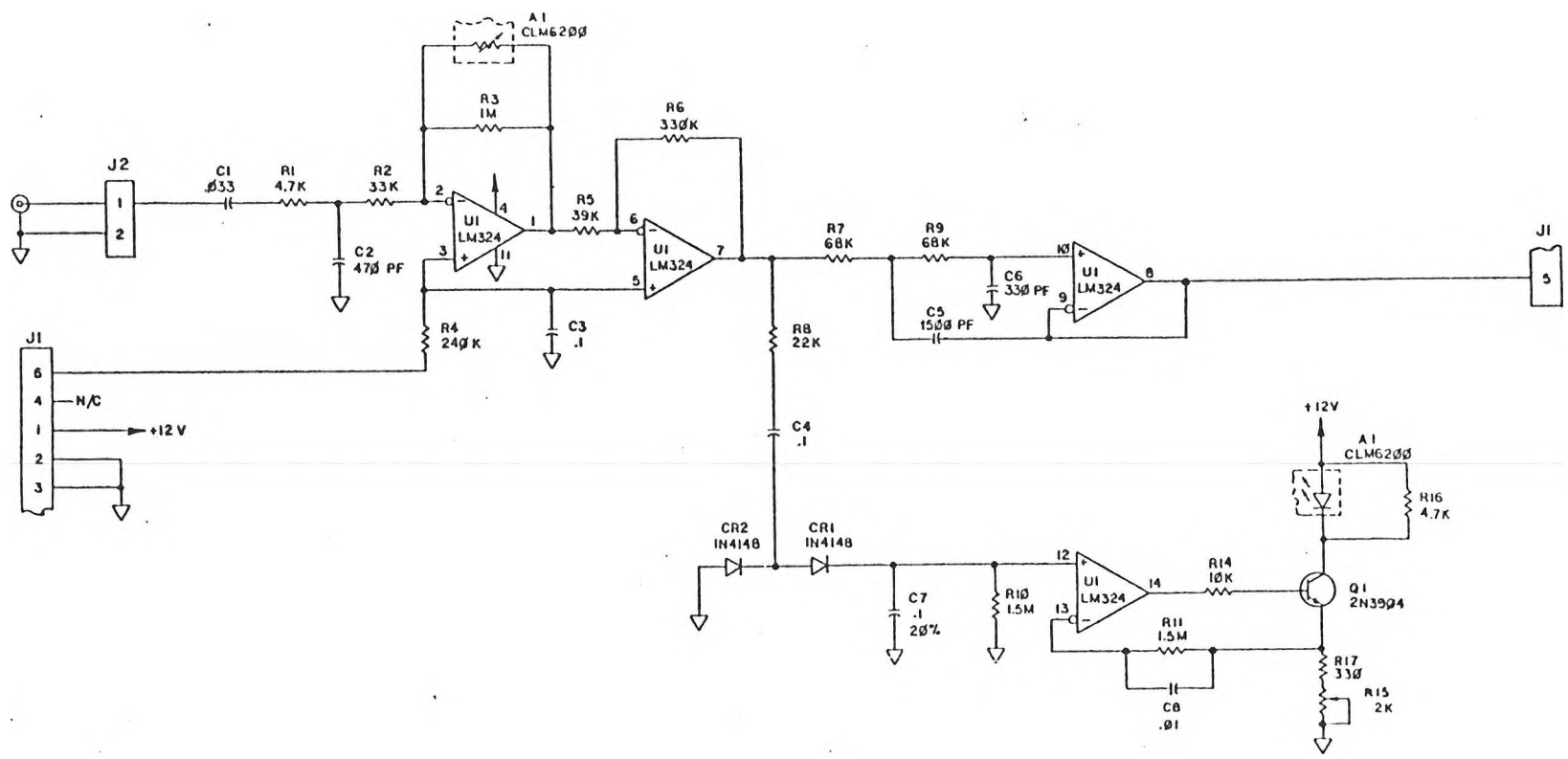
DESIGNED BY	DATE	REV
APPROVED BY	DATE	REV
TESTED BY	DATE	REV
APPLICATION	DO NOT SCALE DRAWING	



MAY 11 1982

DESIGNED BY	DATE	REVISIONS	REVISIONS
100601			
SIRIUS SYSTEMS TECHNOLOGY, INC.		PART LIST	
UNLESS OTHERWISE SPECIFIED DIMENSIONS AND WEIGHTS FRACTIONS DECIMALS ANGLES ALL DIMENSIONS ARE IN INCHES		CONTRACT NO.	DATE
MATERIAL		APPROVALS	DATE
DRAWN		KRIS F	11.11.81
CHECKED			
PART NO.			
NEXT ASST.			
USED ON			
APPLICATION			
DO NOT SCALE DRAWING			
SIZE		PART NO.	
D		100601	
SCALE		PAGE 3 OF 3	

REV	DATE	BY	CHKD
A	1/1/72	...	...



NOTES - UNLESS OTHERWISE SPECIFIED:  
 1.) ELECTRICAL VALUES ARE IN OHMS, MICROFARADS,  
 AND MICROHENRIES.  
 2.) ALL RESISTORS ARE  $\pm 5\%$  1/4W.

QTY	FIELD	PART OR	DESCRIPTION	DATE	BY	CHKD
U1	Q1					
J2	CR3					
CB	R17	R12, R13				
LAST USED	NOT USED					
REFERENCE DESIGNATORS						

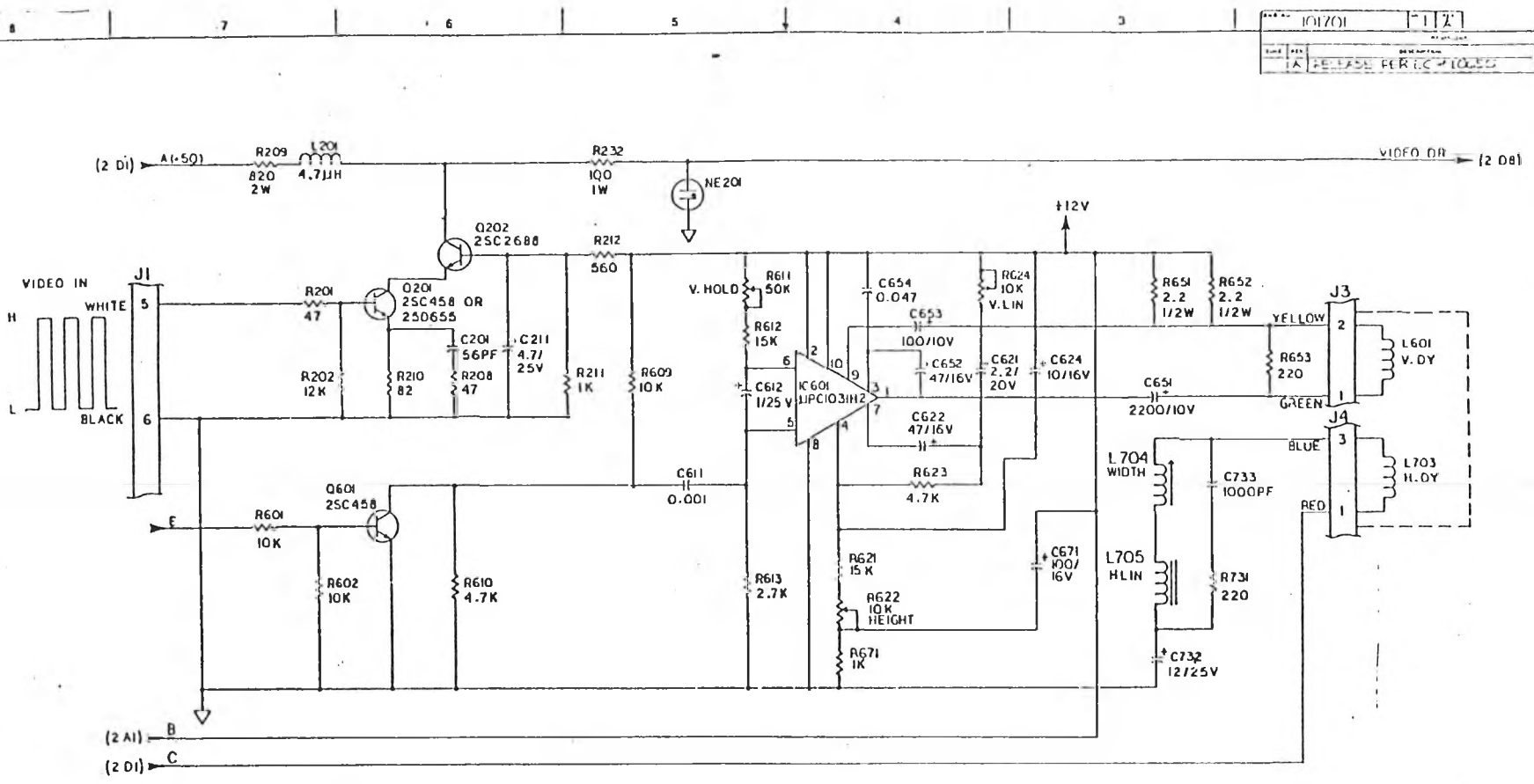
  

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS AND DECIMALS UNLESS OTHERWISE SPECIFIED		CONTRACT NO.	
MATERIAL		DATE	
DESIGN		BY	
CHECKED		DATE	
APPROVED		DATE	
DRAWN		DATE	
DO NOT SCALE DRAWING		SCALE	

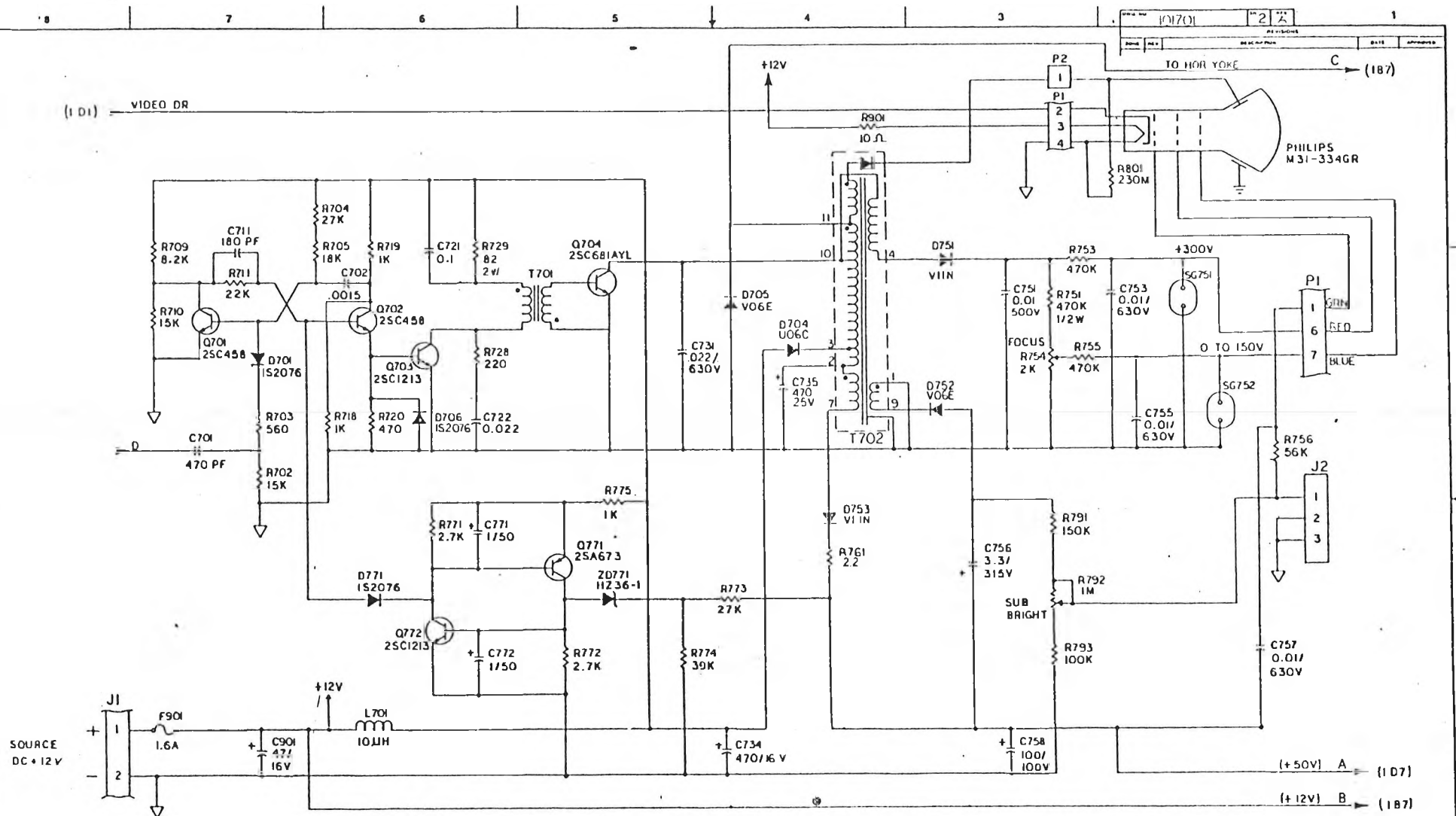
PARTS LIST		VICTOR Electronics Inc.	
SCHEMATIC			
AUDIO PREAMP			
REV	DATE	BY	CHKD
A	1/1/72	...	...

101701		1-11-71	
REV	DESCRIPTION	DATE	BY
1A	RELEASE PER EC 101701	6-17-71	PLG



2 ALL RESISTORS ARE  $\pm 5\%$  1/4 W.  
 1 ELECTRICAL VALUES ARE IN OHMS, MICROFARADS  
 AND MICROHENRIES.  
 NOTES: UNLESS OTHERWISE SPECIFIED.

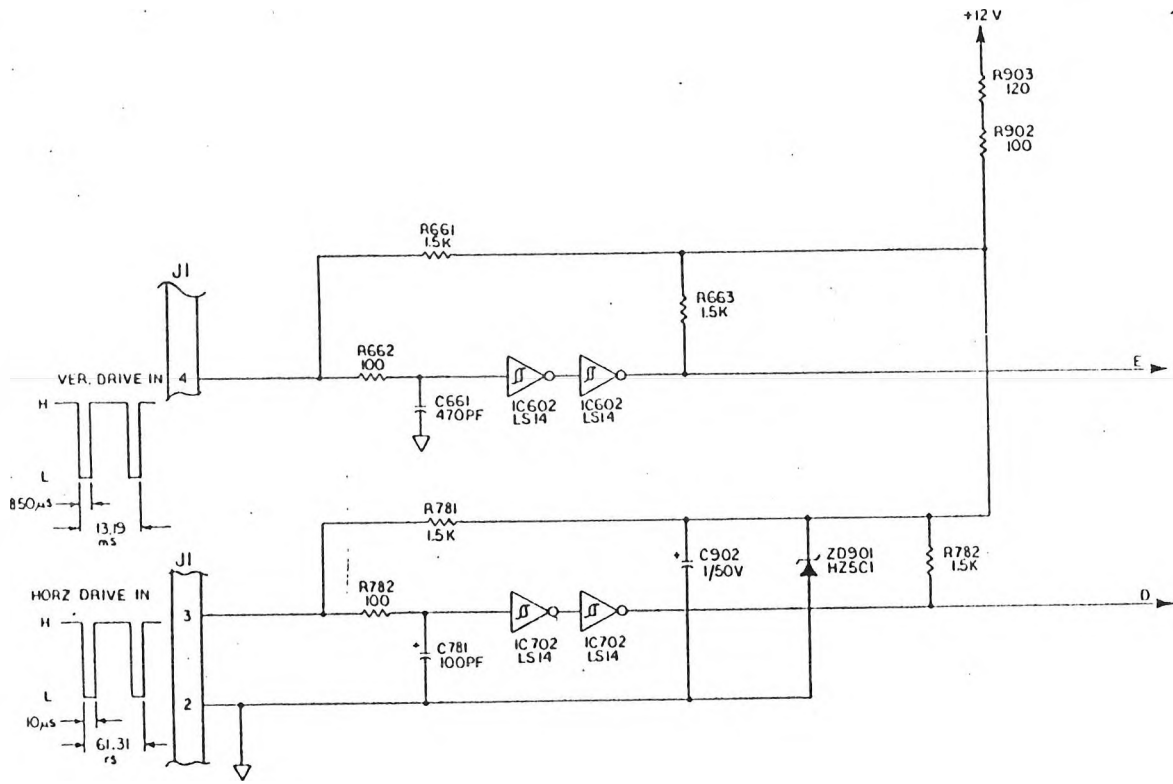
PARTS LIST		APPROVALS		DATE	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ALL		APPROVED	DATE	VICTOR	
LAST USED		NOT USED		SCHEMATIC VIDEO BOARD	
REFERENCE DESIGNATIONS		APPLICATION		101701	
DO NOT SCALE DRAWING		1 OF 3			



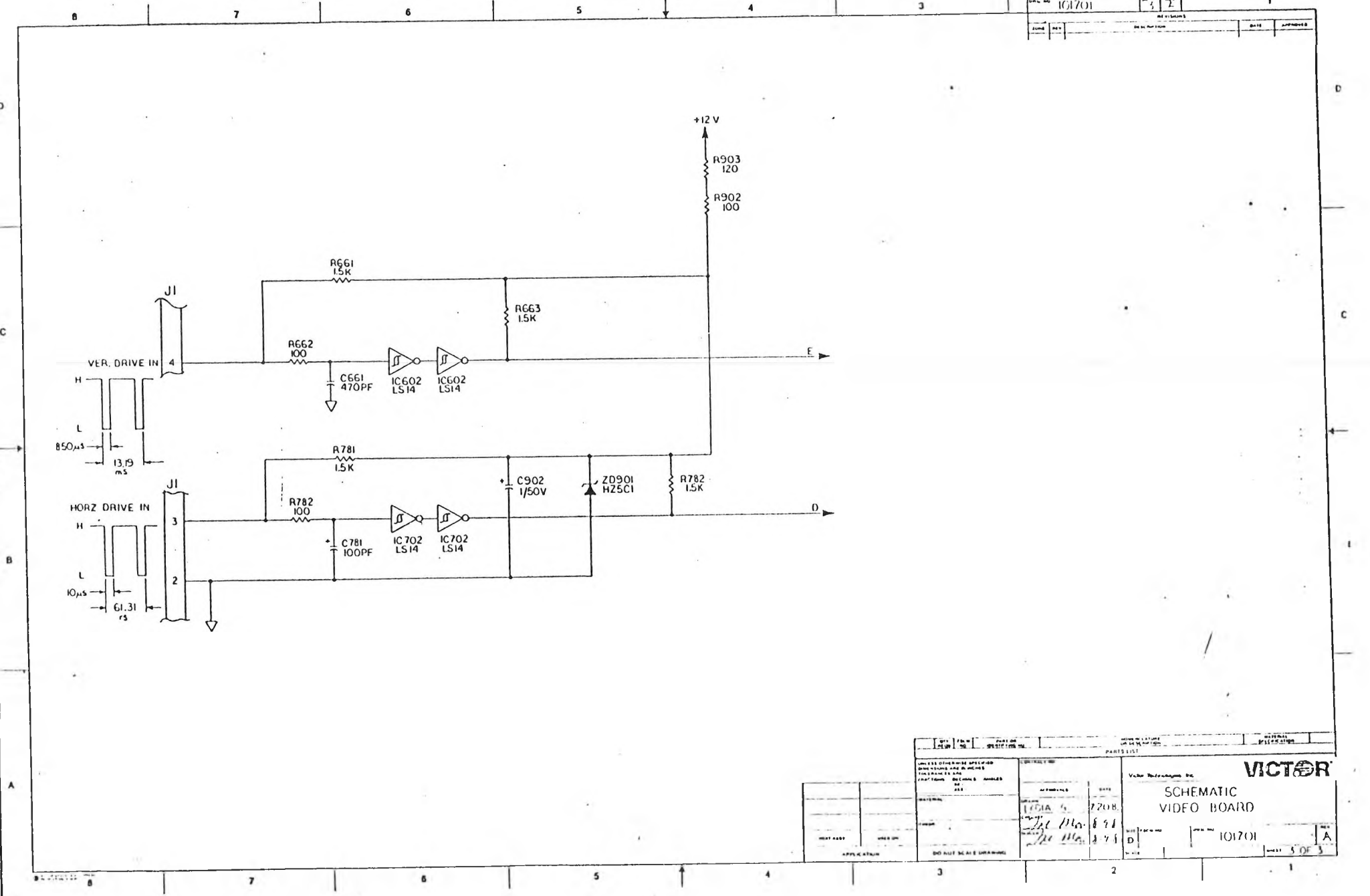
PARTS LIST		CONTROL LOG		VICTOR ELECTRONICS INC.	
DATE	REV.	APPROVED	DATE	DESIGNER	REV.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES ALL DIMENSIONS ARE TO CENTER UNLESS OTHERWISE SPECIFIED			SCHEMATIC VIDEO BOARD		
DESIGNER	DATE	APPRAISER	DATE	REV. NO.	REV.
JAN 11 1964	1/11/64	W. J. A.	1/11/64	101701	A
TESTED	USED ON	DO NOT SCALE DRAWING	SHEET 2 OF 3		



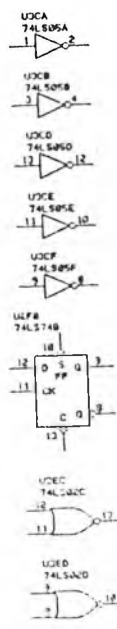
PART NO. IC1701		REV. 2		DATE		APPROVED	
DATE	REV.	BY		DATE		APPROVED	



CHECKED BY: [Signature]		DATE: 7/20/8		VICTOR ELECTRONICS INC.	
DESIGNED BY: [Signature]		DATE: 8/91		VICTOR	
DRAWN BY: [Signature]		DATE: 8/91		SCHEMATIC VIDEO BOARD	
APPLICATION: [Signature]		DATE: 8/91		PART NO. IC1701	
DO NOT SCALE DRAWING		SCALE: 1:1		REV. 2	



**NOTE:**  
SPARE GATES



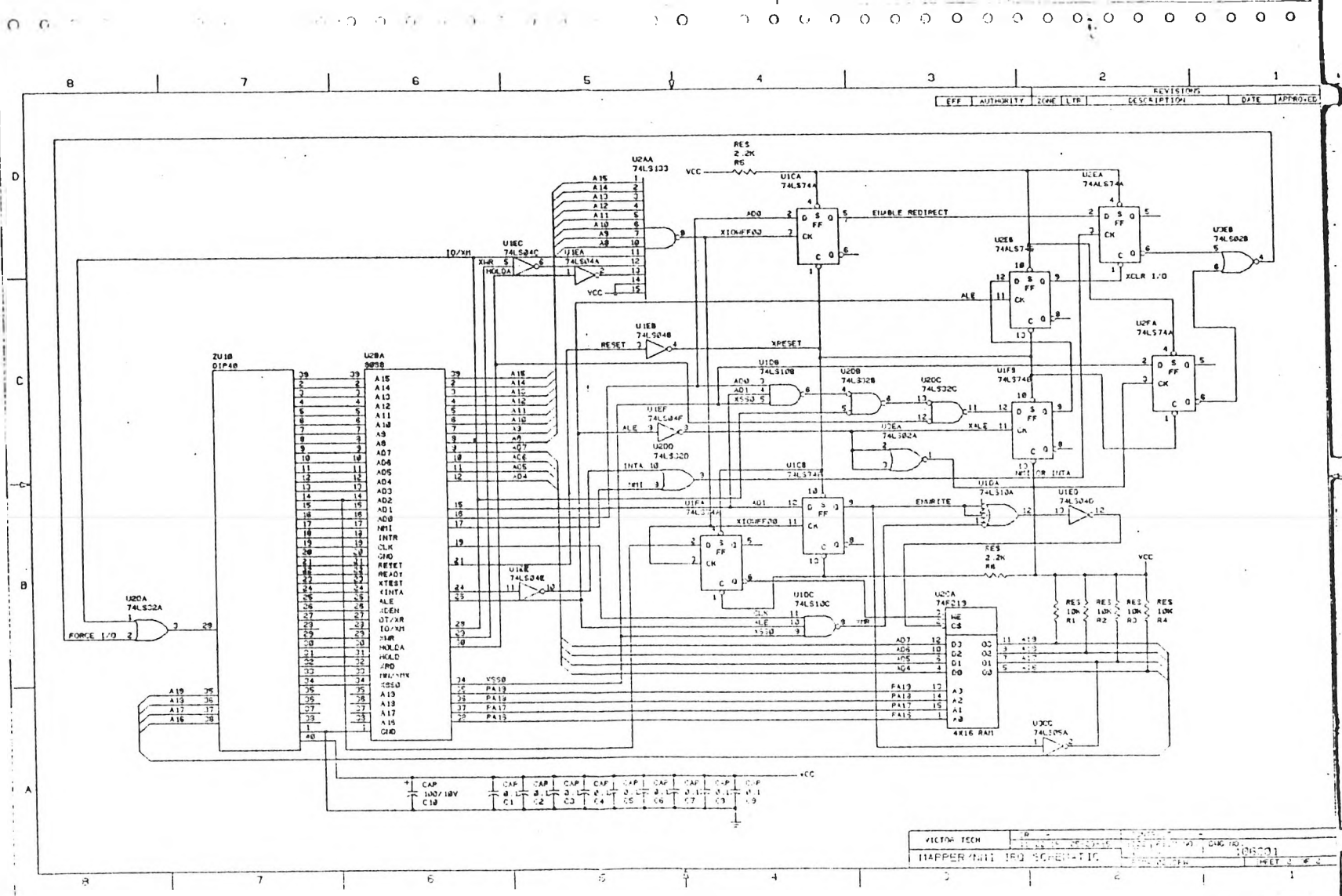
**NOTE:**  
REFERENCE DESIGNATIONS  
LAST USED  
C10  
R6  
Z110  
NOT USED

**NOTE:**

- ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROSECONDS.
- ALL RESISTORS ARE 1/4W 5%.
- IC PINS ARE GND+7 VOL+14 EXCEPT FOR:

DEVICE	GND	VCC
8008	1,20	42
74LS133	8	16
74LS210	8	16

CONTRACT		VICTOR TECHNOLOGIES	
CR		MAPPER/IMI IRQ SCHEMATIC	
ENR			
DATE			
REV			
REVISED BY		REV	DATE
		100001	

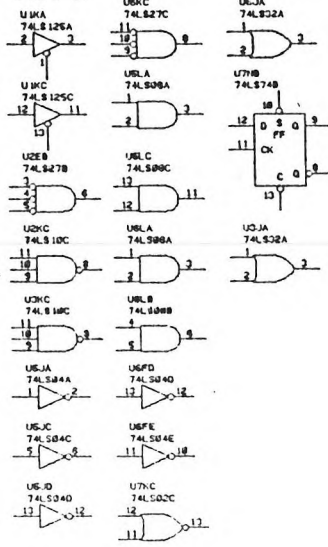


REV	AUTHORITY	DATE	DESCRIPTION	APPROVED

VICTOR TECH  
 HAPPER 7411 100 SCHEMATIC  
 100501  
 REV 1

**NOTE:**

SPARE GATES



**NOTE:**

REFERENCE DESIGNATIONS

- LAST USED  
 C32  
 R13  
 TP1  
 J3  
 J43  
 M2  
 ZP1  
 CR2
- NOT USED  
 RS  
 C12  
 C22

**NOTE:**

- ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROHENRIES.
- ALL RESISTORS ARE 1/4W, 5% EXCEPT FOR:

DEVICE	OHM	VCC
74LS138	8	16
74LS373	18	20
74LS163	8	16
74LS244	10	28
6118	12	24
74LS245	18	20
74LS670	3	16
8237	20	31
27254	14	28

4. NON JUMPER SELECTION

LCC	J42	J43
2732	244	148
2784	142	248
27128	142, 418	348
27258	142, 514	448

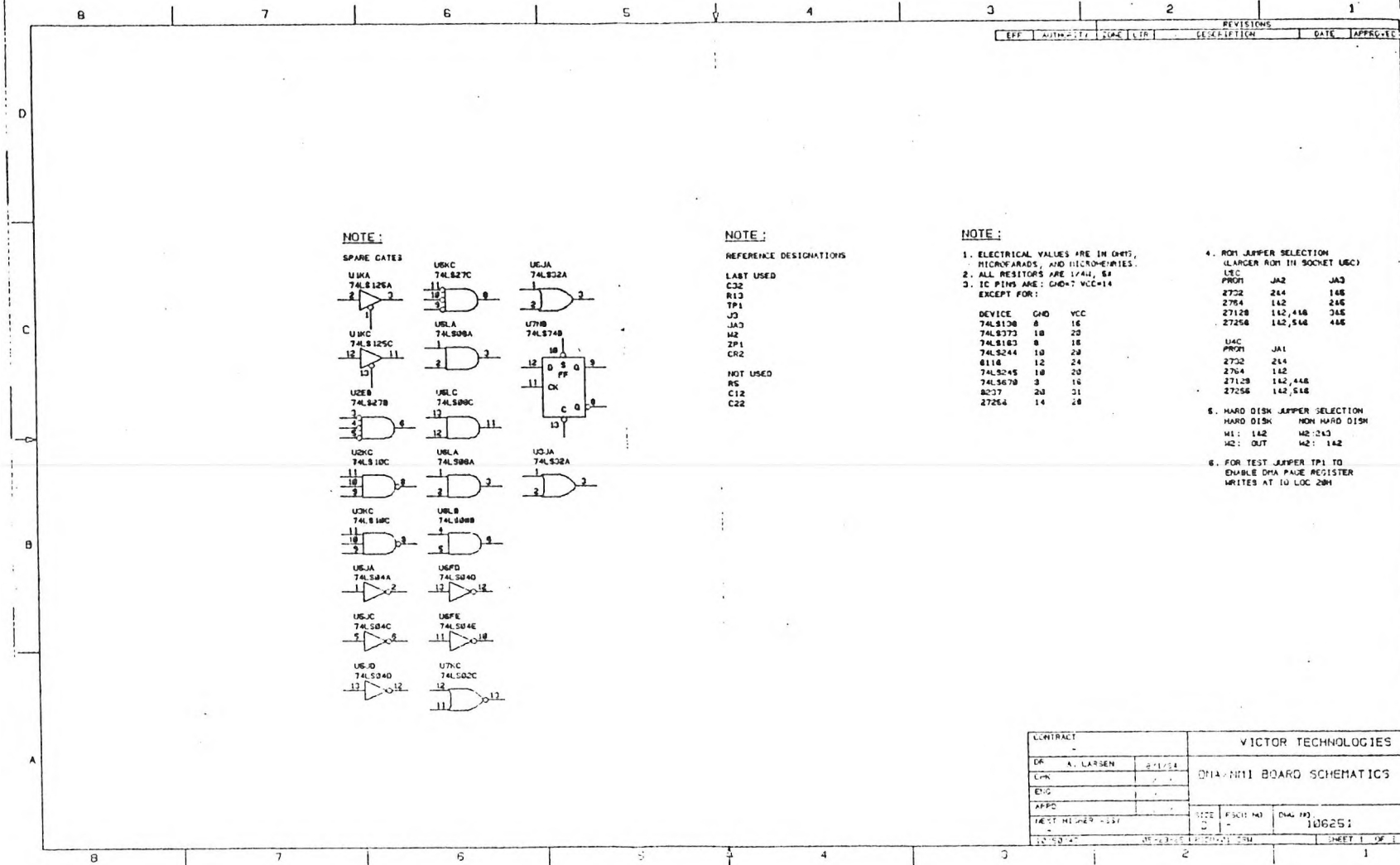
L4C	J41
PROFI	J41
2732	244
2764	142
27128	142, 418
27258	142, 514

5. HARD DISK JUMPER SELECTION

HARD DISK	NON HARD DISK
M1: 142	M2: 243
M2: 142	M2: 142

6. FOR TEST JUMPER TP1 TO ENABLE DMA PAGE REGISTER WRITES AT IO LOC 20H

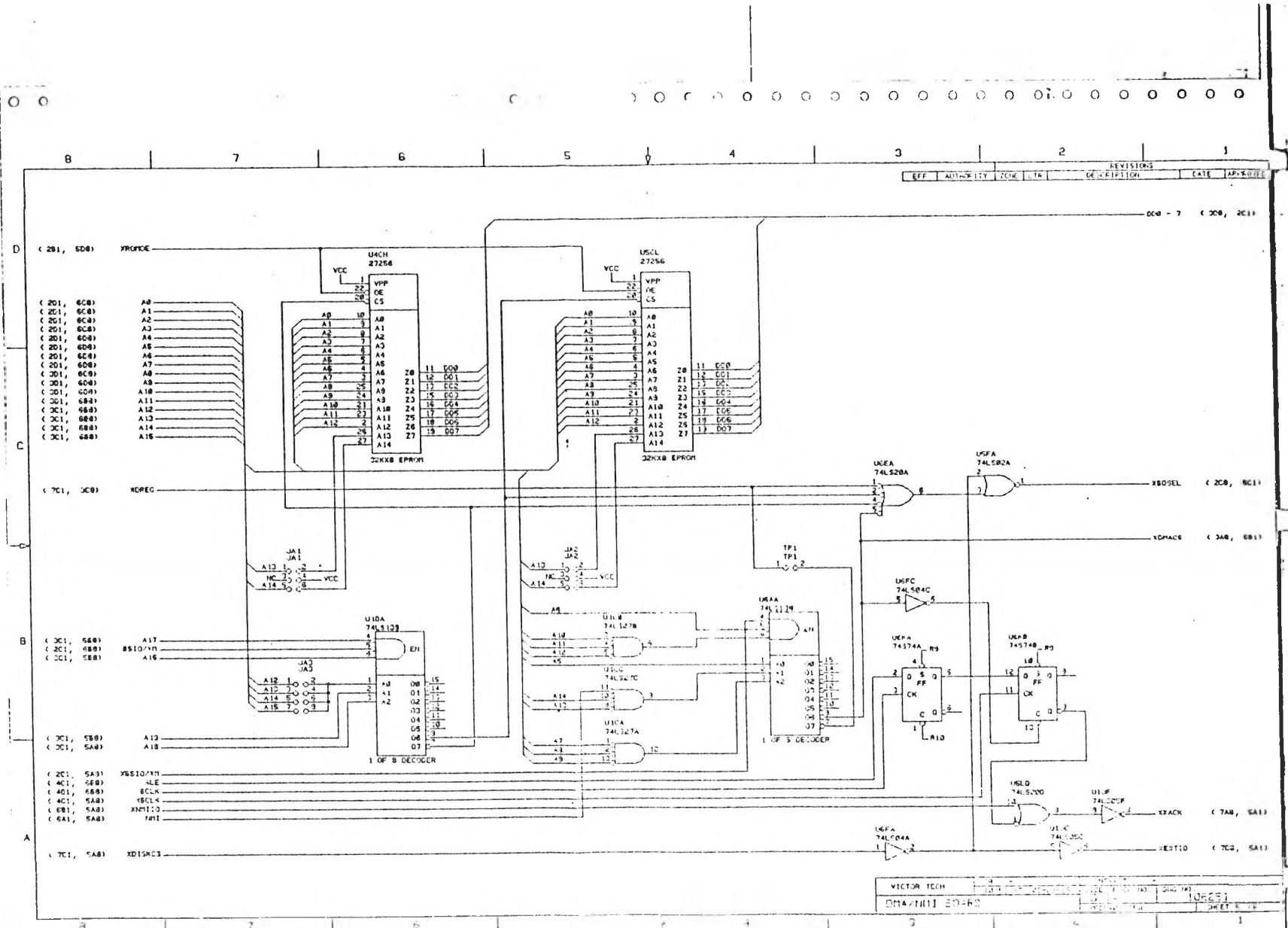
CONTRACT		VICTOR TECHNOLOGIES	
DR	A. LARSEN	DATE	2/11/81
CHK		DMA-0011 BOARD SCHEMATICS	
ENG			
APPD			
TEST NUMBER	106251	DATE	2/11/81
DESIGNED BY	APPROVED BY	CHECKED BY	DATE











REV	DATE	DESCRIPTION	BY	CHKD
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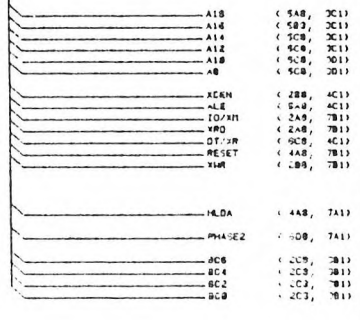
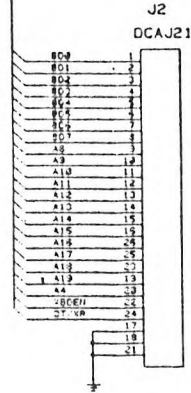
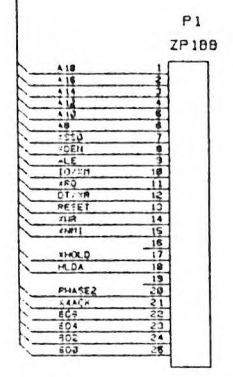
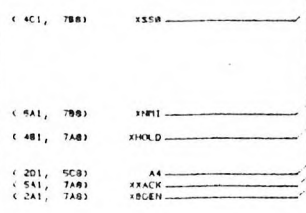
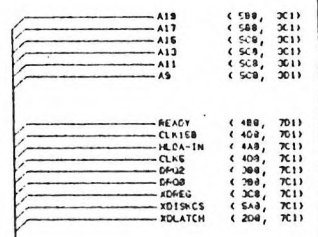
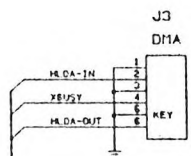
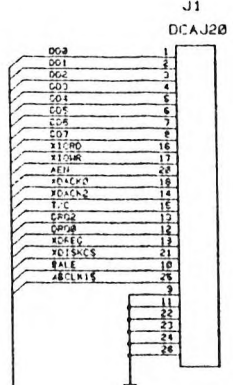
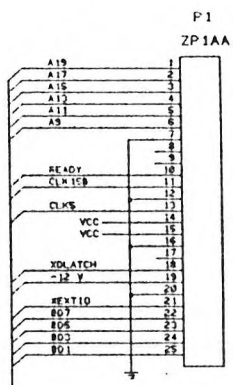
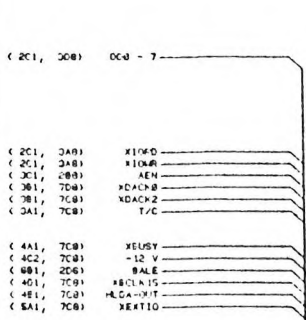
Doc - 7 (208, 201)





8 7 6 5 4 3 2 1

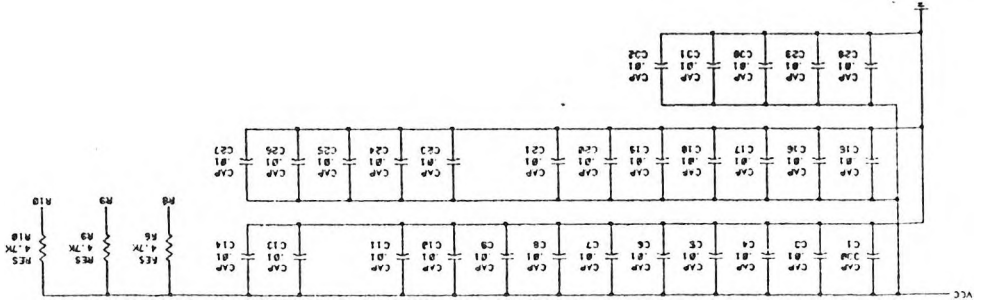
REVISIONS						
EFF.	AUTHORITY	ZONE	LTR.	DESCRIPTION	DATE	APPROVED



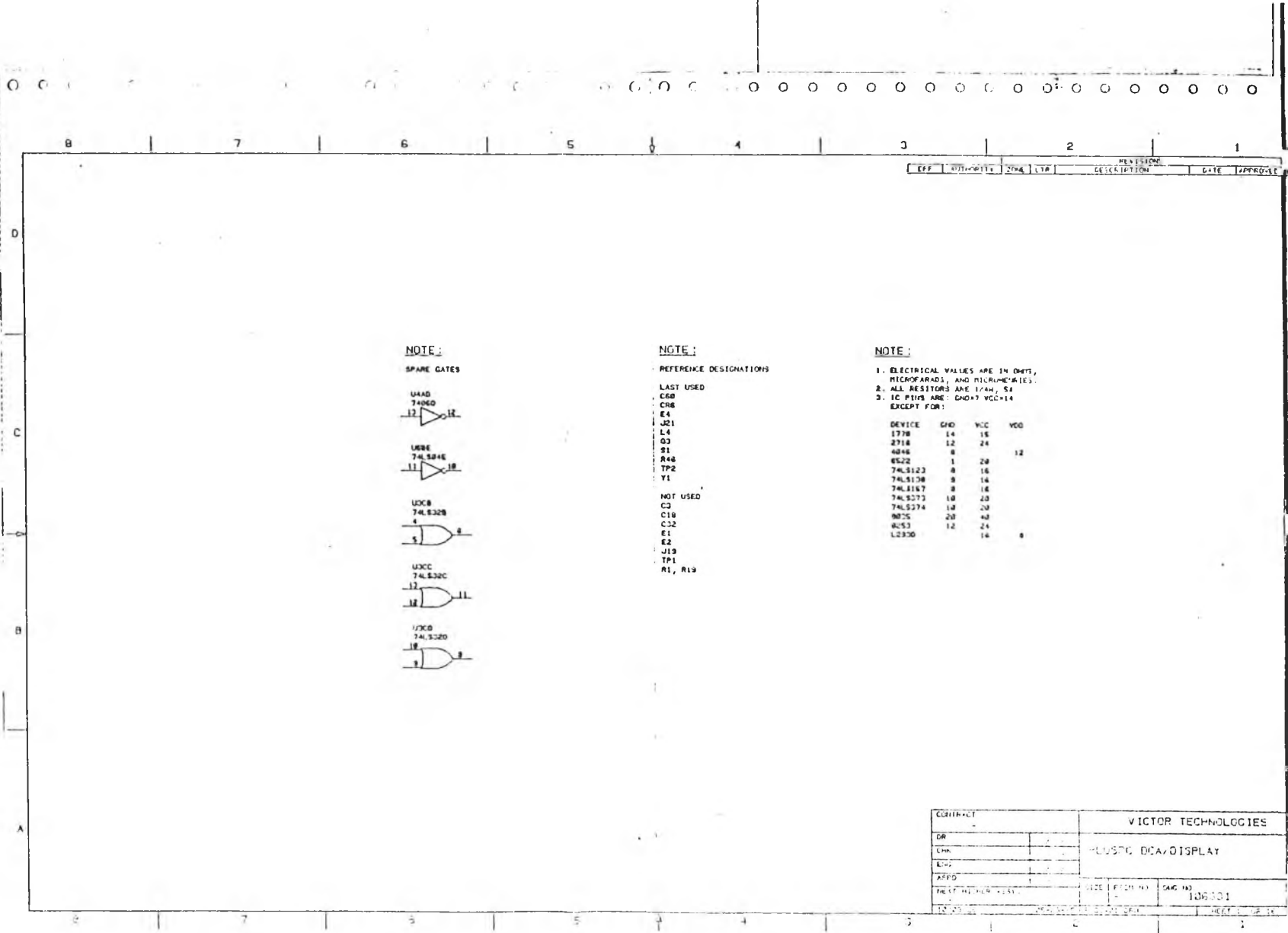
VICTOR TECH	DR	CONTRACT	SIZE	FORM NO.	DWG TAG
DMA/N11 BOARD	11 US 15 MS-22-5		1/2		105152
			PRECED CAN		SHEET 3 OF 3

8 7 6 5 4 3 2 1

DATE	11/07/06	DESIGNED BY	DAVID
REV	01	PROJECT	OMY-1011 BOARD



REV	01	DATE	11/07/06
DESIGNED BY	DAVID	PROJECT	OMY-1011 BOARD



REV	DATE	DESCRIPTION	APPROVE

**NOTE :**

SPARE GATES



**NOTE :**

REFERENCE DESIGNATIONS

LAST USED

- C60
- C8E
- E4
- J21
- L4
- Q3
- S1
- R46
- TP2
- Y1

NOT USED

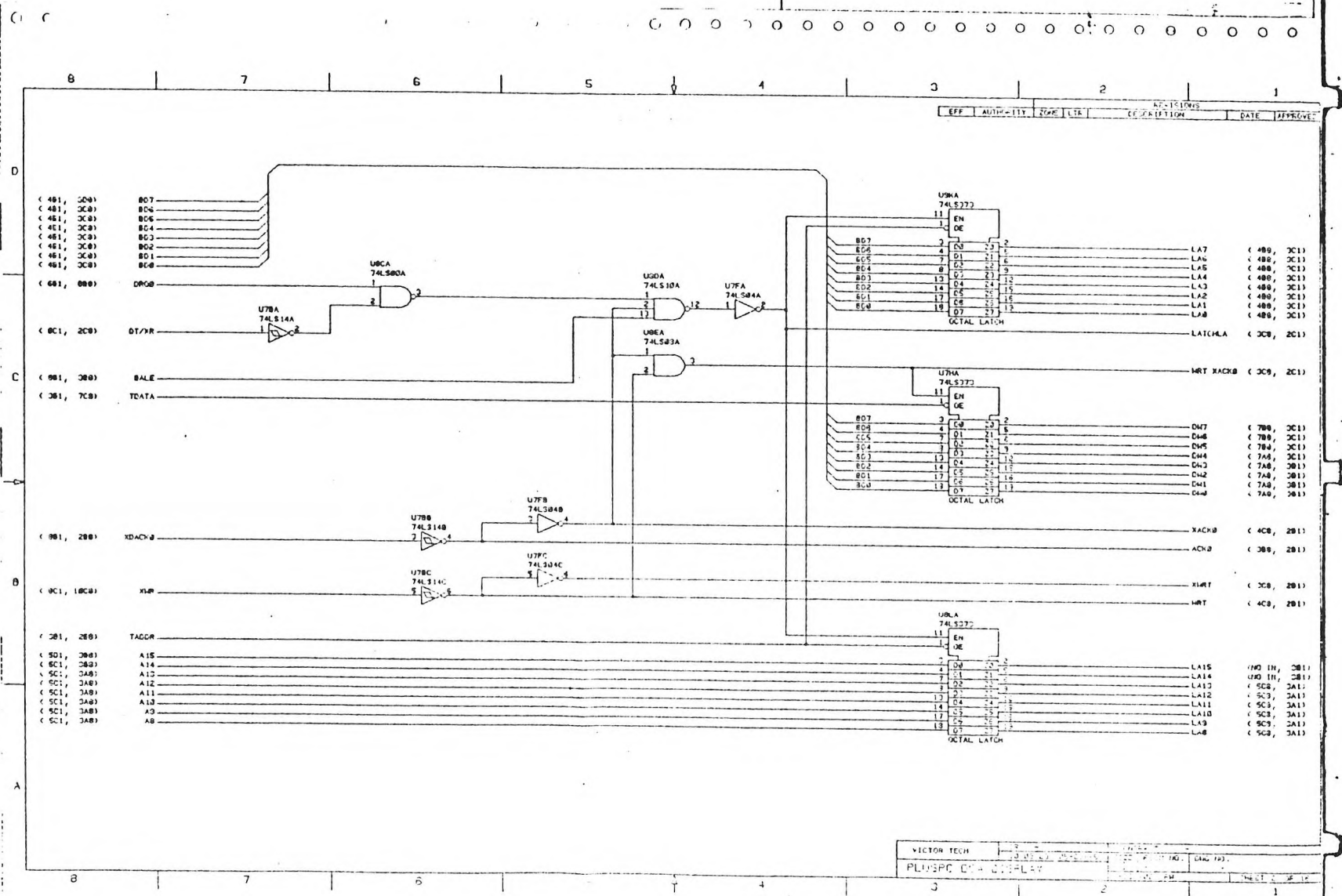
- C3
- C10
- C32
- E1
- E2
- J10
- TP1
- R1, R19

**NOTE :**

1. ELECTRICAL VALUES ARE IN OHMS, MICROFARADS, AND MICROSECONDS.
2. ALL RESISTORS ARE 1/4W, 5%.
3. IC PINS ARE: GND=VCC=14 EXCEPT FOR:

DEVICE	GND	VCC	VDD
1770	14	16	
2718	12	24	
4046	8		12
6522	1	20	
74LS123	8	16	
74LS170	8	16	
74LS167	8	16	
74LS273	10	20	
74LS274	10	20	
9025	20	40	
9253	12	24	
L2350	14		8

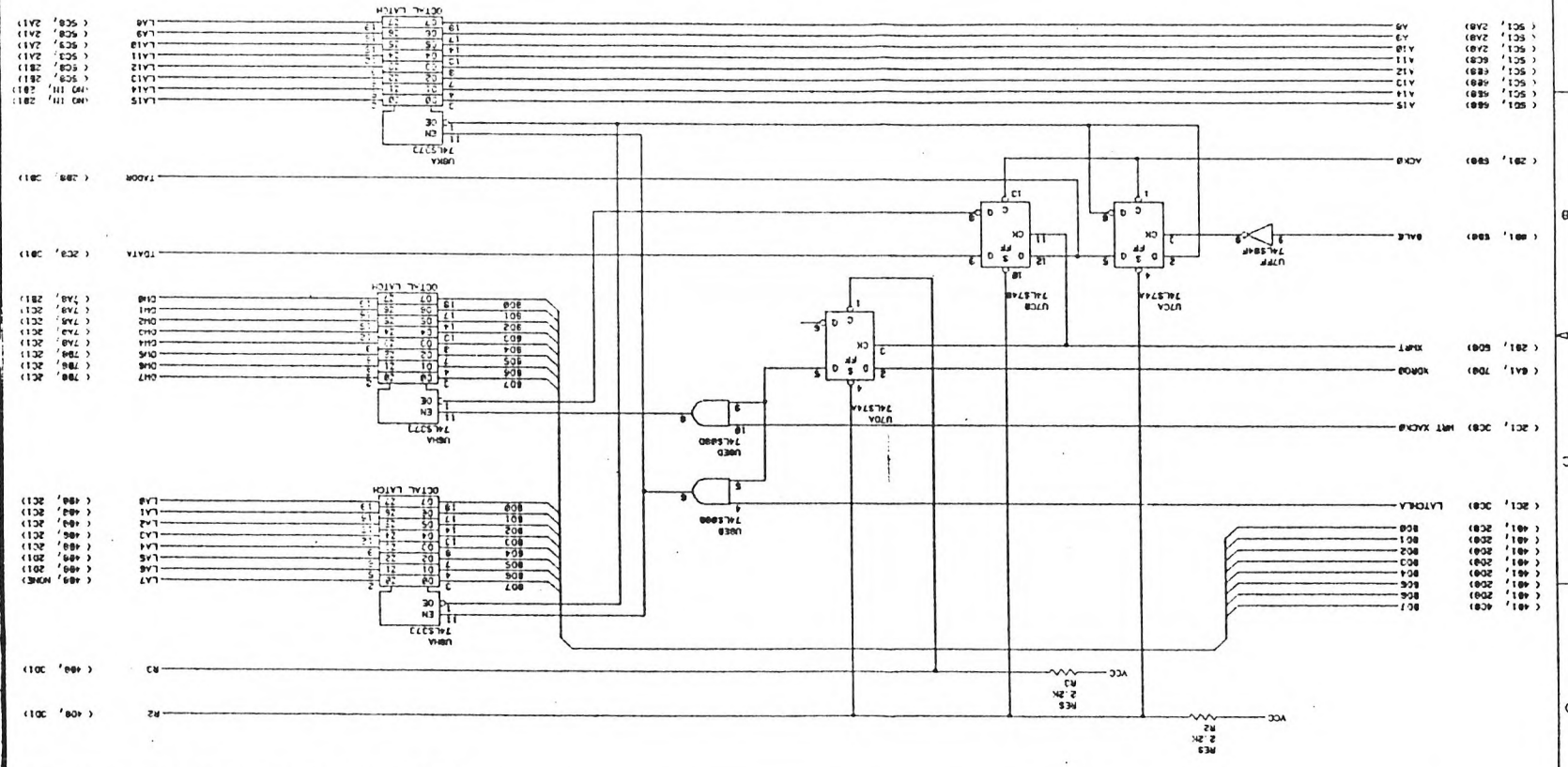
CONTRACT		VICTOR TECHNOLOGIES	
DR		PLUSC DCA/DISPLAY	
ENR			
APPD			
DATE		SIZE	SAG NO
			106001



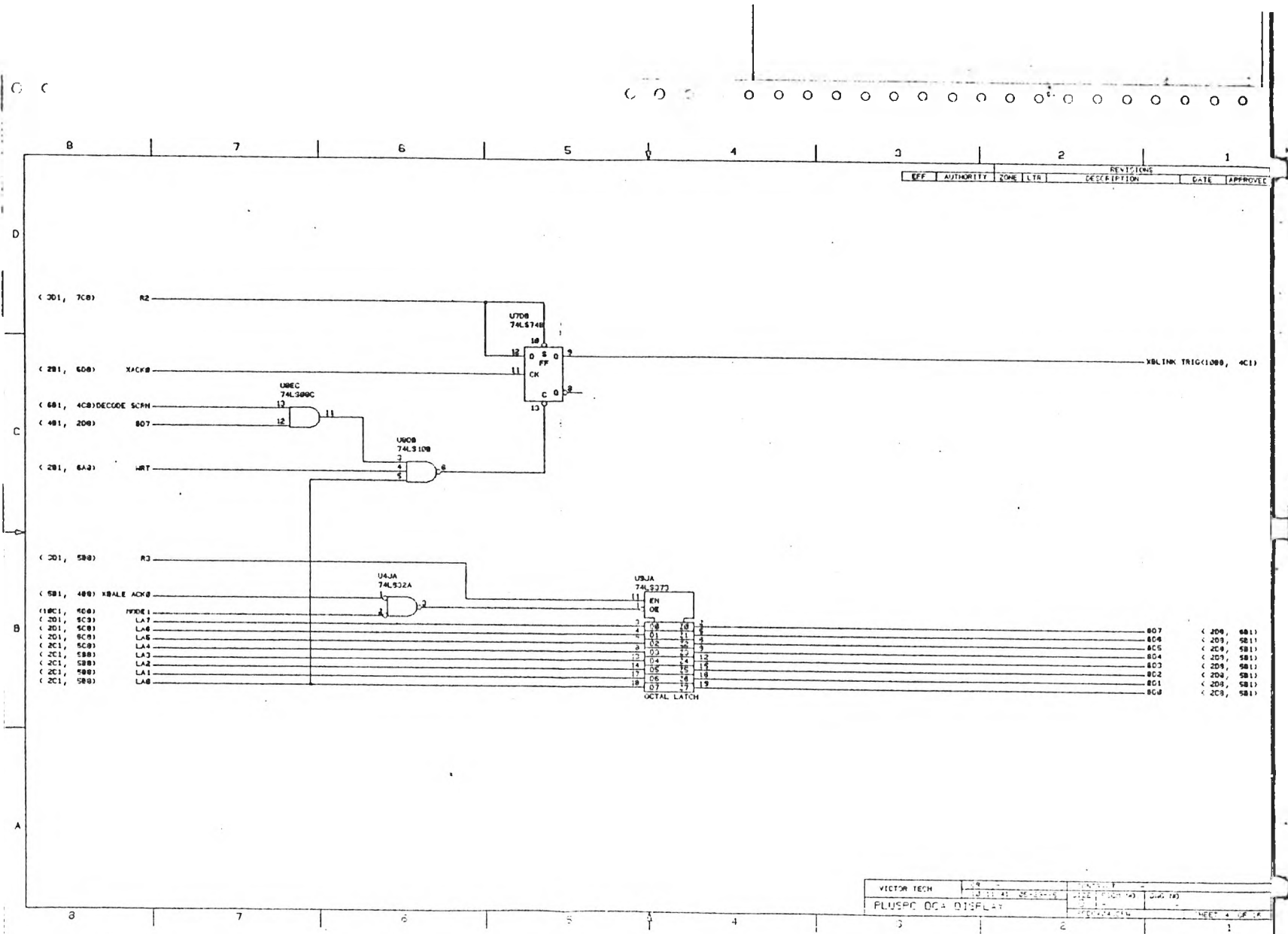
REV	DATE	DESCRIPTION	APPROVED

VICTOR TECH			
PLUSPC EDA DISPLAY			

PLU5PC DCA 015744  
 VICTOR TECH  
 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

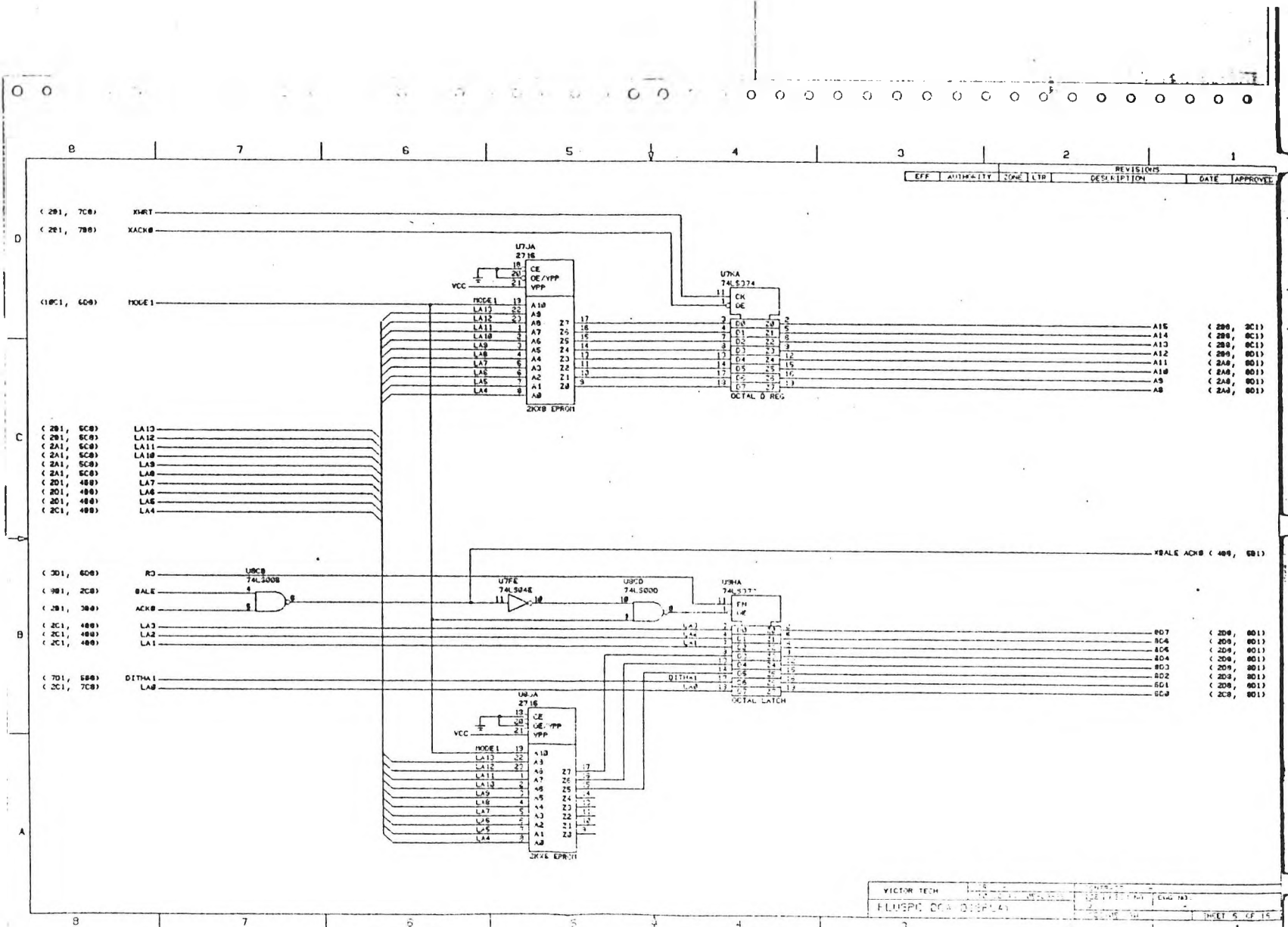


EFF AUTHORITY DATE DESCRIPTION  
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REVISIONS		DATE	APPROVEE
EFF	AUTHORITY	ZONE	LTR
		DESCRIPTION	

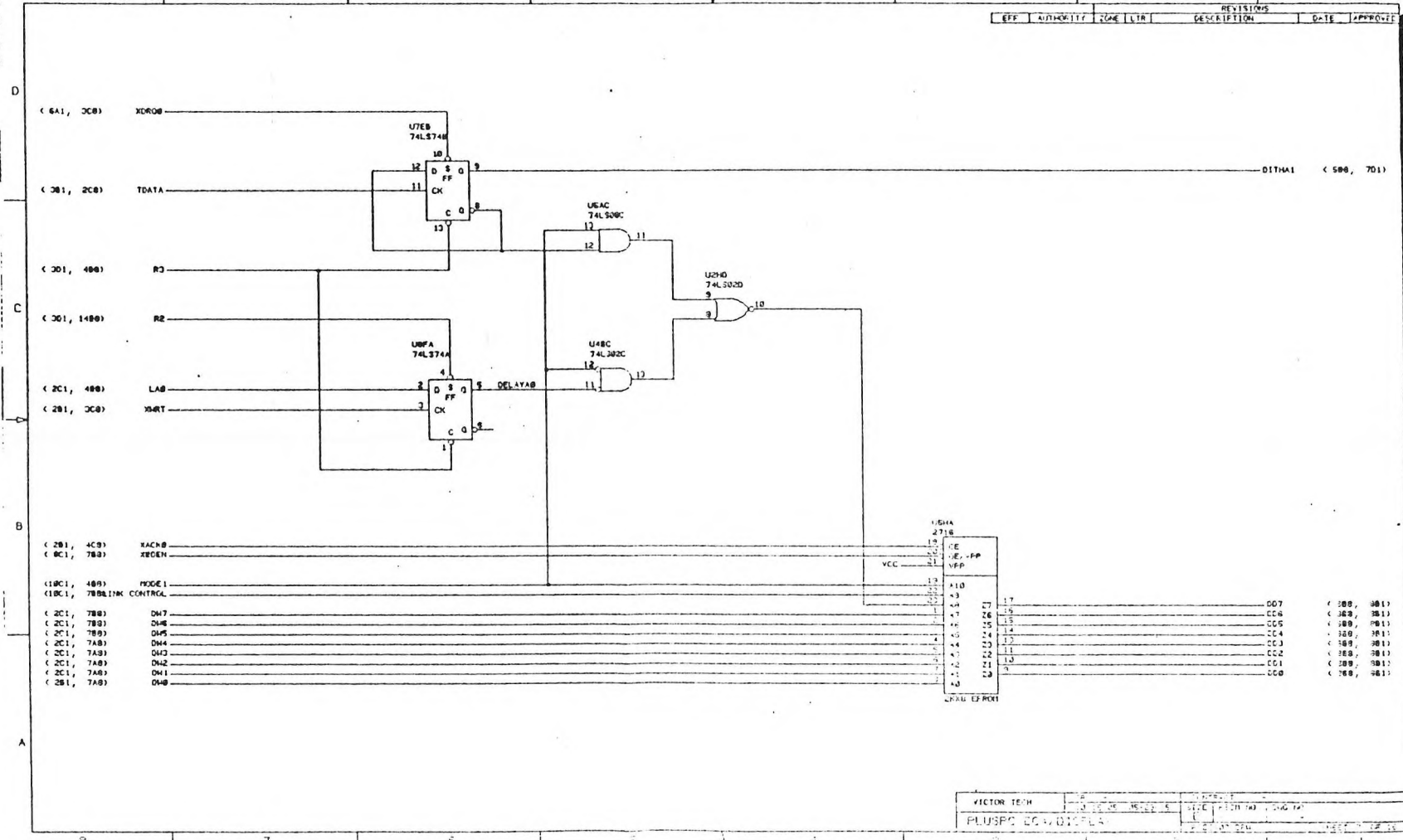
VICTOR TECH	10 11 41	2620116	10 11 41	2620116	10 11 41	2620116
PLUSPC OCA DISPLAY			10 11 41	2620116	10 11 41	2620116





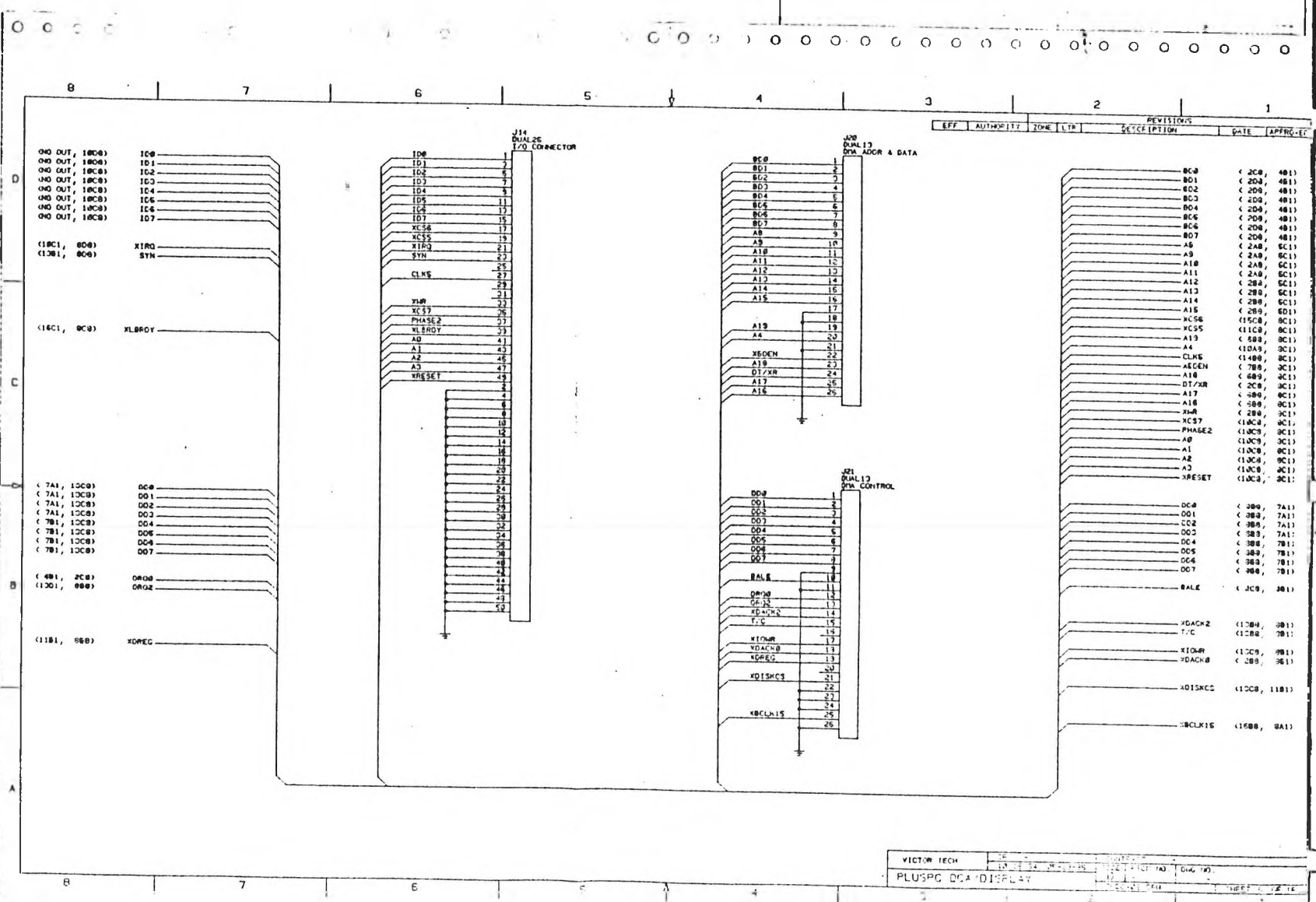


REVISIONS						
EFF	AUTHORITY	ZONE	LTR	DESCRIPTION	DATE	APPROVED

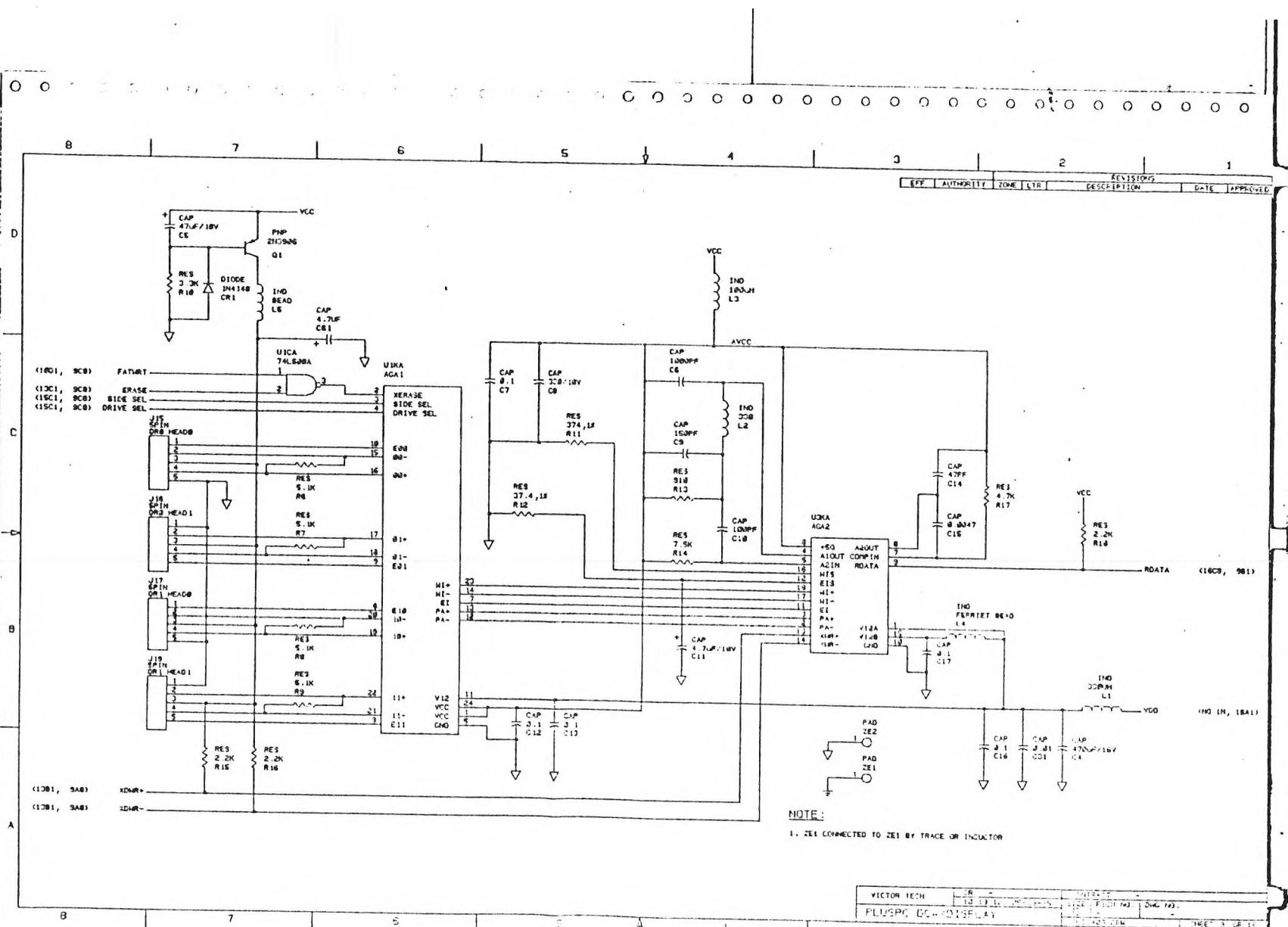






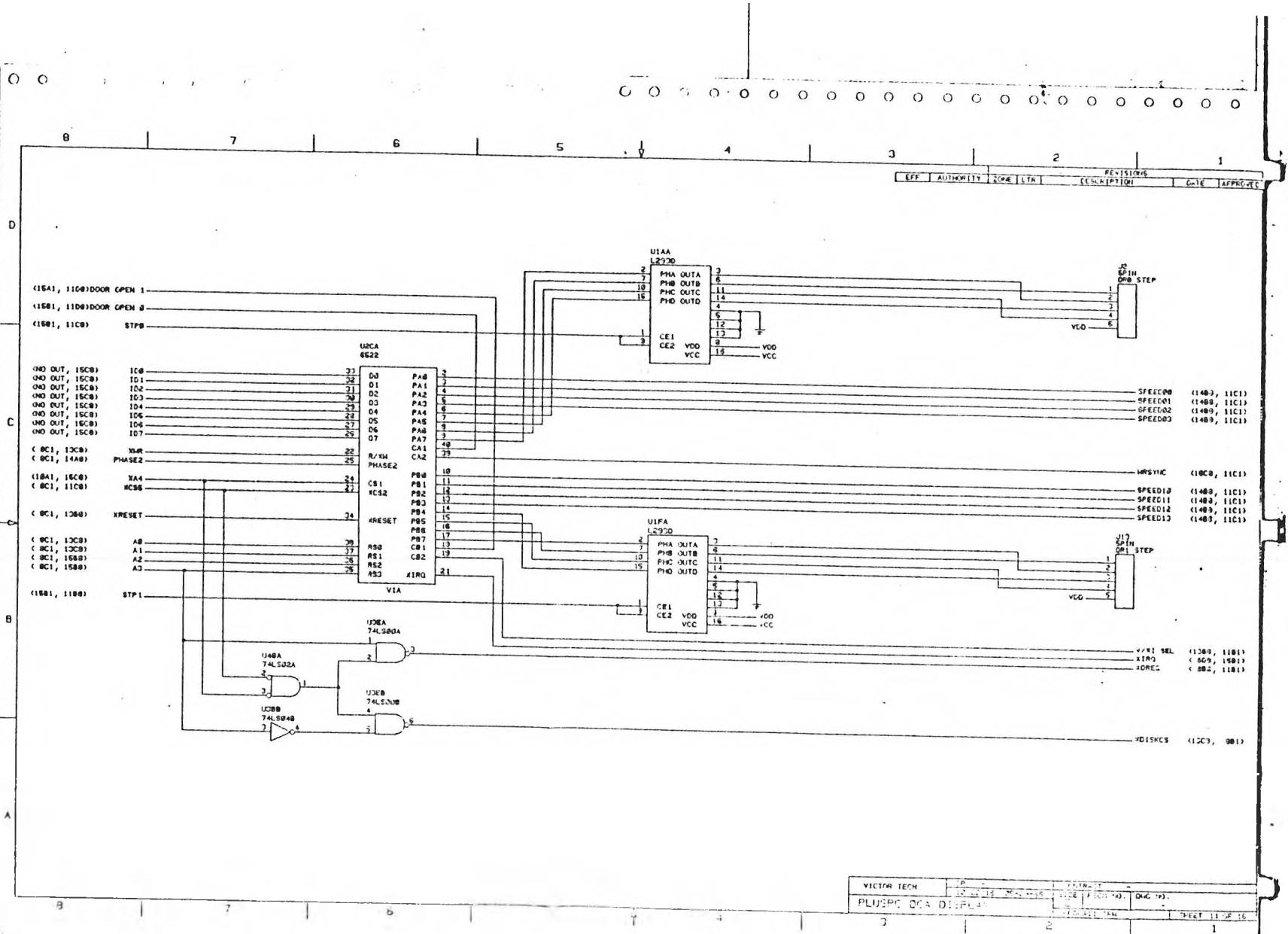


REV	DATE	DESCRIPTION	APPROVED
1			



REVISIONS				
REV.	AUTHORITY	ZONE	DATE	APPROVED

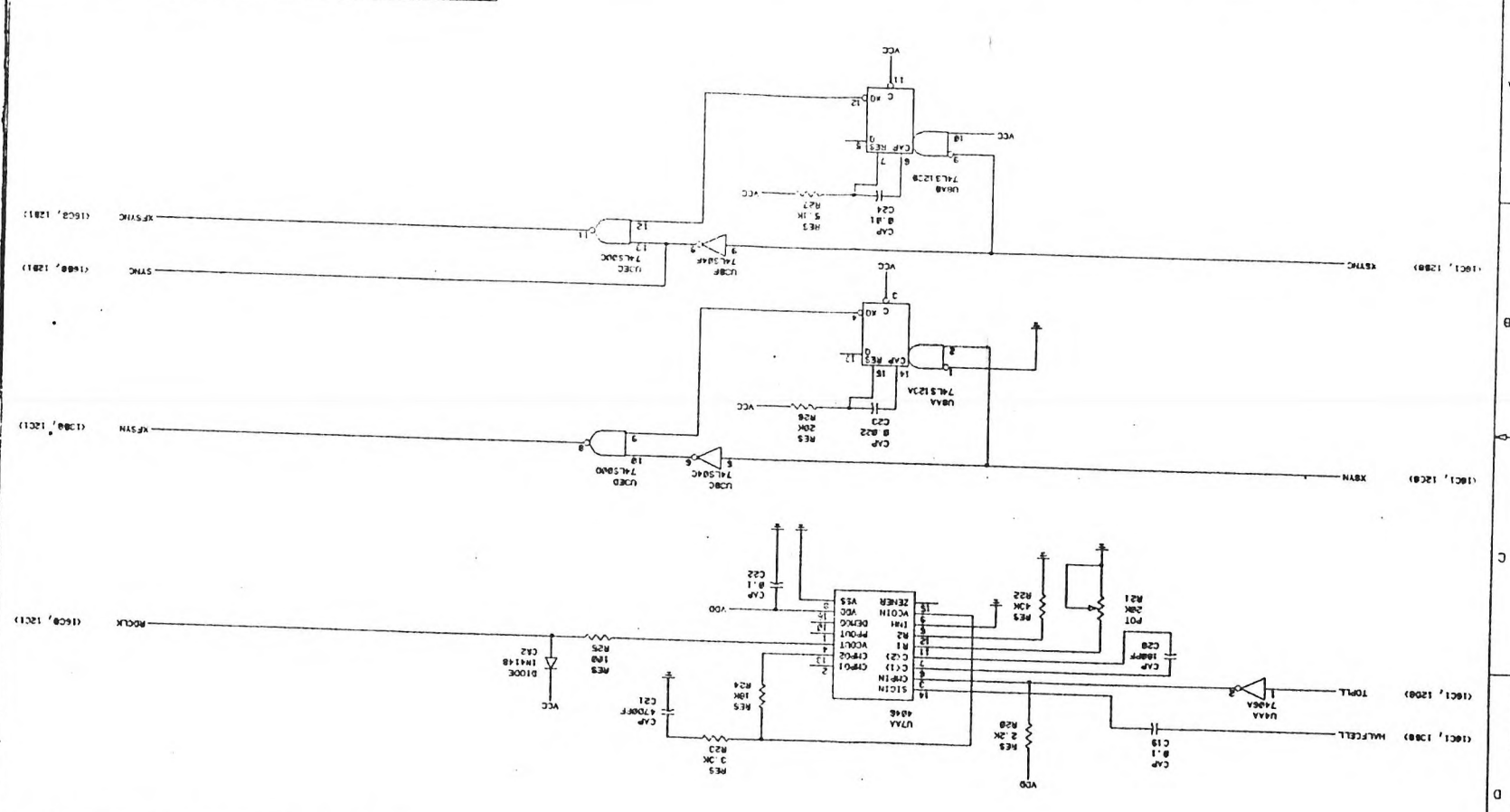
VICTOR TECH	DR -	REVISED	DATE	BY
PLUSPC DC-701SELAY	13 13 13	13 13 13	13 13 13	13 13 13



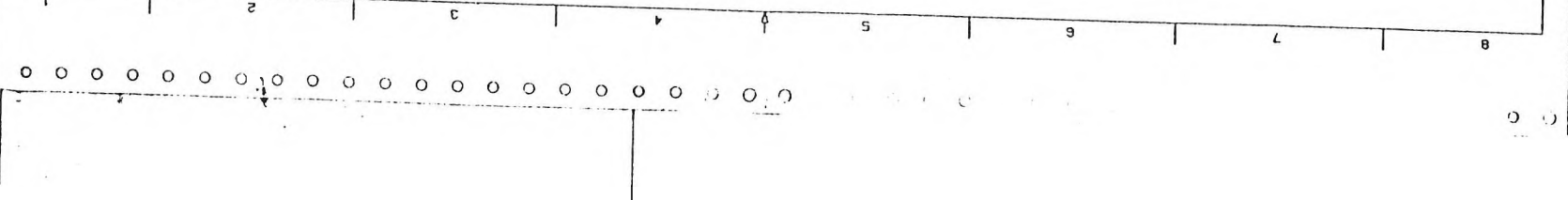
REVISIONS			
EFF	AUTHORITY	DATE	DESCRIPTION

VICTOR TECH	10	PL/5PC DCA DISPLAY	1
PL/5PC DCA DISPLAY	10	PL/5PC DCA DISPLAY	1

REV	DATE	DESCRIPTION	BY	CHKD	APPROVED
1					

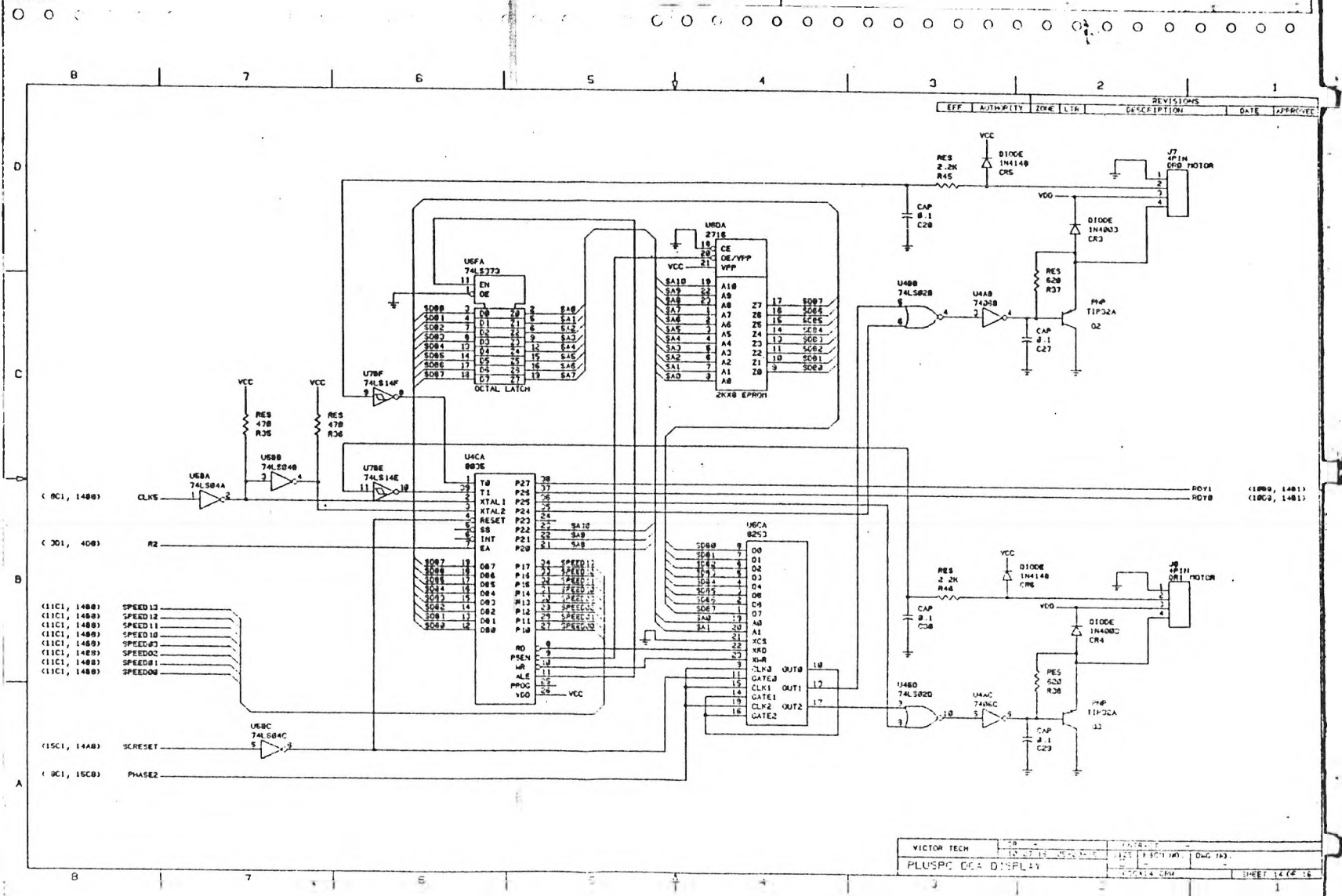


REV	DATE	DESCRIPTION	BY	CHKD	APPROVED
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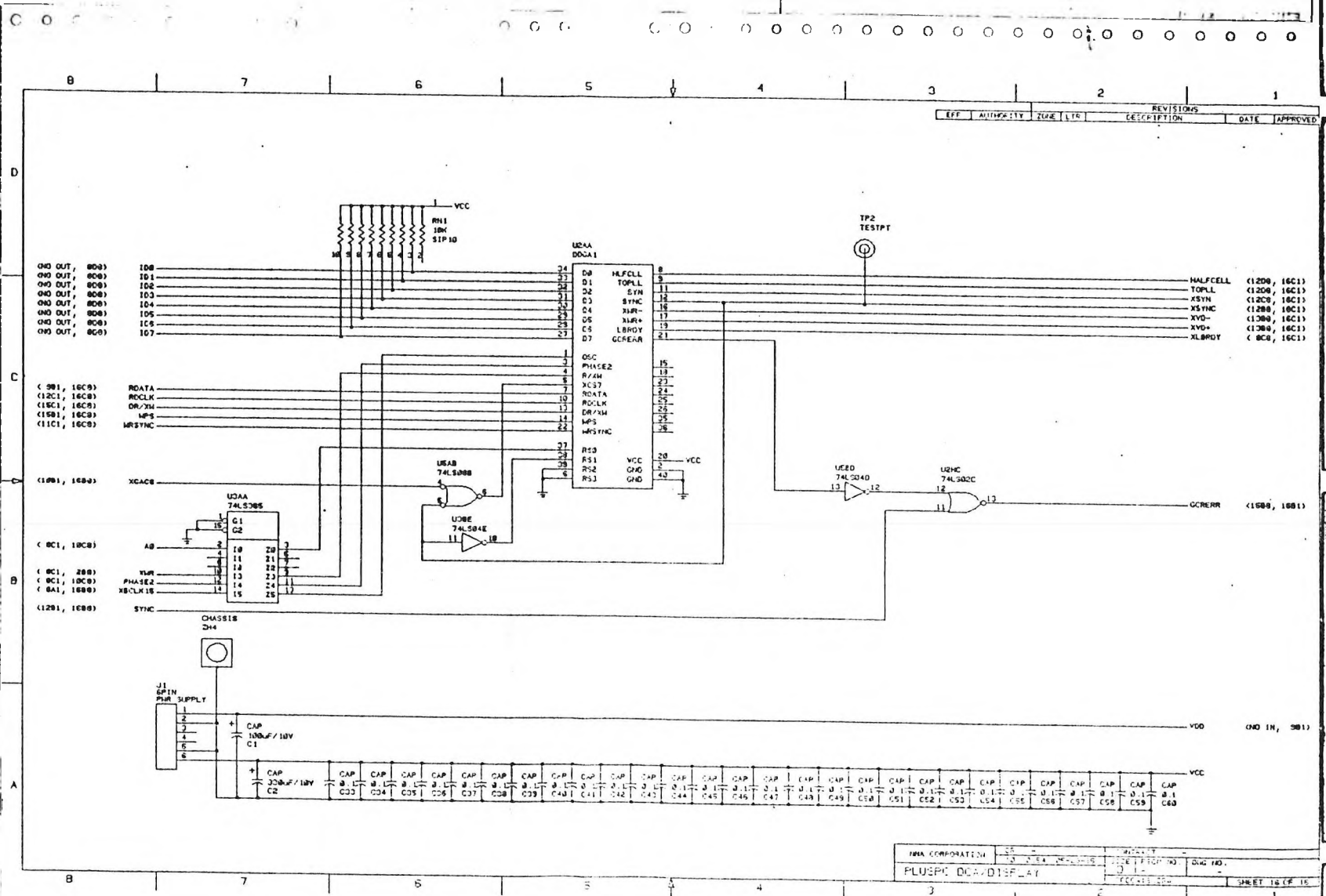


REVISIONS				
EFF	AUTHORITY	ZONE	DATE	APPROVE

- (C01, 1480) CLKS
- (C01, 400) R2
- (C1C1, 1480) SPEED13
- (C1C1, 1480) SPEED12
- (C1C1, 1480) SPEED11
- (C1C1, 1480) SPEED10
- (C1C1, 1480) SPEED09
- (C1C1, 1480) SPEED08
- (C1C1, 1480) SPEED07
- (C1C1, 1480) SPEED06
- (C1C1, 1480) SPEED05
- (C1C1, 1480) SPEED04
- (C1C1, 1480) SPEED03
- (C1C1, 1480) SPEED02
- (C1C1, 1480) SPEED01
- (C1C1, 1480) SPEED00
- (C1C1, 1480) SRESET
- (C01, 1500) PHASE2

(1800, 1401)  
(1800, 1401)





REV#	AUTHORITY	DATE	REVISIONS		
			DESCRIPTION	DATE	APPROVED

- HALFCELL (1200, 16C11)
- TOPLL (1200, 16C11)
- XSYN (1200, 16C11)
- XSYN (1200, 16C11)
- XV- (1200, 16C11)
- XV+ (1200, 16C11)
- XLBDY (1200, 16C11)

XCERR (1600, 1601)

GND IN, 901)