3.4 T99128 I/O Board

3.4.1 Introduction

The T99128 board features 128 bidirectional open collector CRU input/output bits. The CRU bits may be addressed in multiples of 1 to 16 bits. External interface is via four 34 pin ribbon cables. The CRU base address is selected via DIP switches to allow up to 16 T99128 boards in a single system.

3.4.2 Theory of Operation

The T99128 board consists of four functional sections. One section is the control and decoding section and the other three are 32 bit I/O modules. The control and decoding section buffers the incoming signals and provides the necessary decoding of the address lines to select the individual bits. The 32 bit I/O modules each provide 32 bits of bidirectional CRU I/O.

Interface to the rest of the system consists of the address bus and CRU control lines (CRU out, CRU in, CRU clock). These signals are buffered by 74LS367's (U-17, U-18, U-19). Address decoding is accomplished by U-16, U-20, U-15, U-21, and U-22. U-16 (a four input nor gate) detects logical zero on the four most significant address bits (A0 through A3). The output of U-16 is inverted by U-20 to provide the enable for the 1-of-16 decoder (U-15). The 1-of-16 decoder (U-15) decodes the next four address lines (A4 through A7) to provide 16 board select signals. The appropriate board select signal is in turn passed to U-21 and U-22, another pair of 1-of-16 decoders, by the DIP switches S1 and S2. S1 and S2 will select the starting address of the T99128 board as follows:

Switch	CRU base address
S1-1	>700
S1-2	>600
S1-3	>500
S1-4	>400
S1-5	>300
S1-6	>200
S1-7	>100
S1-8	>000
S2-1	>F00
S2-2	>E00
S2-3	>D00
S2-4	>C00
S2-5	>B00
S2-6	>A00
S2-7	>900
S2-8	>800

When the 1-of-16 decoder (U21) is enabled by the board select signal, it will decode the four address lines, A8 through A11, to produce an 8 bit input select signal. The 8 bit input select signal is in turn routed to the appropriate 32 bit module to enable the input bits. Output decoding is accomplished by the other 1-of-16 decoder (U-22). It decodes the address lines A8 through A11, and produces an 8 bit output select signal. The output select, like the input select, is routed to one of the 32 bit I/O modules to select the appropriate output bit. The output select decoder is enabled by both the board select decoder and associated DIP switches and the CRU clock pulse. The CRU clock hs been buffered by U-20 to avoid possible glitch situations.

The 32 bit I/O modules are all identical in nature and are represented by a single schematic drawing. For example, pin 14 of U-4 on the first module is SO(0). On the second it will be SO(4), on the third it will be SO(8), and on the last one it will be SO(12). J-1 is the 34 pin ribbon cable connector containing the 32 bits of bidirectional I/O. Pin 1 and pin 34 of this connector are both connected to ground. Thus, no damage to the T99128 board will occur by reversing the connector. The individual CRU bit number, relative to the base address of the 32 bit module in question is shown below (module 0 is the rightmost module when viewed from the edge of the board with the interface cables):

I/O Module	CRU Bits	CRU Base
0	0 to 1F	0
1	20 to 3F	40
2	40 to 5F	80
3	60 to 7F	C0

J1 Conn. pin no	CRU bit relative to base
1	ground
2	4
3	8
4	5
5	9
6	6
7	A
8	7
9	B
10	1
11	F
12	2
13	E

14	3
15	D
16	0
17	C
18	1F
19	10
20	1E
21	11
22	1C
23	12
24	1D
25	13
26	1B
27	17
28	1A
29	16
30	19
31	15
32	18
33	14
34	ground

Pin one of the connector is marked by an arrow or some other distinctive marking. The odd numbered pins are on that side of the connector. The even numbered pins are on the opposite side with pin 2 directly opposite pin 1. For example, pin 15 of J-1 is bit number 0D (hexadecimal) relative to the base address. If the base address for the module is, let's say 100, the actual CRU bit number is 10D (hexadecimal).

On each of the modules U-11, U-12, U-13 and U14 are the input select chips. When one of these chips is enabled by the 8 bit input select (for example SI(0)) the appropriate bit number selected by the address lines A-12 to A-14 will be placed on the CRU input line. U-1, U-2, U-3, U-4 are the output chips. When one of the output chips is enabled (for example SO(0)) the address lines A-12 to A-14 are decoded to set or clear the appropriate output bit. Each of the output bits are passed through 7407 open collector drivers (U-5, U-6, U-7, U-8, U-9, U-10). These output bits then pass to the edge connector and are also connected to the input bits. Thus any time a program sets or clears an output bit, the resultant status of that bit may be examined using the input portion of the I/O modules. The resistor networks RN1, RN2, RN3, RN4, RN5, provide the necessary pull-up resistors for the open collector drivers U-5 to U-10. These resistor networks may be omitted to obtain non pulled-up bits or to pull the output bits up with external circuitry.

3.4.3 Installation and Operation

To install the T99128 board in the system the address lines (J-4), the control lines (J-6), power and ground must be connected to the board. The starting CRU base address is selected by S1 and S2 as described earlier. If more than one T99128 board is installed in the system it is very important not to place both T99128 boards at the same CRU base address. In this case a bus conflict will exist and may damage either of the boards. In addition, the T99SS CPU module uses bits 0 to F so they must be removed if the base address >000 is selected.

Since the T99128 board is bidirectional it can be checked by the processor using a simple 9900 program. That program is shown at the end of this section. You can enter this program by using the monitor and then execute it by a GO command to branch to location 100. The program will print an error message if any of the input/output bits on the T99128 board in question are not functioning properly. Another method of checking the T99128 board operation is to connect the J-1 connector of one I/O module to the J-1 connector of another module and then transfer bits from one module to the other. If a bad bit is located, another simple program can help isolate the trouble spot. For example, let's assume that bit 35 (hexadecimal) is bad and that the I/O starting address is 100 (hence the actual CRU base address for the bad bit is 100 + 35 * 2=16A hexadecimal). The program shown below will toggle this bit form high to low to high again continously. Simple oscillocope trouble shooting can easily locate the faulty component.

```
        LI R12,bad bit
LOOP    SBO 0
        SBZ 0
        JMP LOOP
```

```
                                TITL '99128 TEST ROUTINE'
0000                            DREG
0100                    BASE    EQU  >100              ; BASE IS THE CRU BASE (BIT*2)
0000 020C 0100                  LI   R12,BASE          ; SET STARTING BASE
0004 1D00               LOOP    SBO  0                 ; SET BIT HIGH
0006 1F00                       TB   0                 ; IS IT HIGH?
0008 1608                       JNE  ERROR             ; NO- ERROR
000A 1E00                       SBZ  0                 ; SET BIT LOW
000C 1F00                       TB   0                 ; IS IT LOW?
000E 1305                       JEQ  ERROR             ; NO-ERROR
0010 05CC                       INCT R12               ; ON TO NEXT BIT
0012 028C 0200                  CI   R12,BASE+>100     ; FINISHED?
0016 1AF6                       JL   LOOP
0018 2C00                       XOP  0,0               ; FINISHED- BACK TO MONITOR
                        *
                        * PRINT ERROR MESSAGE AND RETURN TO MONITOR
                        *
001A 0201 0028          ERROR   LI   R1,MESS
001E 2C91               PRNT    OUT  *R1               ; OUTPUT A CHARACTER
0020 0581                       INC  R1                ; ON TO NEXT
0022 D011                       MOVB *R1,R0
0024 16FC                       JNE  PRNT
0026 2C00                       XOP  0,0
0028 0D0A               MESS    DATA >0D0A
002A 4552 524F                  TEXT 'ERROR- CHECK R12 FOR BIT NO. TIMES 2'
002E 522D 2043
0032 4845 434B
0036 2052 3132
003A 2046 4F52
003E 2042 4954
0042 204E 4F2E
0046 2054 494D
004A 4553 2032
004E 00                         BYTE 0
0050                            END
```

```
 0100 BASE     001A ERROR    0004 LOOP     0028 MESS     001E PRNT
 0000 R0       0001 R1      *000A R10     *000B R11      000C R12
*000D R13     *000E R14     *000F R15     *0002 R2      *0003 R3
*0004 R4      *0005 R5      *0006 R6      *0007 R7      *0008 R8
*0009 R9
EDIT/ASM/LOAD?
```