THE LITTON DUAL L-304
COMPUTER SYSTEM

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THE LITTON DUAL L-304
COMPUTER SYSTEM

26 September 1966

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

THE LITTON DUAL L-304 COMPUTER SYSTEM

I. INTRODUCTION

In the early spring of 1967 flight tests will be initiated on the most powerful stored-program computing system yet to be developed for an airborne application. Included in the system are dual L-304F* processors, 40,960 32-bit words of random access memory (with space and wiring for an additional 40,960 words) a magnetic tape unit, a special control unit and control panel, and the interface units required to communicate with 3 CRT display and control consoles, a radar computer-detector, 2 digital data links and the aircraft's navigation system. The application is an airborne command and control system.

The complete computer and interface system occupies less than 12 cubic feet and weighs approximately 500 pounds. Maximum use is made of monolithic integrated circuits and the latest packaging techniques. The heart of the system is a dual L-304F computer which is now in production. It is the first production model of a series of microelectronic computers being developed by the Litton Data Systems Division.

Litton's L-304 computer resulted from the Data Systems Division's 9-year involvement in the development of tactical data systems. These systems utilize multiple special-purpose computers which share large-capacity drum memories. When these systems were developed, general-purpose computers capable of the required high-capacity real-time processing, could not be packaged within the size, weight, power and environmental constraints of these airborne and helicopter transportable systems.

In 1961, Litton received a contract to examine the feasibility of applying microelectronics in the production version of the airborne system in order to reduce weight and improve reliability. The ground rule was that 3- by 3-inch discrete component circuit cards be replaced on a fit-form-function basis by cards containing microcircuits. The new cards had to be directly interchangeable with the old and be compatible with the same automatic test equipment. Further, the new cards could be no more expensive than the old.

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*The term L-304 is the generic name for the computer. The letter suffix refers to a particular configuration of drawers used in a particular computer system.

The investigation proved so successful that in 1963 Litton began to incorporate several types of cards into new production systems and retrofit into existing systems. The resultant increase in reliability was from 4 to 10 times over the old cards and cost was actually reduced.

With this experience as a background, Litton began in 1963 the design of a general-purpose computer which would contain all the capability and features required of a real-time tactical data processor. These features included high-speed raw execution, high input/output speeds, multiple program and multiple processor capability, the ability to handle many input/output units and the ability to grow from a very small to a very large system.

Circuits, it was determined, should be monolithic integrated, wherever possible, and packaging should take full advantage of the extreme packing density achievable with MICs. It was also determined that ancillary elements should match the computer in size, weight, power consumption and reliability, if the full benefits of a microelectronic computer were to be realized.

Further, it was recognized that a single computer would no more satisfy the broad range of requirements in the military world than one would in the commercial world. Therefore, a broadly ranging family of computers was conceived. The family would make extensive use of the same or similar components and modules, retain program compatibility and provide a range of arithmetic and speed capabilities.

In April of 1965, an L-304E with 4096 words of memory was completed and put in operation. Very shortly thereafter, the computer was tied to a typewriter, paper tape reader and punch, a small magnetic tape, a real-time clock and a small CRT display and control console. The computer, memory and power supply system occupied 0.3 cubic foot and weighed 34 pounds. Several demonstration programs were written and debugged, and in September of 1965 the entire complex of equipment began a series of demonstrations covering most of the United States and parts of Canada. More than 100 demonstrations were given during the subsequent 5 months in 17 different cities. The equipment was packed and unpacked about 35 times and covered 50,000 miles, generally as baggage on commercial airliners.

In August of 1965, partially as a result of having demonstrated an operating microelectronic computer, Litton received the contract to design a command and control system based on the L-304 design.

II.   FUNCTIONAL CHARACTERISTICS

Design ground rules for the L-304 computer were based upon its anticipated use in command and control systems. Word length, operand length, instruction repertoire, addressing modes, index register-accumulator organization and multiprogram capability were all designed as a result of extensive sample programming of these applications. The computer's expandability and multiprocessor arrangement with fail softly modes were incorporated as a result of extensive study of the systems environments in which the computers were expected to be used. Litton's goal was a powerful, easy to program processor which did not push the state of the hardware art, but which achieved its high throughput capability by means of advanced computer organization. It was anticipated that when the computer went into the field it would be accompanied by completely debugged operational programs and that, for the most part, all real-time programs would be held in core. Finally, the computer was to be extremely reliable and as small as possible.

The general characteristics of the design are:

o   Parallel, binary operation

o   32-bit instruction word

o   32-bit memory word

o   2's complement arithmetic

o   16-bit arithmetic (32-bit for some operations)

o   63 basic instructions

o   8 addressing modes

o   64 program levels

o   8 multipurpose process registers per program level (512 total, usable as accumulators or index registers)

o   Accommodation of up to 64 input/output devices

o   Coincident-current, random-access memory using wide-temperature cores, 1.88 microseconds cycle

o   Multiprocessor capability

Figure 1 is a general block diagram of the L-304 and Table I is a summary of the L-304 instruction list including instruction execution times for the direct addressing mode.
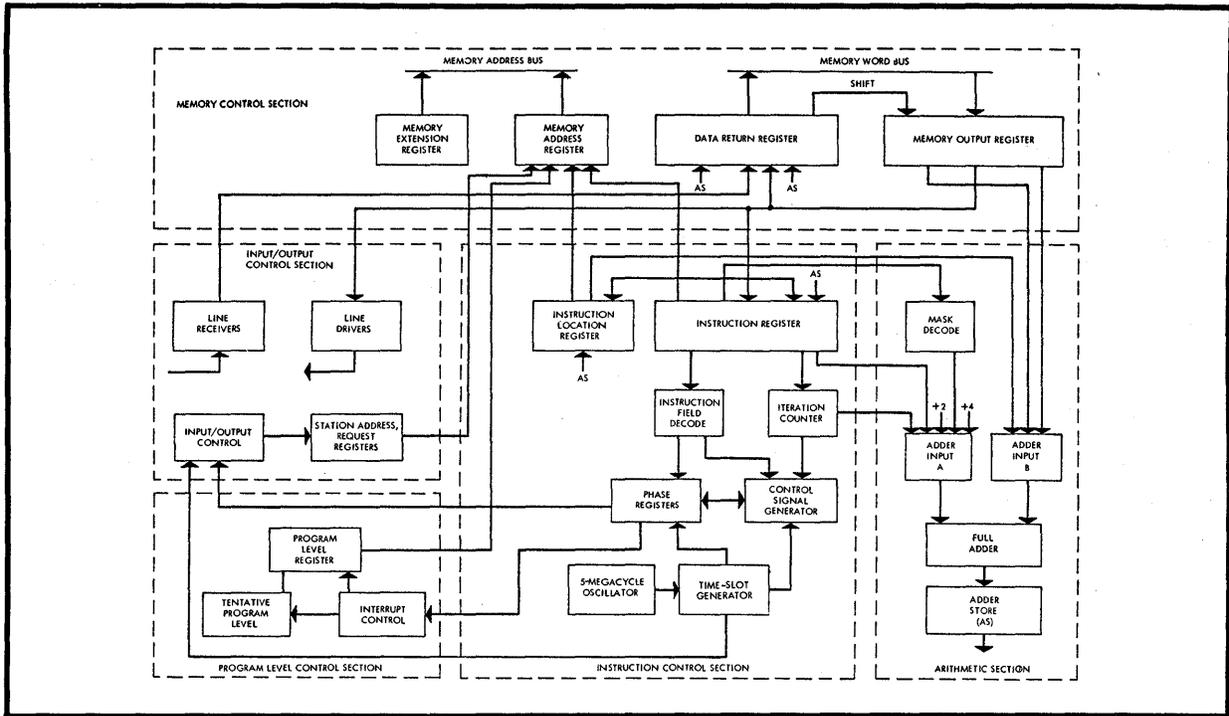
3

Figure 1.   Computer Block Diagram   972-1

INSTRUCTION	EXECUTION TIME*		INSTRUCTION	EXECUTION TIME*	
	OVERLAP	NO OVERLAP		OVERLAP	NO OVERLAP
HALT	4.4	4.4	XFER UNCONDITIONAL, STORE LINK	5.8	6.4
EXECUTE	3.6	4.2	XFER CONSOLE SWITCH	4.4	4.4
EXCHANGE	8.8	8.8	JUMP 3 WAYS	7.4	7.4
EXCHANGE DOUBLE	8.8	9.4	XFER IF H = 0	5.8	6.4
LOAD H	6.6	6.6	XFER IF H $\neq$ 0	5.8	6.4
STORE H	6.6	6.6	XFER IF H NEGATIVE	5.8	6.4
LOAD DOUBLE	5.8	6.4	XFER IF H POSITIVE	5.8	6.4
STORE DOUBLE	5.8	6.4	SHIFT LONG LEFT	$6.0 + 0.8n$	$7.6 + 0.8n$
ADD	6.6	7.2	NORMALIZE LONG LEFT	$9.2 + 0.8n$	$10.6 + 0.8n$
SUBTRACT	6.6	7.2	SHIFT AND COUNT	$6.8 + 0.8n$	$8.4 + 0.8n$
REPLACE ADD	7.4	7.4	REFLECT	$6.8 + 0.8n$	$7.6 + 0.8n$
REPLACE SUBTRACT	7.4	7.4	COMPARE, JUMP IF LESS	6.6	7.2
ADD ABSOLUTE	6.6	7.2	COMPARE, JUMP IF EQUAL	6.6	7.2
SUBTRACT ABSOLUTE	6.6	7.2	COMPARE, JUMP IF UNEQUAL	6.6	7.2
LOAD ABSOLUTE	6.6	7.2	COMPARE, JUMP IF GREATER	6.6	7.2
LOAD COMPLEMENT	6.6	7.2	GATED COMPARE, JUMP IF INSIDE	8.8	9.4
EXCLUSIVE OR	6.6	7.2	GATED COMPARE, JUMP IF OUTSIDE	8.8	9.4
INCLUSIVE OR	6.6	7.2	SHIFT LONG RIGHT, LOGICAL	$6.0 + 0.8n$	$7.6 + 0.8n$
LOGICAL AND	6.6	7.2	SHIFT LONG RIGHT, ALGEBRAIC	$6.0 + 0.8n$	$7.6 + 0.8n$
MEMORY BANK DESIGNATOR	4.4	4.4	SET LOWER BIT	5.2	5.2
MEMORY BASE DESIGNATOR	4.4	4.4	SET UPPER BIT	5.2	5.2
REPLACE EXCLUSIVE OR	7.4	7.4	RESET LOWER BIT	5.2	5.2
REPLACE INCLUSIVE OR	7.4	7.4	RESET UPPER BIT	5.2	5.2
REPLACE AND	7.4	7.4	TEST LOWER BIT, JUMP IF 0	5.2	5.2
MEMORY BANK ASSIGNMENT	4.4	4.4	TEST UPPER BIT, JUMP IF 0	5.2	5.2
MULTIPLY	30.0	31.6	TEST LOWER BIT, JUMP IF 1	5.2	5.2
DIVIDE	32.4	33.2	TEST UPPER BIT, JUMP IF 1	5.2	5.2
DECREMENT H BY 2	6.6	7.2	MOVE RIGHT AND ZERO	$6.6 + 0.8n$	$6.6 + 0.8n$
INCREMENT H BY 2	6.6	7.2	MOVE LEFT AND ZERO	$6.6 + 0.8n$	$6.6 + 0.8n$
DECREMENT H BY 1	6.6	7.2	MOVE RIGHT AND INSERT	$7.4 + 0.8n$	$7.4 + 0.8n$
INCREMENT H BY 1	6.6	7.2	MOVE LEFT AND INSERT	$7.4 + 0.8n$	$7.4 + 0.8n$
XFER, UNCONDITIONAL	4.4	4.4	STORE ALL ZEROS	4.4	4.4
NO OP	2.2	2.2	EXTERNAL DEVICE COMMAND	6.8	6.8
INPUT TO REGISTER	6.6	7.2	EXTERNAL DEVICE AND SUICIDE	7.4	8.0
OUTPUT FROM REGISTER	6.6	7.2			

*OVERLAP GENERALLY OCCURS WHEN THERE IS MORE THAN ONE
MEMORY MODULE IN THE SYSTEM.

Table I.   Computer Instruction List   976-250
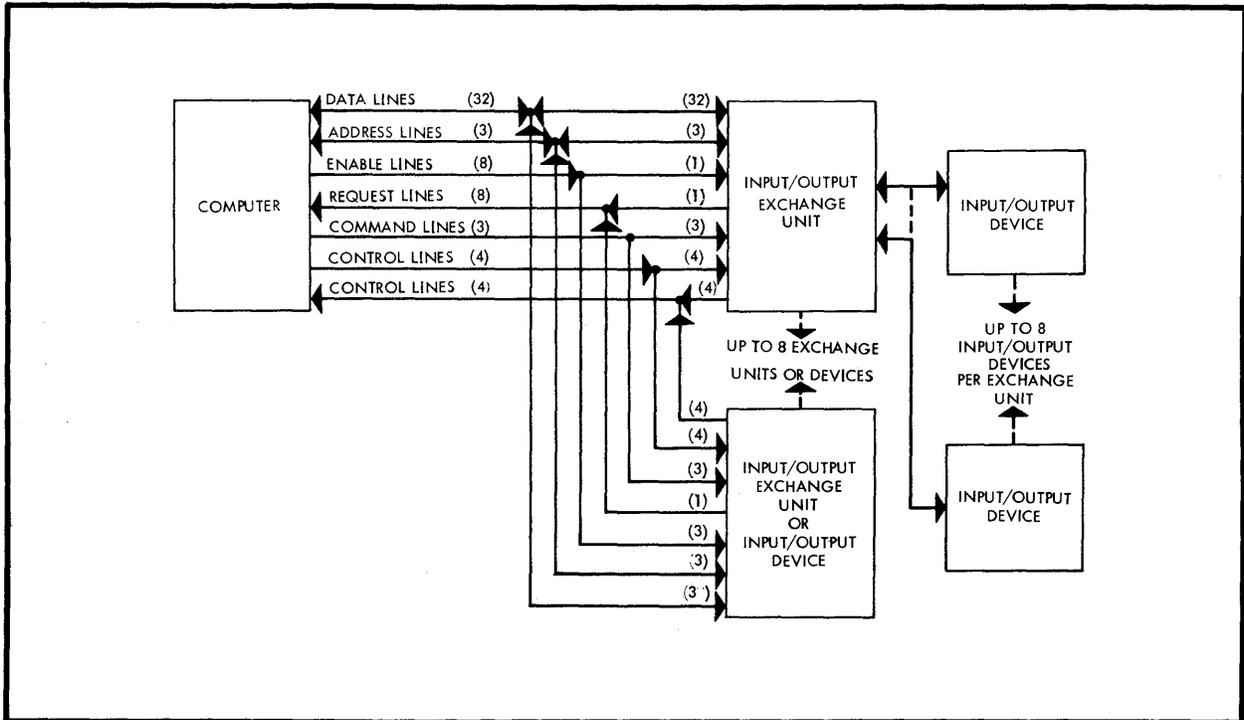
4

Figure 2. Computer Input/Output Organization   652-4

The input/output system of the L-304 computer can communicate with as many
as 64 input/output devices (Figure 2). Eight of these devices can be accessed directly
by the computer. If more than eight devices are required in the system, these can
be communicated with by the addition of input/output exchange logic. The addition
of this logic does not change the basic computer modules. Input/output transfer rates
can be as high as 435,000 32-bit words or 8-bit characters per second.

Of particular interest in the organization of the computer are the multipurpose
process registers, the multiprogram capability, the extended memory addressing
system, and the dual processor organization.

Eight 16-bit process registers are provided for each program level to be
used either as accumulators or index registers. As indicated in the instruction for-
mat (Figure 3), H indicates which of the registers is to be used as an accumulator
and S, which is to be used as an index register. This dual usage of the registers
greatly increases the flexibility with which index registers can be used, reduces the
amount of data shuffling required among accumulators, index registers and memory,
and coupled with the 8 addressing modes, makes the computer particularly efficient
in data manipulation and table look-up operations.
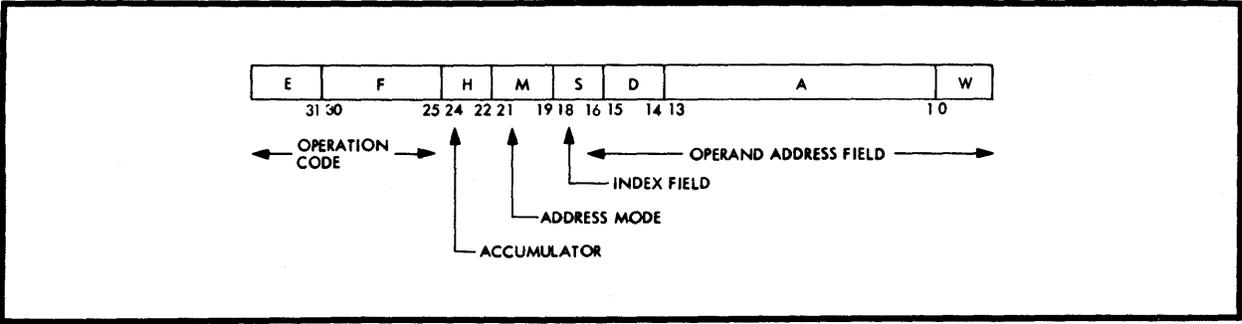
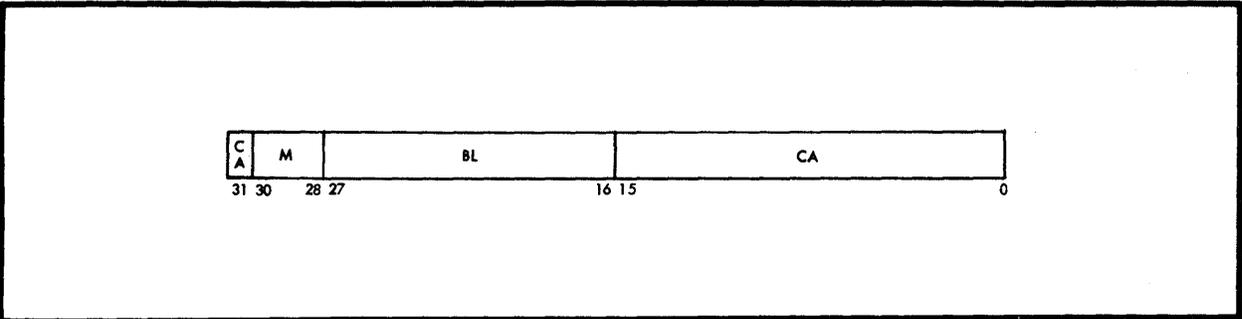Figure 3. Instruction Word Format   976-213

Figure 4. Input/Output Key Word Format   806-7

Each of the 64 program levels in the L-304 has its own set of process regis-
ters. Because of this, each program can be written as if it were the only program
in the computer, aside from memory limitations. Once the programs have been
written, assembled, and assigned priorities, the hardware keeps track of the pro-
grams running and waiting to run, handles interrupts and saves the status of all in-
terrupted programs. The time required to verify the priority of an interrupting pro-
gram, save the status of the interrupted program and enter the new program is less
than 10 microseconds. New programs can be entered under program control as the
result of an input or output operation, an external interrupt or an elapsed time indi-
cator. Interrupts can be inhibited by programmed reset of any of the 64 inhibit bits.

The logic permits control of up to 64 input/output devices all operating simul-
taneously with a maximum combined transfer rate of 237, 000 32-bit words or 8-bit
characters per second. Devices capable of higher transfer rates automatically enter
a burst mode in which data can be transferred at up to 435, 000 words per second.
Data transfers are controlled by one of 64 key words (Figure 4). At the conclusion
of a data transfer, either successful or unsuccessful, the key words' corresponding
termination word (Figure 5) is accessed by the hardware and the activity bit of the
appropriate program level is set. A check on the relative priority of the operating
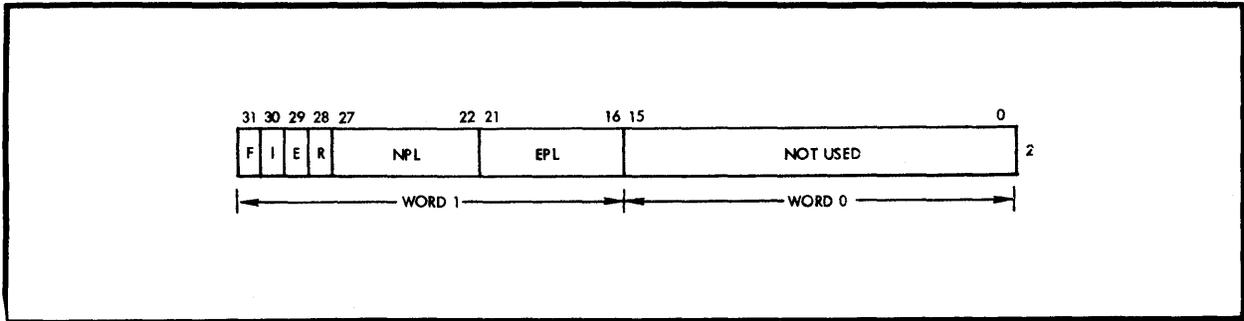program is then made and a program level change takes place, if required.

6

```
31 30 29 28 27        22 21        16 15                    0
┌─┬─┬─┬─┬──────────┬──────────┬───────────────────────┐
│F│I│E│R│   NPL    │   EPL    │       NOT USED        │ 2
└─┴─┴─┴─┴──────────┴──────────┴───────────────────────┘
├──────────────── WORD 1 ────────────┼──────── WORD 0 ───────────┤
```

Figure 5.   Input/Output Termination Word Format   1420-10

        The L-304 approach to addressing 131,072 32-bit words of memory comple-
ments the multiprogram organization of the computer.   Because the operand address
field of the instruction is 16 bits long and addressing is to the half word, a direct ad-
dressing scheme would have permitted addressing only 32,768 32-bit words.   Several
techniques for extended memory addressing were evaluated before selecting the one
which offers the most power and flexibility.   Each of the 64 program levels has as-
sociated with it a 16-bit register, the Memory Extention Register, which is divided
into four 4-bit fields.   By means of this register, the program can select any four
of the up to 16 8K memory modules available to the system, with any combination of
4 modules possible with each program level.   Although the memory bank assignments
can easily be changed by program, experience has verified that 32K of memory is
quite adequate for a program level and that once memory assignments have been made,
they need almost never be changed.

        The 2-bit "D" portion of the operand address field serves to choose the particular
memory module addressed.   This technique therefore allows all of the 8 addressing modes
to be used without restriction regardless of which portion of memory is being addressed.
Each program can therefore be written as if it were being written for a 32K machine.

        The multiprocessor organization of the L-304 results in an extension of the
multiprogram arrangement of the computer.   Each memory module in the system
has the capability of communicating with two computers and the decision logic and
registers required to operate independently of other modules and to resolve conflicts
should both processors attempt to access the module simultaneously.   In most L-304
dual processor systems, both processors will have access to all memory modules so
that either processor can execute any program and have access to any data.

        Assignment of programs to a processor for execution is accomplished by ap-
propriately setting the mask bits in each processor's program priority control reg-
isters.   Programs can be stored anywhere in memory and can be executed by either
processor, regardless of location.   Subroutines are written to be usable by any pro-
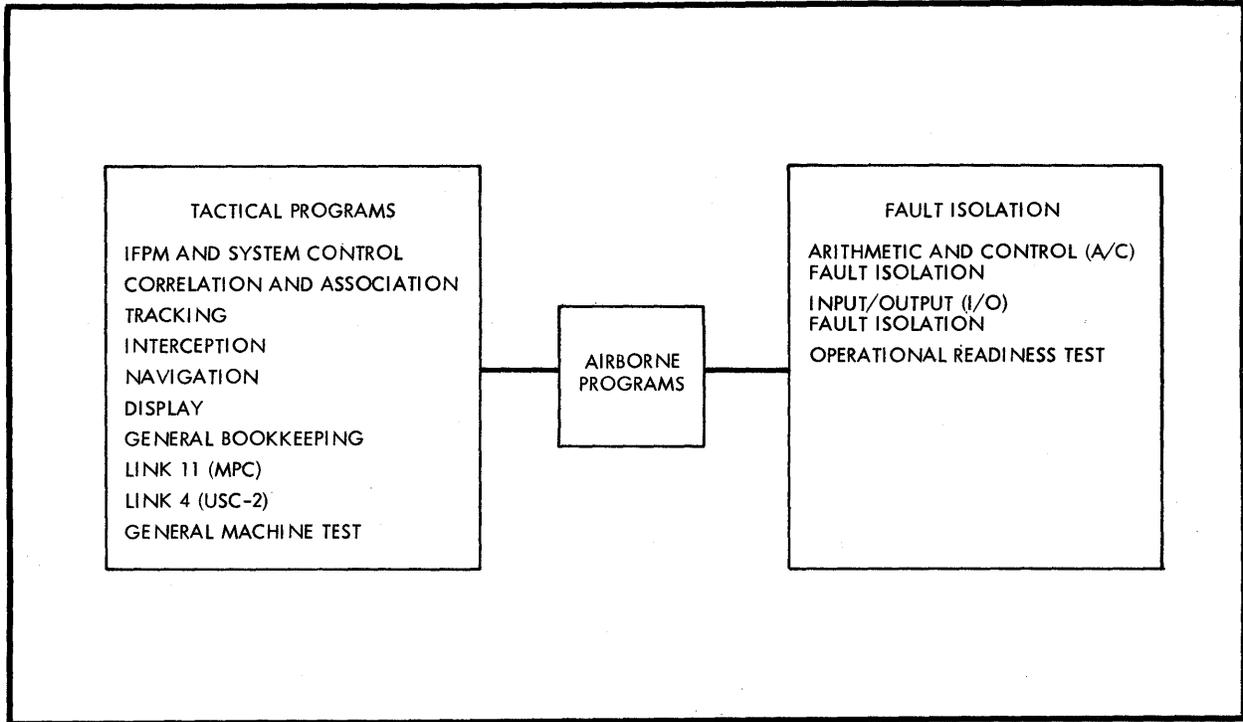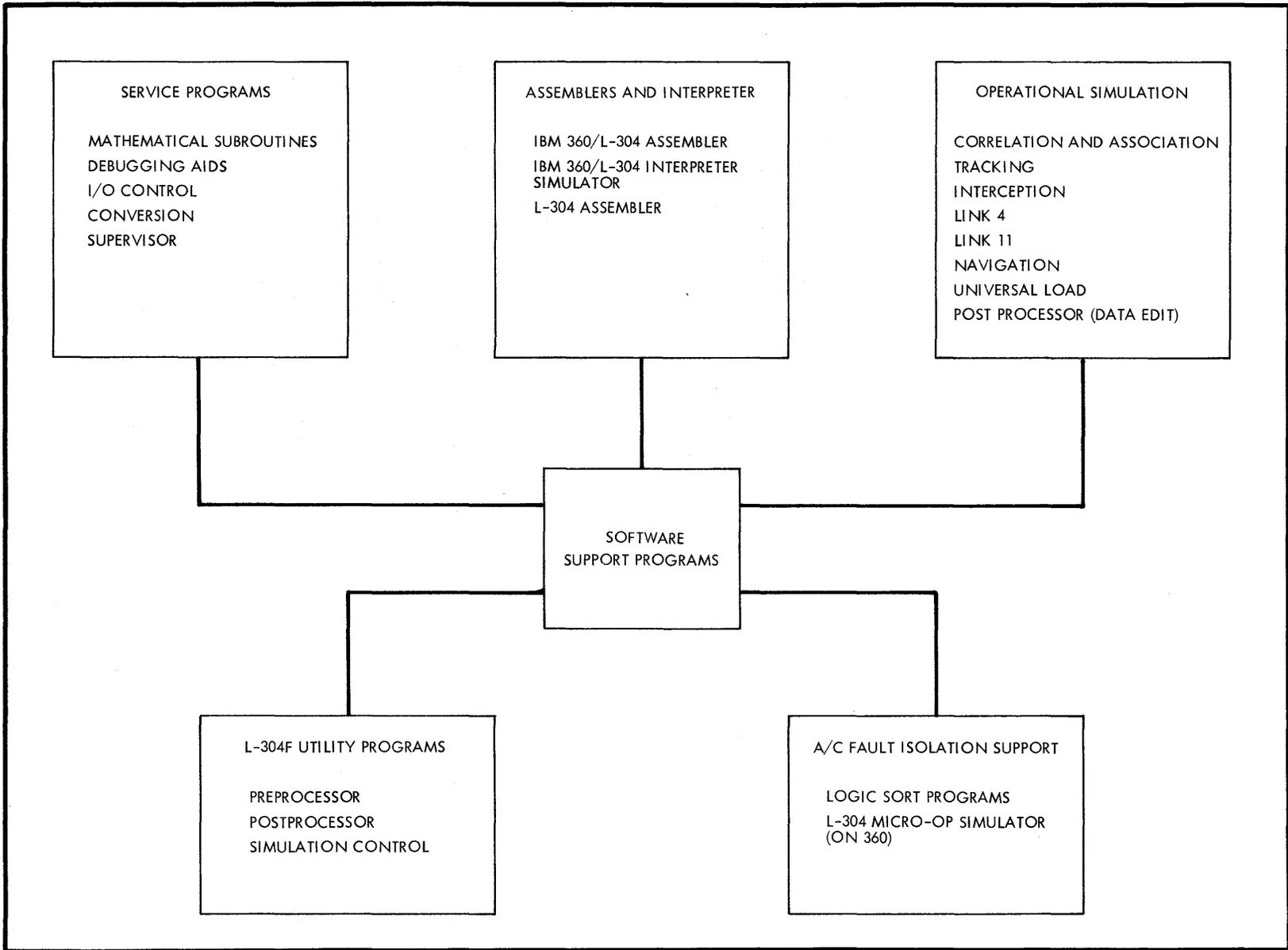gram level of either processor without restriction on interruptions.

7

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┌─────────────────────────────────────────────────────────────────────────────┐
│                                                                             │
│   ┌──────────────────────────────┐           ┌──────────────────────────┐   │
│   │      TACTICAL PROGRAMS        │           │     FAULT ISOLATION       │   │
│   │                              │           │                          │   │
│   │  IFPM AND SYSTEM CONTROL      │           │  ARITHMETIC AND CONTROL (A/C) │
│   │  CORRELATION AND ASSOCIATION  │           │  FAULT ISOLATION          │   │
│   │  TRACKING                    │  ┌────────┐│  INPUT/OUTPUT (I/O)       │   │
│   │  INTERCEPTION                │  │AIRBORNE││  FAULT ISOLATION          │   │
│   │  NAVIGATION                  │──│PROGRAMS│──  OPERATIONAL READINESS TEST│ │
│   │  DISPLAY                     │  └────────┘│                          │   │
│   │  GENERAL BOOKKEEPING          │           │                          │   │
│   │  LINK 11 (MPC)               │           │                          │   │
│   │  LINK 4 (USC-2)              │           │                          │   │
│   │  GENERAL MACHINE TEST         │           │                          │   │
│   └──────────────────────────────┘           └──────────────────────────┘   │
│                                                                             │
└─────────────────────────────────────────────────────────────────────────────┘
```

Figure 6.   Airborne Programs   1466-1

III.   SOFTWARE DEVELOPMENT

Litton Data Systems Division has developed the entire software package for the new airborne system. Because the computer development paralleled the software development, it was necessary to develop programs which would also run on commercially available equipment. Additionally, an entire software package was developed in addition to the operational programs required for airborne use.

The airborne software support and hardware support programs are shown in Figures 6, 7, and 8. The number of instructions and the percent of real time for one processor for the airborne programs is shown in Figures 9 and 10. As it has turned out, the second processor, although used to share the processing load (so that the system percent of real time is actually only a little more than half of the times shown), is actually required only for growth, to reduced probable system downtime and to enhance fault isolation capability.

The ability of Litton to complete this extensive programming task in a minimum period of time can be credited to:

(1)   A well defined problem

(2)   A small but exceptionally capable staff of programmers

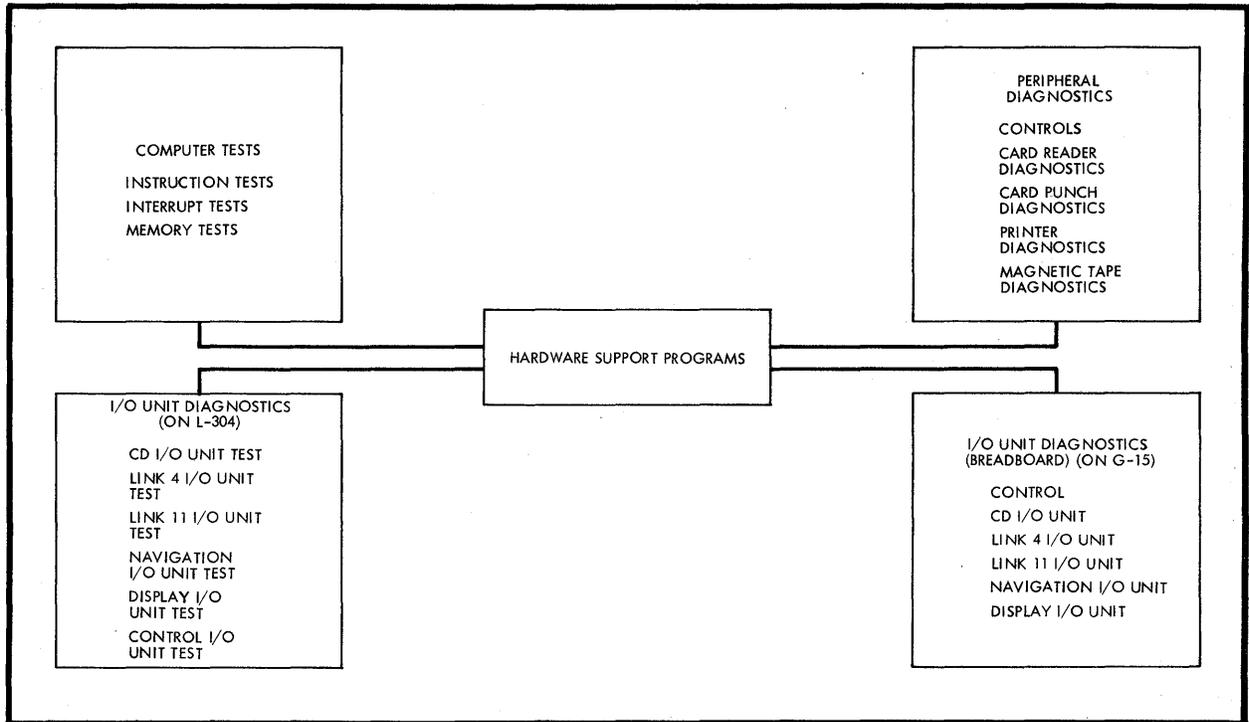(3)   A computer organization which simplified the programming task

8

SERVICE PROGRAMS

MATHEMATICAL SUBROUTINES
DEBUGGING AIDS
I/O CONTROL
CONVERSION
SUPERVISOR

ASSEMBLERS AND INTERPRETER

IBM 360/L-304 ASSEMBLER
IBM 360/L-304 INTERPRETER
SIMULATOR
L-304 ASSEMBLER

OPERATIONAL SIMULATION

CORRELATION AND ASSOCIATION
TRACKING
INTERCEPTION
LINK 4
LINK 11
NAVIGATION
UNIVERSAL LOAD
POST PROCESSOR (DATA EDIT)

SOFTWARE
SUPPORT PROGRAMS

L-304F UTILITY PROGRAMS

PREPROCESSOR
POSTPROCESSOR
SIMULATION CONTROL

A/C FAULT ISOLATION SUPPORT

LOGIC SORT PROGRAMS
L-304 MICRO-OP SIMULATOR
(ON 360)

Figure 7. Software Support Programs

Figure 8.   Hardware Support Programs   1466-3

The simplified programming can primarily be credited to the multiple program levels of the computer which:

(1)   Permitted programs to be broken into small segments, generally 300 instructions or less

(2)   Allowed programmers to proceed independently of one another on their own program segments

(3)   Permitted program segments to be modified without affecting other segments

(4)   Virtually eliminated the need for extensive and complex executive routines to handle interruptions, priority control, and queuing

10

SUPPORT PROGRAMS

SOFTWARE SUPPORT		HARDWARE SUPPORT	
E2A UTILITY PROGRAM	1,300	PERIPHERAL DIAGNOSTICS	1,580
OPERATIONAL SIMULATION	8,730	COMPUTER TESTS	950
SERVICE PROGRAM	6,600	I/O UNIT DIAGNOSTICS (ON L-304)	1,610
ASSEMBLIES AND INTERPRETERS	10,500	I/O UNIT DIAGNOSTICS (ON G-15)	5,350
A/C FAULT ISOLATION SUPPORT	8,400		9,490
	35,530		

AIRBORNE PROGRAMS

	INSTRUCTION	FILES, ETC.	TOTAL
TACTICAL	20,695	14,160	34,855
FAULT ISOLATION	7,400	2,000	9,400

TOTAL INSTRUCTIONS

AIRBORNE	28,095
SUPPORT	45,020
	73,115

Figure 9. Core Storage Estimates (All Programs)   1466-4

	CALCULATED AVERAGE INSTRUCTION EXECUTION TIME	PERCENT REAL TIME (BASED ON CALCULATED AVERAGE)	
		MAXIMUM	AVERAGE
IFPM AND SYSTEM CONTROL	5.0	0.4	0.4
CORRELATION AND ASSOCIATION	7.1	24.4	5.2
TRACKING	8.0	3.5	1.7
INTERCEPTION	7.0	10.9	6.3
NAVIGATION	7.9	9.7	9.7
DISPLAY	7.4	4.4	3.5
GENERAL BOOKKEEPING	6.5	2.8	2.1
LINK 11	7.0	4.9	3.5
LINK 4	6.0	1.6	0.8
GENERAL MACHINE TEST	7.4	4.1	4.1
PROCESSING TOTALS		66.7	37.3
I/O TOTALS		9.9	9.7
GRAND TOTALS		76.6	47.0

ORIGINAL TIME ESTIMATE BASED ON 10-MICROSECOND AVERAGE
INSTRUCTION TIME; CALCULATED AVERAGE INSTRUCTION
EXECUTION TIME IS 7.2 MICROSECONDS

Figure 10. Tactical Program Real-Time Estimates Summary   1466-5

11
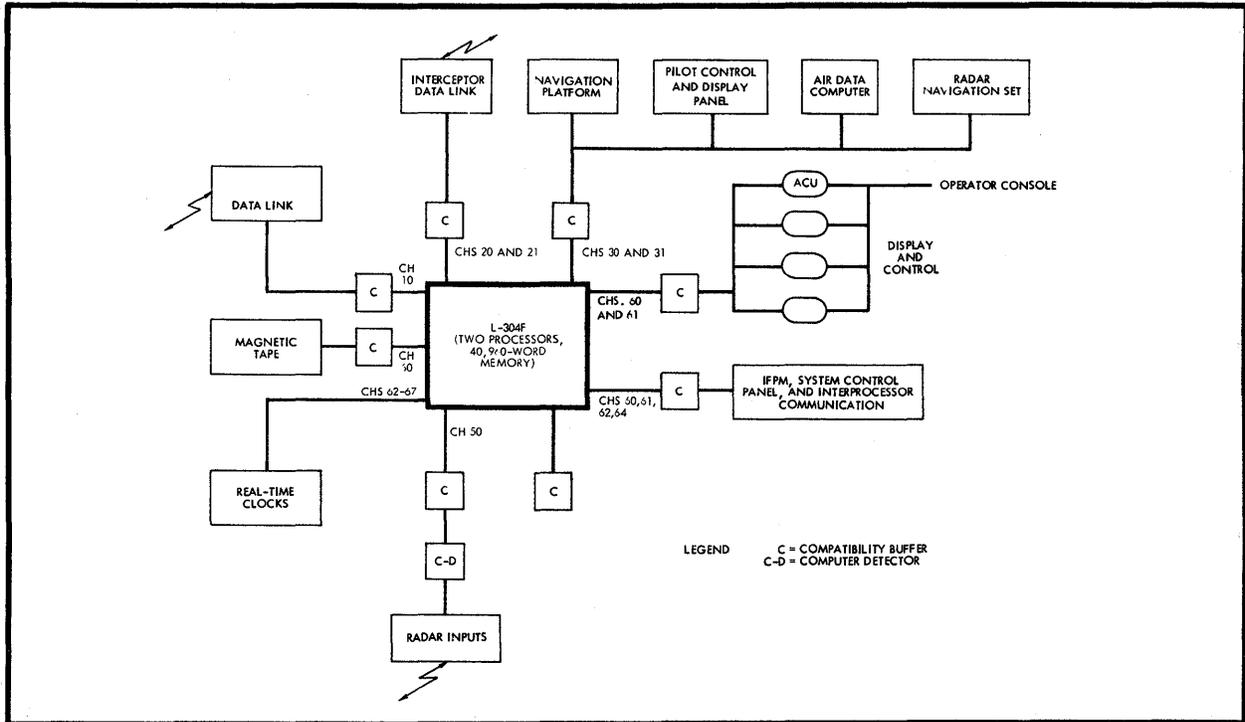
Figure 11. Computer and Related Components   1386-1

The airborne system is an integrated man-machine system the functions of which are the automatic detection, acquisition, identification, and tracking of targets; reporting and display of target information; and control of interceptors (Figures 11 and 12).

The Litton L-304F computer is responsible for:

a. Maintaining within its memory a current and readily accessible digital description of all tracks (orders and track reports)

b. Filtering and correlating data reports on geographical area, track identifier, track-versus-report coordinates, track description, and track quality

c. Servicing all input and output buffers in an optimum manner

d. Satisfying control and display functions as initiated by operator-controlled equipment external to the computer

e. Monitoring and controlling orders

f. Maintaining ownship position via inputs derived from analog navigation devices

12
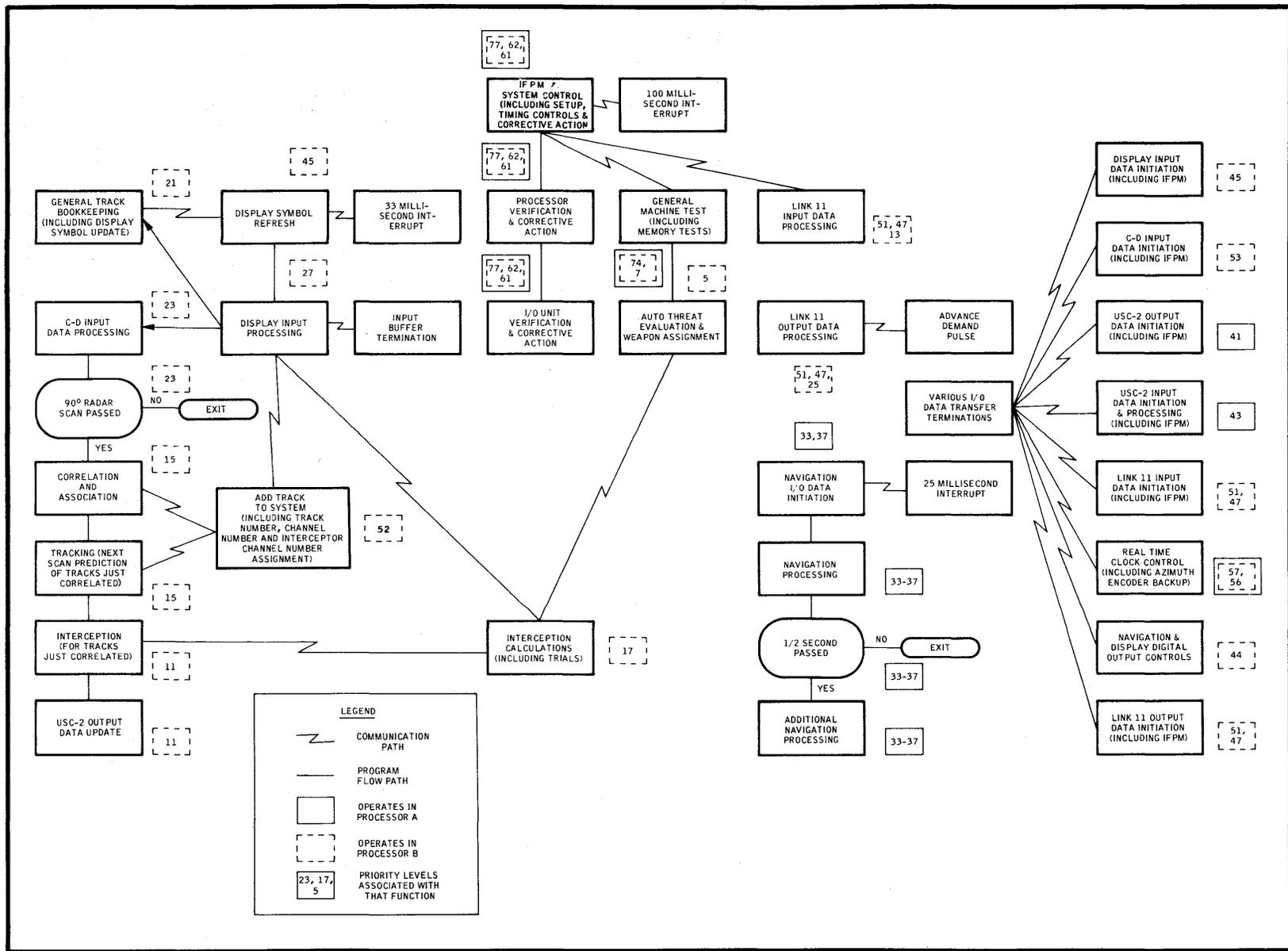
Figure 12. Tactical Program

1386-3

13
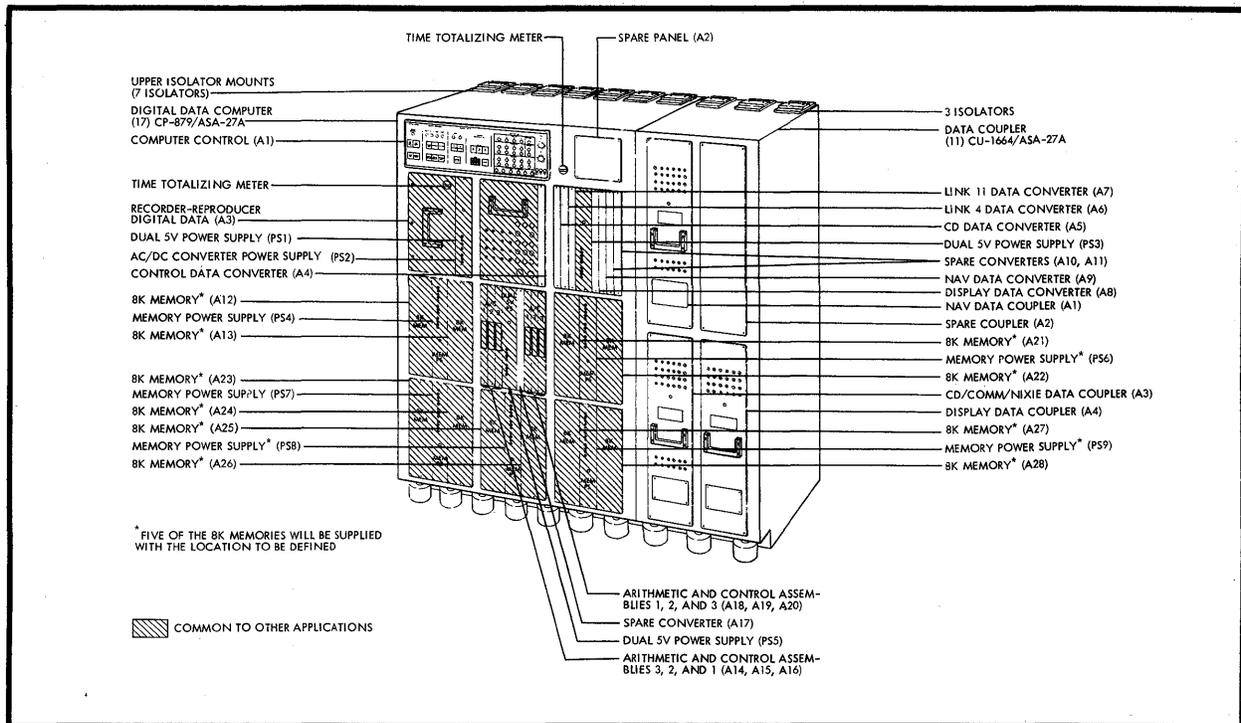
Figure 13. Data Processor Layout   1445-11

g. Controlling select interceptors' flight paths as directed by the console operator

h. Monitoring system performance and performing diagnostic recovery actions

IV. HARDWARE DEVELOPMENT

System and operational support philosophy required that Litton design a processing system comprised of individual replaceable assemblies (drawers) which would be extremely rugged and which could be expected to survive operational deployment of up to six months without failure (Figures 13 and 14). Planned maintenance philosophy is to do no computer module maintenance in the field. All maintenance will be of a depot nature. This requirement was one that Litton had anticipated for all tactical data systems and, though the realization was accomplished only through extensive testing and design verification, it was a natural evolution of the basic Litton L-304 computer design.

The evolution of each major assembly of the L-304F was an iterative process of design, build and test. Using the 8192-word memory drawer as a typical example of this process, one may examine the second step of the development cycle in detail (Figure 15).

14
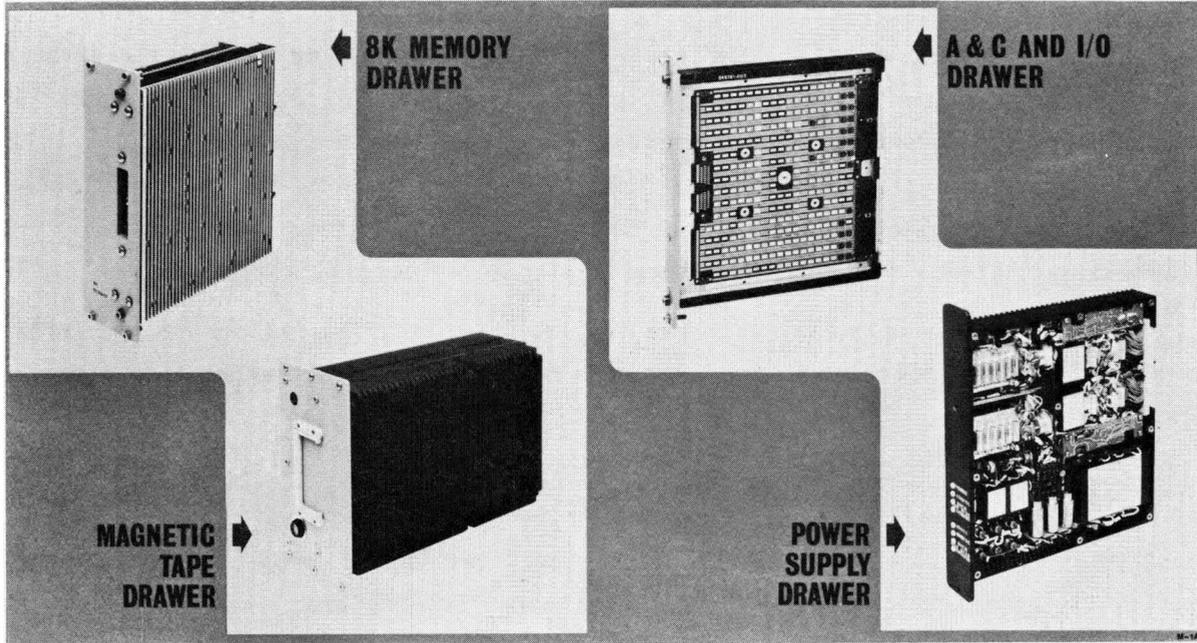
Figure 14. Major Computer Assemblies

U-9629-2
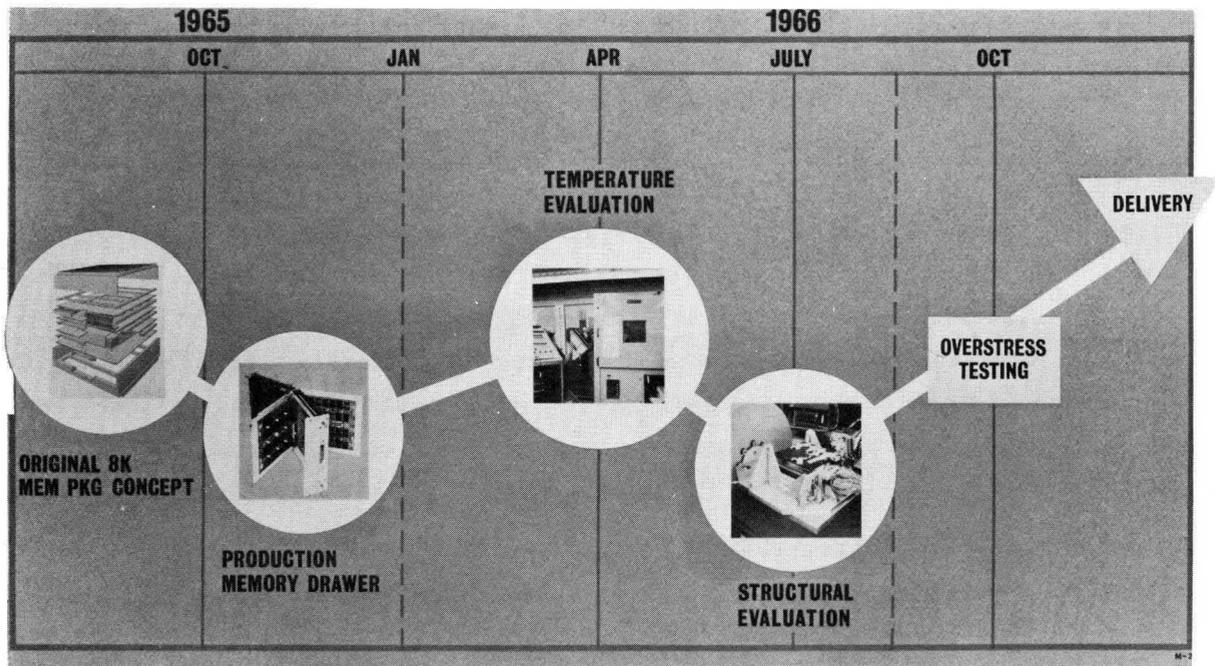
Figure 15. Memory Development Cycle

U-9629-1

15

The memory development cycle started with a packaging concept to extend the 4096-word, 32-bit memory, which was built for the development model L-304E, to 8192-word capacity. Certain deficiencies in this initial package design were noted, and as a result an entirely new concept in memory packaging was hypothesized. This design became a reality only after extensive component testing, dimensional, thermal and structural analysis, culminating in the production memory drawer. Following the fabrication the package design was first subjected to extreme temperature evaluation, then to structural evaluation, and finally to overstress testing.

Parallel with this hardware evaluation, the electrical design was verified through the use of breadboard and prototype models which then joined the hardware development for total memory system verification, prior to the temperature and structural evaluation of the total assembly.

Figure 16 portrays the original memory package concept. At the center of the module is a standard core stack array, packaged with four 64 by 64 core mats to a side, giving a total of eight double-sided mats. The electronics were packaged on multilayer interconnection boards (MLBs) surrounding this array. Interconnections between the MLBs were to be accomplished either with jumper connectors using a ribbon wire, or pressure spring contacts (used on the L-304E model). Heat transfer was accomplished by a grid work of thermal bus bars separating the individual MLBs. This design had three problem areas which were felt to be inadequate solutions to the need for a rugged militarized production memory.

The first was the geometry of the core stack itself. Litton, in conjunction with the Computer Products Division of the Ampex Corporation, ran a series of tests on the standard Ampex array, and found that the basic array geometry was unsuited for the environmental testing of aircraft electronic equipment, MIL-T-5422. The stack and electronics by themselves had no difficulty in passing the test requirements of this specification, but when this assembly was considered part of the total system and that the total system itself must pass the shock and vibration requirements, it was realized that the cabinet structure, at its own resonant frequency, would amplify the input force (10g) and that the memory package itself could expect to see as high as 35g.

Thermal paths were another potential problem. Litton was well aware of the fact that microelectronics are only as reliable as the packaging and in particular, the thermal design allows them to be. Microintegrated circuits operating at rated loads in free space, should not be expected to operate over one hour without failure, whereas
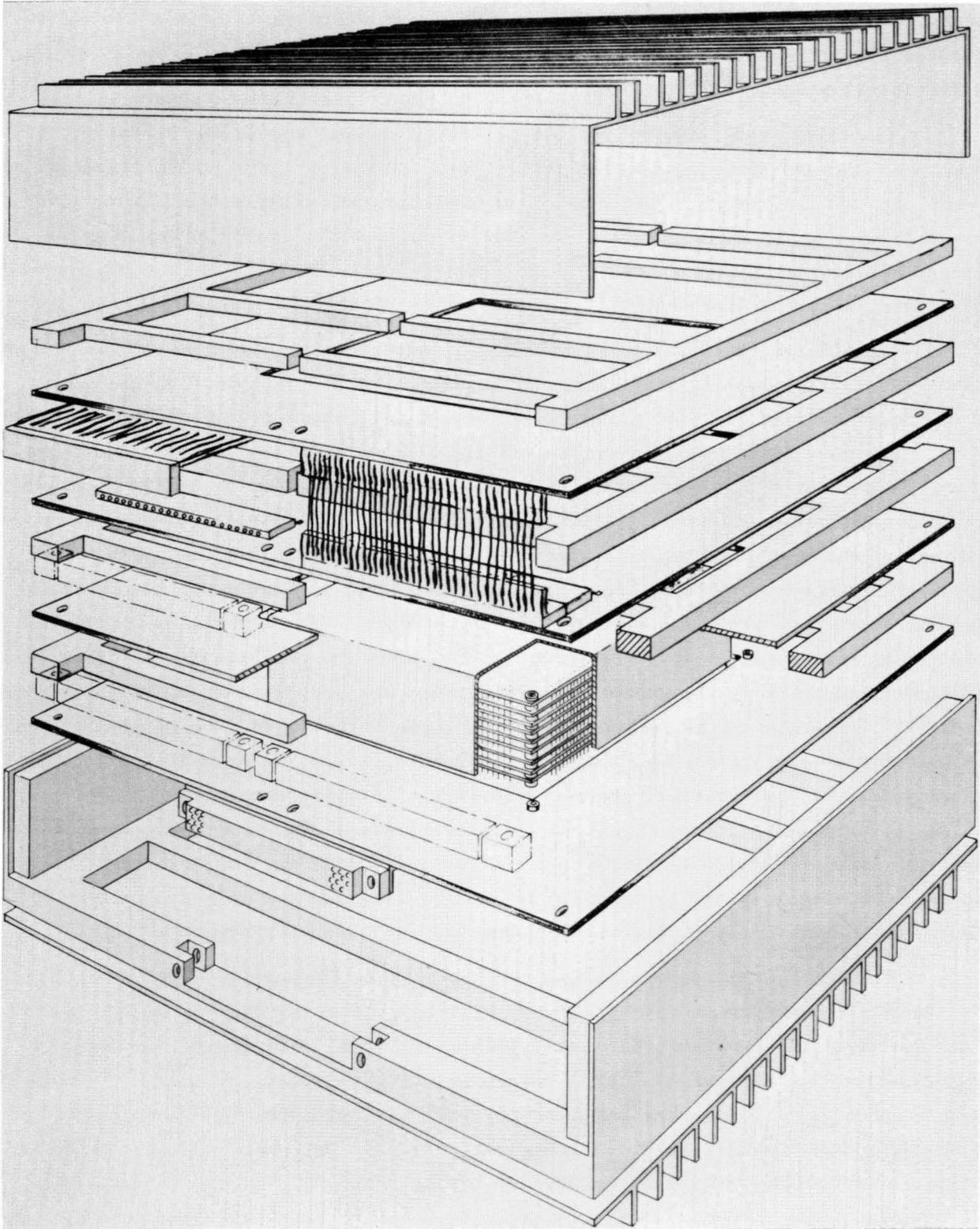
16

Figure 16.   Original Memory Packaging Concept   U-9629-4

if the package ensures that the junction temperature never goes above nominally 80°C, through the use of heat sinks, these same integrated circuits can be expected to operate reasonably for 25 to 50 million hours.

The third problem posed by this packaging concept was one of producibility and, secondarily, effecting depot repair. The total module could not be operated while exposed for probing while in a unit test station, and therefore problems that could develop in the manufacture of the drawer could not be identified while in the closed system environment and could not possibly be duplicated when the module was disassembled for testing.

All of these problems were solved with the production memory drawer design (see Figure 17). Looking at the last problem first, we see that the drawer opens, like a book, without the need for disconnection of any electrical paths between modules. The core stack is shown in its case (the black module in the picture pointing out at 10 o'clock). The electronics is housed in the main structure and is packaged on four multilaminate boards. Attached to both sides of the center web are the boards containing the microelectric circuits. Each of these circuits is bonded with a high grade thermal adhesive to a copper pad on the top layer of the board. Underneath each of these pads are two copper thermal posts which have been plated up from the bottom layer to the top. It is these two thermal posts (by analysis one post would be sufficient but there was space for two) which allow the heat from each integrated circuit to be conducted to the bottom or thermal layer of the board. From here the heat is transferred along the center aluminum web out to the edges of the frame and also through thermal bosses which connect with each of the cover assemblies. The hybrid circuits, the black modules slightly larger than a postage stamp, are also bonded to thermal pads on the boards and the posts under these pads are plated through directly to the fin surfaces of the covers. These circuits dissipate the most heat and were therefore placed on the covers allowing the shortest possible conduction paths.

The total memory core stack assembly (Figure 18) is made up of five boards; the first is a diode board, the second and third are two array boards, each of them having sixteen 64- by 64-bit mats packaged on both sides of the board, the fourth is another diode board, and the fifth is the sense amplifier board. The array boards represent a major innovation in core array design. These boards are made up of an epoxy aluminum laminate holding sixteen 64 by 64 core mats on each side. The aluminum was chosen over the more common copper to add stiffness to the total array without a corresponding penalty in weight and size. Another innovation found in this design is the short center-to-center spacing of the attachment hardware. It was this
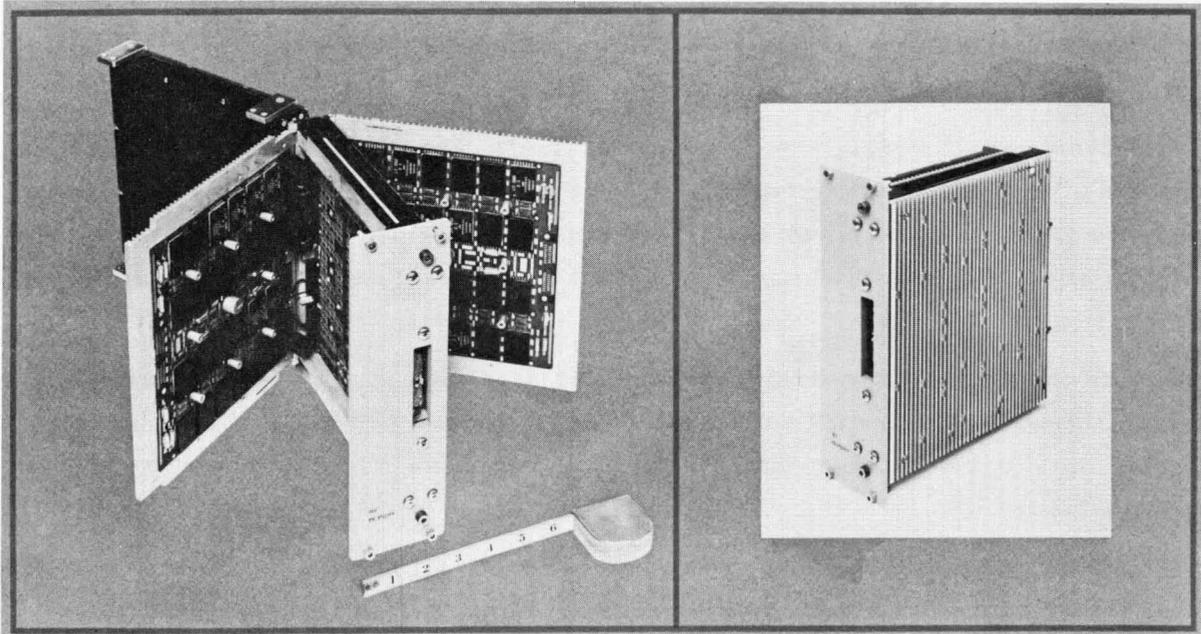
Figure 17.   Production Memory Drawer   U-9629-6
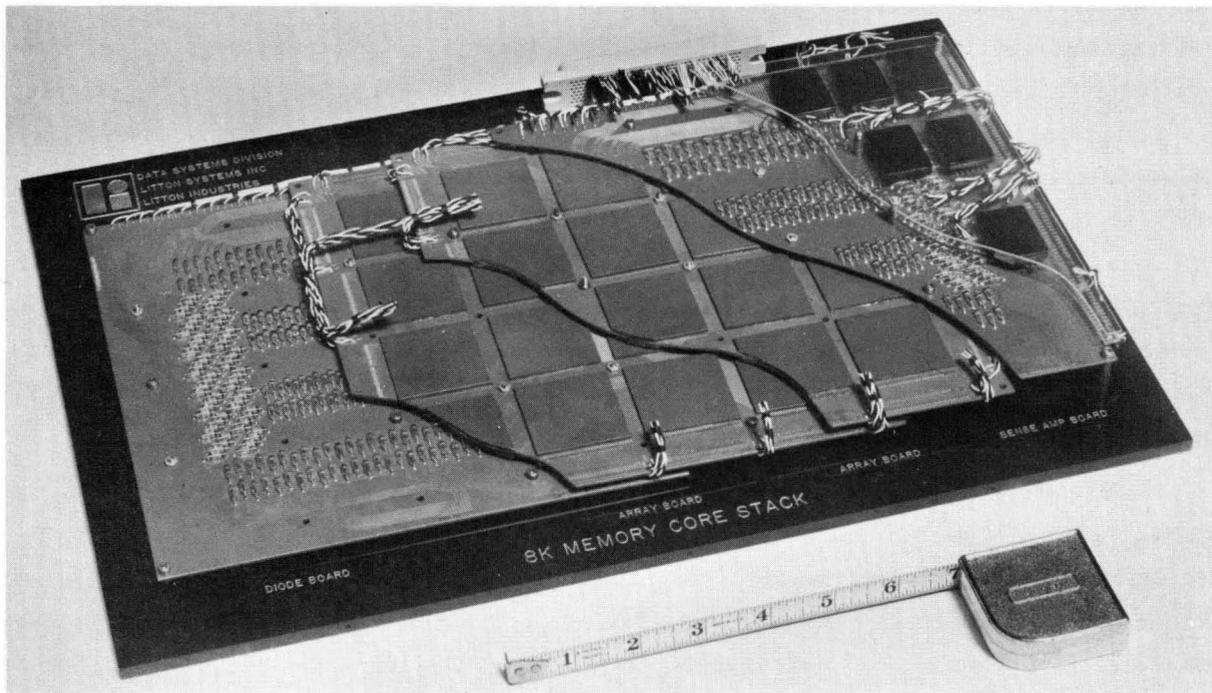

Figure 18.   Exploded 8192-Word Memory Core Stack   U-9630-1

spacing which was identified as being necessary in order that the total stack assembly be able to withstand its potential vibration environment (see Figure 19).

Following the thermal and structural analysis and having completed the electrical design verification, the assembly was then subjected to thermal evaluation (Figure 20). The memory assembly, which is within the chamber, is shown with the memory exerciser which has been developed concurrently with the memory and serves as not only an engineer's evaluation tool but also as the unit test station for production memories.

Following the temperature testing the assembly was then subjected to a vibration analysis. In Figure 20 note that the leads coming directly out of the stack assembly are monitoring signals, that wiring not being present in the normal production assemblies.

The results of this testing are summarized in Figure 21. These first tests have been designed as exploratory in nature and were used to develop confidence limits. From the vibration test, it is interesting to note that the stack's main resonant frequency is 365 Hz. The design goal for this assembly was a resonant frequency between 350 and 400 Hz.

Each of these assemblies has been designed to be as stiff as possible so that their resonant frequencies will be much higher than that of a typical cabinet structure and the cabinets in turn will be designed to resonate at a frequency higher than the prime input frequency of a shock load. By comparison the vibration of an M-35 truck has a fundamental frequency of about four Hz with peak forces of less than 5g. At higher frequencies the amplitude falls off rapidly, so that at 365 Hz the force is so small as to be virtually nonexistent. Similarly, the XM-720 transporter tests show its highest forces transmitted at about 6 Hz and 6g. These also drop off a higher frequencies to insignificant values. In a drop test the computer cabinet will experience a nearly sinusoidal shock peaking at about 18g. The cabinet will be designed to resonate at a frequency near 100 Hz so that it will act as an attenuator at both the fundamental input frequencies and at the resonant frequencies of the modules.

The Arithmetic and Control drawer and each of the Input/Output drawers have generally the characteristics shown in Figure 22. The weight, volume and MTBF are those for a representative drawer fully loaded with microelectronic circuits. The resonant frequency of 294 Hz is also high enough that the unit will see no effect whatsoever from the shock and vibration loads of Type III mobility.
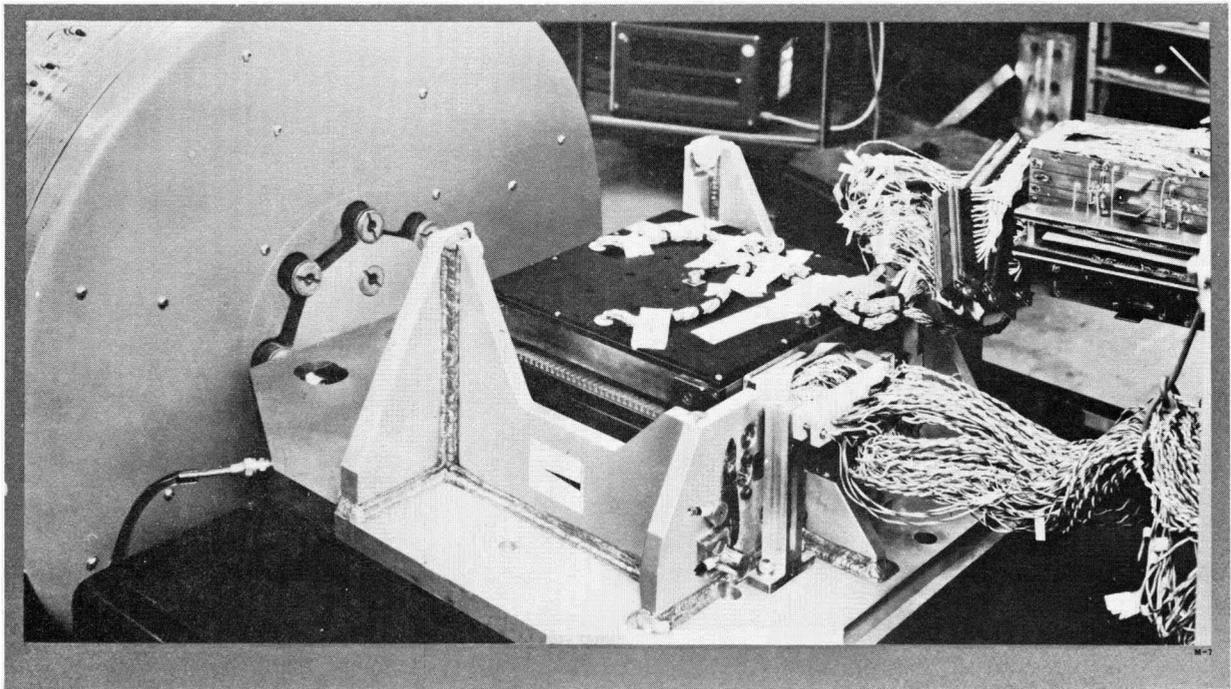
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Figure 19. Memory Module Structural Evaluation   U-9629-5
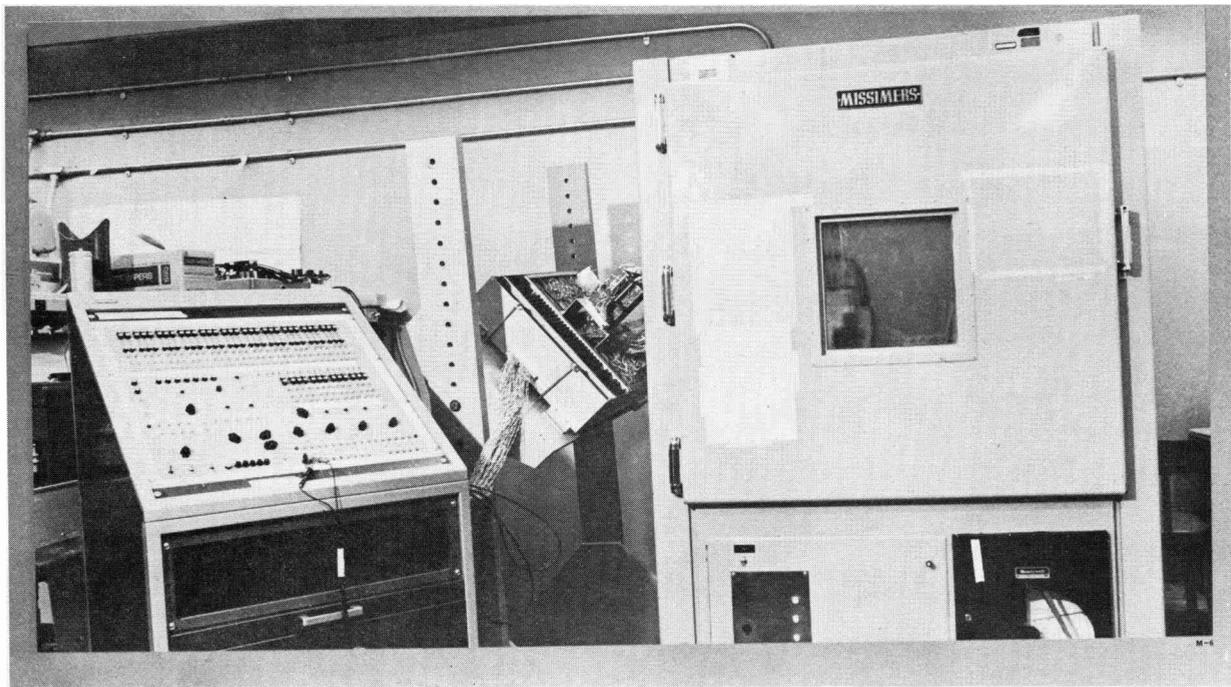

Figure 20. Memory Module Thermal Evaluation   U-9629-7
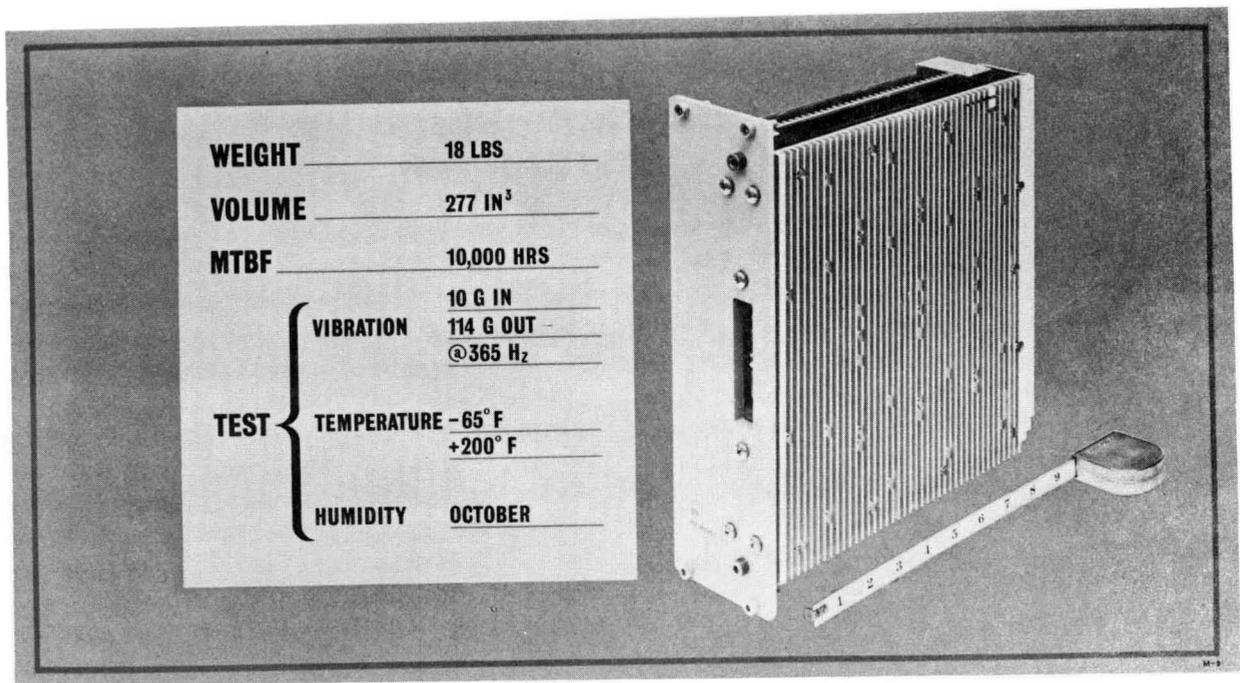
Figure 21. Memory Module Verified Parameters
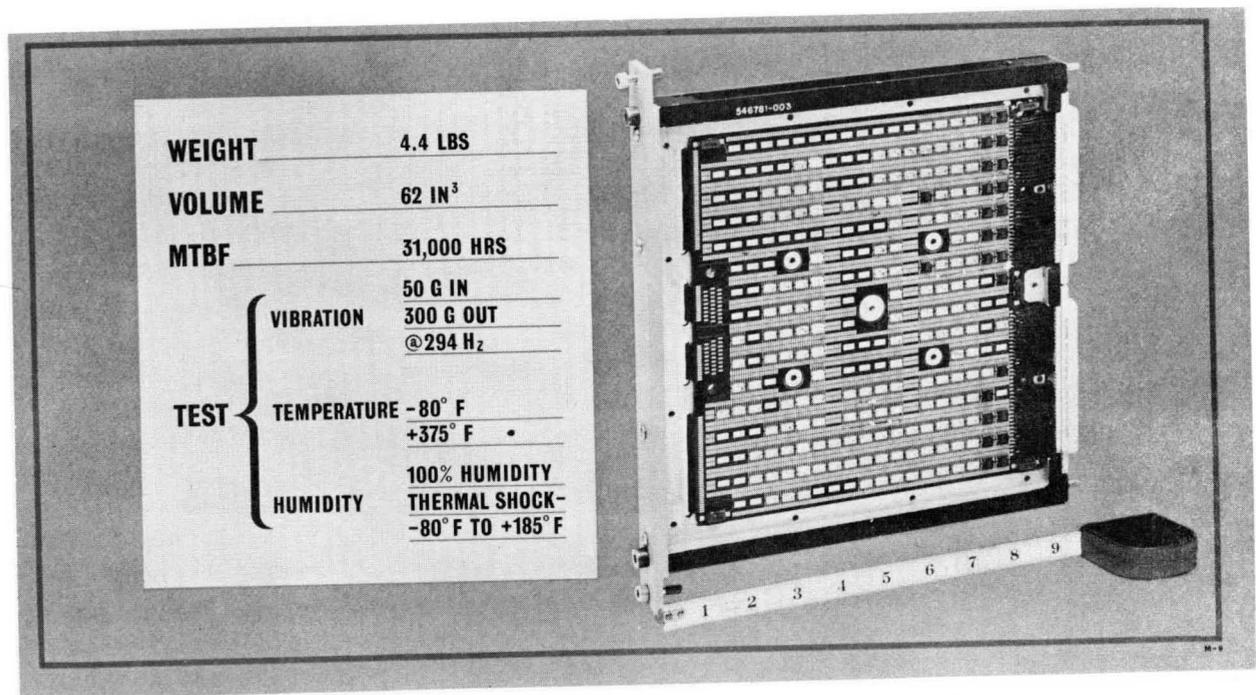
U-9629-6

Figure 22. Arithmetic and Control Module Parameters

U-9629-10

The results of the testing denote the completion of the verification test program. The drawer can withstand a 50g input in its resonant frequency, and it can operate at a temperature extreme of -80°F to +375°F in any humidity condition. Future thermal shock tests are planned to even greater extremes than those shown, since no failures could be induced at the listed limits.

The Magnetic Tape drawer (Figure 23), designed as part of the family of L-304 computing hardware, provides auxiliary data storage, and program storage, for the data processing system. The unit uses half-inch wide, 1-1/2 mil mylar tape. It has a 4.8-inch reel capable of holding 610 feet of tape. The unit can read and write 20 inches per second and is designed for recording at both 800 bytes per inch and 556 bytes per inch; the 556 being a preferred mode for tactical environments. The vibration data shown in Figure 24 is that at the resonant frequency of the assembly. The unit was additionally subjected to a 30g input from 96 to 120 cycles where no resonant frequencies were found. This test was conducted to verify operation in a cabinet where amplifications were imagined at a theoretical cabinet's resonant frequency. The dwell period was one hour without any dropout. Over the frequency range of 10 cycles to 96 cycles the unit was subjected to a constant 0.08-inch double amplitude input, this being done to verify operation when subjected to low frequency forced vibration found in trucks, transporters and aircraft. The MTBF of the Magnetic Tape drawer excludes the tape and assumes periodic maintenance, nominally every 100 hours of operating time.

The Power Supply drawer shown in Figure 25 is the dual 5-volt supply used by the Magnetic Tape Unit and the Arithmetic and Control and Input/Output drawers of the system. The system also requires a special supply for the memory assemblies, which though composed of different electronics, is packaged in the same case (form factor) as the 5-volt supply shown. The figures given represent the worst case of the two supplies; that is, the weight and the MTBF are independently worst case number for this family.

V.   COMPUTER STATUS AND QUALIFICATION

The L-304 computer is currently under contract on three programs. Units are in production and delivery to customers will begin before the end of December 1966. The final step required of the computer development is that it be qualified for the military environments. This is being formally accomplished on the airborne command and control system which will qualify those parts which would be applicable to other L-304 applications. Extensive testing performed before qualification has placed Litton close to its goal of a qualified machine by reducing qualification testing to essentially a demonstration.
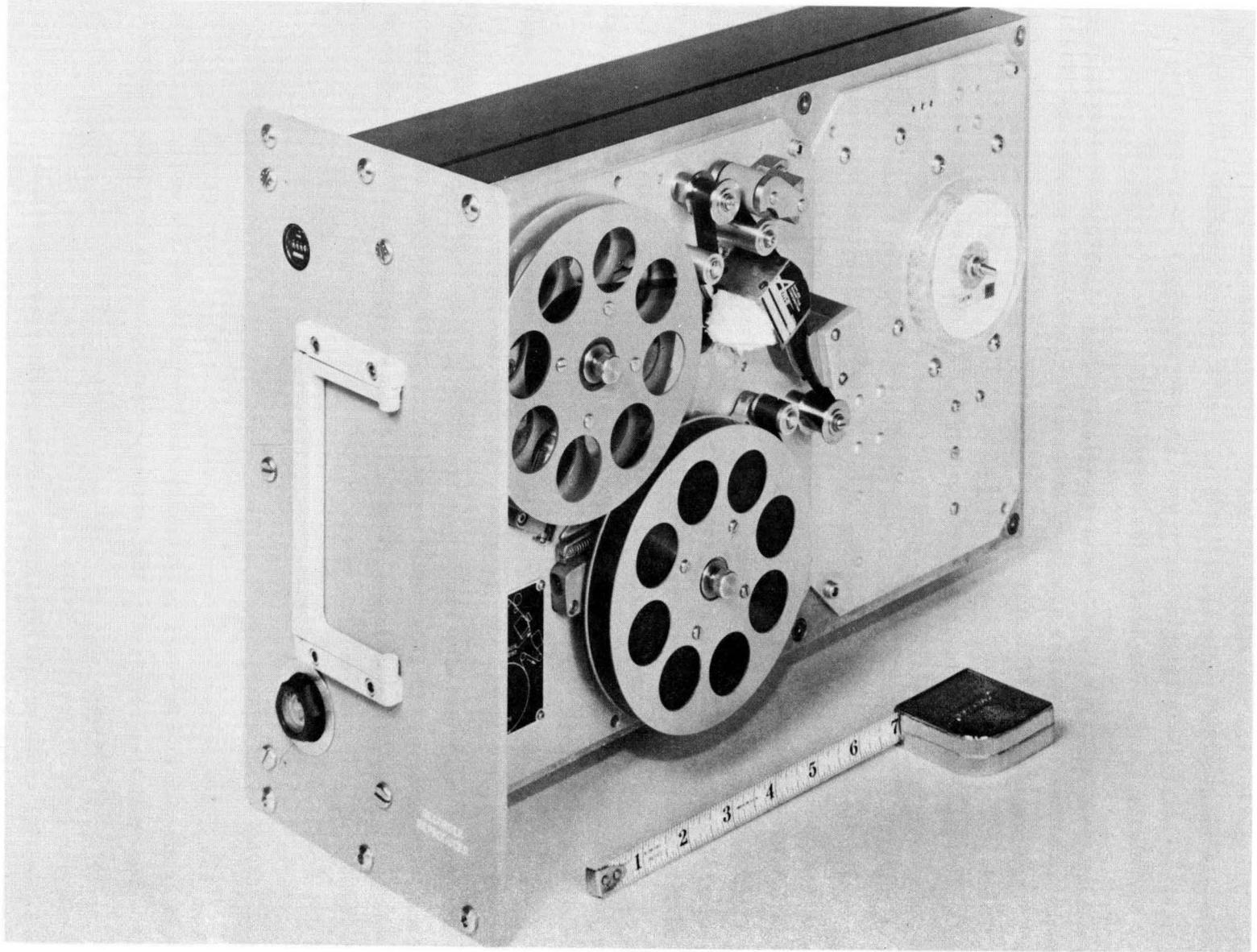
Figure 23.   Magnetic Tape Drawer
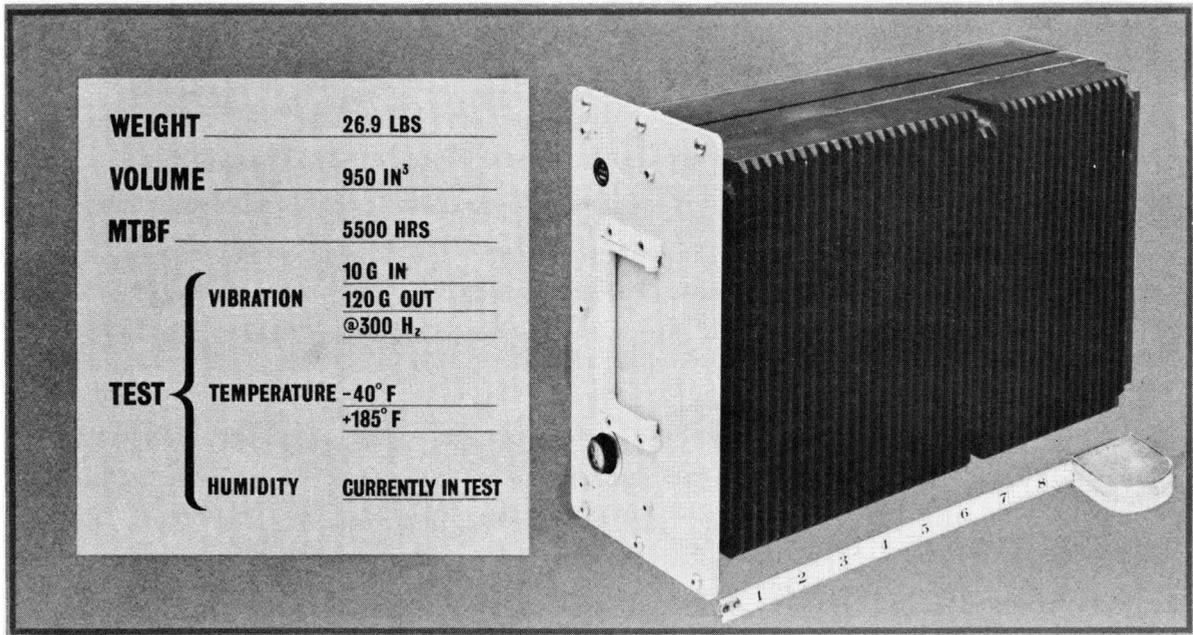
Figure 24. Magnetic Tape Drawer Parameters   U-9629-8
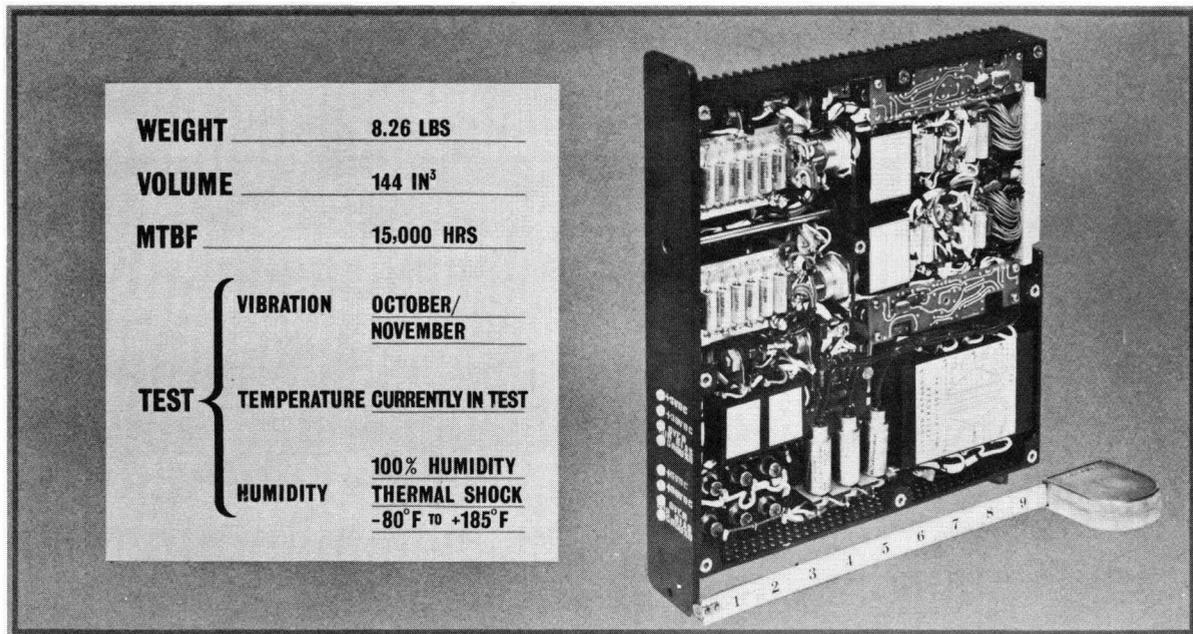

Figure 25. Power Supply Drawer Parameters   U-9629-11

Design verification of each of the assemblies proved conclusively before formal qualification, that the equipment will pass all qualification imposed environments. Litton is proceeding to an overstress testing program on three each of the five production assemblies. First, the components used by the L-304F modules went through an extensive material and process evaluation. The objective of these tests was to evaluate the performance limitations of new and critical components and process under extended equipment operating environments. The results of these tests were then used to identify inherent failure mechanisms and failure modes that could be expected when the equipment is subjected to temperature and vibration overstress environments.

Having completed the component evaluation phase and the verification phase, Litton Data Systems Division has undertaken overstress or step-stress evaluation. It is Litton's contention that most failures being experienced in equipment used by the armed services are not a result of random failure, but the result of basic failure mechanisms present in most equipment. When identified and examined they can be eliminated by relatively minor redesign. The first step in this program is weeding out all components that have inherent weaknesses. Having accomplished this, the next step is to eliminate physical interactions that, though difficult to identify, do cause premature failure, which in the past has been dismissed as merely the inherent reliability of the components and/or article.

Through the use of this overstress testing, Litton is confident that these flaws can be eliminated and that the final assemblies can expect to realize the true reliability potential that is possible with the microelectronic circuit now available to both the manufacturer of military systems, and the users.

The program is well under way — the Arithmetic and Control drawer having completed most of its scheduled test program, with the other assemblies either in process or scheduled for completion by the end of 1966. The method used is to first subject the unit to one variable at a time; i.e., temperature, vibration, voltage, humidity, at stepped increases until failure. Having identified the various mechanisms for the one variable case, the article is then subjected to a composite of these parameters in the hope of identifying, for example, temperature-vibration related and dependent failure mechanisms. The result of this program will be assemblies that can exceed their predicted reliabilities by a factor of three or four without regard for the environment to which they will be knowingly subjected.

Basic design has simplified production testing. Each of the multilaminate boards used in the data processor has identical patterns on the top surface. This has allowed the use of standard loading trays for placing the circuits on the board, standard joining techniques employed for joining the integrated circuit leads to their respective pads, and the use of a specially developed 5000-pin contact fixture which is used to analyze the signal and voltage wiring of these boards in under a minute and a half. By changing test tapes used on the test fixture, any drawer in the system can be verified in this time. The test tapes are machine generated directly from the logic listings for the drawer. This same fixture is used as the unit test station for the drawer assemblies and can verify all circuits and connections also in the minute and one-half time period.

Litton has essentially reached its initial goal of developing a militarized machine which:

(1) Is sufficiently powerful and flexible for complex system applications

(2) Is sufficiently compact and light for airborne applications

(3) Is highly reliable and easily maintainable

(4) Can be produced economically and reliably in volume

(5) Can be readily tested in the factory and in the field