KONELAR

UNIBUS Extended Memory System
RVM128/RVM512 Hardware Manual

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RVM-128/RVM-512 User's Manual

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INTRODUCING THE RVM-128 AND RVM-512

Digital Pathways' Real Virtual Memory is a random access memory module that greatly increases the main memory space of your DEC PDP-11 series computer. Each RVM-128 provides 128K words on a single board while each RVM-512 provides 512K words. In both cases a word consists of 16 data bits plus two parity bits.

Both modules fit into the hex-wide small peripheral controller slots of the UNIBUS backplanes in all PDP-11 computers from the model 04 through the model 70. Furthermore, each module draws only 5 volts DC and therefore requires no additional power supplies (even in early PDP-11 configurations).

The RVM modules employ a bank-switching scheme that makes it possible for you to add a virtually unlimited number of RVM-128 and/or RVM-512 modules to your PDP-11. By changing four jumper settings and replacing the dynamic RAM chips, you can easily upgrade an RVM-128 to an RVM-512. This manual describes the installation and use of RVM modules.

BANK-SWITCHING

Before installing the RVM-128, you should understand its bank-switching technique. Standard DEC PDP-11 computers use eighteen address lines to reference 128K words of memory (256K bytes). Since the topmost 4K words of address space are reserved for peripherals, only 124K words of memory are available for data storage. In fact, early PDP-11s use only sixteen of eighteen address lines and therefore have only 28K words of memory available for data. The RVM-128 considers the 128K word address space to be logically divided into 64 sectors of 2K words each (see figure 1). Similarly, the physical memory of each RVM-128 memory board is logically divided into blocks, also 2K words each in size. There are 64 blocks on an RVM-128, 256 on an RVM-512. Special hardware on the RVM-128 board associates each of the 64 sectors of address space with a single physical block of memory. In this way, blocks of memory can be dynamically assigned to respond to different address ranges.

SECTOR NUMBER	ADDESS RANGE OF SECTOR	OFFSET FROM BASE OF SAT
0	000000_8–007776_8	+0
1	010000_8–017776_8	+2
2	020000_8–027776_8	+4
3	030000_8–037776_8	+6
.	.	.
.	.	.
.	.	.
(76_8) 62	760000_8–767776_8	$+174_8$
(77_8) 63	770000_8–777776_8	$+176_8$

Figure 1. Sector Boundaries

Since the actual number of sectors is fixed at 64, the PDP-11 never has more than 128K words of memory available to it at any given instant. However, the 128K words can consist of any combination of 2K blocks chosen from the total number of blocks available (up to 16,384). A single PDP-11 instruction can cause any 2K block to be replaced instantly by any other block. (This represents an effective transfer rate of over twenty billion bits per second.) Blocks are distinguished one from another by a Logical Block Number (LBN) unique to each block. In fact, a unique base LBN is assigned to each RVM-128 (or RVM-512) board, creating 64 (or 256) consecutive Logical Block Numbers beginning at that base number.

The actual assignment of physical blocks of memory to sectors of address space is controlled by a set of 64 registers in the UNIBUS peripheral space called the Sector Assignment Table (SAT). Each of the 64 SAT registers correspond to one of the 64 sectors of address space, with the first register linked to sector 0, the second to sector 1, and so forth (see figure 2). Each SAT register is a single word in size and contains the LBN of the physical block that is currently mapped to the sector associated with that register. To change an assignment,

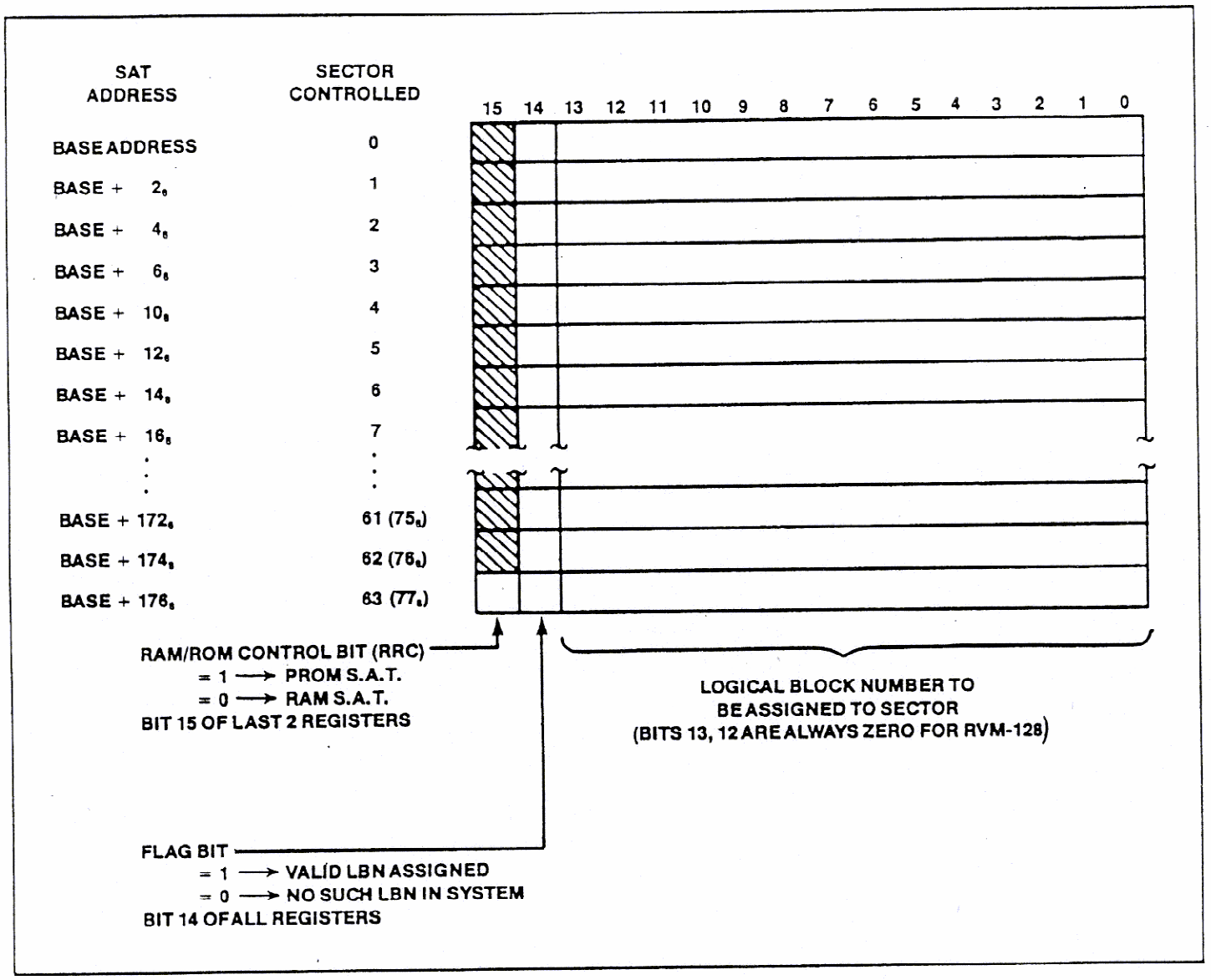


Figure 2. Sector Assignment Table

you simply write the LBN of the desired physical 2K block into the appropriate SAT register. Note that when reading a SAT register, bit 14 (the flag bit) is always a one (1) if there is an existing 2K block assigned to that sector. If no block is yet assigned to a sector, reading the corresponding SAT register will show all bits of the register to be zero (including bit 14). Also note that there is a clear distinction between a valid assignment of physical block zero to a sector (all bits zero except bit 14) and no assignment at all (all bits zero).

The flag bit (bit 14) is present only during a read of a SAT register. It is neither necessary nor possible for you to alter this bit. The flag bit is provided as a means to nonambiguously determine the state of the sector/block mapping in systems employing multiple RVM-128 memory boards.

For example, writing the number 10 to the first SAT register immediately channels all subsequent memory requests in the range 000000_8–007776_8 to physical block number 10. Changing the 10 to a 20 immediately replaces block 10 with block 20. Although block 10 is no longer directly available to the processor, its latest contents are preserved and can be accessed by merely reassigning block 10 to a sector.

The Sector Assignment Table described above is stored in volatile MOS memory and therefore will likely come up with scrambled contents after a power failure. This could

result in a random sector/block assignment, making it difficult if not impossible to boot the rest of the computer system. To avoid this problem, the RVM-128 contains two separate SATs: the RAM SAT described above and a parallel SAT stored in two fusable link PROMs installed on the board. The format of these PROMs is discussed in Section 2. You determine which SAT is in control at any time by the state of the RAM/ROM control bit (RRC). Whenever the RRC is a one, the PROM SAT controls the block/sector assignments. When the RRC is a zero, the RAM SAT is in control. To avoid the power-up random SAT problem, the RRC bit is always set to a one after any power failure. Thus by programming the PROMs, you may define any convenient default mapping to take effect after power failures. The RRC can also be set or cleared under program control by writing to the last RAM SAT register address (base address + 176_8 and setting or clearing the most significant bit in that word (bit 15). Note that when the RRC bit is a one and the PROM map is in control, the SAT registers available in the peripheral page are still the RAM SAT registers. It is not possible to investigate the contents of the PROM SAT.

INSTALLATION

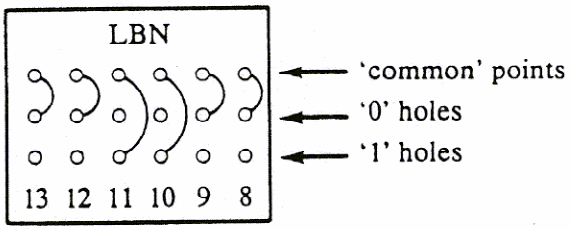
Installation of the RVM-128 is quite simple but requires some care to ensure proper operation.

STEP 1: Assigning the LBN

Each RVM module must be assigned a base Logical Block Number that allows all of the blocks contained on that board to be differentiated from blocks on other RVM modules in the same system. For this purpose, there is a row of 6 jumpers, labelled "LBN," provided on the board (see figure 3). Due to the different number of blocks on the RVM-128 and the RVM-512, the procedure for setting the base LBN differs slightly between them. In either case, the base LBN must be specified as a binary number. Each bit of this binary number must be specified as a one or a zero by soldering a jumper from the common point for that bit to either one of the two adjacent holes, one of which is labeled "1" and the other labeled "0."

- LBN for RVM-512

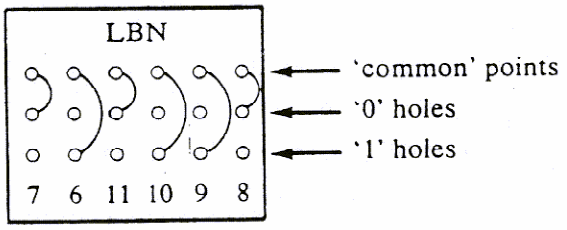
  Since the RVM-512 contains 256 blocks, you do not specify the lower order 8 bits of the LBN. The six LBN posts then represent bits 8 through 13, allowing a total of 14 bits to specify an individual block. This allows a maximum of 16,384 blocks distributed among 64 RVM-512 boards.



Example wiring for base LBN = 6000_8

- LBN for RVM-128

  Since the RVM-128 contains 64 blocks, you do not specify the lower order 6 bits of the LBN. The six LBN posts then represent bits 6 through 11, allowing a total of 12 bits to specify an individual block. This allows a maximum of 4,096 blocks distributed among 64 RVM-128 boards.



Example wiring for base LBN = 3100_8

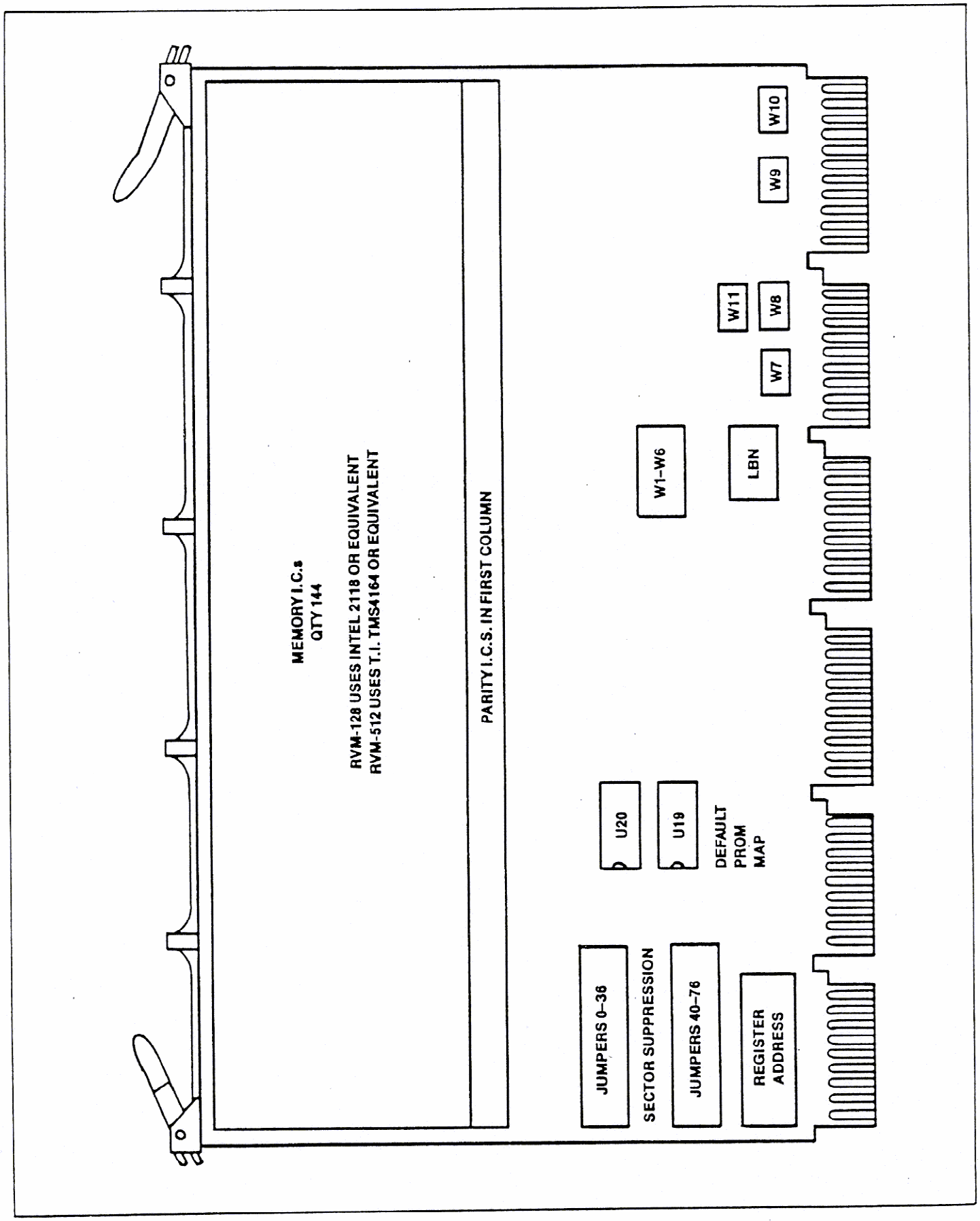
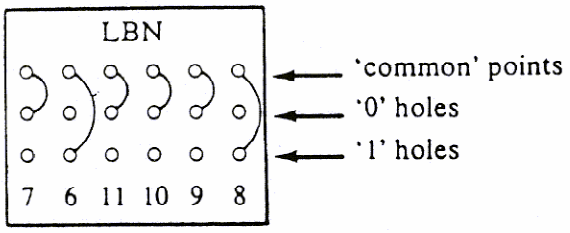


Figure 3. Location of Jumpers

For example, assume that you wish to declare a base LBN of 500_8 for an RVM-128 board in your system. You first break the desired LBN number down into binary and find that only bits 6 and 8 are ones. All others are zeroes. To assign the base LBN of 500_8, set the RVM-128 jumpers as follows:



LBN

11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	1	0	0	0	0	0	0
	0			5			0			0	

Not user defineable

Please note that base LBNs are always multiples of the number of blocks on the board (multiples of 64 on an RVM-128 and multiples of 256 on an RVM-512). Also note that the jumper grouping labeled LBN on the RVM-128 board shows pins numbered 8 through 13 with no numbers 6 or 7. When your board is configured to be an RVM-128, the pin labeled 13 actually controls bit 7 while the pin labeled 12 controls bit 6. It is not possible to specify bits 12 and 13 on an RVM-128. Likewise, it is not necessary to specify bits 6 and 7 on an RVM-512.

STEP 2: Suppression Jumpers

An RVM module is incapable of bank-switching memory boards not manufactured by Digital Pathways. For this reason, if your system includes some "foreign" memory, it will be necessary to inform the RVM-128 of that memory's location so that the RVM-128 will be prevented from assigning blocks to those sectors. Without this precaution, it would be possible to inadvertently assign two memories simultaneously to the same sector, most likely causing a fatal system error (though there is no danger to the hardware itself). To prevent this , you must install jumpers in the sector-suppression field (see figure 3). Each jumper installed will prohibit the RVM-128 from responding to a particular 4K word sector of address space. Conversely, the RVM-128 will be able to assign blocks of memory only to those ranges of address space not suppressed. The jumper labelled "0" will disable all block assignments in the range 000000_8–017776_8 (sectors 0 and 1). The jumper labelled "76" disables sectors 63 and 64 (address range 760000_8–777776_8).

To install a jumper, solder a short wire from the appropriate numbered hole to the unnumbered hole immediately adjacent to it.

STEP 3: Register Address

Although the 64-register Sector Assignment Table may be located anywhere in memory by altering the register address jumpers (see figure 3), it is strongly recommended that it be located in the peripheral page. Digital Pathways sets the register address to 760400_8. Note that in early PDP-11s with only a 32K address space, all references to the address range 160000_8–177776_8 will be automatically translated to the address space 760000_8–777776_8. Hence, when you define the Register Address, you should place it in the range 760000_8–777776_8 regardless of which model PDP-11 you have.

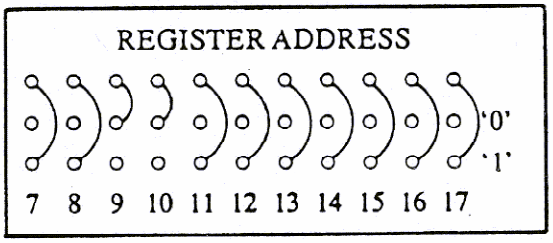
To set the Register Address to a new value, you first determine the binary equivalent of the desired address and then set the corresponding register address jumpers to either a one or a zero. This is done by soldering a short wire from the numbered common pin to the adjacent "0" or "1" pin. Note that bits 0 through 6 are not assignable by the user since the SAT occupies 64 words (128 bytes) of peripheral page address space.

For example, you would set the register address jumpers to 774600_8 as follows:

1) Figure out the binary equivalent of 774600_8:

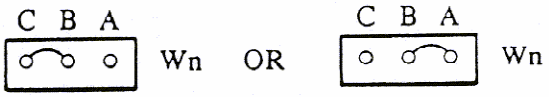
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0

2) Solder wires to the register address jumpers as follows:



STEP 4: Configuration Jumpers

Jumpers W1-W7 control the basic configuration of the RVM module. They should not be changed unless the effect is clearly understood. Each jumper consists of three holes, labelled A, B and C. The jumper has two allowed states: "A" connected to "B" or "B" connected to "C." NEVER CONNECT POINT "A" TO POINT "C."



Memory Chip Type (W1, W2, W3, W4)

W1 through W4 determine the overall memory size of the board. RVM-128 has 128K words using the standard 16K dynamic memory chip (2118 or equivalent). For RVM-128 jumpers W1 and W2 must be in the B-C position, and W3 and W4 must be in the A-B position.

RVM-512 has 512K words of memory using 64K dynamic RAM chips (TMS4164 or equivalent). W1 and W2 must be in the A-B position, and W3 and W4 must be in the B-C position.

Master/Slave Operation (W5, W11)

In systems containing two or more RVM modules, you must draw a distinction between a master unit and a slave unit. (See Section 4 for a more complete description.) If there is only one RVM module in the system, it must be a master.

A master board must have jumpers W5 and W11 set as follows:

W5 = B-C
W11 = A-B

A slave board must have jumpers W5 and W11 set as follows:

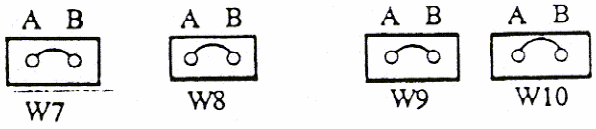
W5 = A-B
W11 = B-C

Source of Set Pulse (W6)

The RAM/ROM control bit (RRC) is always set to a one (ROM SAT in control) after a power-up sequence. This guarantees a legitimate SECTOR/BLOCK assignment at a time when the contents of the volatile RAM SAT may be scrambled. However, if you wish to set the RRC bit also on a UNIBUS INIT pulse from the CPU, you must set W6 to the B-C position. Be forewarned, however, that the software "RESET" instruction generates a bus INIT pulse. Leaving W6 in the A-B position will set the RRC bit automatically only after a power-up sequence.

STEP 5: Parity (W7, W8, W9, W10)

The RVM modules contain 18 bits of data which allows two parity bits compatible with standard DEC parity controllers. If you have the parity bits installed (some RVM modules are sold without the parity memory chips) and if your PDP-11 supports parity, you may enable it by setting jumpers W7 through W10 as follows:

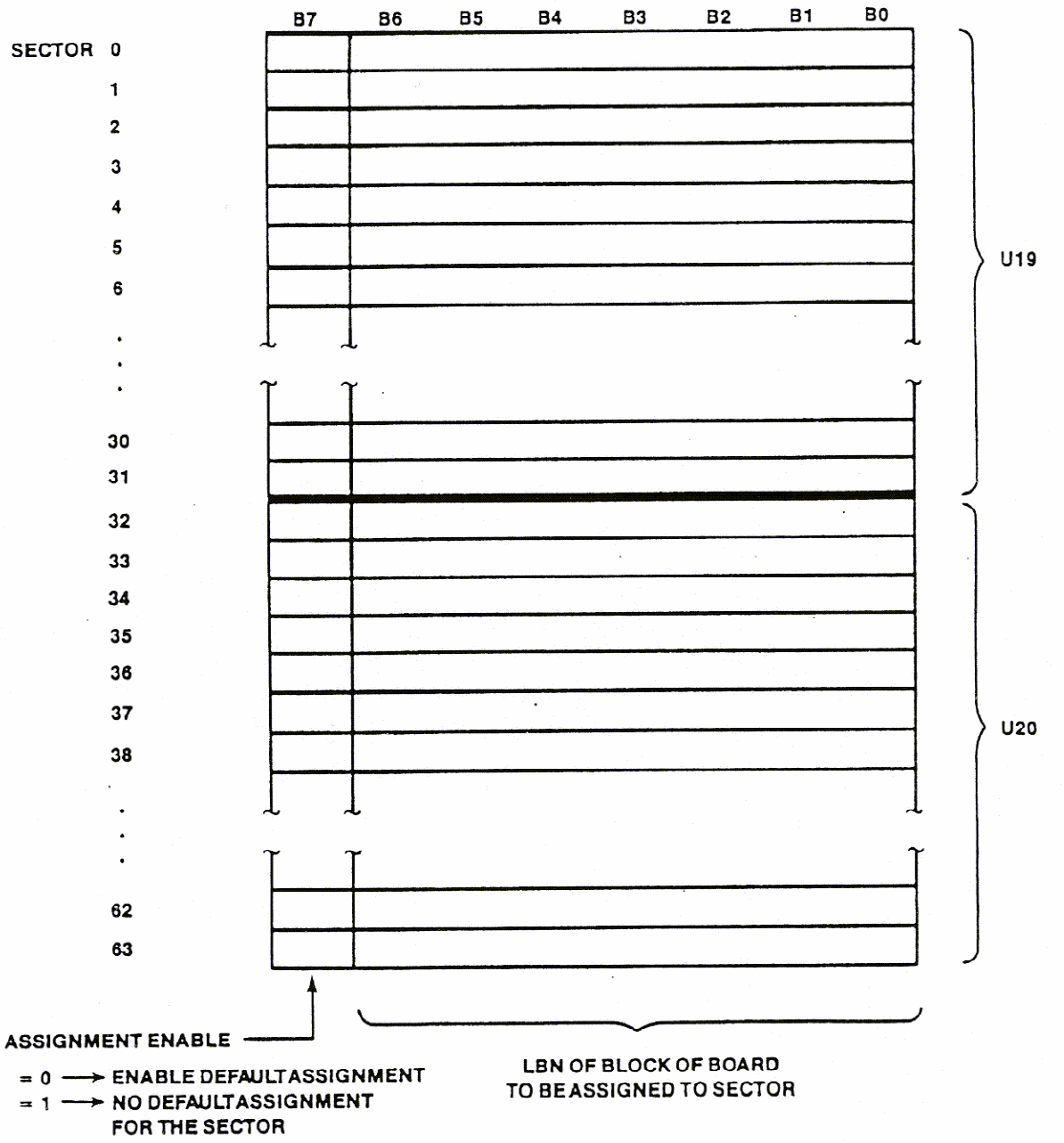


To disable parity remove all connections from W7 W8, W9, and W10. If parity is enabled, you should be careful to initialize the RAM contents after power up to ensure a valid state in the parity bits. Otherwise, the volatile memory chips may come up in a random state. (There is a fifty percent chance of a parity error.) The parity bits can be set most easily by writing a number (any number) into each word of memory on the board. This may require some bank-switching to access all the available words.

STEP 6: Default PROM Map

I.C. sockets U19 and U20 contain two 82S123 or equivalent fusable link PROMs. Together these two PROMs form the default Sector Assignment Table that controls the block-to-sector assignment whenever the RAM/ROM control bit (RRC) is set to a one (this may be done either under program control or as the result of the power-up initialization sequence). Each PROM is organized internally as 32 bytes of 8 bits each. The 64 registers of the SAT are mapped into the PROMs, with the first 32 registers taken from I.C. U19 and the last 32 registers contained in U20 (see figure 4). In other words, when the RRC bit is high, the block assigned to the address space 000000_8–007776_8 (sector 0) will be that block whose logical block number is found as the first byte of the PROM in socket U19.

Together, the two PROMs can assign a block to each of the 64 sectors in the 128K memory space. Sectors which are to remain unassigned (when the RRC bit is a one) should have the most significant bit (B7) of the appropriate byte of PROM set to a one. This causes the rest of the bits in that byte (B0–B6) to be ignored and no assignment to take place. When the most significant bit (B7) is a zero, the lower bits (B0–B6) are interpreted as the desired LBN. This leaves only seven bits to specify the desired LBN. On the RVM-128 board, only six bits are required to select among the 64 available blocks. On an RVM-512, however, there are 256 blocks, requiring eight bits to fully differentiate. Hence, it will be impossible to assign the first 128 of these 256 blocks using the default PROM. This is because the circuit provides the missing eighth bit and asumes it to be set to a one. Of course, no such limitation exists with the RAM SAT because it provides a complete 12 or 14 bits. Since a maximum of 64 sectors can be assigned in any case, the above limitation should present no problems.



PROMS (U19 & U20) ARE 82S123 OR EQUIVALENT.

NO PROM INSTALLED APPEARS AS ALL ONES.

RVM-128: B0–B5 SELECT ONE OF 64 BLOCKS ON BOARD.

RVM-512: B0–B6 SELECT ONE OF 128 BLOCKS. B7 IS ASSUMED AS 1 FORCING CHOICE FROM UPPER HALF OF AVAILABLE 256 BLOCKS.

Figure 4. Default PROM Format

To sum up, if the first byte in the PROM in socket U19 of an RVM-512 contains a zero, then whenever the RRC bit is set, physical block 128 (200_8) on that board is assigned to sector zero (remember, the unspecifiable eighth bit is assumed to be a one). If that same byte contains a zero in the ROM SAT on an RVM-128 board, then there is no ambiguity and LBN 0 on that board is assigned.

Leaving a PROM out of its socket simulates a PROM set to all ones. This sets B7 to a one in all cases and ensures no mapping to the sectors controlled by that PROM (whenever the RRC bit is set to a one). This practice can be used on all boards where no default assignment is required (all but one board in multiple board systems, for instance). In fact, the LBN specified by the default PROM actually refers only to the "relative" block number on the board in question. That is, if the base LBN of a particular RVM-128 module is 400_8, a default PROM byte containing a zero will map block zero ON THAT BOARD—in this case block 400_8—NOT the actual physical block zero which may reside on an entirely different board.

Note that PROMs are normally shipped unprogrammed (set to all zeros) by Digital Pathways. The use of such PROMs redundantly assigns the first block on that board to ALL sectors of address space whenever the RRC bit is high.

STEP 7: Plugging in the Module

After planning your configuration and setting all jumpers as described above, you then install the RVM module in any hex-wide small peripheral controller slot in the UNIBUS chassis. Do NOT use a prewired memory slot. In a PDP-11/70, you MUST use a UNIBUS small peripheral controller slot.

EXAMPLE

In this example, it is assumed that you have a PDP-11/05 with 8K of core memory located in the bottom four sectors (000000_8–037776_8). The following is also assumed:

- the base LBN of the RVM module is 0.
- the bottom 8K and the top 4K (peripheral space) have been suppressed by installing sector suppression jumpers "0," "2," and "76."
- the Register Address is 770400_8. The PROMs have been removed from sockets U19 and U20 to avoid any default mapping.
- the board is configured as an RVM-128 with 128K words of memory. It is a master board with no parity and the RRC bit is set only on power up (factory-standard configuration).
- the RVM-128 is installed in an available UNIBUS small peripheral controller slot.

The following memory manipulations are now performed using the front panel console and the "deposit" and "examine" functions:

1) Power-up and verify CPU operation.

2) Examine the contents of locations 770400_8–770576_8 to verify the existence of the sector assignment table. Note that even though the RRC bit is high (check bit 15 of address 770576_8 and see that it is a one) and the sector/block assignment is being performed by the default PROM map, you are seeing the contents of the RAM SAT. The default PROM map is NEVER visible to the software; hence the contents of the PROM should be noted carefully at the time it is being programmed.

3) Clear the RRC bit by writing a 7777_8 to location 770576_8. If you did not first install the suppression jumpers, you may now have multiple memories assigned.

4) Deposit the number zero into location 770420_8. Now, when you examine address 100000_8, you should find RAM assigned to that location (when before there was none). Fill the first few locations starting at 100000_8 with a pattern you will recognize—125252_8 for instance.

5) Deposit the number 000001 into location 770420_8. Now examine those same addresses around location 100000_8. The pattern you just stored there should no longer be visible. This is because those values were stored in block zero and you have now assigned block one to this sector.

6) Deposit a zero again into location 770420_8. Now examine locations starting at 100000_8 and you should see your pattern returned. Examine address 770420_8 and note that the flag bit (B14) is set to indicate that a valid block number has been assigned to this sector —the value displayed should be 040000_8.

7) Repeat the above experiment with different block numbers (00–77_8 allowed on a single RVM-128). Also try using different SAT entries such as address 770422_8 to control address range 110000_8–117776_8.

8) Remember each time you power-off and then power-on, the RRC bit will be set high and you will have to clear it again before the RAM SAT registers will have any effect.

USING MULTIPLE RVM-128s AND RVM-512s

It is possible to use multiple RVM modules in any system, adding 64 (for RVM-128) or 256 (for RVM-512) blocks with each board. Since each board contains its own set of registers in the SAT (and ALL SATs must be set to the SAME REGISTER ADDRESS), it is necessary to draw the distinction between a master board and a slave board. See Section 2 for a description of the required jumper changes. In any given system, one of the RVM boards must be a master and all the rest must be slaves. Typically, the master board is assigned the lowest base logical block number. Each board must be assigned a unique base LBN to avoid overlap in the block numbers. Also, the master board must be placed the furthest electrically from the CPU.

If you use any expansion chassis or bus extenders, the master board must be located in the most remote chassis that contains any RVM boards. In addition, if any of the boards are located in remote chassis, it is important that all chassis be powered and active before any values are written to the SAT. Once the above conditions are met, the use of a multiple board system is identical to the use of a single board system, with the exception that there are now more blocks available than on a single board. There are still only 64 registers in the SAT, since there are still only 64 sectors. Unlike most peripherals that require their peripheral page control registers to occupy unique regions of memory, the RVM modules require all SATs in the system to be originated at the same peripheral page address.

The RMV-512 supports up to a 14-bit LBN allowing for up to 16,384 blocks or a total of 64 megabytes, while the RVM-128 supports only a 12-bit LBN allowing for up to a total of 16 megabytes. If you mix RVM-512 and RVM-128 boards in the same system, in addition to being especially careful to assign unique logical block numbers, you must also limit yourself to a 12-bit LBN. Set the most significant two bits of the LBN base address on each of the RVM-512 boards to zero.

Users requiring more than 64 megabytes in their systems are encouraged to contact Digital Pathways, Inc. for information on adapting their RVM boards.

APPENDIX A
SPECIFICATIONS

RVM-128 fully loaded with 144 2118 RAM chips:

Storage temperature	−50°C to +150°C
Operating temperature ..	0°C to +70°C
Current at 5 volts	1.7 amps
Access time	350 nanoseconds
Cycle time	430 nanoseconds
Physical dimensions	15.68″ x 8.5″
UNIBUS loading	one unit DC load two unit AC loads

RVM-512 fully loaded with 144 4164 RAM chips:

Storage temperature	−50°C to +150°C
Operating temperature ..	0°C to +70°C
Current at 5 volts DC ...	1.9 amps
Access time	350 nanoseconds
Cycle time	430 nanoseconds
Physical dimensions	15.68″ x 8.5″
UNIBUS loading	one unit DC load two unit AC loads