10084 Hardware/Software Manual

VMEbus DR11-W Emulator

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1. Introduction

This manual contains programming and hardware set-up information for the etched-board version of the IKON Model 10084 VMEbus DR11-W emulator. The Model 10084 is a full emulation of a Digital Equipment Corporation DR11-W and will support any device or application supported by the DEC product.

The DR11-W emulator is a high-speed parallel DMA interface which may be used in interprocessor links based on cross-coupled DR11-Ws or emulators. Linkable systems include VAX, LSI-11, PDP-11, Gould/Sel, Data General, Harris, and IBM using other manufacturer's DR11-Ws, and Multibus, VERSAbus, VMEbus, and Prime systems using IKON's family of DR11-W emulators.

The 10084 can also be used to connect the VMEbus to any peripheral device, network node, mainframe channel interface, or workstation with a DR11-W type interface -- including a wide variety of graphics equipment made by several manufacturers.

NOTE: The following registered trademarks are used in this manual for descriptive purpuses to identify compatibility:

VERSAbus - Motorola, Inc.

Multibus - Intel Corporation

DEC, PDP-11, VAX, LSI-11 - Digital Equipment Corporation

2. General Specifications

Slave Mode Access

16 bit i/o map or 24 bit standard map with switch-selectable address.

PAL-selectable address modifier decode. Standard factory PAL responds to hex modifier codes of 29 and 2D in the i/o map and 39, 3A, 3D, and 3E in the standard map.

Interrupts

Jumper-selected interrupt level with software-selected vector.

DMA

24 bit linear address generation with 16 bit range (word) counter for up to 128k byte DMA blocks anywhere in a 16M byte address space.

DMA logic is all-bipolar, asynchronous, delay line driven for maximum speed and bus efficiency.

Jumper-selectable bus priority.

Single transfer per arbitration with early BBSY* release--allowing concurrent bus arbitration and maximum bus access by other devices.

2M byte/second+ transfer rate with the bus efficiency of 4M byte/second+ device.

External Interface

All DR11-W i/o modes supported, including control of bus address and range counter incrementation.

Input de-skew and output settling times jumper selectable.

Cycle request (CRQA & B) and BUSY polarities jumper selectable.

I/o connectors and pin-out identical to DEC format.

All input and output signals terminated and driven-received with high-hysteresis unified-bus type open collector transceivers.

Optional byte swapping to and from the external device with separate jumpers for p-i/o and DMA.

Power and Environmental

Power consumption - 3A

Commercial temperature range and humidity to 90% non-condensing.

3. Detailed Hardware Specifications

All timings are typical.

Slave Mode

DS0* and DS1* L.E. to DTACK* L.E.	550ns
D00-D15 driven to DTACK* L.E.	300ns
D00-D15 released to DTACK* T.E.	5ns
DS0* or DS1* T.E. to DTACK* T.E.	70ns
DS0* or DS1* L.E. to A01-23, IACK, WRITE* latched	100ns
DS0* or DS1* L.E. to D00-15 latched	450ns

Interrupts

DS0* and IACKIN* L.E. to DTACK*	550ns
D00-D07 driven to DTACK* L.E.	300ns
D00-D07 released to DTACK* T.E.	5ns
DS0* T.E. to DTACK* T.E.	70ns
DS0* and IACKIN* L.E. to IACKOUT* L.E.	500ns
AS* T.E. to IACKOUT* T.E.	40ns

DMA - Data Transfer Timing

internal grant and bus available to bus driven	30ns
A01-A23, WRITE*, IACK*, LWORD* driven to AS* L.E.	75ns
D00-D15 driven to DS0* or DS1* L.E.	70ns
AS* L.E. to DS0* or DS1* L.E.	20ns
DTACK* L.E. to A01-A23 released	130ns
DTACK* L.E. to D00-D15 released	150ns
DTACK* L.E. to DSTB* T.E.	130ns
DS0* or DS1* T.E. to WRITE* released	20ns
All bus and strobe signals released to AS* T.E.	0ns
AS* T.E. to AS* released	2ns
Full DMA transfer (with 200ns memory)	450ns

DMA - Bus Arbitration

BGxIN* L.E. to internal grant	60ns
BGxIN* L.E. to BBSY* asserted	70ns
BBSY* asserted to BRQx* released (min)	30ns
BBSY* asserted (min)	150ns

AS* asserted to BBSY* released	75ns
BGxIN* to BGxOUT*	70ns

Bus Interface

All bus and strobe receivers 74LS245 or equivalent.

All bus drivers 74LS645-1 or equivalent.

All strobe drivers 74F241 or equivalent.

All open collector drivers 74S38 or equivalent.

External Interface

All external signals terminated with 180 ohms to vcc and 390 ohms to ground.

All external signals received/driven with DS8838 type transceivers with 70ma sink capability and 1v hysteresis (1v and 2v thresholds).

Input de-skew (cycle request - CRQA or B - to input data & control signals latched) 110ns (short), 175ns (medium), or 300ns (long).

Output settling time (data valid to BUSY trailing edge) 160ns (short), 225ns (medium), or 350ns (long).

END CYCLE H pulse 125ns.

ACLO FNCT2 H, INIT H, GO H pulses 250ns.

FNCT1, 2, 3 signals change with the leading edge of GO H (these bits may also be changed without pulsing GO H).

Complete DMA external cycle = input de-skew + output settling + DMA overhead + memory access time + bus arbitration = approximately 800ns in medium cycle mode in system with 200ns memory and a fast arbitrator. (only 450ns of this time is actually spent controlling the VMEbus--the rest of the time is consumed meeting the DR11-W timing specification and does not use any VMEbus bandwidth).

4. On-Board Registers

The Model 10084 on-board registers occupy a 32 byte block of addresses which may be located anywhere in the VME standard map or short i/o map. Address and map selection is via switches. The address modifier codes recognized for each map are PAL determined and may be modified if necessary. See the general specifications for standard modifier codes supported.

The low order five bits of the system address (actually 4 bits + two data strobes on the bus) are used to determine which on-board register is being accessed. The remaining address bits and the address modifier codes are examined to determine when the board is being addressed.

All on-board registers may be read as bytes or words. Only word writes are allowed, with the exception of the modifier and interrupt vector register which may be written as two separate bytes, and the High DMA Address register which is only 8 bits wide and may be written as a word or byte. Longword accesses to these registers are not allowed.

4.1. On-Board Register Addressing

xxxx + 4 bits switch selectable -- all values in hex

Address	Write	Read
xxxx00	Control	Status
xxxx02	Data Out	Data In
xxxx04	Modifier+Vector	Modifier+Vector
xxxx04	(byte) Modifier	(byte) Modifier
xxxx05	(byte) Vector	(byte) Vector
xxxx06	Pulse Command	
xxxx08		
xxxx0A		
xxxx0C		
xxxx0E		
xxxx10		
xxxx12	DMA Address Low	
xxxx14	DMA Range Count	DMA Range Count
xxxx16		DMA Address Low
xxxx18		
xxxx1A	DMA Address High	
xxxx1C		
xxxx1E		DMA Address High

Note that the DMA Address registers have different read and write addresses. This is done to preserve software compatibility with IKON's other DR11-W emulators.

4.2. Register Formats

For all 16 bit registers, bit 15 is the most significant bit. Bit 7 is the MSB for all 8 bit registers.

Control

Bit	Name-Signal	Function
15	RDMA	reset DMAF and BERR flags
14	RATN	reset ATTF flag
13	RPER	reset PERR flag
12	MCLR	master clear board and pulse INIT H
11		
10		
09		
08	CYCL	force DMA cycle
07		
06	IENB	enable-disable interrupts
05		
04		
03	FCN3	FNCT3 H signal
02	FCN2	FNCT2 H signal
01	FCN1	FNCT1 H signal
00	GO	pulse GO H signal & enable DMA

RDMA Writing a 1 to this bit resets the DMA end of range flag and associated interrupt, if set. It also clears the bus error flag.

RATN Resets the attention flag bit and its associated interrupt.

RPER Resets the parity error flag if set.

MCLR Resets all latched functions and flags in the interface, terminates DMA, and pulses the INIT H signal to the external device.

CYCL Forces an immediate DMA cycle if DMA is enabled. This bit is the software equivalent of an external cycle request.

IENB This is the master interrupt enable bit for the interface. If it is a 1, the interface will place an interrupt request on the bus whenever ATTF or DMAF is set. Interrupts may be disabled by setting this bit to 0. Note that IENB is reset during an interrupt acknowledge sequence.

FCNx The three function bit latches drive the FNCTx H signals to the external device. They may be set to 0 or 1, and are reset to 0 by MCLR. FCN2 also drives the ACLO FNCT2 H signal.

GO The go bit pulses GO H to the external device and enables DMA transfers. DMA transfers will not occurr unless the external device or the software generates cycle requests.

The above functions which are pulses--GO, CYCL, MCLR, RPER, RATN, RDMA, and pulsed forms of IENB and FCN2--are also available in the Pulse Command register.

Status

Bit	Name-Signal	Function
15	DMAF	DMA end-of-range flag
14	ATTF	attention flag
13	ATTN	state of ATTENTION H
12	PERR	parity error flag
11	STTA	state of STATUS A input
10	STTB	state of STATUS B input
09	STTC	state of STATUS C input
08	0	
07	REDY	interface ready indication
06	IENB	interrupt enable latch
05	BERR	bus error flag
04	0	
03	FCN3	state of FCN3 latch
02	FCN2	state of FCN2 latch
01	FCN1	state of FCN1 latch
00	0	

DMAF DMA end-of-range flag. Set by last transfer in block, or when DMA is terminated by ATTENTION H. Causes an interrupt if IENB is true (1). Reset by MCLR or RDMA.

ATTF Set by a false-to-true transition on the ATTENTION H input. ATTF will cause an interrupt if IENB is true. Reset by MCLR or RATN.

ATTN This bit follows the state of the ATTENTION H input.

PERR The parity error flag is set by an external (DR11-W) parity error during a DMA input or p-i/o read. It is reset by MCLR or RPER, but otherwise will stay

true once set by an error. Note that parity is an IKON-only enhancement to the DR11-W specification and will work properly only when this interface is connected to a device which implements parity on the DR11-W i/o signals.

STTx The STTx bits follow the state of the STATUS x inputs.

REDY This bit reflects the state of the READY H output and indicates that the interface is ready for another command, such as GO. When REDY is false it indicates that the interface has been enabled to do DMA (by GO) and that the external device may issue cycle requests. REDY is reset by GO and set by MCLR, DMA end-of-range, or ATTENTION H.

IENB This bit reflects the state of the interrupt enable latch.

BERR This bit is set by a VMEbus error during DMA. It is reset by MCLR or RDMA.

FCNx These bits indicate the states of the function bit latches, and are primarily diagnostic in nature.

Data Out

Data written to this register is latched and presented to the external device via the DO00-DO15 output signals. This register is also used during DMA output and should not be written when REDY is false.

Odd parity over 17 bits is maintained for output data. The 17th bit (POXX H) replaces a GROUND pin in the DEC DR11-W specification. Its use is optional.

Data In

This register contains the current state of the DI00-DI15 input signals from the external device. It is used during DMA input, but may be read by the program at any time. Parity is checked whenever this register is read by the program or by DMA input.

Odd parity over 17 bits is checked on input data and PIXX H.

Address Modifier and Interrupt Vector

Address Modifier -- High byte of combined register

15	14	13	12	11	10	09	08
x	x	AM5	AM4	AM3	AM2	AM1	AM0

Interrupt Vector -- Low byte of combined register

07	06	05	04	03	02	01	00
D07	D06	D05	D04	D03	D02	D01	D00

This is a pair of 8 bit registers that may be written and read separately or combined as a 16 bit word. The Address Modifier is the bit pattern that will be applied to the address modifier lines of the VMEbus when the interface is the bus master (DMA). There are several possible address modifier values; all are somewhat system dependent. Consult documentation for the target system, and the VMEbus technical specification for appropriate values. Note that there are only 6 address modifier lines on the VMEbus, and that they correspond to the low order 6 bits of the 8 bit address modifier register.

The 8 bit value in the interrupt vector register is applied to the low order byte of the VMEbus during an interrupt acknowledge cycle. The VMEbus specification refers to this byte as the status-id byte. Its use is system dependent; typically it is multiplied by four (by the interrupt handler) and used as an index into a dispatch table. Consult the appropriate target system documentation for suitable values for this register.

Pulse Command

Bit	Name-Signal	Function
15	RDMA	reset DMAF and BERR flags
14	RATN	reset ATTF flag
13	RPER	reset PERR flag
12	MCLR	master clear board and pulse INIT H
11		
10		
09		
08	CYCL	force DMA cycle
07		
06	SMSK	set IENB
05	RMSK	reset IENB
04		
03		
02	FCN2	pulse ACLO FNCT2 H
01		
00	GO	pulse GO H signal & enable DMA

All bits in the Pulse Command register are pulsed functions which only affect interface and device functions when written as 1s. Writing a 0 to any of these bits has no effect. They are included as a convenience to allow the programmer to generate pulses without having to worry about the static, latched functions in the Control register. This eliminates always having to carry a copy of the Control register and 'or' in the pulse bits. It also allows pulsing the ACLO FNCT2 H (typically used to interrupt the external device) wihtout having to set FNCT2 to 1 and then 0.

SMSK This bit does a pulsed set of the interrupt enable latch. Writing a 1 to this bit sets the latch. Writing a 0 has no effect.

RMSK Writing a 1 to this bit clears the interrupt enable latch. Writing a 0 has no effect.

FCN2 Writing a 1 to this bit pulses the ACLO FNCT2 H output. Writing a 0 has no effect. Note that the ACLO signal is the 'or' of this pulse and the FCN2 latch in the Control register.

See the Control register section of this manual for a description of the other bits in this register.

DMA Address

The DMA address register is a 23 bit counter that is accessed by the program as a pair of registers, one 16 bits and one 8 bits wide. Note that register bit 00 maps onto address bus bit 01, and so on. Any address value in this register is effectively multiplied by 2 before being applied to the bus. Prior to enabling the DMA mechanism, this register is loaded with the buffer starting address divided by 2 (right-shifted one place). After each DMA transfer the register is incremented by 1 unless counting is inhibited by the BA INC ENB H input signal being brought to GROUND.

DMA address register to VMEbus address bus correspondence

DMA Address Low -- 16 bits

07	06	05	04	03	02	01	00
A08	A07	A06	A05	A04	A03	A02	A01

15	14	13	12	11	10	09	08
A16	A15	A14	A13	A12	A11	A10	A09

DMA Address High -- 8 bits

07	06	05	04	03	02	01	00
x	A23	A22	A21	A20	A19	A18	A17

DMA Range Count

The DMA range counter is a 16 bit register that controls the number of words transferred to the external device during a DMA block transfer. Prior to starting the DMA mechanism, this counter is set to the number of words to be transferred minus 1. During each DMA transfer the counter is decremented by one unless counting is inhibited by the WC INC ENB H input signal being brought to GROUND. When the range counter goes negative, further DMA transfers are inhibited, the READY H output and REDY bit are asserted, the DMAF flag is set, and an interrupt is generated if enabled.

5. External Signals

It is important to understand the pin-numbering convention used by the IKON family of DR11-W emulators, and how this convention relates to the DEC scheme.

The 10084 external connectors correspond exactly--both electrically and physically to the DEC connectors. This means that the pin labelled on the connector as pin 1 (usually by an arrow or equivalent) corresponds to the DEC pin designated VV. The fact that DEC numbers (letters!) their pins in reverse order when compared to the physical connectors used has caused all kinds of grief to the customer trying to install DR11-W compatible products in a computer system. Some designers have chosen to make pin 1 correspond to DEC pin A which produces a connector that is physically backward from the DEC product--and only adds to the confusion.

A further confusing factor is that the preferred cables are assembled with a stripe on the pin 40 end! This is necessary since the cable's internal ground plane drain wire is at the striped end of the cable and must be terminated to pin 40.

Customers using this or any other DR11-W compatible product must determine from their various suppliers which pin numbering convention is used, and whether the cables need a half-twist between the connected devices. IKON cables are keyed, and can only be plugged in correctly at the IKON end.

It is strongly recommended that IKON's ground-plane cables or their equivalent be used for DR11-W applications. Ordinary ribbon cables have unsuitable impedance control and cross-talk characteristics when used with the DR11-W pin-out and may adversely affect data integrity.

Signals to External Device

All signals asserted when high

DO00-DO15 H — Output data lines. DO15 H is the msb. These lines follow the state of the Output Data register which is written by the program or by DMA output.

POXX H — This is the IKON-specified optional output parity signal. Odd parity is maintained over 17 bits (DOxx and POXX).

INIT H — Initialize signal to the external device. Asserted whenever the bus initialize signal SYSRESET* is true. Pulsed true for 250ns by writing a 1 to the MCLR bit in the Control or Pulse Command register.

FNCT1,2,3 H — User-defined function bits sent to the external device. Set by writing to the FCNx bits in the Control register. These bits change with the leading edge of GO H (if it is written--it is not necessary to pulse GO to change these bits).

READY H — Corresponds to the REDY bit in the Status register. When false it indicates that the DMA mechanism has been enabled and that the external device may issue cycle requests. It is set false by GO in the Control register and is set true by MCLR, system reset, DMA end-of-range, or ATTENTION H.

BUSY H — Indicates that the 10084 has received a valid cycle request and is doing a DMA cycle. The trailing edge of BUSY H indicates that the DMA cycle is complete and that the device may read the DOxx lines (if an output cycle) and issue another cycle request. The delay from stable output data to the trailing edge of BUSY H is jumper selectable.

BUSY H is normally asserted high. Its polarity is jumper selectable. In interprocessor link applications it is asserted low so that its trailing edge causes a cycle request at the other end of the link. Many external devices also require that BUSY H be asserted low. The device documentation should be consulted for correct BUSY H polarity.

ACLO FNCT2 H — This signal is set by writing to FCN2 in the Control register or pulsed for 250ns by writing to FCN2 in the Pulse Command register. It is typically used to pulse ATTENTION H or its equivalent in the external device.

GO H — A 250ns pulse caused by writing a 1 to GO in the Control or the Pulse Command register. The leading edge of GO H occurs simultaneously with the true-to-false transition of READY H. It may be used to indicate to the external device that DMA has been enabled, or may be used as a strobe to indicate that the FNCTx H lines should be read by the external device.

END CYCLE H — This is a 125ns pulse that is simultaneous with the trailing edge of BUSY H. It may be used to strobe output data into the external device or instead of BUSY H as a handshake signal.

Signals from External Device

All signals true when high except BURST RQ L

Input terminations will hold floating inputs true.

All inputs except ATTENTION H and STATUS A, B, C H are latched following each cycle request. The latch delay (input de-skew) is jumper selectable.

DI00-DI15 H — Input data from the external device. DI15 is the MSB. The state of these lines may be read in the Data In register, or by doing DMA input. During DMA input these lines are latched a jumper-selectable delay time after the cycle request is issued.

PIXX H — The IKON-specified optional input parity line. Odd parity is tested for over 17 bits (DIxx and PIXX).

C0,C1 CNTL H — DMA mode control lines. They are used by the external device to control the direction and type of the DMA transfer. These inputs are latched a jumper-selectable delay time after each cycle request, and may be changed from one DMA word to the next.

Note that read-modify-write requests are actually handled in the 10084 as a read followed by a write and do not hold the bus between the read and the write.

C0 CNTL H	C1 CNTL H	OPERATION
0	0	Read Word
1	0	Read-Modify-Write
0	1	Write Word
1	1	Write Byte

During a Write Byte operation the byte selected is determined by the A00 H input signal. Model 10084 byte addressing follows the DEC format; A00 H low selects the low-order byte, A00 H high selects the high-order byte.

CYCLE RQ A,B H — A 0 to 1 transition on either of these lines while the other is held low, or a simultaneous 0 to 1 transition on both inputs will request a DMA cycle. If READY H is high, or if BUSY H is true cycle requests will be

ignored. The end of the DMA cycle will be indicated by the END CYCLE H pulse and by the trailing edge of BUSY H. All input data and control signals except ATTENTION H and STATUS x H are latched a jumper-selectable delay after the cycle request is issued.

The polarity of the cycle request inputs may be reversed (they will be falling edge active) by jumpers on the board. This is useful when connecting to devices intended to interface to the DR11-B. With either polarity, the inactive input (typically CYCLE RQ B) should be held low. There is a jumper available on the 10084 to accomplish this if for some reason it is not possible for the external device to control CYCLE RQ B H.

ATTENTION H — The attention input signal can be used by the external device to terminate the DMA block (if DMA is in progress) and/or interrupt the CPU. ATTENTION H sets READY H and the REDY flag bit true and sets the ATTF flag bit in the Status register. It causes DMAF to set if DMA was terminated. If ATTENTION H is held true it inhibits the starting of further DMA blocks and holds the ATTN bit in the Status register true.

STATUS A,B,C H — User defined input signals. They may be read as STTA, B, C in the Status register.

WC INC ENB H — This input signal controls DMA address register incrementation. It should be held true for sequential word transfers and set true every 2nd transfer for sequential byte transfers.

BA INC ENB H — This input signal controls range counter incrementation. It should be held true for sequential word transfers and set true every 2nd transfer for sequential byte transfers.

A00 H — This bit selects which byte of memory is written during Byte Write DMA cycles. DEC format byte addressing is used: A00 H low selects the low byte of the word, A00 H high selects the high byte of the word. There is a jumper available to hold A00 H at 0 (ground). A00 should be grounded for interprocessor link mode operation or the last word of a DMA input block may be garbled.

Connector Pin-Out

J1 Pin-Out

IKON	DEC	Signal		DEC	IKON
1	VV	DO15 H	DO00 H	UU	2
3	TT	DO14 H	DO01 H	SS	4
5	RR	DO13 H	DO02 H	PP	6
7	NN	DO12 H	DO03 H	MM	8
9	LL	DO11 H	DO04 H	KK	10
11	JJ	DO10 H	DO05 H	HH	12
13	FF	DO09 H	DO06 H	EE	14
15	DD	DO08 H	DO07 H	CC	16
17	BB	POXX H	GROUND	AA	18
19	Z	CYCLE RQ B H	GROUND	Y	20
21	X	END CYCLE H	GROUND	W	22
23	V	STATUS C H	GROUND	U	24
25	T	STATUS C H	GROUND	S	26
27	R	STATUS B H	GROUND	P	28
29	N	INIT H	GROUND	M	30
31	L	STATUS A H	BURST RQ L	K	32
33	J	WC INC ENB H	GROUND	H	34
35	F	READY H	GROUND	E	36
37	D	ACLO FNCT2 H	GROUND	C	38
39	B	CYCLE RQ A H	GROUND	A	40

J2 Pin-Out

IKON	DEC	Signal		DEC	IKON
1	VV	DI15 H	DI00 H	UU	2
3	TT	DI14 H	DI01 H	SS	4
5	RR	DI13 H	DI02 H	PP	6
7	NN	DI12 H	DI03 H	MM	8
9	LL	DI11 H	DI04 H	KK	10
11	JJ	DI10 H	DI05 H	HH	12
13	FF	DI09 H	DI06 H	EE	14
15	DD	DI08 H	DI07 H	CC	16
17	BB	PIXX H	GROUND	AA	18
19	Z	GROUND	GROUND	Y	20
21	X	GO H	GROUND	W	22
23	V	FNCT1 H	GROUND	U	24
25	T	C1 CNTL H	GROUND	S	26
27	R	FNCT2 H	GROUND	P	28
29	N	C0 CNTL H	GROUND	M	30
31	L	FNCT3 H	FNCT3 H	K	32
33	J	BA INC ENB H	GROUND	H	34
35	F	A00 H	GROUND	E	36
37	D	ATTN H	GROUND	C	38
39	B	BUSY H	GROUND	A	40

6. Loopback Testing

The IKON model 10084, like most DR11-Ws and emulators is capable of extensive self-test. All programmed i/o, interrupt, and DMA features may be exercised and tested by 'looping back' the J2 connector to the J1 connector. This is done with a 40-conductor ribbon cable connected pin-for-pin between two 40-pin idc sockets. One of the standard IKON-supplied cables may be used for this purpose.

The signals connected in this way are shown below:

DO00-15 H	>	DI00-15 H
FNCT 1,2,3 H	>	STATUS C,B,A H
FNCT 1 H	>	C1 CNTL H
ACLO FNCT2 H	>	ATTENTION H
BUSY H	>	CYCLE RQ A H
POXX H	>	PIXX H

The loopback connection also causes (by virtue of the way the connector pin-outs line up) WC INC ENB H and BA INC ENB H to be asserted, and C0 CNTL H, CYCLE RQ B H, A00 H to be held false.

BUSY H should be jumpered for low-assertion and CYCLE RQ polarity for rising edge active.

When set up for loopback, the 10084's various features may be tested as follows:

Programmed i/o is tested by writing a value to the Data Out register and verifying that the value appears in the Data In register.

Function and Status bits are tested by writing the FCNx bits in the Control register and reading the resulting STTx bits in the Status register. Note that FCN1 corresponds to STTC, and that FCN2 will also cause the ATTN, and ATTF Status bits to change.

Interrupts and various pulse commands are tested by setting up the board's interrupt vector and interrupt mask, and then generating an attention interrupt by pulsing ACLO FNCT2 H by writing a 1 to FCN2 in the Pulse Command register.

DMA output is tested by setting up the range and address registers, setting the address modifier register, setting FCN1 to 0, and then pulsing GO and CYCL in the Control register or Pulse Command register. GO enables DMA, and CYCL actually initiates the first

transfer. The end of the first-and later-transfers cause BUSY H to go from low to high, which causes another cycle request, continuing the handshake until the range counter has been exhausted. End-of-range sets the REDY and DMAF flags in the Status register, and causes an interrupt, if enabled.

If the data buffer has been previously set to a known pattern, the last word of that pattern should appear in the Data In register when the DMA block transfer is complete.

DMA input is tested in the same way except that FCN1 is set to one before starting DMA. If a known value has been previously written to the Data Out register it should be repeated in every word of the input buffer.

7. Interprocessor Links

The IKON model 10084 may be used in a high-speed parallel interprocessor link with other IKON DR11-W emulators, or those made by DEC or other manufacturers. This technique of linking processors and systems produces very high transfer rates -typically 1Mbyte/second- and can usually be implemented with a simple, efficient protocol.

The physical interprocessor link connection is made by connecting the J1 connector of each DR11-W to the J2 connector of the other DR11-w, jumpering for BUSY H asserted low, CYCLE RQ rising edge active, and A00 H forced off.

The signal connection accomplished is similar to loop-back, and is shown below.

DR11-W #1		DR11-W #2
DO00-15 H	>	DI00-15 H
POXX H	>	PIXX H
DI00-15 H	<	DO00-15 H
PIXX H	<	POXX H
BUSY H	>	CYCLE RQ A H
CYCLE RQ A H	<	BUSY H
FNCT 1,2,3 H	>	STATUS C,B,A H
STATUS C,B,A H	<	FNCT 1,2,3 H
FNCT1 H	>	(loop back
C1 CNTL H	<	to #1)
(loop back	<	FNCT1 H
to #2)	>	C1 CNTL H
FNCT3 H	>	BURST RQ L
BURST RQ L	<	FNCT3 H
ACLO FNCT 2 H	>	ATTENTION H
ATTENTION H	<	ACLO FNCT 2 H
CYCLE RQ B H	<	0
C0 CNTL H	<	0
A00 H	<	0
WC INC ENB H	<	1
BA INC ENB H	<	1
0	>	CYCLE RQ B H
0	>	C0 CNTL H
0	>	A00 H
1	>	WC INC ENB H
1	>	BA INC ENB H

Note that each device's C1 CNTL H (direction control) is derived from its own FNCT 1 H output. If the device sets its FNCT 1 H output it will be doing an input into its memory.

The exact software link protocol chosen is customer and application dependent, but most are based on the link protocol suggested by DEC in its DR11-W user's guide. This protocol involves exchanging single word messages via ATTENTION H interrupts to set up word count and data direction, and synchronize the start of DMA transfers. Block mode DMA accomplishes the actual data transfer. An example of an enhanced version of this protocol used by several of IKON's customers is available on request.

When ATTENTION H is used as part of a DMA protocol (typically driven by ACLO FNCT2 H as a clear-to-send indicator), it must be a pulse rather than a level. If the program that received the ATTENTION H signal attempts to start DMA while ATTENTION H is still asserted, DMA operation will be inhibited, and will not start when ATTENTION H is de-asserted. The end of the link generating the ATTENTION H signal should use a pulse that is as short as practical--which may be relatively long if more than one operating system call is required--and the end of the link receiving the ATTENTION H pulse should wait until it is removed before starting DMA.

The IKON Model 10084 pulse command register may be used to generate a 250ns ACLO FNCT2 H pulse at the IKON end of the link.

8. Hardware Switch/Jumper Options

Board Address Selection

The location of the 10084's on-board register set in the system memory map(s) is determined by switches at U51, U52, and U53.

U51		U52		U53	
1	A23	1	A15	1	A07
2	A22	2	A14	2	A06
3	A21	3	A13	3	A05
4	A20	4	A12	4	
5	A19	5	A11	5	
6	A18	6	A10	6	
7	A17	7	A09	7	
8	A16	8	A08	8	I-O MAP

Note that the address selection switches are complemented. Any address switch set to on will decode a zero in that address bit position.

Address map selection is done with switch U53-8. If that switch is off, the board will respond to any of the four standard map address modifier codes: 39, 3A, 3D, and 3E. If switch U53-8 is on, the board will respond to either of the short i/o map address modifier codes: 29 and 2D.

Interrupt Level Selection

The bus interrupt level of the board is controlled by jumpers W55-68, and W69-84. The jumpers must be set to the same level.

W	INT RQ	W	INT ACK
55-56	IR7	69-70	IA1
57-58	IR6	71-72	IA2
59-60	IR5	73-74	IA3
61-62	IR4	75-76	IA4
63-64	IR3	77-78	IA5
65-66	IR2	79-80	IA6
67-68	IR1	81-82	IA7
		83-84	NO ACK

Note that the physical order of the INT RQ jumpers is reversed from that of the INT ACK jumpers.

Bus Priority Selection

The bus priority level used by the board during DMA transfers is selected by jumpers W31-46 and W47-54. The bus levels selected must agree.

Bus Request Selection

W	Bus Level
47-48	BR0
49-50	BR1
51-52	BR2
53-54	BR3

Bus Grant Matrix

Bus Grant	W	W	Internal Grant
BG0IN	32	31	BGIN
BG0OUT	34	33	BGOUT
BG1IN	36	35	BGIN
BG1OUT	38	37	BGOUT
BG2IN	40	39	BGIN
BG2OUT	42	41	BGOUT
BG3IN	44	43	BGIN
BG3OUT	46	45	BGOUT

The bus level to be used by this board is selected by jumpering the appropriate BGxIN pin to the adjacent BGIN pin, and the corresponding BGxOUT pin to the adjacent BGOUT pin. The three remaining bus levels are passed through the board by jumpering each level's BGxIN pin to its BGxOUT pin.

A board set up to use bus level 3 would have the following jumpers in place:

W53-54, W32-34, W36-38, W40-42, W43-44, and W45-46.

Consult target system documemtation for information on selecting the appropriate priority level for this board.

External Device I/O Options

Jumpers W25-30 control the byte ordering of data to and from the external device.

W25-W26	NO P I-O SWAP
W26-W27	P I-O SWAP
W28-W29	NO DMA SWAP
W29-W30	DMA SWAP

Jumpers W1-3 allow holding CYCLE RQ B H at ground (off). This may be useful for special applications when it is inconvenient for the external device to control this signal. CYCLE RQ B H should be grounded by the external device or jumpers for most applications including interprocessor link operation.

W1-W2	CYCLE RQ B H GROUNDED
W2-W3	NO EFFECT ON CYCLE RQ B H

Jumpers W4-6 allow holding A00 H at ground (off). This prevents the external device form doing odd byte DMA accesses. A00 H should be grounded by the external device or jumpers for most applications including interprocessor link mode operation.

W4-W5	A00 H GROUNDED
W5-W6	NO EFFECT ON A00 H

Jumpers W22-24 control cycle request polarity. Rising edge active should be selected for interprocessor link operation and most other applications including loopback testing.

W22-W23	CYCLE REQUEST (A OR B) RISING EDGE ACTIVE
W23-W24	FALLING EDGE ACTIVE

Jumpers W19-21 control BUSY H polarity. BUSY H asserted low should be selected for interprocessor link and loop-back operation.

W19-W20	BUSY H ASSERTED LOW
W20-W21	BUSY H ASSERTED HIGH

Jumpers W7-18 control input de-skew and output settling times. The 175ns, 225ns combination is the closest to DEC timing. The 110ns, 160ns combination may be used for somewhat increased performance. The 300ns, 350ns jumpers allow attachment of devices with poor settling and de-skew times, and/or the use of poor quality cables (not

recommended!).

W - W	INPUT	OUTPUT
7-10 and 13-16	110ns	160ns
8-11 and 14-17	175ns	225ns
9-12 and 15-18	300ns	350ns

The timing jumper combinations shown above are the only ones allowed.

IKON Model 10084 DR11-W Emulator

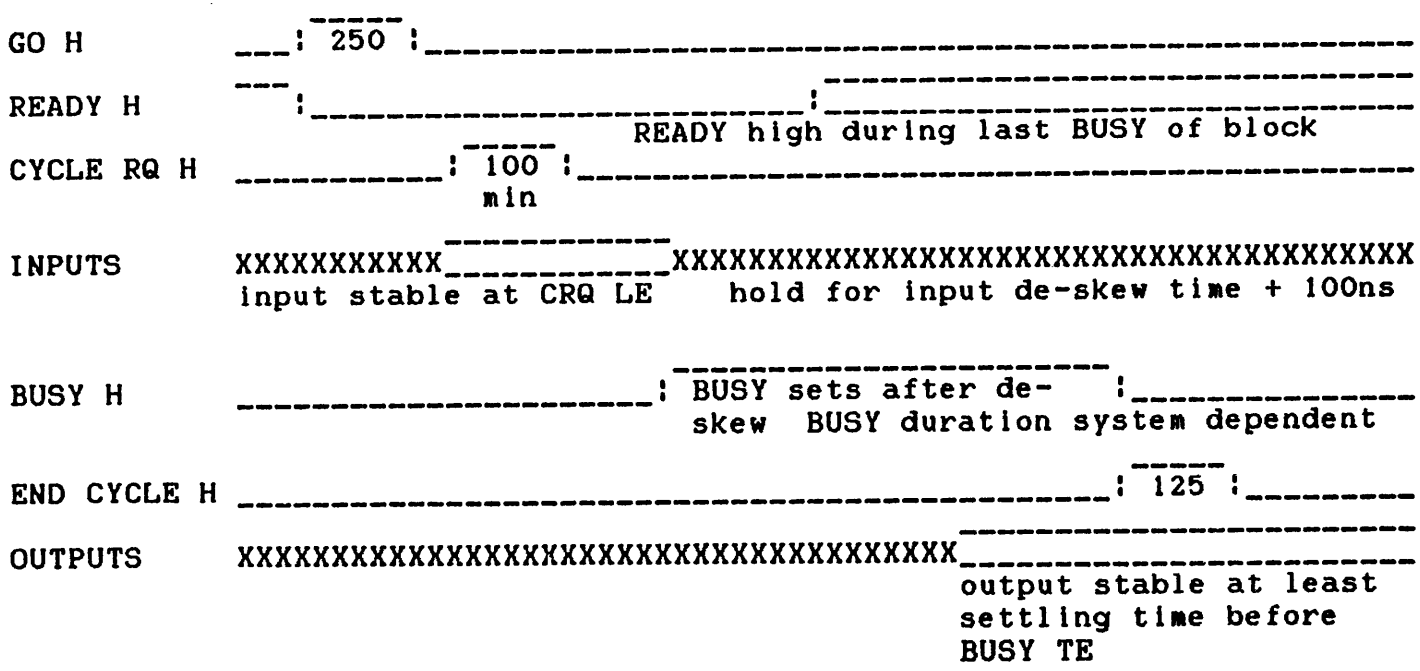
APPENDIX A

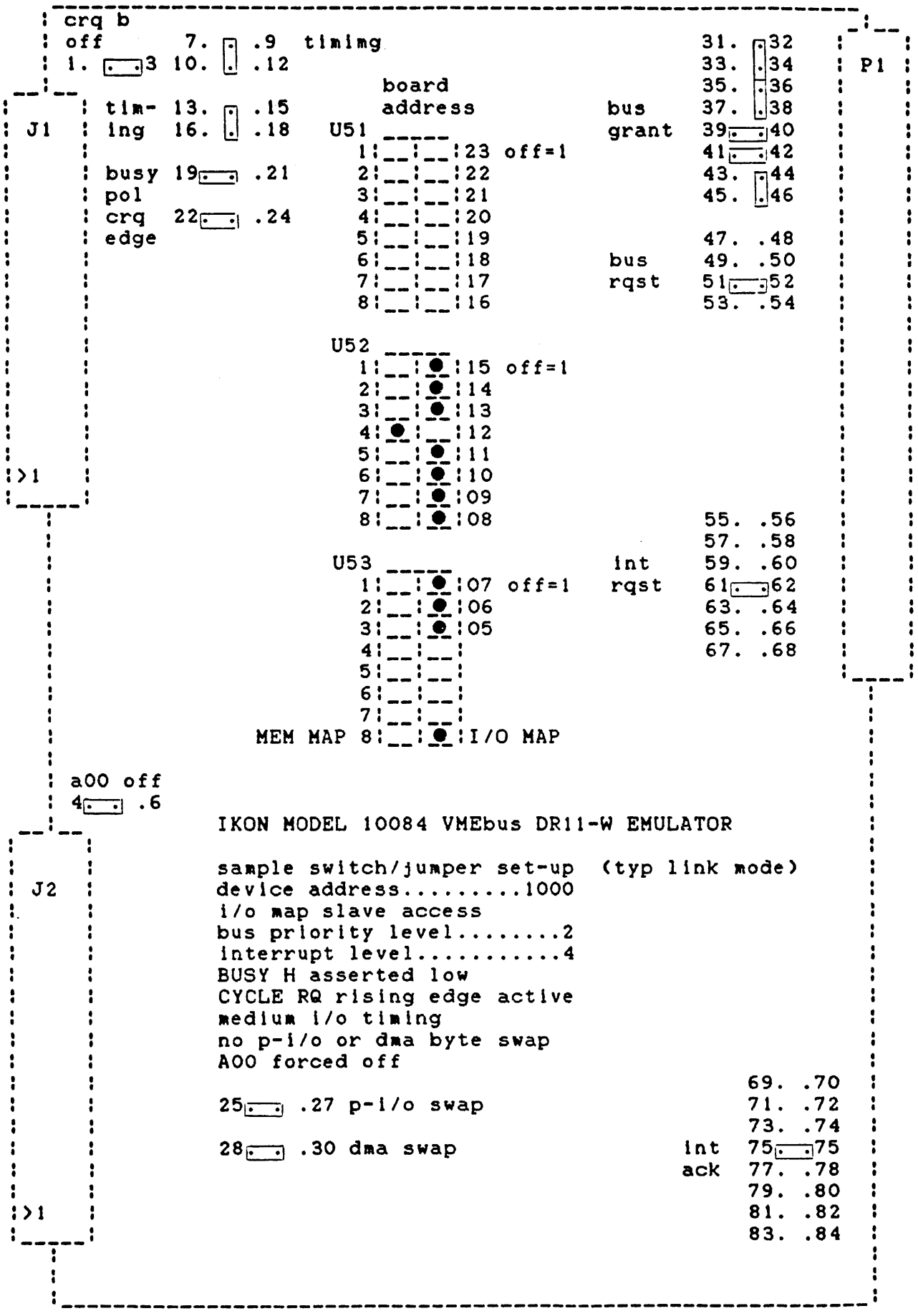
External I/O Timing

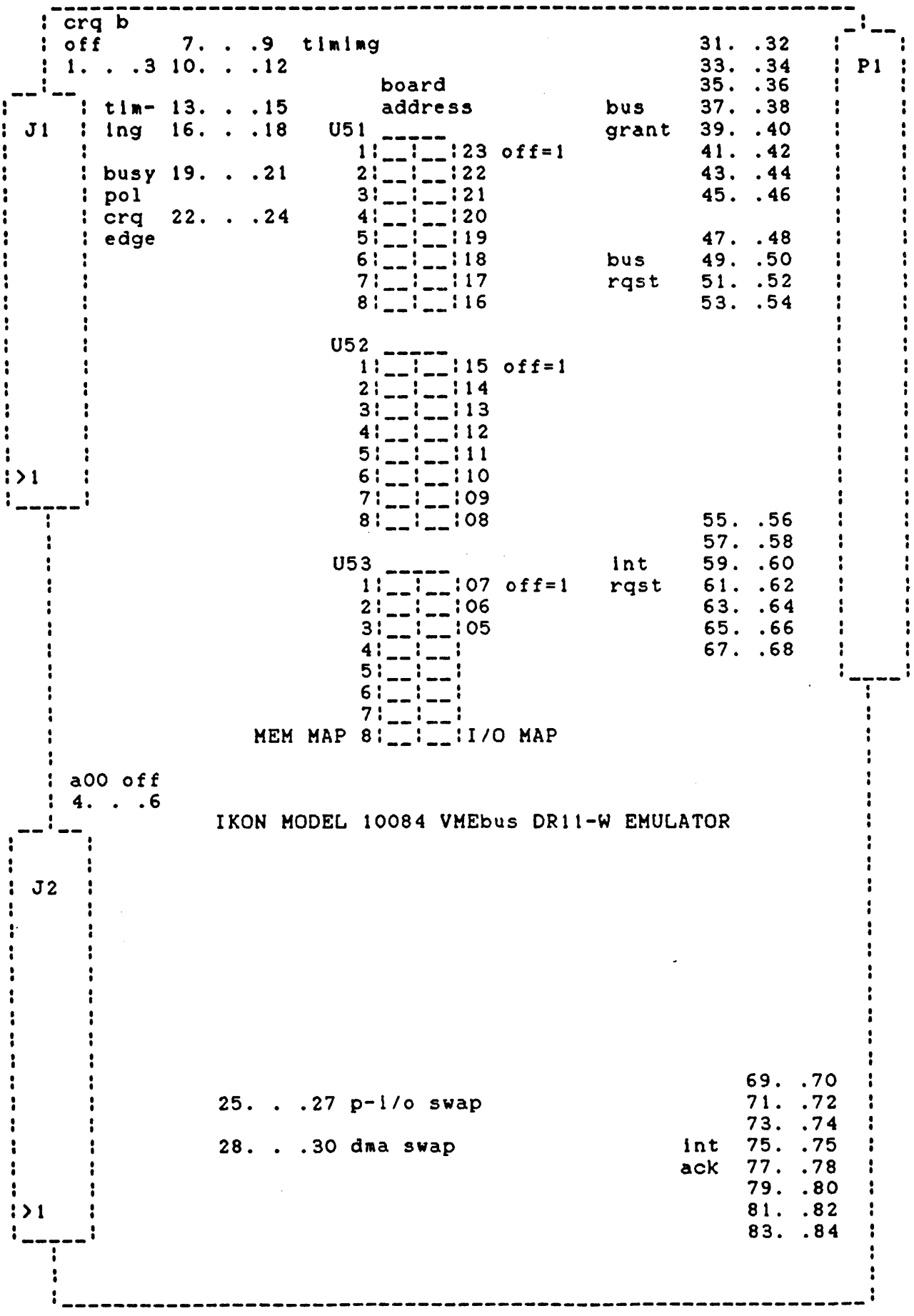
ikon corporation

2617 WESTERN AVENUE ● SEATTLE, WASHINGTON 98121 ● (206) 624-3410

IKON MODEL 10084 I/O TIMING




crq b
off
1.
3
7.
.9
10.
.12
timing
board
address
tim-
ing
busy
pol
crq
edge
13.
.15
16.
.18
19
.21
22
.24
J1
>1
U51
U52
U53
23 off=1
22
21
20
19
18
17
16
15 off=1
14
13
12
11
10
09
08
07 off=1
06
05
MEM MAP
I/O MAP
bus
grant
bus
rqst
int
rqst
31.
32
33.
34
35.
36
37.
38
39
40
41
42
43.
44
45.
46
47.
.48
49.
.50
51
52
53.
.54
55.
.56
57.
.58
59.
.60
61
62
63.
.64
65.
.66
67.
.68
P1
a00 off
4
.6
IKON MODEL 10084 VMEbus DR11-W EMULATOR
sample switch/jumper set-up (typ link mode)
device address.....1000
i/o map slave access
bus priority level.....2
interrupt level.....4
BUSY H asserted low
CYCLE RQ rising edge active
medium i/o timing
no p-i/o or dma byte swap
A00 forced off
25
.27 p-i/o swap
28
.30 dma swap
int
ack
69.
.70
71.
.72
73.
.74
75
75
77.
.78
79.
.80
81.
.82
83.
.84
J2
>1


crq b
off
1. . .3
7. . .9
10. . .12
timing
13. . .15
16. . .18
19. . .21
22. . .24
J1
tim-
ing
busy
pol
crq
edge
>1
board
address
U51
23 off=1
22
21
20
19
18
17
16
U52
15 off=1
14
13
12
11
10
09
08
U53
07 off=1
06
05
MEM MAP
I/O MAP
31. .32
33. .34
35. .36
37. .38
39. .40
41. .42
43. .44
45. .46
47. .48
49. .50
51. .52
53. .54
55. .56
57. .58
59. .60
61. .62
63. .64
65. .66
67. .68
P1
bus
grant
bus
rqst
int
rqst
a00 off
4. . .6
IKON MODEL 10084 VMEbus DR11-W EMULATOR
J2
25. . .27 p-i/o swap
28. . .30 dma swap
69. .70
71. .72
73. .74
int
ack
75. .75
77. .78
79. .80
81. .82
83. .84
>1