# HP 27112A
# General Purpose I/O Interface (GPIO)

## Technical Reference Manual

Card Assembly: 27112-60001
Date Code: D-2308

HEWLETT PACKARD

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# PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with the user-inserted update information. New editions of this manual will contain new information, as well as updates.


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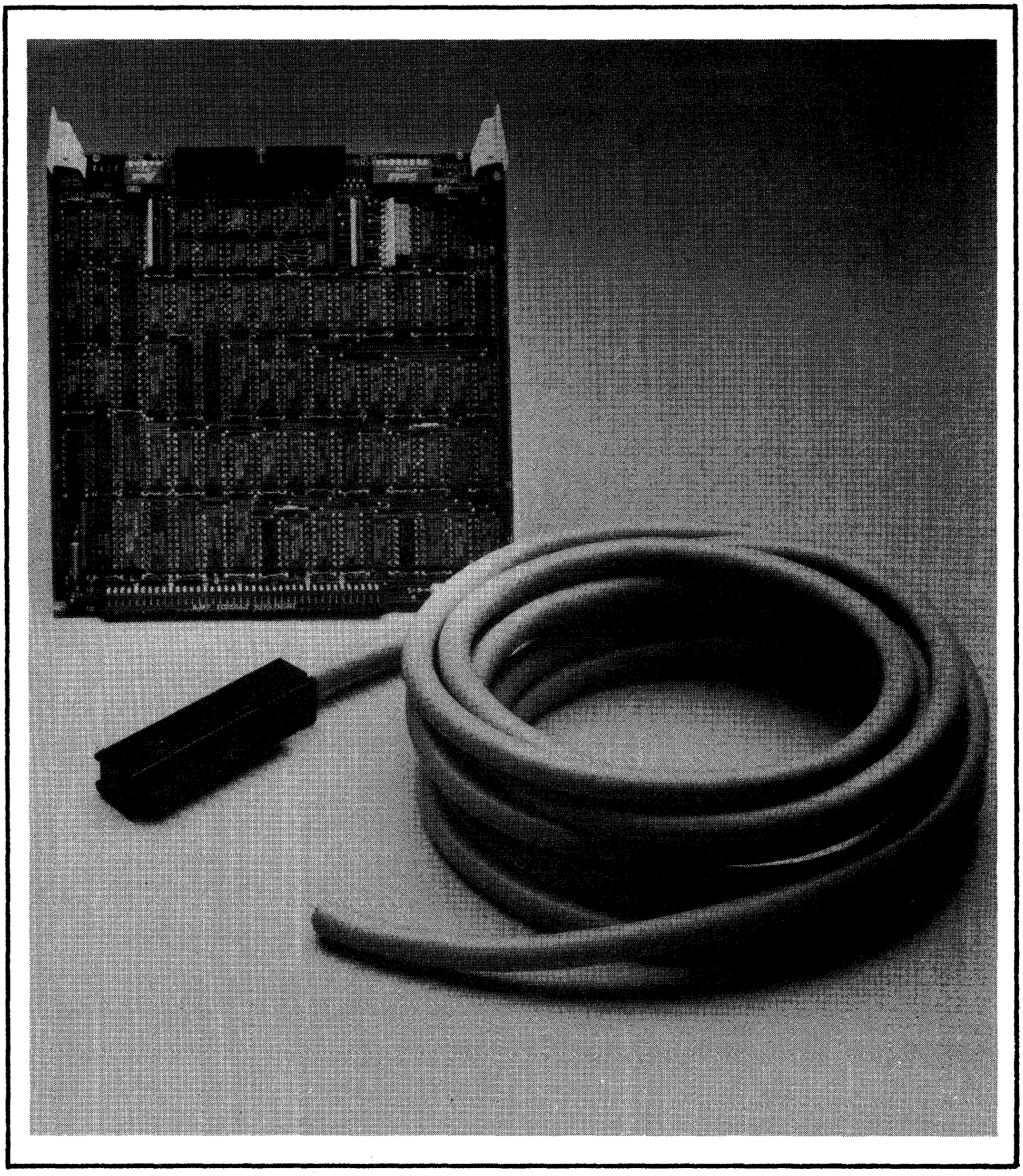


Figure 1-1. HP 27112A General Purpose Input/Output Interface

# GENERAL INFORMATION

SECTION I

This manual provides general information, installation, theory of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the Hewlett-Packard HP 27112A General Purpose Input/Output (GPIO) Interface. This section contains general information concerning the GPIO, and includes a description and specifications.

## PHYSICAL DESCRIPTION

The HP 27112A General Purpose I/O Interface (GPIO) is shown in figure 1-1 and consists of a printed circuit assembly, a five-meter unterminated cable, and an installation manual.

## FUNCTIONAL DESCRIPTION

The GPIO provides 16-bit parallel data communication between a Hewlett-Packard computer system and a peripheral device.

Figure 1-2 shows a typical Hewlett-Packard computer system using CHANNEL I/O and the GPIO. (CHANNEL I/O is a Hewlett-Packard standard defining the physical and electrical characteristics for an I/O system consisting of an I/O channel, an I/O channel adapter, and I/O cards. The GPIO is one of the I/O cards.)

Note that the computer system CPU and memory communicate directly along a Memory/Processor Bus (MPB). I/O data to/from peripheral devices reaches the CPU/memory through the I/O channel, the I/O channel adapter, and an I/O card such as the GPIO. The I/O data is received from and transmitted to peripheral devices by the I/O card, which converts device-specific data to a format compatible with the I/O channel, and thus the computer. The I/O channel interface (see figure 1-2) controls the flow of data traffic between the I/O channel and the memory/processor bus.

The GPIO decodes the device address, interprets device-to-channel operations, and initiates the appropriate action.

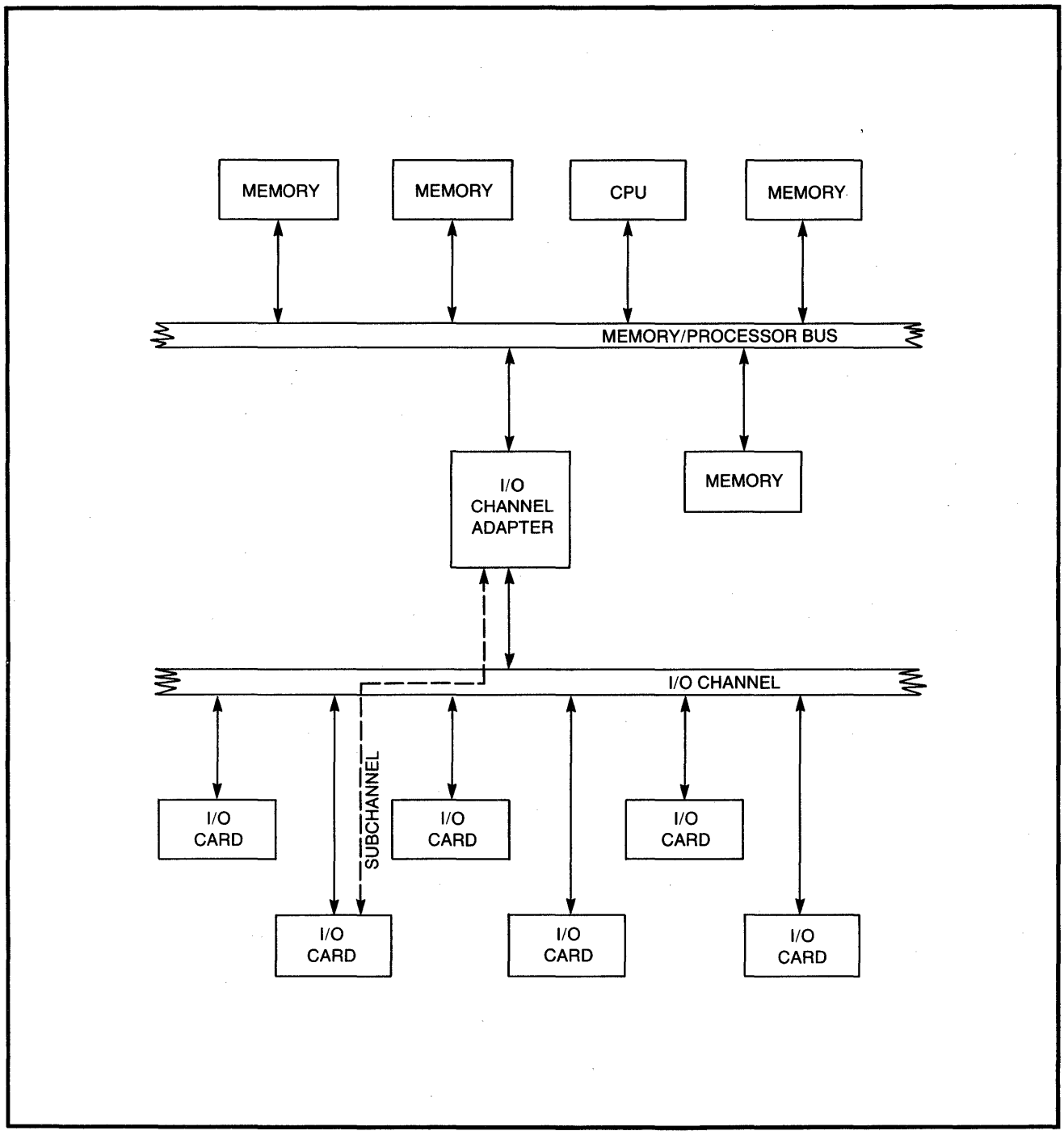



Figure 1-2. GPIO Interface in a Typical Hewlett-Packard Computer System

# EQUIPMENT SUPPLIED

The standard HP 27112A General Purpose I/O Interface consists of the following items (see figure 1-1):

GPIO interface card, part number 27112-60001

Five-meter unterminated cable, part number 27112-63002 - CABLE # = 8120-1695 DUPONT CABLE 50 CONDUCTOR 26 AWG TINNED COPPER 22 AWG DRAIN WIRE

HP 27112A Installation Manual, part number 27112-90001

The following options are available with the HP 27112A product:

001 Replaces unterminated cable (part number 27112-63002) with a 2.5-meter HP 9885 disc interface cable, part number 27112-63003

# IDENTIFICATION

## The Product

Up to five digits and a letter (27112A in this case) are used to identify Hewlett-Packard products. The digits identify the product; the letter indicates the revision level of the product.

## Interface Card

The interface card supplied with the HP 27112A is identified by a part number on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., C-2308). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number on the GPIO card could be:

27112-60001
C-2308

If the date code stamped on the card does not agree with the date code on the title page of this manual, there may be differences between your card and the card described herein. These differences are described in manual supplements available at the nearest Hewlett-Packard Sales and Service Office (a list of Hewlett-Packard Sales and Service Offices is contained at the back of this manual).

## Manuals

The Installation Manual (part number 27112-90001), supplied with the HP 27112A product) and this manual (HP 27112A Technical Reference Manual, part number 27112-90003) are identified by name and part number (note that this manual is part of the HP 27132A Technical Reference Package). The name, part number, and publication date are printed on the title page of each manual. If the manual is revised, the publication date is changed. In this manual, the "Printing History" page (page ii) records the reprint dates. Printing history information for the Installation Manual is printed on the title page.

## SPECIFICATIONS

Table 1-1 lists the specifications of the GPIO.

Table 1-1. Specifications

### FEATURES

* Clocked mode for data transfers with handshake, transparent mode for transfers without handshake
* TTL +5 volt and +12 volt signal level compatibility on outputs, TTL +5 volt inputs
* Positive true or negative true logic
* Separate 16-bit input and output storage registers
* Data handshake control and flag lines
* Two control and two status lines
* Transfer Rate:

  Byte Mode: 300 Kbytes per second

  Word Mode: 600 Kbytes per second

Table 1-1. Specifications (Continued)

## PHYSICAL CHARACTERISTICS

| | |
|---|---|
| Size: | 193.04 mm long by 171.45 mm wide by 16.38 mm thick (7.60 by 6.75 by 0.65 inches) |
| Weight: | 250 grams (8.7 ounces) |
| I/O Channel Interconnects: | 80-pin connector, J1 |
| Device Interconnects: | 50-pin connector, J2 |

## POWER REQUIREMENTS

| | +5V Outputs | | +12V Outputs | |
|---|---|---|---|---|
| Voltage | Current | Power | Current | Power |
| +5V | 2.2A | 10.9W | 2.1A | 10.6W |
| +12V | 0 | 0 | 0.15A | 1.8W |
| Total Dissipation | | 10.9W | | 12.4W |

MTBF = 133K Hrs (6-19-86)

# INSTALLATION

SECTION II

This section provides information on installing and checking the operation of the GPIO.

## COMPUTATION OF CURRENT REQUIREMENTS

The GPIO interface card obtains its operating voltages from the computer power supply through the I/O channel. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the GPIO card are listed in the power requirements entry of table 1-1. Current requirements for all other I/O cards can be found in the appropriate Technical Reference Manuals.

## LOGIC LEVELS

Peripheral device interface outputs are 75453B open-collector drivers with pullup resistors for 5-volt or 12-volt levels. The pullup voltages are determined by jumpers which select 5-volt or 12-volt operation, depending on where the jumper is installed. If a jumper is installed in the 5-volt position, the output voltage is +5V; if the jumper is installed in the 12-volt position, the output voltage is +12V. The locations of the jumpers on the card, and the positions of the jumpers for 5-volt or 12-volt operation, are shown in figure 2-1. The jumpers are listed below with the signals they control.

| JUMPER | SIGNAL |
|---|---|
| W1 | DOUT[15:8] |
| W2 | DOUT[7:0] |
| W3 | CTL[1:0], PCNTL, DIR, PRESET |

The peripheral interface signals DIN[15:0] and PEND use 5-volt LS-TTL levels. The remaining inputs, PFLAG and STS[1:0], are 5-volt LS-TTL schmitt trigger inputs.

# LOGIC SENSE

All peripheral interface signals can operate either positive true or negative true.

Positive true signals are considered "asserted" when their voltage level is 2.4 to 5 volts above ground potential (i.e., is "high"). They are considered "deasserted" when their voltage level is less than 0.8 volts above ground potential ("low").

Negative true signals are considered "asserted" when their voltage level is low, and are considered "deasserted" when their voltage level is high.

# CONFIGURATION SWITCH DEFINITIONS

Two sets of switches are used to configure the GPIO: an eight-switch assembly (SW1) selects the logic sense of the peripheral interface signals, and a five-switch assembly (SW2) controls the handshake operation.

Switch functions are listed in tables 2-1 and 2-2, and the locations of the switch assemblies on the GPIO card are shown in figure 2-1.

Switch settings should be as shown below when the GPIO card is installed in an HP 9000 Computer System and is connected to an HP 9885 Disc Drive. Other switch settings depend on the host system in which the GPIO card is installed and the peripheral device which is connected to the GPIO card.

| | SW1 | | | | | | | | SW2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 1 | 2 | 3 | 4 | 5 |
| HP 9885 Disc Drive | C | C | C | C | C | C | O | C | O | O | O | C | O |

C = closed
O = open

## Data Input Register Clock Select

The Data Input register may be clocked by one of three selectable clocking events during data transfers. The specific clock is determined by the mode selected by switches 4 and 5 on switch assembly SW2 as shown in table 2-3. Data is clocked every time a clocking event occurs even if the old data has not been read.

Mode 1 selects the transition of the peripheral interface signal PFLAG from the ready state to the busy state within the data transfer.

Mode 2 selects the transition of the peripheral interface signal PFLAG from the busy state to the ready state. This mode should be used only with FULL handshake mode.

Mode 0 or 3 selects the subchannel operation read_data to clock the Data Input register. In this mode, the handshake completes without clocking data in. Instead, data is clocked at the end of each backplane sync cycle, regardless of address lines or type of operation (i.e., effectively, data is continuously clocked in). This is referred to as "input following" because the data read is that data present at the inputs whenever the last sync cycle completed.

Table 2-1. Configuration Switch SW1 Definitions

| SWITCH ASSEMBLY SW1 - LOGIC SENSE SELECTION | | | |
|---|---|---|---|
| SWITCH | CONTROLS | OPEN<br>HI = 1 | CLOSED<br>LO = 1 |
| S1 | DIN[15:0] | POSITIVE TRUE | NEGATIVE TRUE |
| S2 | CTL[1:0] and STS[1:0] | POSITIVE TRUE | NEGATIVE TRUE |
| S3 | PRESET | POSITIVE TRUE | NEGATIVE TRUE |
| S4 | PDIR ASSERTED = WRITE | POSITIVE TRUE | NEGATIVE TRUE |
| S5 | DOUT[15:0] | POSITIVE TRUE | NEGATIVE TRUE |
| S6 | PEND | POSITIVE TRUE | NEGATIVE TRUE |
| S7 | PFLAG | POSITIVE TRUE<br>BUSY = HIGH<br>READY = LOW | NEGATIVE TRUE<br>BUSY = LOW<br>READY = HIGH |
| S8 | PCNTL | POSITIVE TRUE<br>ACTIVE = HIGH<br>IDLE = LOW | NEGATIVE TRUE<br>ACTIVE = LOW<br>IDLE = HIGH |

Table 2-2. Configuration Switch SW2 Definitions

| SWITCH ASSEMBLY SW2 - HANDSHAKE CONFIGURATION | | | |
|---|---|---|---|
| SWITCH | CONTROLS | OPEN | CLOSED |
| S1 | BIDIRECTIONAL BUS ENABLE | DISABLED | ENABLED |
| S2 | INTERNAL HANDSHAKE ENABLE | DISABLED | ENABLED |
| S3 | PULSE HANDSHAKE ENABLE | DISABLED | ENABLED |
| S4 | INPUT CLOCK SEL 0 | SEE TABLE 2-3 | |
| S5 | INPUT CLOCK SEL 1 | SEE TABLE 2-3 | |

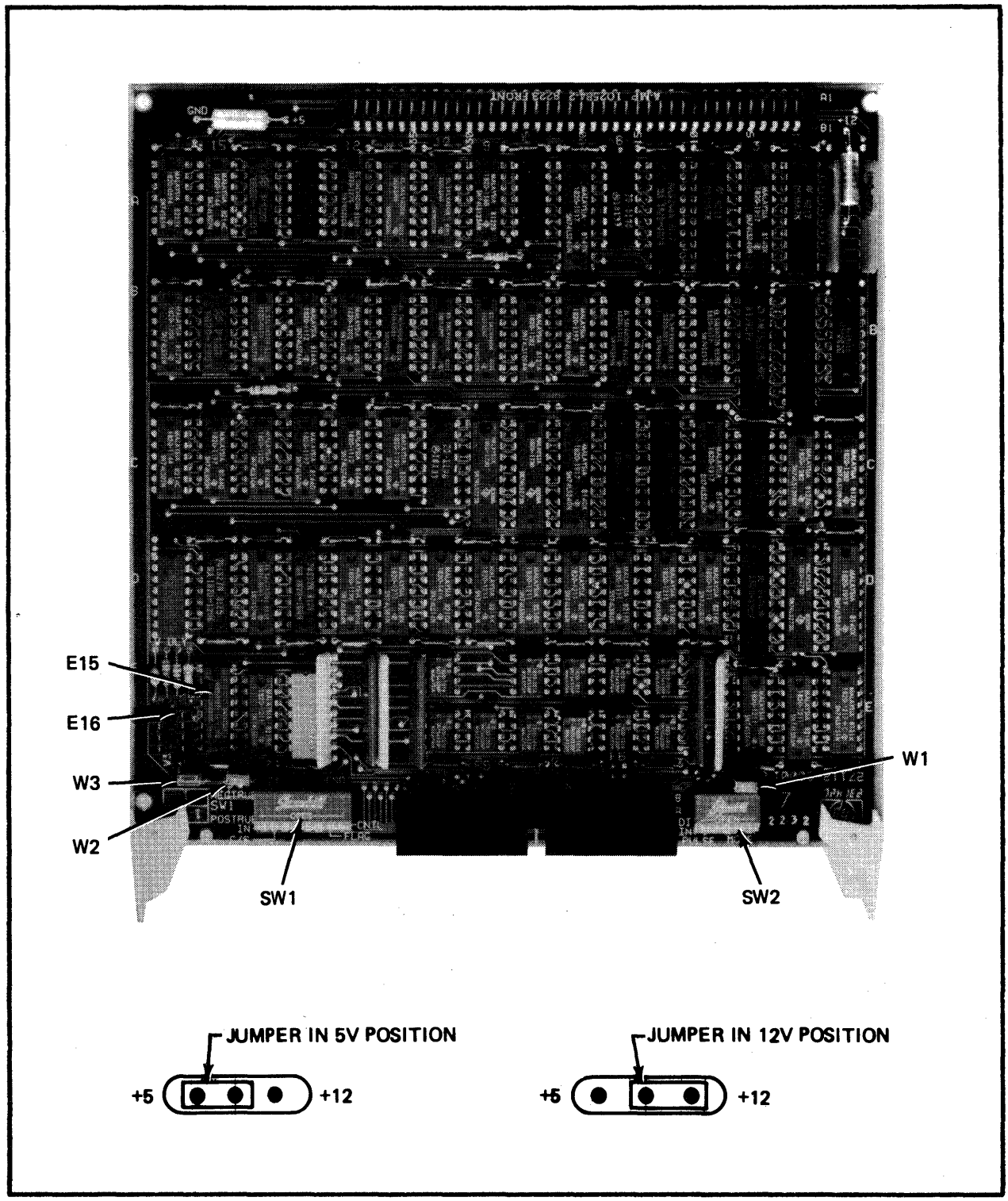



Figure 2-1. Switch and Jumper Locations

Table 2-3. Switch Settings for Data Input Register Clock Selection

| SWITCH | | MODE | DATA CLOCKED ON |
|---|---|---|---|
| SW2 - S5 | SW2 - S4 | | |
| CLOSED | CLOSED | 0 | Backplane sync cycle completion |
| CLOSED | OPEN | 1 | Ready to busy edge of PFLAG (leading edge) |
| OPEN | CLOSED | 2 | Busy to ready edge of PFLAG (trailing edge) |
| OPEN | OPEN | 3 | Backplane sync cycle completion (Note that this mode is the same as mode 0) |

## Full/Pulse Handshake Select

The peripheral interface signal PFLAG, in addition to functioning as handshake acknowlege, can function as a peripheral "READY" signal. If the peripheral requires that before a data transfer may begin the peripheral must be ready, then "Full mode" is required and "Pulse Mode" must be disabled.

## Internal Handshake

Internal handshake is used in applications where a two-wire handshake is not required. When internal handshake is enabled, a one-shot provides an internal FLAG signal, eliminating the need for the peripheral signal PFLAG. The internal FLAG will be asserted approximately 3 usec after PCNTL is asserted. You can increase this delay by adding an additional timing capacitor. The signal PCNTL is still available externally and may be used to clock data.

## Bidirectional Bus Enable

When the bidirectional bus enable switch is closed, the DOUT[15:0] lines are forced high regardless of the contents of the Data Output register whenever a write_data_order is not present. Since the output drivers on these lines are open collector, these lines may then be driven external to the device. This is usually necessary when the GPIO is used to interface to a device with a bidirectional bus. When the bidirectional bus enable switch is open, the data output lines are driven at all times. This is usually necessary when the GPIO outputs are going to a non-clocked device (such as a relay).

If the GPIO is used to interface to a device with a bidirectional bus and it is necessary that the output data to be available at times when a write_data_order is not present, the Data Output register must be written with all 1's or all 0's (depending on the DOUT[15:0] sense switch) so that the DOUT[15:0] lines are in the high state before the Data Input register can clock in data.

## PCNTL Sense

The peripheral interface signal PCNTL is positive true when the PCNTL switch is open and negative true when the switch closed. The deasserted state of PCNTL indicates that a GPIO data transfer is idle, and the asserted state indicates indicates that it is active.

## PFLAG Sense

The peripheral interface signal PFLAG is positive true when the PFLAG switch is open and negative true when the switch is closed. The deasserted state of PFLAG indicates ready and the asserted state indicates busy.

## PEND Sense

The peripheral interface signal PEND is positive true when the PEND switch is open and negative true when the switch is closed.

## DOUT[15:0] Sense

The peripheral interface signals DOUT[15:0] are positive true when the DOUT[15:0] switch is open and negative true when the switch is closed.

## PDIR Sense

The peripheral interface signal PDIR is positive true when the PDIR switch is open and negative true when the switch is closed. PDIR is asserted when a Write_data_order is present.

## PRESET Sense

The peripheral interface signal PRESET is positive true when the PRESET switch is open and negative true when the switch is closed.

## CTL and STS Signal Sense

The sense of the peripheral interface signals CTL[1:0] and STS[1:0] is controlled by the CTL & STS switch. When the switch is open all the signals operate in positive true mode. When the switch is closed all the signals operate in negative true mode.

## DIN[15:0] Sense

The peripheral interface signals DIN[15:0] are positive true if the DIN[15:0] switch is open and are negative true if the switch is closed.

# TIMING CAPACITORS

There are two one-shots (E15) on the GPIO card which generate the write delay and the internal handshake delay.

## Write Delay One-Shot

The write delay one-shot (see figure 6-1, quadrant E5 of sheet 2) provides approximately 100 nsec for the output data to settle between the time it is clocked into the output latch and the assertion of PCNTL. When extra long cables are used or when the peripheral requires additional settling time for the data, the delay can be increased by adding a capacitor between pins 1 and 4 of the socket at E16.

The formula for the value of the capacitor required is:

```
C = (T - 100) / 1.5
```

where

```
C = Additional capacitance (in pf)
T = Total time delay required (in nsec)
```

## Internal Handshake Delay One-Shot

The internal handshake delay one-shot (see sheet 2, D7 of figure 6-1) provides a delay of approximately 3usec between the assertion of PCNTL and the assertion of FLAG when the card is in internal handshake mode. It has no effect when internal handshake mode is disabled. The delay can be increased by adding a capacitor between pins 5 and 8 of the socket at E16.

The formula for the value of the capacitor required is:

```
C = ( T - 3000 ) / 3
```

where

```
C = Additional capacitance (in pf)
T = Total time delay required (in nsec)
```

# I/O CHANNEL INTERFACE

All interface between the GPIO and the host computer occurs on the I/O channel. An 80-pin connector (J1) located on the GPIO mates with a receptacle on the I/O channel. Connections to J1 are listed in table 2-4.

Table 2-4. I/O Channel Connector J1

| PIN NO. | SIGNAL MNEMONIC | SIGNAL DEFINITION |
|---|---|---|
| A1 | --- | Not used |
| A2 | DB14- | Data Bus, bit 14 |
| A3 | DB12- | Data Bus, bit 12 |
| A4 | GND | Ground |
| A5 | DB10- | Data Bus, bit 10 |
| A6 | DB8- | Data Bus, bit 8 |
| A7 | GND | Ground |
| A8 | DB6- | Data Bus, bit 6 |
| A9 | DB4- | Data Bus, bit 4 |
| A10 | GND | Ground |
| A11 | DB2- | Data Bus, bit 2 |
| A12 | DB0- | Data Bus, bit 0 |
| A13 | GND | Ground |
| A14 | AD2- | Address Bus, bit 2 |
| A15 | AD0- | Address Bus, bit 0 |
| A16 | GND | Ground |
| A17 | DOUT- | Data Out |
| A18 | BP0- | Bus Primitive, bit 0 |
| A19 | CEND- | Channel End |
| A20 | SYNC- | Synchronize |
| A21 | GND | Ground |
| A22 | --- | Not used |
| A23 | GND | Ground |
| A24 | BR- | Burst |
| A25 | DBYT- | Device Byte |
| A26 | MYAD- | My Address |
| A27 | GND | Ground |
| A28 | --- | Not used |
| A29 | --- | Not used |
| A30 | --- | Not used |
| A31 | --- | Not used |
| A32 | --- | Not used |
| A33 | PPON | Primary Power On |
| A34 | GND | Ground |
| A35 | --- | Not used |
| A36 | --- | Not used |
| A37 | --- | Not used |
| A38 | +12 | +12V |
| A39 | --- | Not used |
| A40 | +5 | +5V |

Table 2-4. I/O Channel Connector J1 (Continued)

| PIN NO. | SIGNAL MNEMONIC | SIGNAL DEFINITION |
|---|---|---|
| B1 | --- | Not used |
| B2 | DB15- | Data Bus, bit 15 |
| B3 | DB13- | Data Bus, bit 13 |
| B4 | GND | Ground |
| B5 | DB11- | Data Bus, bit 11 |
| B6 | DB9- | Data Bus, bit 9 |
| B7 | GND | Ground |
| B8 | DB7- | Data Bus, bit 7 |
| B9 | DB5- | Data Bus, bit 5 |
| B10 | GND | Ground |
| B11 | DB3- | Data Bus, bit 3 |
| B12 | DB1- | Data Bus, bit 1 |
| B13 | GND | Ground |
| B14 | AD3- | Address Bus, bit 3 |
| B15 | AD1- | Address Bus, bit 1 |
| B16 | GND | Ground |
| B17 | UAD- | Unary Address |
| B18 | BP1- | Bus Primitive, bit 1 |
| B19 | --- | Not used |
| B20 | POLL- | Poll |
| B21 | GND | Ground |
| B22 | IOSB- | I/O Strobe |
| B23 | GND | Ground |
| B24 | ARQ- | Attention Request |
| B25 | DEND- | Device End |
| B26 | IFC- | Interface Clear (Reset) |
| B27 | GND | Ground |
| B28 | --- | Not used |
| B29 | --- | Not used |
| B30 | --- | Not used |
| B31 | --- | Not used |
| B32 | --- | Not used |
| B33 | --- | Not used |
| B34 | GND | Ground |
| B35 | --- | Not used |
| B36 | --- | Not used |
| B37 | --- | Not used |
| B38 | +12 | +12V |
| B39 | --- | Not used |
| B40 | +5 | +5V |

# PERIPHERAL DEVICE INTERFACE

A cable from connector J2 on the GPIO provides interface between the GPIO and the peripheral device. Connections to J2 are listed in table 2-5.

Table 2-5. Device Connector J2

| GPIO CONN. PIN NO. | SIGNAL MNEMONIC | WIRE COLOR | 9885 CONN. PIN NO. | SIGNAL DEFINITION |
|---|---|---|---|---|
| A1 | Shield | Drain | 1 | Chassis Ground |
| A2 | DOUT 15 | BRN | 18 | Data Output, bit 15 |
| A3 | DOUT 14 | RED | 19 | Data Output, bit 14 |
| A4 | DOUT 13 | ORN | 20 | Data Output, bit 13 |
| A5 | DOUT 12 | YEL | 21 | Data Output, bit 12 |
| A6 | DOUT 11 | GRN | 22 | Data Output, bit 11 |
| A7 | DOUT 10 | BLU | 23 | Data Output, bit 10 |
| A8 | DOUT 9 | VIO | 24 | Data Output, bit 9 |
| A9 | DOUT 8 | GRY | 25 | Data Output, bit 8 |
| A10 | DOUT 7 | WHT | 26 | Data Output, bit 7 |
| A11 | DOUT 6 | WHT-BLK | 27 | Data Output, bit 6 |
| A12 | DOUT 5 | WHT-BRN | 28 | Data Output, bit 5 |
| A13 | DOUT 4 | WHT-RED | 29 | Data Output, bit 4 |
| A14 | DOUT 3 | WHT-ORN | 30 | Data Output, bit 3 |
| A15 | DOUT 2 | WHT-YEL | 31 | Data Output, bit 2 |
| A16 | DOUT 1 | WHT-GRN | 32 | Data Output, bit 1 |
| A17 | DOUT 0 | WHT-BLU | 33 | Data Output, bit 0 |
| A18 | GND | WHT-VIO | 8 | Ground |
| A19 | PCNTL | WHT-GRY | 10 | Peripheral control |
| A20 | PDIR | WHT-BLK-BRN | 15 | Peripheral direction |
| A21 | GND | WHT-GRN-BLU | N/C | Ground |
| A22 | PRESET | WHT-BLK-RED | 5 | Peripheral reset |
| A23 | CTL0 | WHT-BLK-ORN | 4 | Control Output Bus, bit 0 |
| A24 | CTL1 | WHT-BLK-YEL | 6 | Control Output Bus, bit 1 |
| A25 | GND | WHT-BLK-GRN | 11 | Ground |

Table 2-5. Device Connector J2 (Continued)

| GPIO CONN. PIN NO. | SIGNAL MNEMONIC | WIRE COLOR | 9885 CONN. PIN NO. | SIGNAL DEFINITION |
|---|---|---|---|---|
| B1 | Shield | Shield | 1 | Ground Shield |
| B2 | DIN 15 | WHT-BLK-VIO | 35 | Data Input, bit 15 |
| B3 | DIN 14 | WHT-BLK-GRY | 36 | Data Input, bit 14 |
| B4 | DIN 13 | WHT-BRN-RED | 37 | Data Input, bit 13 |
| B5 | DIN 12 | WHT-BRN-ORN | 38 | Data Input, bit 12 |
| B6 | DIN 11 | WHT-BRN-YEL | 39 | Data Input, bit 11 |
| B7 | DIN 10 | WHT-BRN-GRN | 40 | Data Input, bit 10 |
| B8 | DIN 9 | WHT-BRN-BLU | 41 | Data Input, bit 9 |
| B9 | DIN 8 | WHT-BRN-VIO | 42 | Data Input, bit 8 |
| B10 | DIN 7 | WHT-BRN-GRY | 43 | Data Input, bit 7 |
| B11 | DIN 6 | WHT-RED-ORN | 44 | Data Input, bit 6 |
| B12 | DIN 5 | WHT-RED-YEL | 45 | Data Input, bit 5 |
| B13 | DIN 4 | WHT-RED-GRN | 46 | Data Input, bit 4 |
| B14 | DIN 3 | WHT-RED-BLU | 47 | Data Input, bit 3 |
| B15 | DIN 2 | WHT-RED-VIO | 48 | Data Input, bit 2 |
| B16 | DIN 1 | WHT-RED-GRY | 49 | Data Input, bit 1 |
| B17 | DIN 0 | WHT-ORN-YEL | 50 | Data Input, bit 0 |
| B18 | GND | WHT-ORN-GRN | 9 | Ground |
| B19 | PFLAG | WHT-ORN-BLU | 13 | Peripheral flag |
| B20 | GND | WHT-ORN-VIO | 3 | Ground |
| B21 | PEND | WHT-ORN-GRY | 16 | Peripheral end |
| B22 | --- | WHT-YEL-GRN | 17 | Not used |
| B23 | STS 0 | WHT-YEL-BLU | 14 | Status Input Bus, bit 0 |
| B24 | STS 1 | WHT-YEL-VIO | 7 | Status Input Bus, bit 1 |
| B25 | GND | WHT-YEL-GRY | 12 | Ground |
| --- | --- | N/C | 34 | Not used |
| N/C | --- | BLK | 2 | Not used |
| N/C | --- | WHT-BLK-BLU | N/C | Not used |

# INSTALLATION

**CAUTION**

ALWAYS ENSURE THAT THE POWER TO THE BACKPLANE IS OFF BEFORE INSERTING OR REMOVING THE GPIO CARD AND CABLE. FAILURE TO DO SO MAY RESULT IN DAMAGE TO THE GPIO.

To install and check the operation of the GPIO card, follow the steps below in the order given:

1. Determine if your computer system can supply the power needed for the GPIO card. Refer to Section I, table 1-1 for power requirements.

2. Install jumpers in W1, W2, and W3, depending on whether 5-volt or 12-volt logic levels are to be used. The locations of W1, W2, and W3, and the positions of the jumpers for +5-volt or +12-volt operation are shown in figure 2-1.

3. Set the card's switches for proper operation in your system. Refer to tables 2-1, 2-2, and 2-3 for switch information. Actual switch settings will vary according to the computer system and the device which is connected to the GPIO card. However, switch settings for the HP 9885 disc drive (a typical device used with the GPIO) are shown below:

| DEVICE | SW1 | | | | | | | | SW2 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 1 | 2 | 3 | 4 | 5 |
| HP 9885 Disk Drive | C | C | C | C | C | C | O | C | O | O | O | C | O |

O = open
C = closed

4. There are two one-shots (E15, see figure 2-1) on the GPIO card which generate the write delay and the internal handshake delay. The write delay one-shot provides approximately 100 nsec for the output data to settle. When extra long cables are used, or when the peripheral device requires additional settling time for the data, the delay can be increased by adding a capacitor between pins 1 and 4 of the socket at E16 (see figure 2-1 for location of E16).

   The formula for selecting the capacitor value is:

$$C = (T - 100)/1.5$$

   where

   C = additional capacitance (in pf)
   T = total time delay required in nsec

The internal delay one-shot provides a delay of approximately 3 usec between the assertion of PCNTL and the assertion of FLAG. The delay can be increased by adding a capacitor between pins 5 and 8 of the socket at E16 (see figure 2-1 for location of E16).

The formula for the value of the capacitor is:

$$C = (T - 3000)/3$$

where,

C = additional capacitance (in pf)
T = total time delay required (in nsec)

5. Install the card in the appropriate slot in the computer. Refer to the computer system installation manual to determine the correct slot.

6. Connect the cable, supplied with the card, from J2 on the card to the peripheral device. If you have the test hood, which exercises more of the card's circuitry, and can be ordered (Hewlett-Packard part number 1251-8003), connect it to J2 instead of connecting the cable.

**NOTE**

A "grounding grommet" on the interface cable allows the cable shield to be "grounded" at that point in some applications. Refer to your computer installation manual.

7. Turn on computer system power.

8. Run the card verification program. Refer to the appropriate host computer system manual for information on running this program.

9. If a test hood was used, turn off computer power and remove the test hood. Connect the cable and, if necessary, reset the switches for your application.

## RESHIPMENT

If the GPIO is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the GPIO.

Pack the card in the original factory packing material, if available. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to repack the item. BE SURE TO OBSERVE ANTI-STATIC PRECAUTIONS.

# PRINCIPLES OF OPERATION

SECTION III

## INTRODUCTION

The GPIO provides 16-bit parallel data communications between the I/O channel and a peripheral device. The devices supported by the GPIO fall into two categories: "word devices" and "bit devices". Word devices associate all the data communicated in parallel as one logical unit of information. Bit devices use the parallel bits independently.

Word devices that are commonly supported by the GPIO are paper tape readers and punches, card readers, line printers, disc drives (including flexible discs), and magnetic tape drives. These devices usually combine several units or words into records which have unit logical significance. These records are referred to as "messages".

Bit devices that are commonly supported by the GPIO are typically involved in low-level control operations. Relay sequencers and contact closures are bit-oriented. For example, relay one has a function independent of relay two even though data bits one and two are presented together by the GPIO.

## FUNCTIONAL THEORY OF OPERATION

A functional block diagram of the GPIO is shown in figure 3-1. Reference also should be made, as necessary, to the schematic logic diagram contained in figure 6-1. Note that figure 6-1 consists of four sheets. References to this figure will be as follows: 1-A3, 6-1, 2-C8, 6-1, etc., where the first number, 1 through 4, refers to the sheet number, the combination of letters A through E and numbers 1 through 8 (A3, C8, etc.) refer to the quadrants on the sheet, and 6-1 refers to the figure number.

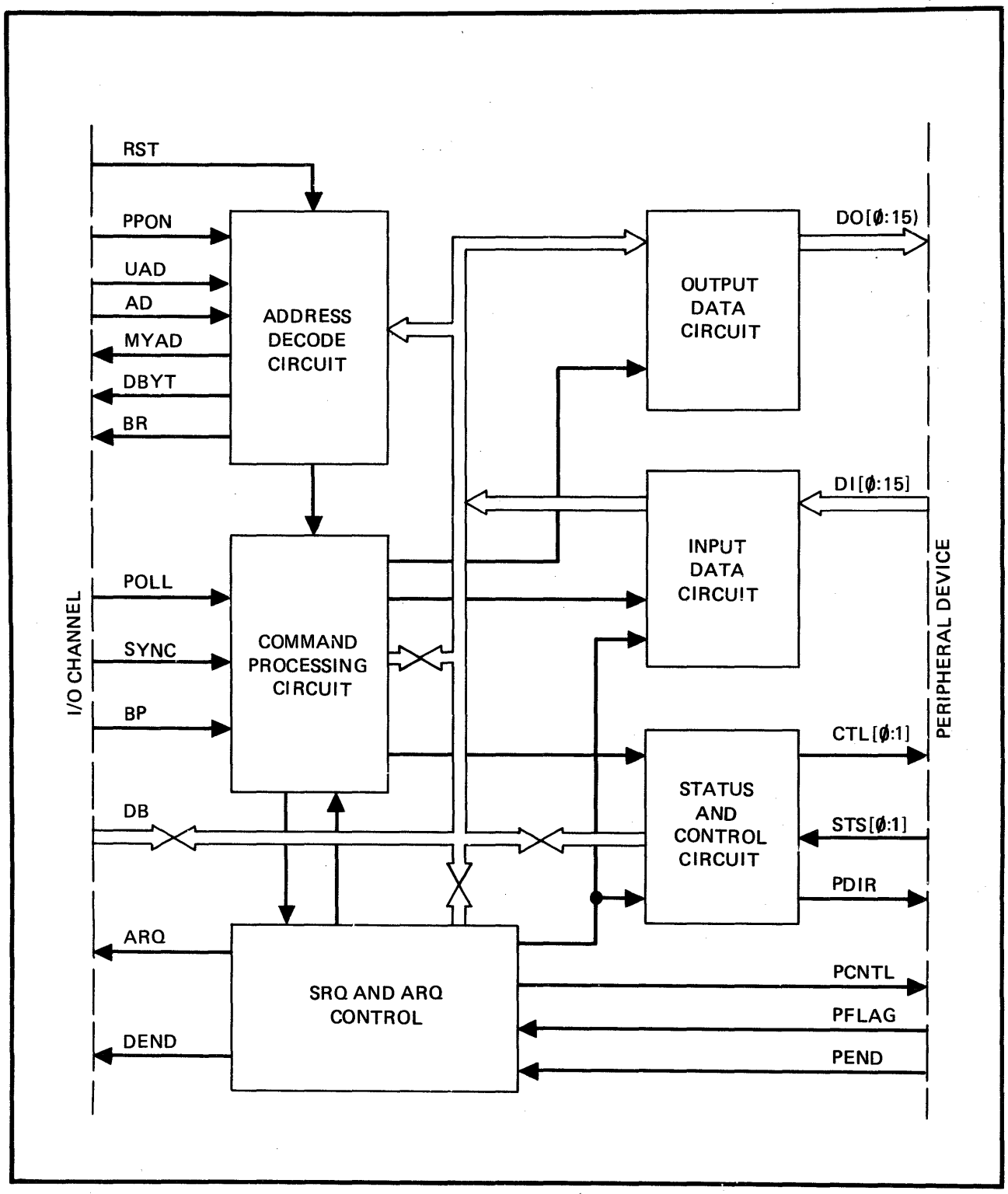



Figure 3-1. GPIO Functional Block Diagram

The GPIO consists of six functional sections, as follows:

Address Decode Circuit (ADC)

Command Processing Circuit (CPC)

SRQ and ARQ Control (SAC)

Input Data Circuit (IDC)

Output Data Circuit (ODC)

Status and Control Circuit (SCC)

## Address Decode Circuit

The components comprising the Address Decode Circuit (ADC) are shown on sheet 1 of figure 6-1. The ADC learns the GPIO device address at power up or after a reset. Once having learned the address, the ADC screens all addressed I/O channel bus operations and informs the Command Processing Circuit whether or not the current I/O channel operation is addressed to the GPIO. Finally, the ADC signals to the I/O channel interface that it is responding to the current addressed I/O channel operation.

## Command Processing Circuit

The CPC (figure 6-1, sheets 1 and 4) interprets channel operations and initiates the appropriate operation throughout the GPIO. Two classes of operations are interpreted by the CPC: GPIO-I/O channel operations and peripheral device-I/O channel operations. GPIO-I/O channel operations manipulate the GPIO and affect GPIO interaction with the I/O channel, but have no direct effect on the peripheral device. Peripheral device-I/O channel operations are intended to transfer data to or from the device, or to directly affect the device; these are the primary operations of the GPIO.

## SRQ and ARQ Control

The SRQ (Service Request) and ARQ (Attention Request) Control (SAC) is the pacing mechanism for the GPIO. SAC consists of device handshake logic, card status logic, and request generation logic. The circuitry is shown on sheet 1, area E6-8 (ARQ and card status logic) and sheet 2 (SRQ and device handshake logic) of figure 6-1. The device handshake logic is activated by the Command Processing Circuit (CPC) and communicates directly with the peripheral device to control the progression of data through the data registers. The card status logic determines when an Abort or an interrupt has occurred. The request generation logic, based on inputs from the peripheral device handshake or card status logic, activates SRQ or ARQ.

## Input Data Circuit

The Input Data Circuit (IDC) consists of a 16-bit register and 16 line receivers (see 3-B3, 6-1). The line receivers (with selectable data sense) connect directly to the peripheral device through connector J2. The IDC is clocked by the device handshake logic of the SRQ and ARQ Circuit except on input following mode. The Command Processing Circuit enables the outputs of the register, which transfers the 16-bit incoming data, via the GPIO internal data bus (signals IDB0- through IDB15-), to the I/O channel when this bus is ready for read data.

## Output Data Circuit

The Output Data Circuit (ODC) consists of a 16-bit register (Output Data register) and 16 line drivers with selectable data sense (see 3-B5, 6-1). The line drivers connect directly to the peripheral device through connector J2. When the I/O channel has write data ready for transfer, the ODC is clocked by the Command Processing Circuit and the data is transferred via the internal data bus (signals IDB0- through IDB15-), the register, the line drivers and connector J2 to the peripheral device.

## Status and Control Circuit

The Status and Control Circuit (SCC) consists of the Status register, Control register, line drivers, and line receivers (see 3-E2 to 3-E7, 6-1). The SCC facilitates control of the peripheral outside the data path by examining or asserting status and control signals as appropriate.

# SIGNAL DEFINITIONS

The following paragraphs describe GPIO/peripheral device interface signals. Information included for each signal includes the signal name, where it originates, where it goes, its function, timing data, and where it can be found on the schematic logic diagram of figure 6-1 in Section 6. Pin connections for the signals (connector J2) are presented in table 2-4, Section 2.

All outputs are driven by 75453B open collector drivers with 2.2K ohm pull up resistors to the selected output high voltage level (+5V or +12V). All inputs are terminated with 1K ohm resistors to +5V and 1.5K ohm resistors to ground. The STS[1:0] and PFLAG inputs are 74LS14 schmitt trigger inputs; all other inputs are 74LS86 (two LSTTL loads).

## PDIR

Full Name: Peripheral Data Direction

Driven By: GPIO

Received By: Peripheral device

Function: PDIR signals when the GPIO is set for Write_Data operations, thus signalling the peripheral device that the GPIO is going to assert DOUT[15:0]. Primary use of PDIR occurs in bidirectional data bus cable configurations.

Timing: PDIR is asserted upon receipt of a Write_Data order. PDIR is deasserted when any order other than Write_Data is received, or when GPIO reset conditions occur.

Schematic Location: Sheet 2, B8

## DIN [15:0]

Full Name: Data Input Bus

Driven By: Peripheral device

Received By: GPIO

Function: Data Input Bus receives data from the peripheral device.

Timing: Data may be driven onto the DIN by the peripheral device at any time. Refer to the paragraph "Input Handshake Timing" for additional timing data on Data Input Bus operation.

Schematic Location: Sheet 3, A1 through D1

## DOUT

Full Name: Data Output Bus

Driven By: GPIO

Received By: Peripheral device

Function: Data Output Bus transmits data from the GPIO to the peripheral device.

Timing: If the bidirectional bus switch (SW2-1) is closed, DOUT signals are active only when PDIR is asserted. Otherwise, DOUT signals are always active. When operating a bidirectional bus, DOUT[15:0] should be set to a voltage high (regardless of logic sense) when input data is transmitted.

Schematic Location: Sheet 3, A8 through D8

## STS [1:0]

Full Name: Status Input Bus

Driven By: Peripheral device

Received By: GPIO

Function: Status Input Bus provides an auxiliary data path and an event detection path from the peripheral device. The data path is normally used to receive peripheral device status pertinent to the ongoing data transfer. Event detection may be used to alert the host CPU that a status transition has occured. Schmitt trigger receivers are used on these inputs.

Timing: Status Input Bus signals may be driven by the peripheral device at any time. In order to cause an interrupt, event detection must be enabled before operation. Refer to the "Interrupt ARQs" paragraph for additional timing data on Status Input Bus operation.

Schematic Location: Sheet 3, E1

## CTL [1:0]

Full Name: Control Output Bus

Driven By: GPIO

Received By: Peripheral device

Function: Control Output Bus provides an auxiliary data path to the peripheral device. This data path is normally used to transmit control information pertinent to the ongoing data transfer.

Timing: Control Output Bus signals are always active.

Schematic Location: Sheet 3, E8

## PFLAG

Full Name: Peripheral Flag

Driven By: Peripheral device

Received By: GPIO

Function: Peripheral Flag signals completion of the data transfer in progress (note that it does not signal termination of the data transfer interaction). When FULL handshake mode is selected, Peripheral Flag indicates when the peripheral device is willing to participate in the next data transfer.

Timing: Peripheral Flag may be driven at any time by the peripheral device. Refer to the "Handshake Timing" paragraph for additional timing data on Peripheral Flag operation.

Schematic Location: Sheet 2, C1

## PCNTL

Full Name: Peripheral Control

Driven By: GPIO

Received By: Peripheral device

Function: Peripheral Control signals the beginning of a data transfer. (Note: No signal defines the beginning of a sequence of transfers; PCNTL defines the beginning of each data exchange.)

Timing: Peripheral Control is asserted for each data bus transfer. Refer to the "Handshake Timing" paragraph for additional timing data on Peripheral Control operation.

Schematic Location: Sheet 2, B8

## PEND

Full Name: Peripheral End

Driven By: Peripheral device

Received By: GPIO

Function: Peripheral End signals termination of the current data transfer interaction.

Timing: Peripheral End timing is the same as Data Input Bus timing, and may be asserted at any time.

Schematic Location: Sheet 2, E8

## PRESET

| | |
|---|---|
| Full Name: | Peripheral Reset |
| Driven By: | GPIO |
| Received By: | Peripheral device |
| Function: | PRESET signals the peripheral device to return to a power-up state of readiness. |
| Timing: | PRESET is asserted whenever the I/O channel asserts Reset (RST), or asserts Power On (PPON), or performs a Write_Control (Device Clear) operation. |
| Schematic Location: | Sheet 2, B8 |

## HANDSHAKE TIMING

Data is transferred between peripheral device and I/O channel (backplane) in a synchronous manner using the backplane signal SRQ and peripheral signals PCNTL, PFLAG, PDIR, and PEND. SRQ is asserted by the GPIO card when it is ready for the next backplane data transfer. PCNTL and PFLAG provide a two-line handshake for data transfers to the device. PDIR is driven by the GPIO to indicate the direction of data. PEND is asserted by the device to request termination of the transfer.

Data handshake timing depends on whether input data or output data is transferred, and whether the peripheral simply acknowledges data transfer or if data transfer must be postponed until the peripheral is ready. If the peripheral simply acknowledges data transfer, the handshake mode is referred to as "Pulse". If data transfer must be postponed until the peripheral is ready to continue the handshake mode is referred to as "Full".

If an external handshake is not required by the application, the internal handshake can be enabled and a one-shot will provide an internal FLAG signal to replace PFLAG. The internal FLAG will be asserted approximately 3 usec after PCNTL is asserted. You can increase this delay by adding an additional timing capacitor. If Internal Handshake Mode is enabled, then in the following descriptions the internal FLAG replaces PFLAG and the card operates in Pulse Handshake Mode regardless of the switch setting.

If a handshake is not required and the delay incurred with internal handshake is undesirable, the PCNTL output can be connected to the PFLAG input. In this case the pulse width of PCNTL/PFLAG may be very short, so to ensure reliable operation it is recommended that only input following clocking mode be used (Input Clocking Mode No. 0 or No. 3).

### Data Handshake Overview

A single data transfer begins when the GPIO card (and possibly the peripheral) is ready for data transfer. The GPIO card is the master in a master-slave relation with the peripheral, and begins the transfer with the assertion of the PCNTL signal.

PCNTL signals to the peripheral that the transfer has begun and the peripheral responds by gating read data onto the lines or accepting write data. When the data transfer is complete (i.e., the peripheral is sourcing read data or has accepted write data), the peripheral asserts signal PFLAG. At this point, if the "Pulse" handshake mode was selected, the GPIO card may begin the next data transfer. If the "Full" handshake mode was selected, the GPIO card will wait until the signal PFLAG returns to the ready state (i.e., PFLAG is deasserted).

Data transfers continue under PCNTL, PFLAG control until a terminating condition arises. One of two conditions will normally terminate data transfers: The channel asserts CEND (channel end) if it has detected an end condition (such as character match or transfer count completed), or the peripheral asserts signal PEND if it detects an end condition.

## Output Handshake Timing

Figure 3-2 illustrates output data transfer timing with the GPIO in full handshake mode. All conditions significant to output data transfer are shown, including: duration of the order(write_data); backplane write data transfers; the backplane line CEND; GPIO lines SRQ, DOUT[15:0], PDIR, and PCNTL; and the peripheral line PFLAG.

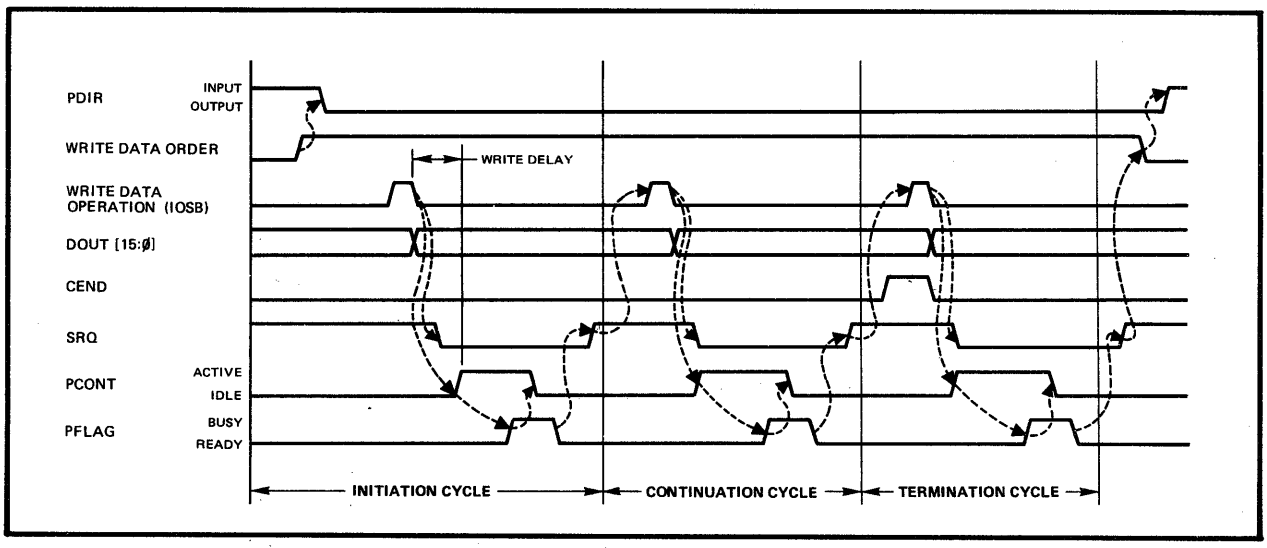



Figure 3-2. Output Data Transfer Timing

The diagram describes the initiation, continuation (normal transfer), and the termination cycles of an output data transaction. A transfer cycle follows a prescribed sequence of events as follows:

1. Initiation begins when the Write_order (write_data) is received. The PDIR line is asserted to show that an output data transaction is in progress. The PEND latch on the GPIO card is cleared to remove any old end conditions. SRQ is asserted (unless the GPIO is in "full" handshake mode and PFLAG is not ready) and GPIO waits for the first data value.

2. Write_data strobes the write data into the Output Data register and the data appears on DOUT[15:0].

3. SRQ is deasserted and, after the write delay (settling time for outputs) PCNTL is asserted to indicate data available to the peripheral. The GPIO then waits until ...

4. PFLAG is asserted by the peripheral to indicate data accepted.

5. PCNTL is then deasserted to acknowlege data acceptance. At this point the transfer is complete if the pulse handshake mode was selected. If full handshake mode was selected, then the GPIO card idles until PFLAG becomes ready (deasserted).

6. The GPIO will reassert SRQ to indicate that the transfer has completed.

   a. If CEND and DEND are deasserted, the process repeats at step 2 with the next write_data operation.

   or,

   b. If the I/O channel asserted CEND (channel end) with the current data operation, no more output data transfers are expected.

   or,

   c. If the peripheral asserted PEND (peripheral end) with the current data operation; the process will repeat at step 2., the GPIO will assert DEND (device end) with the backplane transfer, and the transaction will stop after step 6. is reached again.

## Input Handshake Timing

Figure 3-3 illustrates input data transfer timing with the GPIO in full handshake mode. All conditions significant to input data transfer are shown, including: duration of the order (read_data); backplane read data transfers; the backplane line CEND; GPIO lines SRQ, DIN[15:0], PDIR, and PCNTL; and the peripheral lines PFLAG and PEND.

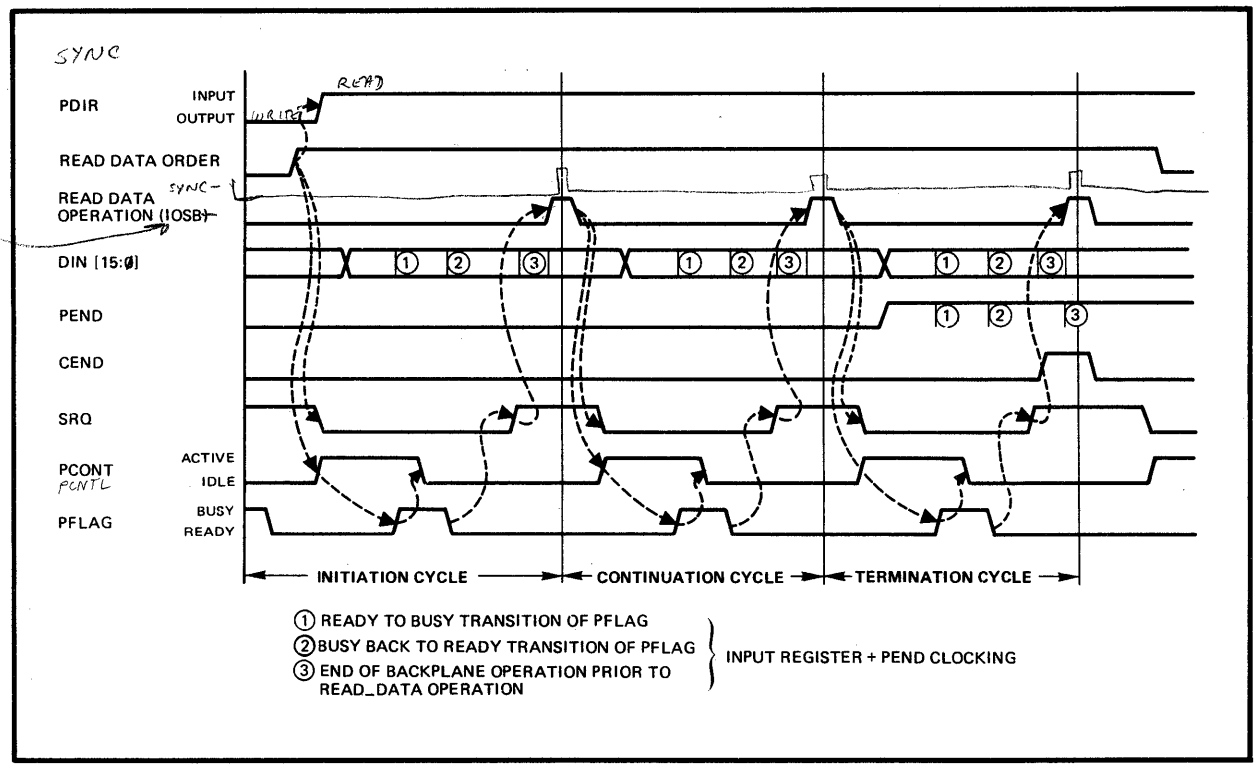



Figure 3-3. Input Data Transfer Timing

The diagram describes the initiation, continuation (normal transfer), and termination cycles of an input data transaction. A transfer cycle follows a prescribed sequence of events as follows:

1. Initiation begins when the Write_order (read_data) is received. The PDIR line is deasserted to show that an input data transaction is in progress.

2. SRQ is deasserted and PCNTL is asserted to indicate that the GPIO is ready for data from the peripheral. The GPIO then waits.

3. Data is sourced by the peripheral.

4. PFLAG is asserted by the peripheral to indicate that data is available. In clocking mode No. 1, data will be clocked at the time of PFLAG (indicator No. 1).

5. PCNTL is then deasserted to acknowlege data acceptance. If pulse handshake mode was selected, the transfer is complete. If full handshake mode was selected, the GPIO idles until PFLAG becomes ready (deasserted). In clocking mode No. 2, data will be clocked at the deassertion of PFLAG (indicator No. 2). In this case, full mode handshake should be used to prevent the GPIO from progressing to completion of the transfer before data is clocked.

6. The GPIO will then assert SRQ to prompt the channel to Read_data.

7. The channel performs a Read_data. In clocking mode 0 or 3, the data will have been clocked in by the end of the backplane operation prior to the Read_Data. If CEND and DEND are deasserted, the GPIO will assert SRQ when the cycle completes to prompt the channel to Read_data, and the process repeats at step 2.

   or,

   a. If the channel asserted CEND (channel end) with the Read_data, no more input data transfers are expected, and a new handshake with the device is not initiated.

   or,

   b. If the peripheral asserted PEND at the time DIN[15:0] was clocked, no more input data transfers are expected, the GPIO asserts DEND (device end) during the Read_data, and a new handshake with the device is not initiated.

## Abnormal Termination

The I/O channel may cause an abnormal termination at any time by issuing an abort command (refer to Write_command) which immediately terminates any data transfer in progress and disconnects the I/O channel. The peripheral can perform a similar function by stopping any transfers in progress (i.e., not asserting PFLAG in response to PCNTL), and by causing an interrupt on STS[1] or STS[0] in order to cause an ARQ. (Note that interrupts on that input must be enabled, refer to the paragraph "Control Output Register".) A program must then respond to the ARQ by issuing an abort command.

## ARQ

There are two sources of ARQ (Attention Request) on the GPIO card: acknowledgement of the abort command (ADT), and asynchronous event sense (AES).

## Aborted ARQs

If the GPIO card has a valid subchannel (i.e., a transaction is in progress) and it receives an abort command, it will abort the subchannel and drive the ARQ bit in the Sense register. The card will not respond to SRQ polls. If ARQs are enabled (ARE), the card will also assert the ARQ signal and respond to ARQ polls. The card will respond to a read_status with the ADT status byte. The low four bits of the status byte will contain the subchannel address. If there is no valid subchannel, nothing will happen.

## Interrupt ARQs

There are two status inputs, STS[0] and STS[1], that can cause an asynchronous event to sense ARQ. Signals INT.EN and INT0 or INT1 in the device dependent control register must be set to enable interrupts from STS[0] or STS[1], respectively. If an STS input is enabled to interrupt, the deasserted to asserted edge of the input causes an interrupt. When interrupts on one of the status inputs are disabled, the Interrupt flip-flop for that input is cleared and no interrupts will be detected on that input until it is reenabled. (Any interrupts occurring between 0 and 120 nsec after the IOSB on which the interrupt enable is set may or may not be detected due to propagation delays.)

When an interrupt is detected, the GPIO card will assert the ARQ bit in the Sense register. If ARQs are enabled, it will also assert the ARQ signal and respond to ARQ polls. The card will respond to read status with an AES status byte unless an ADT status byte is also present. If an ADT status byte and an AES status byte are both present, the first read status will return the ADT status and ARQ will remain until the AES byte is read by a second read status.

## Clearing ARQ Conditions

A reset to the card (PPON, IFC, or DCL) resets INT.EN, INT0, and INT1. It also removes any pending AES or ADT status bytes and deasserts ARQ.

An ADT status byte is cleared by reading it, by resetting the GPIO card, or by connecting a new subchannel. The last condition should not occur in normal CHANNEL I/O operation. An AES status byte is cleared by reading it, by resetting the card, or by disabling the interrupt that caused it.

The GPIO card is the slave in a master/slave relation with the I/O channel adapter. As such, backplane operation is driven by the channel adapter via standard CHANNEL I/O bus operations. All CHANNEL I/O level 1 bus operations are supported by the GPIO card. Bus operations are specified by I/O channel signals SYNC, POLL, BP[1:0], DOUT, and AD[3:0] (see table 3-1).

Additionally, the GPIO card will respond to a special backplane operation for purposes of learning an operating (card) address.

Table 3-1. Operations Summary

| SYNC | POLL | DOUT | BP[1:0] | AD[3:0] | BACKPLANE OPERATION |
|---|---|---|---|---|---|
| 0 | X | 1 | 00 | card address | assign_address * |
| 0 | 1 | X | 00 | X | poll_srq_grp_0 |
| 0 | 1 | X | 01 | X | poll_srq_grp_1 |
| 0 | 1 | X | 10 | X | poll_arq_grp_0 |
| 0 | 1 | X | 11 | X | poll_arq_grp_1 |
| 1 | 0 | 0 | 00 | subchannel address | read-data |
| 1 | 0 | 0 | 01 | card address | read_sense |
| 1 | 0 | 0 | 10 | X | no_operation |
| 1 | 0 | 0 | 11 | card address | read_status |
| 1 | 0 | 1 | 00 | subchannel address | write_data |
| 1 | 0 | 1 | 01 | card address | write_control |
| 1 | 0 | 1 | 10 | subchannel address | write_order |
| 1 | 0 | 1 | 11 | card address | write_command |

* assign_address requires UAD asserted

## ADDRESS ASSIGNMENT OPERATION

Address assignment is required for the GPIO card to qualify backplane operations. The GPIO card address is programmed by the I/O channel via a special Write_data operation. The Write_data is additionally qualified by backplane signal UAD and the GPIO card state "no adapter address currently assigned".

A qualified Write_data operation assigns the GPIO card the address specified by I/O channel signals AD[3:0], and the card does not use the signals DB[15:0]. Signals DB[15:0] may be used, however, to drive signal UAD on the I/O channel itself.

The address assignment must be performed before any other I/O channel operation can be recognized. Also, once an address is assigned, further address assignment operations will be ignored until the I/O channel issues IFC or PPON to the GPIO card.

## POLL OPERATIONS

Poll operations, SRQ or ARQ, directly reflect requests for subchannel or GPIO card service, respectively. The frequency of poll operations determines the maximum throughput and worst case latency in data transfer.

Only one of the poll operations of each type, SRQ and ARQ, will be responded to by the GPIO card. The response depends on the previously assigned addresses for subchannel and card (see table 3-2).

Table 3-2. Poll Operations

| BACKPLANE OPERATION | REQUIRED ADDRESS * |
|---|---|
| poll_srq_grp_0<br>poll_srq_grp_1 | subchannel address 0-7<br>subchannel address 8-15 |
| poll_arq_grp_0<br>poll_arq_grp_1 | card address 0-7<br>card address 8-15 |
| * only addresses in this range will produce a response | |

If no subchannel address or card address has been assigned by the I/O channel adapter, no SRQ or ARQ (respectively) response will be generated by the GPIO card.

# OUT-OF-SUBCHANNEL OPERATIONS

Card operations, read_sense, write_control, read_status, and write_command directly control the GPIO card and its operation with the I/O channel. The sense and control operations affect signal level interaction, while status and command operations affect subchannel interaction.

## Read_Sense

Read_sense may occur at any time and immediately gates the sense byte to the backplane. The sense byte format is:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RFC | PST | PRE | NMI | r | ARE | r | ARQ |

where,

RFC = Ready For Command. This bit is ALWAYS asserted by GPIO.

PST = Passed Self Test. This bit is ALWAYS asserted by GPIO.

PRE = Present. This bit is ALWAYS asserted by GPIO.

NMI = Non-Maskable Interrupt. This bit is NEVER asserted by GPIO.

ARE = Attention Requests Enabled. This bit is asserted when GPIO is enabled to respond to arq polls.

ARQ = Attention Request. This bit is asserted when GPIO is requesting attention.

r = reserved (always returns 0).

## Write_Control

Write_control may occur at any time and immediately invokes the control action specified by the control byte. The control byte format is:

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| r | r | DCL | DEN | NMK | RQA | ARE | ARD |

where,

r = reserved

DCL = Device Clear. This bit establishes an addressed device clear condition.

DEN = Device Enable. This bit terminates an addressed device clear condition.

NMK = Non-Maskable_interrupt acknowledge. Ignored by GPIO.

RQA = Request Attention. Ignored by GPIO.

ARE = Attention Request Enable. Sets the GPIO ARE flip-flop enabling assertion of the ARQ I/O channel signal.

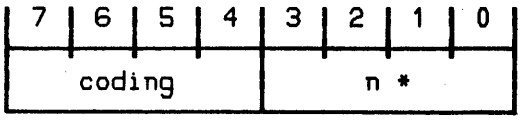
ARD = Attention Request Disable. Resets the GPIO ARE flip-flop disabling assertion of the ARQ I/O channel signal.

**NOTE**

If both DCL and DEN are asserted, the state of the addressed device clear condition toggles. Similarly, if both ARE and ARD are asserted, the state of the GPIO ARE flip-flop toggles.

## Read_Status

Read_status may only occur after an Attention Request (ARQ), because it may reset the reason for ARQ. The status byte indicates the reason for ARQ. The format of the status byte is:




where,

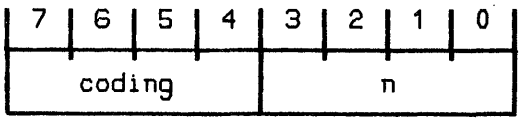
| STATUS | CODING ** | |
|---|---|---|
| RFC | 0 = | Ready For Command. GPIO is ALWAYS ready for command and will not arq with RFC status. |
| AES | 1 = | Asynchronous Event Sensed. Indicates that the GPIO has sensed an interrupt on STS[1] or STS[0]. The interrupt must be enabled in order to cause this condition. |
| ADT(n) | 3 = | Aborted - subchannel n. GPIO subchannel transaction terminated. |

* - n is only valid for the ADT(n) coding, n is undefined otherwise.

** - codings not specified may have unpredictable results.

## Write_Command

Write_command may occur at any time and commands operation of the GPIO subchannel. The command byte format is:




where,

| COMMAND | CODING * | |
|---|---|---|
| ABT(n) | 0 = | Abort - subchannel n. Aborts the currently assigned GPIO subchannel regardless of (n) and disallows further subchannel operations. |
| STT(n) | 2 = | Start Transaction - subchannel n. Sets GPIO subchannel to n and allows subchannel operations. |

* - codings not specified may have unpredictable results.

## IN-SUBCHANNEL OPERATION

Subchannel operations read_data, write_data, and write_order compose the interactions of the subchannel with the backplane. All interactions begin with a write_order operation which specifies the source or destination for succeeding data operations.

Subchannel operations are SRQ driven. Specifically, verification that srq is asserted (by poll_srq) should be performed before every subchannel operation. This insures that the GPIO subchannel is ready and can accurately complete the subsequent step in the subchannel interaction.

It is possible to invoke a subchannel operation without checking if SRQ is asserted. This may be desirable in closed loop operations where data writes are immediately followed by data reads, due to the fact that only one handshake circuit exists.

## Subchannel Operation Summary

The three subchannel operations

Write_order( order )

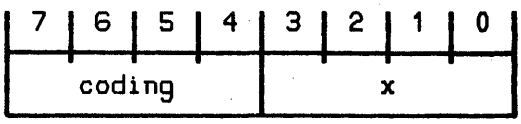
Write_data ( data [, end])

Read_data ( data [, end])

are described in detail in the following paragraphs.

## Write_Order

Write_order operations may occur whenever the subchannel is in connection. The write_order specifies the current interaction. The order byte format is:




where,

| ORDER | CODING * | | |
|---|---|---|---|
| IDY | 0 | = | Identify |
| DIS | 3 | = | Disconnect |
| RS | 4 | = | Read_peripheral_status |
| WC | 5 | = | Write_peripheral_control |
| RD | 6 | = | Read_peripheral_data |
| WD | 7 | = | Write_peripheral_data |

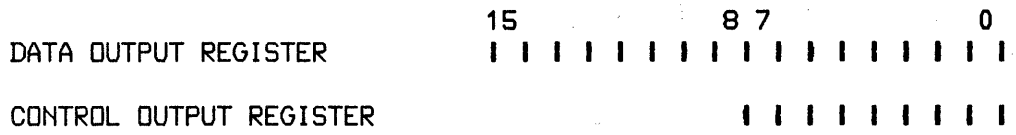
* codings not specified may have unpredictable results.

Use of Write_orders is detailed in the paragraph "Peripheral Interactions".

## Write_Data

Write_data_operations may occur whenever the subchannel is in connection. Data is immediately latched from the backplane into one of two output (write) registers (Data Output register and Control Output register). The write register is selected by the current interaction.

## Write Register Summary




## Data Output Register

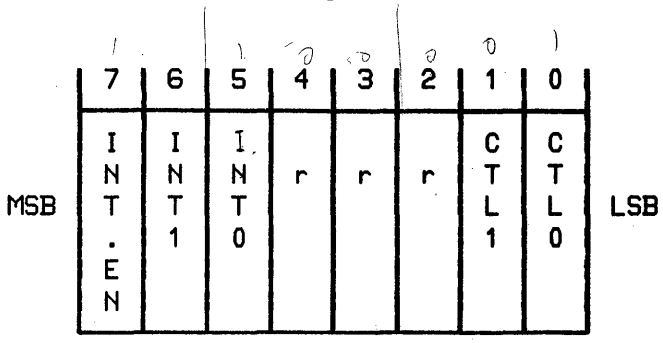

The Data Output register holds the positive true state of the signals DOUT[15:0]. The data is clocked by the Write_data_operation into the Data Output register. The data remains in the Data Output register until the next write to the register or until a GPIO reset. Disconnection or completion of the current interaction will not affect the Data Output register.

The GPIO initiates a handshake with the peripheral at the completion of the Write_data_operation.

DEND: Reflects PEND

Selected by: Write_order(WD)
(RD)

## Control Output Register



| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MSB | INT.EN | INT1 | INT0 | r | r | r | CTL1 | CTL0 | LSB |

where,

CTL[1:0] = Control Output Signals

r = Reserved

INT[1:0] = Status Interrupt Enables

INT.EN = Interrupt enable (global mask for Status Interrupts)

The Control Output register holds the positive true state of the outputs CTL[1:0]. Additionally, interrupt enables are contained in the Control Output register.

Data is clocked by the Write_data operation into the Control Output register. The data remains in the Control Output register until the next write to the register or until a GPIO reset occurs. Channel disconnects, aborts, or completion of interactions will not affect the contents of the Control Output register.

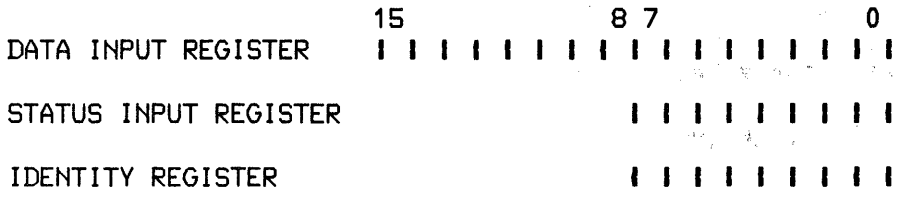
DEND: Asserted Every Operation

Selected by: Write_order(WC)
(RS)

## Read_Data

Read_data operations may occur whenever a subchannel is connected. Data is immediately sourced onto the backplane from one of three input (read) registers (Data Input register, Status Input register, and Identity register). The read register is selected by the current interaction.

## Read Register Summary




## Data Input Register


The Data Input register holds the positive true state of the inputs DIN[15:0] as of the last data input clock. Refer to the paragraphs "Input Clocking" and "Input Handshake Timing" for information on when input clocks occur.

The GPIO initiates a handshake with the peripheral at the completion of the Read_data_operation if CEND and DEND are both deasserted.

DEND: Reflects PEND

Selected by: Write_order(RD)
(WD)

## Status Input Register

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| MSB | INT.EN | INT1 | INT0 | r | CTL1 | CTL0 | STS1 | STS0 | LSB |

where,

STS[1:0] = Status Input Signals

CTL[1:0] = Control Output Signals

INT[1:0] = Status Interrupt Enables

INT.EN = Interrupt Enable (global mask for Status Interrupt)

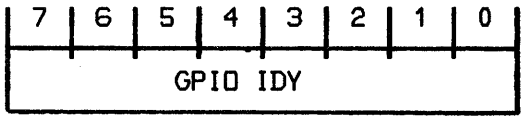
r = reserved (always returns 0)

The Status Input register holds the positive true state of the STS[1:0] signals. Additionally, the Status Input register returns the contents of the Control Output register.

DEND: Asserted every operation.

Selected by: Write_order(RS) READ STATUS
(WC) WRITE CONTROL

## Identity Register




where,

GPIO IDY = 1 (Per CHANNEL I/O standard assignment)

The Identity register always reflects the GPIO identity. No operation can alter the contents of the Identity register.

DEND: Asserted Every Operation

Selected by: Write_order (IDY)

# GPIO OPERATION

GPIO accomplishes I/O via sequences of low level operations called "interactions" These interactions have specific constructs to insure reliable data transfer. Also, these interactions occur "in subchannel" which requires initialization before they can begin.

## Initialization

Two phases of initialization must occur in GPIO operation: The lowest level of initialization is GPIO card address assignment, which is required before any other backplane operation can take place (refer to the paragraph "Address Assignment Operation" for details). Next, once an address has been assigned, GPIO requires subchannel connection in order to perform useful data transfers.

**Establishing Subchannel Connection.** Subchannel connection can be established (initialized) via a Write_adapter_command (STT) operation. The extension field of the command coding specifies which subchannel address (0 thru 15) is to be used for GPIO subchannel operations.

Until a subchannel is assigned, GPIO will ignore all I/O channel operations requiring the subchannel address for qualification. Once the subchannel is established, GPIO is ready to begin an interaction with the I/O channel. Specifically, as soon as a subchannel is assigned the GPIO card asserts SRQ to request an order for the first interaction.

**SRQ Operation.** Once the subchannel is established, the GPIO asserts SRQ to inform the I/O channel that it is ready to begin an interaction. After an order has been written, the condition of readiness depends on the order. For the read_data_order and write_data_order, SRQ is only asserted when the GPIO is ready for the next data transfer (see the paragraph "Handshake Timing" for further information). For all other orders, the GPIO is always ready for the next operation, and therefore always asserts SRQ.

## Interactions

An interaction is a logically indivisible transfer between channel and the GPIO card. In most cases, the transfer also involves the peripheral device. Specifically, an interaction consists of a write_order operation followed in most cases by one or more read_data or write_data operations (see table 3-3).

Table 3-3. Interactions

| BP[1:0] & DOUT | DB[15:0] | CEND or DEND |
|---|---|---|
| write_order | order coding | |
| write/read_data | data | |
| write/read_data | data | |
| write/read_data | data | |
| write/read_data | data | |
| . . . | . . . | |
| write/read_data | data | |
| write/read_data | data | end |

**Initiation.** An interaction is initiated by a write_order operation. The purpose of write_orders is to select the proper data path between the I/O channel and GPIO registers and to properly synchronize handshake when that path is to the data registers (input or output).

**Progression.** After the interaction has been initiated, if a data part is associated with this interaction, the data part will progress. Progression continues with each data operation (read or write), transferring words (16 bits) or bytes between the I/O channel and the GPIO register specified by the order until termination occurs.

**Termination.** A normal termination may occur in one of two ways: The I/O channel may signal an end to the data part by asserting CEND, or the GPIO may signal an end by asserting DEND. If the current order is read_data_order or write_data_order, the peripheral causes the GPIO to assert DEND by asserting PEND. All other data transfers are always accompanied by DEND.

## Standard Interactions

To provide normal GPIO-type operation, several interactions are necessary. Beyond the standard interactions, the GPIO card is capable of variations to allow optimal operation for certain special peripheral devices. These variations are noted in the paragraph "Special Interactions".

**Standard Interaction Summary.** Standard interactions are summarized below and described in the following paragraphs.

IDENTITY INTERACTION

DATA INPUT INTERACTION

DATA OUTPUT INTERACTION

STATUS INPUT INTERACTION

CONTROL OUTPUT INTERACTION

**Identity Interaction.** The identity interaction is intended for transferring the identity of the GPIO card. The card_ID_byte of the GPIO card is 1, as specified by the CHANNEL I/O standard. Because the default values of the remainder of the identity message are correct for the GPIO, the message will always have a data part length of 1. Specifically, even in the event of specifying a data part larger than one to the channel adapter, the GPIO card uses DEND to terminate the interaction with the first read_data.

**Data Input Interaction.** The data input interaction is used for transferring data from the peripheral device to the I/O channel adapter. It transfers one logical record and normally completes on expiration of the transfer length counter, or a character match in the I/O channel adapter.

The length of the data part of the interaction depends on the peripheral device. The logical record may be as small as one byte, as in the case of a paper-tape reader, where each character must be examined to determine if the transfer should continue. Or, it may have infinite length, as in the case of a measurement sensor, where data may be input continuously (for days) until the transfer in progress stops. Most typically, however, the data part length has a direct correspondence to a physical record in the peripheral device.

Completing a data input interaction allows the GPIO card to begin a new interaction which may have a logical relation to previous interactions. This logical division allows other interactions to occur, possibly transacting status or control information related to the input interaction.

**Data Output Interaction.** The data output interaction is used for transferring data from the I/O channel adapter to the peripheral device. It transfers one logical record and normally completes on expiration of the transfer length counter in the I/O channel adapter.

Refer to the paragraph "Data Input Interaction" for information on logical record size.

**Status Input Interaction.** The status input interaction is used for transferring the state of the status inputs and the Configuration register to the I/O channel. Because this information has a static nature, status input interactions always have a data part length of one. Specifically, even in the event of specifing a data part larger than one to the I/O channel adapter, the GPIO card signals end to terminate the interaction with the first read_data.

**Control Output Interaction.** The control output interaction is used to statically set the state of peripheral interface signals CTL[1:0], and the interrupt enables. The data part length of the control output interaction, as with the status input interaction, will be forced to one.

# SPECIAL INTERACTIONS

Certain interactions are accomodated by the GPIO card to minimize backplane overhead. These interactions are special because they do not strictly follow the CHANNEL I/O constructs for interactions.

## Status/Control Interactions

Status/control interactions provide reduced overhead when multiple Status Input register or Control Output register operations are required. In particular, the initiating write_order operation can be omitted on the second and successive qualified interactions. Qualified interactions include only interactions conducted with the Status Input register or the Control Output register.

**Status/Control Interaction Format.** The first status/control interaction is initiated by a write_order (RS or WC). From then until a new write_order occurs, all write_data operations will write to the Control Output register and all read_data operations will read the Status Input register.

## Data Interactions

Data interactions provide reduced overhead when multiple data input register and/or data output register operations are required. In particular, the initiating write_order operation can be omitted on the second and successive qualified interactions. Qualified interactions include only interactions conducted with the Data Input register or the Data Output register.

**Data Interaction Format.** The first data interaction is initiated by a write_order (RD or WD). From then until a new write_order occurs, all write_data operations will write to the Data Output register and all read_data operations will read the Data Input register.

# MAINTENANCE

SECTION IV

The only maintenance recommended by Hewlett-Packard for the GPIO is to return a malfunctioning card to Hewlett-Packard for repair.

To determine if a card is malfunctioning, perform the following:

1. Remove cable and connect the test hood, part number 1251-8003, to connector J2 on the card.

2. Set the card's switches as required by the card verification program. Refer to Section II, tables 2-1, 2-2, and 2-3 for switch information.

3. Run the card verification program. Refer to the appropriate host computer system manual for information on running this program.

If the system determines that the GPIO is malfunctioning, remove the card from the system and return it to Hewlett-Packard. Refer to "Reshipment" in Section II for instructions on shipping the card.

If desired, isolation to a defective part may be performed. Please be advised, however, that such work is at your discretion and is your responsibility; moreover, NOTE THAT CUSTOMER REPAIR OR MODIFICATION OF THE GPIO CARD WILL INVALIDATE WARRANTY AND RENDER THE CARD INELIGIBLE FOR EXCHANGE OR REPAIR BY HEWLETT-PACKARD COMPANY. If such service is performed, the replaceable parts information in Section V and the schematic logic diagrams in Section VI will be of assistance.

# REPLACEABLE PARTS

SECTION V

This section contains information for ordering replaceable parts for the GPIO. Table 5-1 contains a list of replaceable parts, table 5-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 5-1, and figure 5-1 shows the locations of the parts on the GPIO card.

Table 5-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 5-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

## ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the kit containing the part (refer to the product identification information supplied in Section 2).

2. Description and function of the part.

3. Quantity required.

## Table 5-1. HP 27112A Replaceable Parts

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|---|
| | 27112-60001 | 4 | 1 | PCA CSGIO GPIO | 28480 | 27112-60001 |
| A2 | 1820-2862 | 7 | 2 | IC-DS 3667 | 28480 | 1820-2862 |
| A3 | 1820-1917 | 1 | 5 | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| A4 | 1820-2862 | 7 | | IC-DS 3667 | 28480 | 1820-2862 |
| A5 | 1820-2024 | 3 | 1 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN74LS244N |
| A6 | 1820-1196 | 8 | 2 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74LS174N |
| A7 | 1820-1917 | 1 | | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| A8 | 1820-0668 | 7 | 1 | IC BFR TTL NON-INV HEX 1-INP | 01295 | SN7407N |
| A9 | 1820-1568 | 8 | 1 | IC BFR TTL LS BUS QUAD | 01295 | SN74LS125AN |
| A10 | 1820-1240 | 3 | 4 | IC DCDR TTL S 3-TO-8-LINE 3-INP | 01295 | SN74S138N |
| A11 | 1820-1240 | 3 | | IC DCDR TTL S 3-TO 8-LINE 3-INP | 01295 | SN74S138N |
| A12 | 1820-1275 | 4 | 1 | IC GATE TTL S NOR DUAL 5-INP | 01295 | SN74S260N |
| A13 | 1820-0688 | 1 | 1 | IC GATE TTL S NAND DUAL 4-INP | 01295 | SN74S20N |
| A14 | 1820-1201 | 6 | 2 | IC GATE TTL LS AND QUAD 2-INP | 01295 | SN74LS08N |
| A15 | 1820-1144 | 6 | 2 | IC GATE TTL LS NOR QUAD 2-INP | 01295 | SN74LS02N |
| A16 | 1820-0694 | 9 | 1 | IC GATE TTL S EXCL-OR QUAD 2-INP | 01295 | SN74S86N |
| B1 | 1820-2056 | 1 | 1 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74LS378N |
| B2 | 1820-1997 | 7 | 4 | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN | 01295 | SN74LS374N |
| B3 | 1820-2465 | 6 | 1 | IC DCDR TTL LS 3-TO-8-LINE | 34335 | AM25LS2538PC |
| B4 | 1820-1077 | 4 | 2 | IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD | 01295 | SN74S157N |
| B5 | 1820-1077 | 4 | | IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD | 01295 | SN74S157N |
| B6 | 1820-1321 | 1 | 1 | IC COMPTR TTL S MAGID 4-BIT | 01295 | SN74S85N |
| B7 | 1820-1197 | 9 | 3 | IC GATE TTL LS NAND QUAD 2-INP | 01295 | SN74LS00N |
| B8 | 1820-1282 | 3 | 3 | IC FF TTL LS J-K BAR POS-EDGE-TRIG | 01295 | SN74LS109AN |
| B9 | 1820-1240 | 3 | | IC DCDR TTL S 3-TO-8-LINE 3-INP | 01295 | SN74S138N |
| B10 | 1820-1240 | 3 | | IC DCDR TTL S 3-TO-8-LINE 3-INP | 01295 | SN74S138N |
| B11 | 1820-0686 | 9 | 1 | IC GATE TTL S AND TPL 3-INP | 01295 | SN74S11N |
| B12 | 1820-1202 | 7 | 2 | IC GATE TTL LS NAND TPL 3-INP | 01295 | SN74LS10N |
| B13 | 1820-1112 | 8 | 2 | IC FF TTL LS D-TYPE POS-EDGE-TRIG | 01295 | SN74LS74AN |
| B14 | 1820-0693 | 8 | 2 | IC FF TTL S D-TYPE POS-EDGE-TRIG | 01295 | SN74S74N |
| B15 | 1820-1201 | 6 | | IC GATE TTL LS AND QUAD 2-INP | 01295 | SN74LS08N |
| B16 | 1820-1208 | 3 | 1 | IC GATE TTL LS OR QUAD 2-INP | 01295 | SN74LS32N |
| C1 | 0180-0116 | 1 | 1 | CAPACITOR-FXD 6.8UF+-10% 35VDC TA | 56289 | 150D685X9035B2 |
| C1 | 1820-1282 | 3 | | IC FF TTL LS J-K BAR POS-EDGE-TRIG | 01295 | SN74LS109AN |
| C2 | 0180-1746 | 5 | 1 | CAPACITOR-FXD 15UF+-10% 20VDC TA | 56289 | 150D156X9020B2 |
| C2 | 1820-1282 | 3 | | IC FF TTL LS J-K BAR POS-EDGE-TRIG | 01295 | SN74LS109AN |
| C3 | 0160-4822 | 2 | 1 | CAPACITOR-FXD 1000PF +-5% 100VDC CER | 28480 | 0160-4822 |
| C3 | 1820-1216 | 3 | 1 | IC DCDR TTL LS 3-TO-8-LINE 3-INP | 01295 | SN74LS138N |
| C4 | 0160-4801 | 7 | 1 | CAPACITOR-FXD 100PF +-5% 100VDC CER | 28480 | 0160-4801 |
| C4 | 1820-1917 | 1 | | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| C5 | 1820-1997 | 7 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN | 01295 | SN74LS374N |
| C5- | | | | | | |
| C6 | 1820-1997 | 7 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN | 01295 | SN74LS374N |
| C7 | 1820-1917 | 1 | | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| C8 | 1820-1730 | 6 | 3 | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74LS273N |
| C9 | 1820-1730 | 6 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74LS273N |
| C10 | 1820-1196 | 8 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74LS174N |
| C11 | 1820-1199 | 1 | 2 | IC INV TTL LS HEX 1-INP | 01295 | SN74LS04N |
| C12 | 1820-1112 | 8 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG | 01295 | SN74LS74AN |
| C13 | 1820-1197 | 9 | | IC GATE TTL LS NAND QUAD 2-INP | 01295 | SN74LS00N |
| C14 | 1820-1202 | 7 | | IC GATE TTL LS NAND TPL 3-INP | 01295 | SN74LS10N |
| C15 | 1820-1197 | 9 | | IC GATE TTL LS NAND QUAD 2-INP | 01295 | SN74LS00N |
| C16 | 1820-1144 | 6 | | IC GATE TTL LS NOR QUAD 2-INP | 01295 | SN74LS02N |
| C61 | 0160-4832 | 4 | 57 | CAPACITOR-FXD .01UF +-10% 100VDC CER | 28480 | 0160-4832 |
| D1 | 1820-1917 | 1 | | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| D2 | 1820-1730 | 6 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG COM | 01295 | SN74LS273N |
| D3 | 1820-1997 | 7 | | IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN | 01295 | SN74LS374N |
| D4 | 1820-1211 | 8 | 10 | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D5 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D6 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D7 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D8 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D9 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D10 | 1820-1416 | 5 | 1 | IC SCHMITT-TRIG TTL LS INV HEX 1-INP | 01295 | SN74LS14N |
| D11 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| D12 | 1820-1199 | 1 | | IC INV TTL LS HEX 1-INP | 01295 | SN74LS04N |
| D13 | 1820-1449 | 4 | 1 | IC GATE TTL S OR QUAD 2-INP | 01295 | SN74S32N |
| D14 | 1820-0693 | 8 | | IC FF TTL S D-TYPE POS-EDGE-TRIG | 01295 | SN74S74N |
| D15 | 1820-1206 | 1 | 1 | IC GATE TTL LS NOR TPL 3-INP | 01295 | SN74LS27N |
| D16 | 1820-1212 | 9 | 1 | IC FF TTL LS J-K NEG-EDGE-TRIG | 01295 | SN74LS112AN |

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-1. HP 27112A Replaceable Parts (Continued)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|---|---|---|---|---|---|---|
| E1 | 1820-1217 | 4 | 1 | IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE | 01295 | SN74LS151N |
| E2 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| E3 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| E5 | 1820-1016 | 1 | 11 | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| E6 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| E7 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| E8 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| E10 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| E14 | 1820-1211 | 8 | | IC GATE TTL LS EXCL-OR QUAD 2-INP | 01295 | SN74LS86N |
| E15 | 1820-1437 | 0 | 1 | IC MV TTL LS MONOSTBL DUAL | 01295 | SN74LS221N |
| E16 | 1200-0796 | 8 | 1 | SOCKET-IC 8-CONT DIP DIP-SLDR | 28480 | 1200-0796 |
| F5 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| F6 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| F7 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| F8 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| F9 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| F10 | 1820-1016 | 1 | | IC DRVR TTL OR DUAL 2-INP | 01295 | SN75453BP |
| J1 | 1251-7276 | 0 | 1 | CONNECTOR-80 PIN | 28480 | 1251-7276 |
| J2 | 1251-7884 | 6 | 1 | CONNECTOR-50 PIN (MALE) | 28480 | 1251-7884 |
| R1 | 1810-0277 | 3 | 5 | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R2 | 1810-0277 | 3 | | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R3 | 0698-0084 | 9 | 2 | RESISTOR 2.15K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-2151-F |
| R4 | 0698-3155 | 1 | 1 | RESISTOR 4.64K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4641-F |
| R5 | 1810-0288 | 6 | 3 | NETWORK-RES 10-SIP MULTI-VALUE | 28480 | 1810-0288 |
| R6 | 1810-0277 | 3 | | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R7 | 1810-0277 | 3 | | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R8 | 1810-0288 | 6 | | NETWORK-RES 10-SIP MULTI-VALUE | 28480 | 1810-0288 |
| R9 | 1810-0277 | 3 | | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R10 | 1810-0288 | 6 | | NETWORK-RES 10-SIP MULTI-VALUE | 28480 | 1810-0288 |
| R11 | 1810-0162 | 5 | 1 | NETWORK-RES 14-DIP4.7K OHM X 13 | 11236 | 760-1-R4.7K |
| R12 | 0698-3154 | 0 | 1 | RESISTOR 4.22K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4221-F |
| R13 | 0698-0084 | 9 | | RESISTOR 2.15K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-2151-F |
| SW1 | 3101-2243 | 6 | 1 | SWITCH-DIP 8 ROCKER | 28480 | 3101-2243 |
| SW2 | 3101-2340 | 4 | 1 | SWITCH-ROCKER 5-1A DIP | 28480 | 3101-2340 |
| W1 | 1251-4670 | 2 | 3 | CONNECTOR-3 PIN (MALE) | 28480 | 1251-4670 |
| W1 | 1258-0141 | 8 | 3 | JUMPER-REM | 28480 | 1258-0141 |
| W2 | 1251-4670 | 2 | | CONNECTOR-3 PIN (MALE) | 28480 | 1251-4670 |
| W2 | 1258-0141 | 8 | | JUMPER-REM | 28480 | 1258-0141 |
| W3 | 1251-4670 | 2 | | CONNECTOR-3 PIN (MALE) | 28480 | 1251-4670 |
| W3 | 1258-0141 | 8 | | JUMPER-REM | 28480 | 1258-0141 |
| | 1480-0116 | 8 | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | 28480 | 1480-0116 |
| | 5041-2467 | 0 | 2 | HP/IO EXTRACTOR (HANDLE ) | 28480 | 5041-2467 |
| | 27112-80001 | 6 | 1 | P/C BOARD (BLANK) | 28480 | 27112-80001 |

See introduction to this section for ordering information
*Indicates factory selected value

Table 5-2. Manufacturer's Code List

| MFR NO. | MANUFACTURER | ADDRESS | ZIP |
|---|---|---|---|
| 01121 | Allen Bradley Company | Milwaukee, Wi. | 53204 |
| 01295 | Texas Instruments, Inc.<br>Semiconductor Components Division | Dallas, Tx. | 75222 |
| 04713 | Motorola Semiconductor Products | Phoenix, Az. | 85008 |
| 07263 | Fairchild Semiconductor Division | Mountain View, Ca. | 94042 |
| 08505 | Tektest, Inc.<br>E-Z Hook Test Products Division | Arcadia, Ca. | 91006 |
| 11236 | CTS of Berne, Inc. | Berne, In. | 46711 |
| 12969 | Unitrode Corporation | Watertown, Ma. | 02172 |
| 24546 | Corning Glass Works (Bradford) | Bradford, Pa. | 16701 |
| 27014 | National Semiconductor Corporation | Santa Clara, Ca. | 95051 |
| 28480 | Hewlett-Packard Company<br>Corporate HQ | Palo Alto, Ca. | 94304 |
| 34335 | Advanced Micro Devices, Inc. | Sunnyvale, Ca. | 94086 |
| 34649 | Intel Corporation | Mountain View, Ca. | 95051 |
| 56289 | Sprague Electric Company | North Adams, Ma. | 01247 |
| 75915 | Littelfuse, Inc. | Des Plaines, Il. | 60016 |

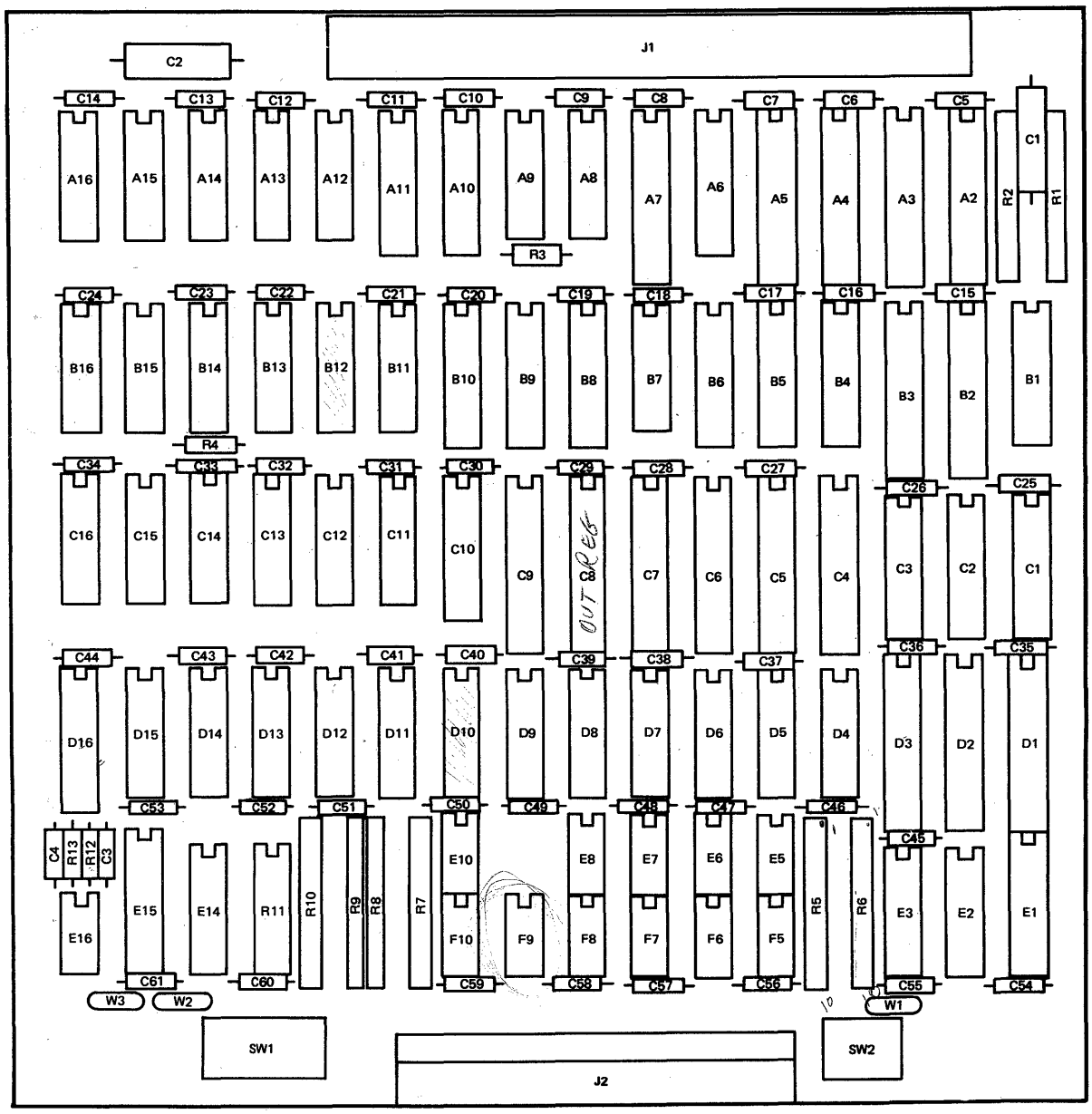



Figure 5-1. HP 27112A Parts Location Diagram

# SCHEMATIC DIAGRAMS

SECTION VI

This section contains schematic logic diagrams for the GPIO card.

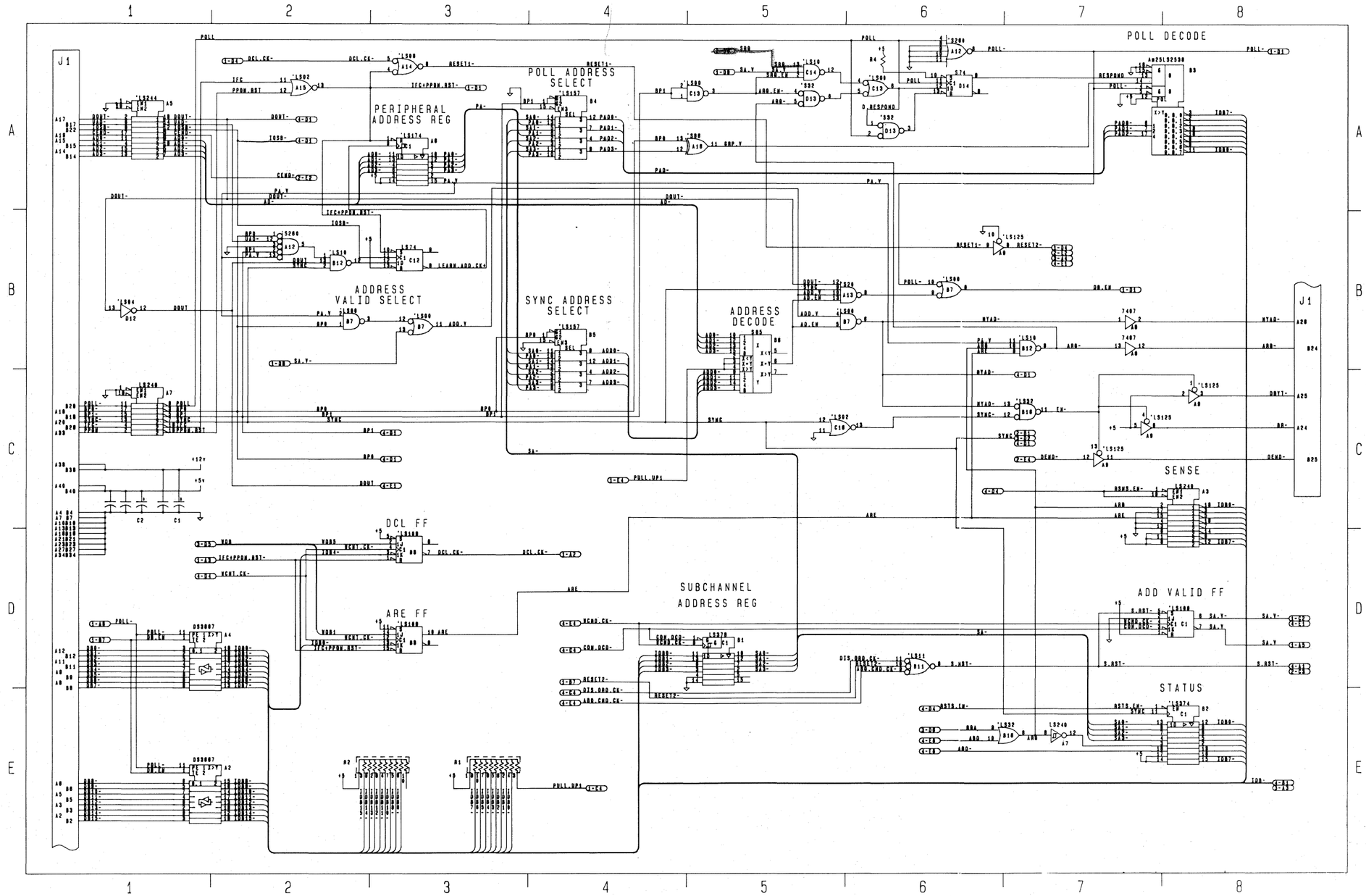



Figure 6-1. GPIO Schematic Logic Diagram (Sheet 1 of 4)

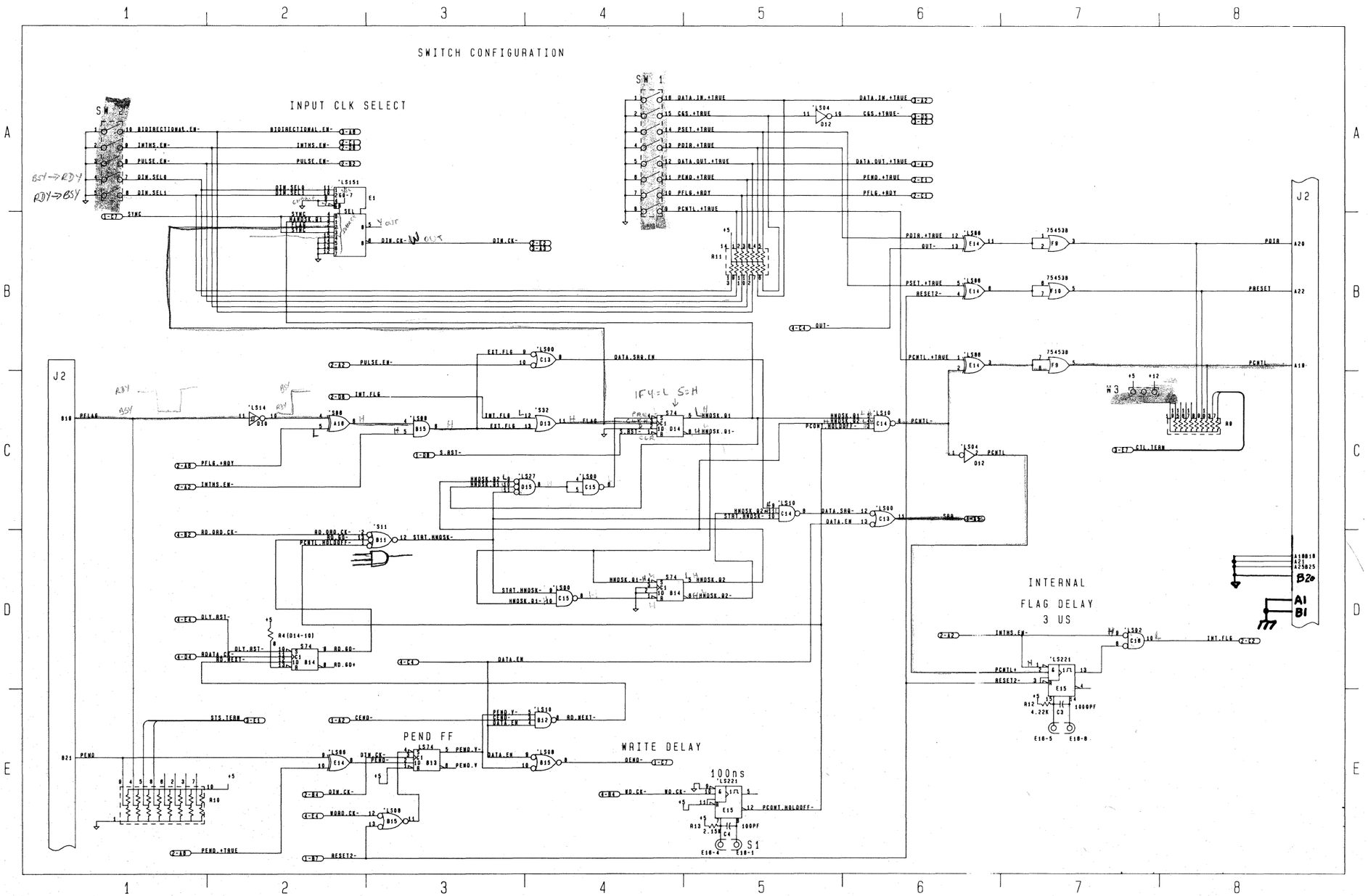



Figure 6-1. GPIO Schematic Logic Diagram (Sheet 2 of 4)

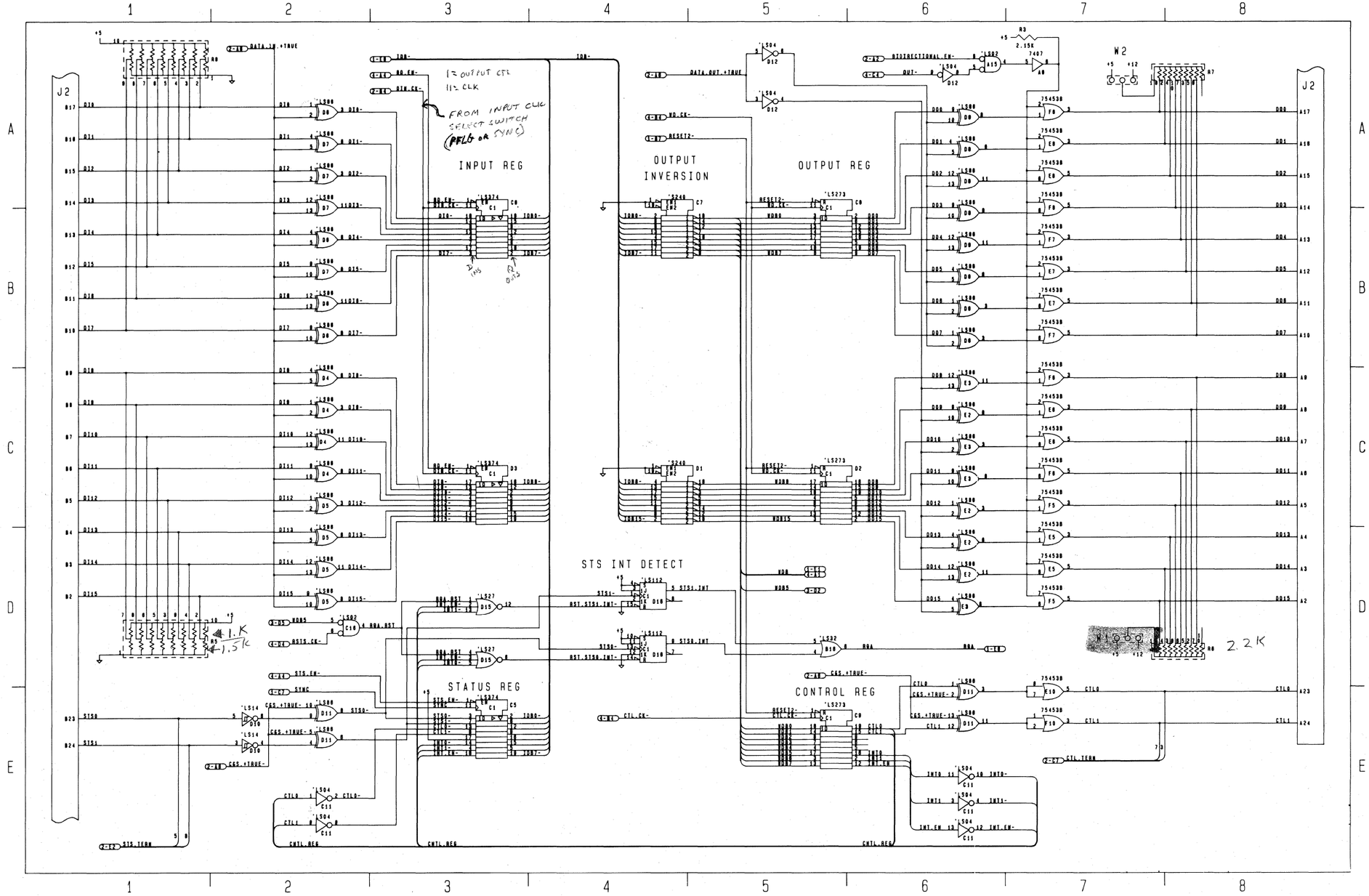



Figure 6-1. GPIO Schematic Logic Diagram (Sheet 3 of 4)

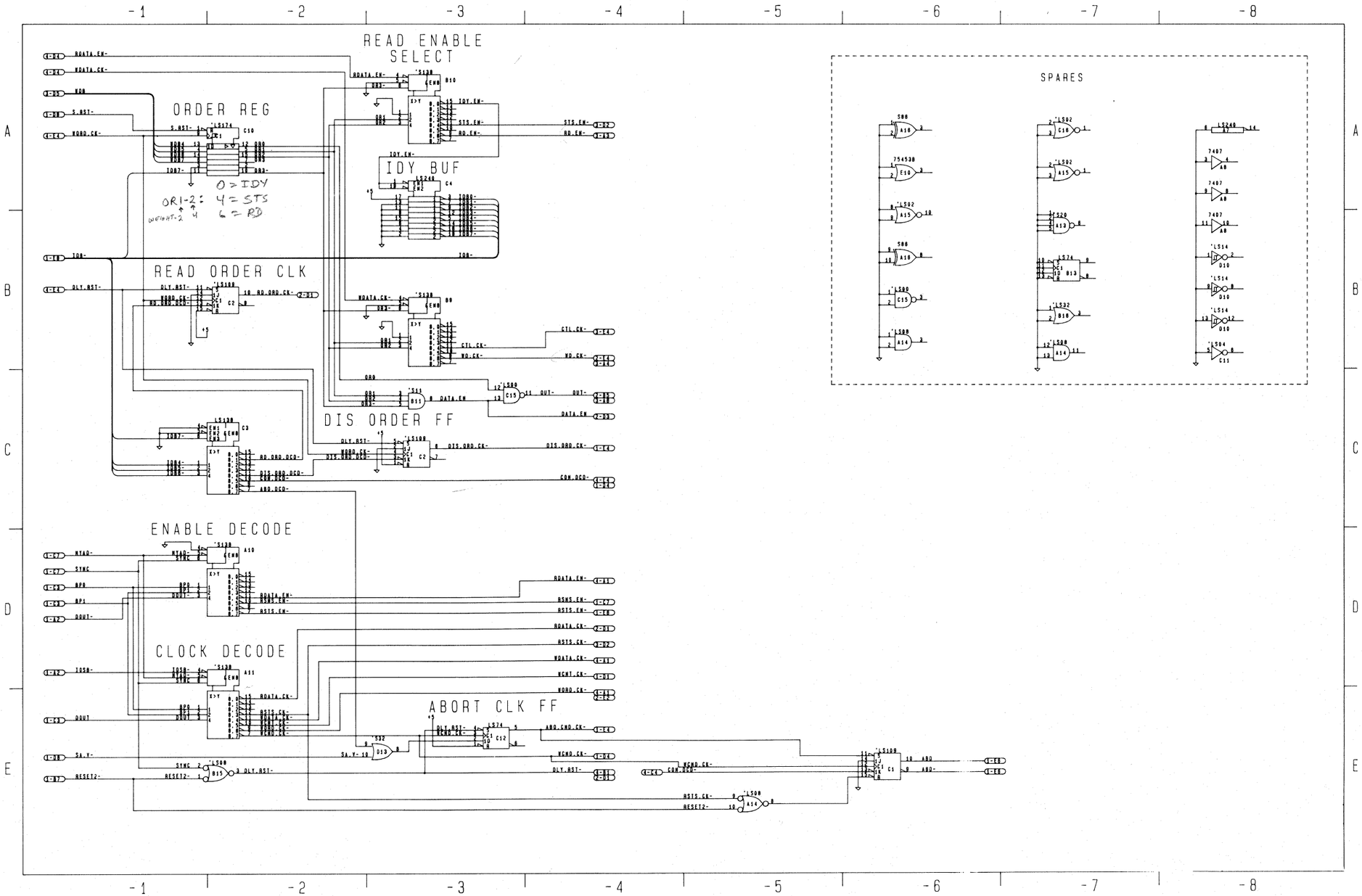



Figure 6-1. GPIO Schematic Logic Diagram (Sheet 4 of 4)

# ASCII CHARACTERS AND BINARY CODES

APPENDIX A

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| 0 | NUL | DLE | sp | 0 | @ | P | ` | p |
| 1 | SOH | DC1 | ! | 1 | A | Q | a | q |
| 2 | STX | DC2 | " | 2 | B | R | b | r |
| 3 | ETX | DC3 | # | 3 | C | S | c | s |
| 4 | EOT | DC4 | $ | 4 | D | T | d | t |
| 5 | ENQ | NAK | % | 5 | E | U | e | u |
| 6 | ACK | SYN | & | 6 | F | V | f | v |
| 7 | BEL | ETB | ' | 7 | G | W | g | w |
| 8 | BS | CAN | ( | 8 | H | X | h | x |
| 9 | HT | EM | ) | 9 | I | Y | i | y |
| A | LF | SUB | * | : | J | Z | j | z |
| B | VT | ESC | + | ; | K | [ | k | { |
| C | FF | FS | , | < | L | \ | l | \| |
| D | CR | GS | - | = | M | ] | m | } |
| E | SO | RS | . | > | N | ^ | n | ~ |
| F | SI | US | / | ? | O | _ | o | DEL |

# INDEX

## A



## B



## C

# INDEX

## D



## E



## F

## G



## H



## I

# INDEX

## L



## M



## O

## P



## R

# INDEX

## S



## T

## W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Roseville Networks Division
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Roseville, California 95678