

RWA-301

Description

The RWA-301 Guzik Technical Enterprises Read Write Analyzer is an integrated tool for the design, analysis and testing of magnetic storage devices and their components. It can be configured for testing disks and heads on a spinstand, drives, head/disk assemblies(HDA's) and head stacks.

With high precision, it performs all traditional measurements such as resolution, PW_{50} , asymmetry, signal-to-noise ratio, overwrite, track average amplitude, missing and extra pulses and modulation. To measure the timing accuracy of a recording system, the RWA-301 performs Phase Margin(Bit Shift) Analysis by means of a programmable data separator, accurate to better than 500 picoseconds, and a phase margin detector with calibrated window settings, accurate to better than 500 picoseconds and repeatable to within 100 picoseconds by use of the crystal controlled calibrator. Through the use of a software controlled bit mask, the RWA-301 can examine bit shift on any one bit or group of bits in the read back data. Any or all bits can be pre-compensated to a resolution of 100 picoseconds. The RWA-301 includes circuitry to generate RLL encoded data, multiple measurement gates for avoiding embedded servo areas, external clock input for synchronizing the internal plo and software controlled frequency zones for testing the advanced magnetic recording devices of today.

The RWA-301 is controlled by menu driven software from a PC/386 computer system. Many software application packages are available to extend the use of the product into all areas of magnetic recording.

Features

Track Average Amplitude	Grading System
Resolution	Remote Communications and Control for Robotic Integration
Signal-to-Noise	Customer Specified Plug-In Filters
Positive and Negative Modulation	Large Variety of Spinstand and Drive Interfaces
Asymmetry	Support for a Variety of Preamplifiers
Overwrite	Built-in Calibrator for Bit Shift Analyzer
Missing Pulse and Extra Pulse	Any User Specified Data Pattern up to a 152 bits of encoded data
Pulse Width	Detector Thresholds Track Read Envelope
Phase Margin(Bit Shift) Analysis	Programmable Peak Detector Time Constant
Phase Margin Measurement on Operator Selected Bit(s) in the Read Back Data(Early and Late)	Multiple Programmable Measurement Gates Suitable for Embedded Servo Skipping
Programmable Write Current	True RLL Recording to 29.9 Mbits/Second by use of a Software Configurable Encoding Scheme
Write Pre-compensation of Individual Data Bits	Programmable Positive and Negative Erase Currents
Variable Frequency to 29.9 Mbits/second	Digital Output Signals for Oscilloscope Connection
External Clock Input for Synchronizing PLO	Software for Head, Disk, HDA and Head Stack Certification
Multiple Recording Zones	Operator Specifiable Curve Fitting and Extrapolation
Result Logging to Disk and/or Printer	

Specification

Analog Channel

Bandwidth:	10 Khz 40 Mhz
Flatness:	+/- .2dB(100 Khz to 40 Mhz)
System Noise:	< -55dB
Programmable Attenuator:	36dB(6dB/step)
Filter Matrix:	4 customer specified filters
Preamplifier:	Customer specified
Write Current:	Programmable, 0 to 64 ma(zero to peak)
Frequency Synthesizer:	5 Mbits/second to 29.9 Mbits/second 1/7 Code = 39.9 Mbits/second Example: 2/7 Code = 9.97 Mhz HF MFM Code = 14.9 Mhz HF 1/7 Code = 14.9 Mhz HF

Parametric Measurement Accuracy

TAA:	+/- 1.5%
Modulation:	+/- 2.0%
Signal-to-Noise Ratio:	+/- 0.5dB
Crest Factor:	+/- 2.0%
Overwrite:	+/- 0.3dB
Asymmetry:	+/- 0.5%
Pulse Width:	+/- 2.0%

Surface Testing

Missing Pulse:	+/- 2%, 0% to 100% threshold(normalized to 2F envelope)
Extra Pulse:	+/- 2%, 0% to 50% threshold(normalized to 2F envelope)
Individual Recording Zones:	1 - 8 programmed zones

Digital Test

Data Separator:	+/- 500 picosecond, 5 Mbits/second to 29.9 Mbits/second
Bit Shift Analyzer with Internal Calibrator:	Consistent window error of 500 picoseconds Repeatability <= 100 picoseconds
Pattern Generator:	Any user specified data pattern up to a maximum of 152 bits of encoded data
Pre-compensation:	User programmable to a resolution of 100 picoseconds on an individual bit basis
Differentiator:	Operator selectable between 2
