TC02/FS

(TS11 COMPATIBLE)

TAPE COUPLER

TECHNICAL MANUAL

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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation and use of the TC02/FS Tape Coupler. The manual also provides applicable diagnostic and applications information.

1.2 OVERVIEW

1.2.1 General Description

The TC02 Magnetic Tape Coupler emulates the Digital Equipment Corporation TS11 tape coupler. The coupler may function in one of two modes. The streaming mode is used to interface streaming tape transports with LSI-11 computers. The formatted mode interfaces all stop/start tape transports having the industry standard (Pertec) interface to LSI-11 computers. Both modes are software compatible with the TS11.

1.2.2 Coupler Modes

The TC02 functions with both streaming and formatted tape drives. The mode of the coupler is determined by the setting of a minimal number of switches. Detailed switch settings may be found in Section 4. Below is a brief description of the two types of modes in which the coupler may function.

Formatted Tape Drive Mode: When enabled to function with formatted tape drives, the coupler will read and write DEC or IBM compatible 9-track PE (1600 bpi) or 9-track NRZI (800 bpi) formats. This mode accommodates transport speeds in a range of 12.5 to 125 ips. A maximum of four tape transports may be attached to the coupler with any mix of 9-track NRZI, PE or dual density.

Streaming Tape Drive Mode: The streaming mode is media compatible with tapes created on the DEC TS11. Tapes have 9-tracks at 1600 bpi. In streaming mode, the transport speed is typically 100 ips. In non-streaming mode transport speed is typically 25 ips (check manufacturer specs. for exact speed). The coupler shifts from non-streaming mode to streaming mode automatically if enough data to support the additional throughput is available. The shift is software transparent.

1.3 PHYSICAL CHARACTERISTICS

The TC02 is constructed on a single quad-size board which plugs directly into any LSI-11 Q-Bus slot. It is a four layer PCBA and it plugs into connectors A, B, C and D of the backplane. Two 50-wire flat cables connect the controller to the first tape transport. The board draws power from the LSI-11 backplane.

1.4 FEATURES

1.4.1 Microprocessor Architecture

The TC02 design incorporates a high-speed eight-bit microprocessor to perform most of the functions of the controller. It is the microprocessor's flexiblity that allows the TS11 to be emulated so completely and economically. In addition, it is the microprocessor design that allows the extensive self-test capability that the TC02 provides.

1.4.2 Self-Test

The controller incorporates an extensive self-test capability. The self-test is executed every time the controller is powered on. It does not execute self-test with a bus INIT. The LED on the top of the PCBA is turned ON when the controller is cleared and is turned OFF if the coupler gets through the self-test. If the coupler does not properly execute the self-test, the LED remains ON and the coupler cannot be addressed by the CPU.

1.4.3 Efficient DMA

The coupler incorporates 64 bytes of data buffering and it transfers data to or from memory on a word basis, except for odd bytes at the start or end of the record.

1.5 DIAGNOSTICS

The TC02 coupler executes the following DEC TS11 diagnostics in both NRZI and PE modes:

ZTSH - Data Reliability
ZTSI - Coupler Repair Diagnostic (runs first three tests*)

*Requires minor patch

1.6 OPERATING SYSTEMS

The TC02/FS Tape Coupler is fully compatible with all DEC PDP-11 and LSI-11 operating systems.

Table 1-1
General Specifications

FUNCTIONAL	
Recording Standards	IBM, ANSI, DEC
Number of Tracks	9
Recording Method and Density	Streaming: 3200 or 1600 BPI Formatted: 1600 or 800 BPI
Number of Emulations per Coupler (tape units)	4
Tape Speeds (ips)	12.5 to 125
Q-BUS INTERFACE	
Register Addresses	Switch Selectable
Interrupt Vector Address	Switch Selectable
Interrupt Priority Level	BR5
Data Transfer	Direct Memory Access (DMA) with word (16-bit) transfer, except for odd byte at beginning or at end of record.
PHYSICAL	
Mounting	Any Q-Bus slot in standard DEC system unit.
Cables	Two 50-wire flat cables.
ELECTRICAL	
Power	+5V, 6 amps.
ENVIRONMENTAL	
Operating Temperature	0°C to +55°C
Storage Temperature	-10°C to +70°C
Humidity	10 to 90%, no condensation.

BLANK

2.1 PHYSICAL DESCRIPTION

The TC02 Tape Coupler is constructed on a single quad-size printed circuit board. This board contains all circuitry required to control either streaming or formatted tape transports using both NRZI and PE formats.

2.1.1 TC02 Coupler Board

The TC02 Tape Coupler board is designated Part No. TC0210401. This board contains interface circuitry for both a DEC Q-Bus and a modified industry standard tape transport plus all other circuitry required for tape control and data transfer operations.

The TC02 coupler board is shown in Figure 2-1. The board is a 4-layer PCB with power and ground planes on the inner layers and etch interconnects on the outer layers.

As a quad-sized PCBA, the board interfaces only to connector rows A, B, C, and D. The 18 pins of each connector row are designated A through V - excluding the letters G, I, O, and Q - from right to left; the top side pins are designated "1" and the bottom side pins are designated "2".

2.1.1.1 Connectors

The coupler is interfaced to the tape transport via two 50-pin connectors labled J1 and J2 at the top edge of the board.

There are two additional male connectors located on the board, designated J3 and J4. These are used for connecting a special test panel used for factory test and repair operations and are not intended for use in normal coupler operations.

2.1.1.2 Switches

The three DIP switches are for tape speed selection and coupler options.

2.1.1.3 Indicators

The LED located to the right of the two connectors is both a coupler fault and an activity indicator. It will flash during data transfer operations with the tape.

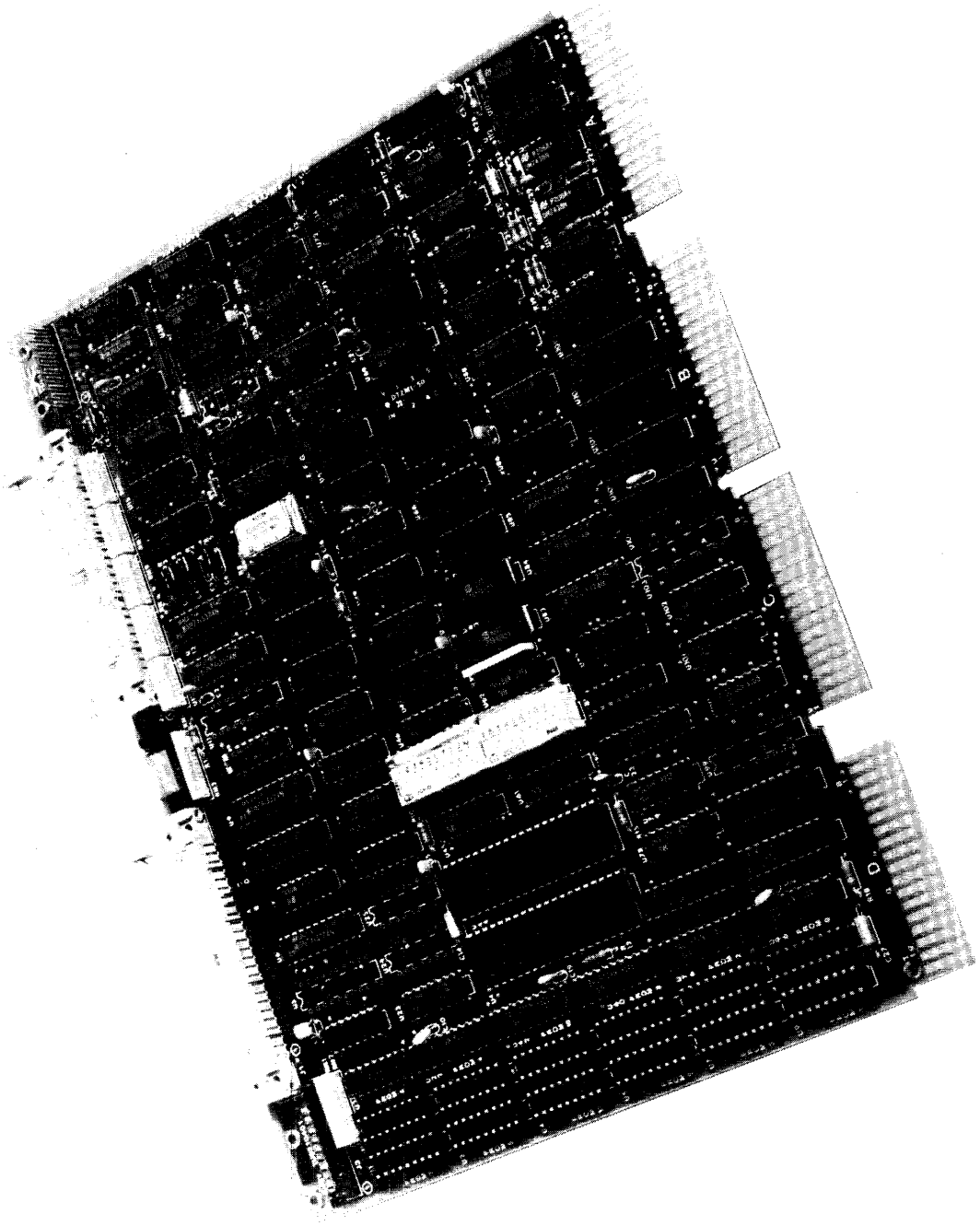


Figure 2-1. TC02 Coupler Board

2.2 ORGANIZATION

2.2.1 Coupler Board

A block diagram showing the major functional elements of the TC02 coupler is shown in Figure 2-2. The coupler is organized around a eight-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with two 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with twelve 2K x 4 PROMs.

All the device registers of the TC02 coupler, the 64-word data buffer and working storage are contained in a 1K x 8 RAM.

The Write Data Register (WDR) holds the nine bits of data to the transport and the Read Data Register (RDR) receives the nine data bits from the transport. The Control Register latches internal microprocessor control signals as well as the external signals used to control the transport. The status signals from the transport are testable signals to the microprocessor.

The Q-Bus interface consists of a 16-bit bi-directional set of data lines and a 22-bit set of address lines. The Q-Bus interface is used for programmed I/O, CPU interrupts, and NPR data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed coupler register. The microprocessor also controls all NPR operations and transfers data between the Q-Bus data lines and the transport via its own internal buffer.

2.3 TAPE TRANSPORT INTERFACE

There is a slight difference in the tape transport interface when the TC02 is functioning with a formatted tape drive rather than a streaming drive. Both interfaces are depicted in Table 2-1. In the few instances where pins have different functions with respect to the mode (and therefore different mnemonics, HSPD/DEN, for example) the first mnemonic applies to the streaming tape transport interface and the second to the formatted tape transport interface. The definitions of all signal mnemonics are contained in paragraph 2.3.4, below. Both interfaces are based on the industry standard Pertec interface.

2.3.1 Connectors and Cable

The tape coupler uses two 50-conductor flat cables to interface to the transports. The cable should be a twisted pair with a maximum daisy-chained length of not over 30 feet. All wires should be 24 AWG minimum, and each pair should have not less than one twist per inch. Connectors are standard 50-pin flat cable connectors.

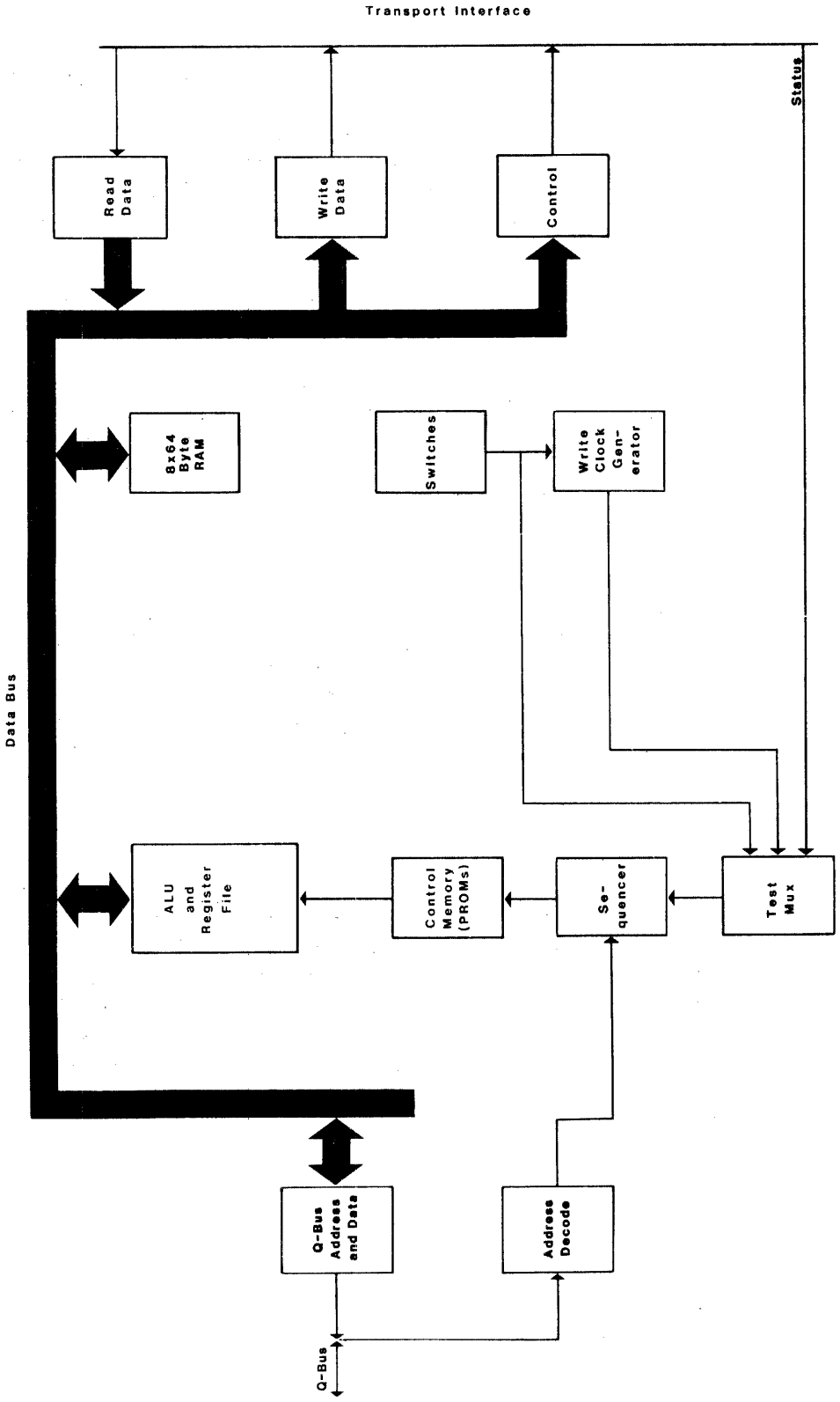


Figure 2-2 TCO2 Block Diagram

2.3.2 Input Circuits

The input lines from the tape transport are terminated with a 220 ohm (5%) resistor to plus five volts, and a 330 ohm (5%) resistor to ground. All input circuits have low-level input voltage of 0.8 v maximum and a high level input voltage of 2.0 volt minimum. The input receivers are all 74LS type circuits.

2.3.3 Output Circuits

All output lines must be terminated at the far end of the daisy-chained cable with a 220 ohm (5%) resistor to plus five volts and a 330 ohm (5%) resistor to ground. Output driver circuits are 74LS374 TTL registers, except for some 7438 open collector gates.

2.3.4 Signal Definitions

2.3.4.1 Coupler to Formatter

Transport Address: TAD0, TAD1

These lines determine which of up to four transports is selected by the coupler. TAD1 is the most significant bit.

Formatter Address: FAD

This signal selects one of two formatters. It is always zero for this emulation.

Initiate Command: GO

A pulse which initiates any command specified by a combination of the command signals REVERSE, WRT, WFM, ERASE, EDIT, LGAP and/or HSPD.

Rewind Command: REWIND

A low level pulse of approximately one microsecond commands the selected transport to rewind to the load point.

Unload Command: UNL

A low level pulse of approximately one microsecond causes the selected tape transport to go off-line, rewind the tape, and when BOT is encountered, unload the tape onto the supply reel.

Write: WRT

Write mode is specified when this signal is TRUE; read mode is specified when it is FALSE.

Write File Mark: WFM

When this signal and WRT are TRUE, the transport will write a file mark on the tape.

Erase: ERASE

When ERASE and WRT are TRUE, the transport executes a dummy write command. The transport will go through all the operations of a normal write command but no data will be recorded. A length of tape will be erased equivelent to the length of the Dummy record (as defined by LWD). If ERASE, WRT and WFM are TRUE, the transport will execute a dummy write file mark command. A fixed length of tape of approximately 3.75 inches will be erased.

High Speed: HSPD

If this signal is TRUE when a read or write command is issued, the transport will read or write at the high speed.

Last Word: LWD

When TRUE during a write or erase command, this signal indicates that the next character to be strobed into the transport (formatter) is the last character of the record.

On-Line: LOL

This signal causes the selected transport to go On-Line.

Reverse: REVERSE

When TRUE, this signal initiates reverse tape motion. When it is FALSE, forward tape motion is specified.

Edit: EDIT

This is a signal which, when TRUE duing a read reverse operation, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When EDIT and WRT are TRUE, the selected transport operates in the edit mode.

Formatter Enable: FEN

When FALSE this signal causes the transport to be held in an initialized state.

Write Data 7:0, Parity: WD7:WD0, WDP

These line transmit data to the transport. Line zero is the most significant. WDP carries the odd parity bit associated with each data word. The parity bit is generated by the coupler.

Long Gap: LGAP

When TRUE, this signal causes the transport to generate a 1.2 in. long IBG.

Read Threshold Level 1: RTH1

This line is used only by transports with single gap heads to specify the operating level of the read threshold circuits. A TRUE level specifies selection of the high read threshold level, and a FALSE level specifies the normal read threshold.

Read Threshold Level 2: RTH2

This line is used only by transports with extra low read threshold capabilities. When TRUE, the extra low threshold is specified; when FALSE, the normal threshold is specified.

Density: DEN

When used with a dual-mode transport, the TRUE level selects NRZI and the FALSE level selects P.E.

2.3.4.2 Formatter to Coupler

Formatter Busy: FBY

When TRUE, this signal inhibits further commands to the formatter. The signal becomes TRUE on the trailing edge of GO when a command is issued by the coupler. FBY remains TRUE until a new command can be given.

On-Line: ONL

A low level indicates that the selected tape transport is on-line and under control of the tape coupler.

Ready: READY

A low level indicates that the selected tape transport is loaded and not rewinding.

Rewinding: RWD

A low level indicates that the selected tape transport is engaged in a rewind operation or the load sequence following a rewind operation.

End of Tape: EOT

A low level indicates that the EOT tab on the tape is being sensed.

Beginning of Tape: BOT

A low level indicates that the selected tape transport is sensing the BOT tab on the tape, has completed its initial load sequence, and the tape transport is not rewinding.

File Protect: FPT

A low level indicates that a reel of tape without a write enable ring installed is mounted on the transport.

Data Busy: DBY

This signal becomes TRUE after a command has been accepted by the transport. DBY remains TRUE until the data transfer is complete and the appropriate post record delay has expired.

Hard Error: HER

A TRUE pulse of this signal indicates that an uncorrectable read error has occured and that the record should either be reread or rewritten.

Corrected Error: CER

A TRUE pulse of this signal indicates that a single track dropout has been detected and the formatter is performing an error correction.

Identification: PEID

When TRUE, this signal indicates that a PE identification burst has been detected. When in 800 bpi mode (NRZI) this signal is TRUE when the read information being transmitted to the coupler is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). It is FALSE when data characters are being transmitted.

File Mark: FMK

This signal is pulsed when a file mark is detected on the tape during a read operation or during a write file mark operation in a read-after-write transport.

High Speed Status: HSPS

When TRUE, this signal indicates that the selected transport is in the 100 ips (streaming) mode. A FALSE level indicates that the transport is operating at low speed (start/stop).

NRZI Mode: INRZ

This signal is TRUE when the transport is in 800 bpi mode (NRZI).

Table 2-1
Cable Interface

Connector	Sig Pin	Grd Pin	Mnemonic	Connector	Sig Pin	Grd Pin	Mnemonic
J1	2	1	$\overline{\text{FBY}}$	J2	1	5	$\overline{\text{RDP}}$
	4	3	$\overline{\text{LWD}}$		2	5	$\overline{\text{RD0}}$
	6	5	$\overline{\text{WD4}}$		3	5	$\overline{\text{RD1}}$
	8	7	$\overline{\text{GO}}$		4	5	$\overline{\text{BOT}}$
	10	9	$\overline{\text{WD0}}$		6	5	$\overline{\text{RD4}}$
	12	11	$\overline{\text{WD1}}$		8	7	$\overline{\text{RD7}}$
	14	13	Spare		10	9	$\overline{\text{RD6}}$
	16	15	$\overline{\text{LOL}}$		12	11	$\overline{\text{HER}}$
	18	17	$\overline{\text{REVERSE}}$		14	13	$\overline{\text{FMK}}$
	20	19	$\overline{\text{REWIND}}$		16	15	$\overline{\text{PEID}}$
	22	21	$\overline{\text{WDP}}$		18	17	$\overline{\text{FEN}}$
	24	23	$\overline{\text{WD7}}$		20	19	$\overline{\text{RD5}}$
	26	25	$\overline{\text{WD3}}$		22	21	$\overline{\text{EOT}}$
	28	27	$\overline{\text{WD6}}$		24	23	$\overline{\text{UNL}}$
	30	29	$\overline{\text{WD2}}$		26	25	$\overline{\text{INRZ}}$
	32	31	$\overline{\text{WD5}}$		28	27	$\overline{\text{READY}}$
	34	33	$\overline{\text{WRT}}$		30	29	$\overline{\text{RWD}}$
	36	35	$\overline{\text{LGAP}}/\overline{\text{RTH2}}$		32	31	$\overline{\text{FPT}}$
	38	37	$\overline{\text{EDIT}}$[1]		34	33	$\overline{\text{RDS}}$
	40	39	$\overline{\text{ERASE}}$		36	35	$\overline{\text{WDS}}$
	42	41	$\overline{\text{WFM}}$		38	37	$\overline{\text{DBY}}$
	44	43	$\overline{\text{RTH1}}$		40	39	$\overline{\text{HSPS}}$
	46	45	$\overline{\text{TAD0}}$		42	41	$\overline{\text{CER}}$
	48	47	$\overline{\text{RD2}}$		44	43	$\overline{\text{ONL}}$
J1	50	49	$\overline{\text{RD3}}$		46	45	$\overline{\text{TAD1}}$
					48	47	$\overline{\text{FAD}}$
				J2	50	49	$\overline{\text{HSPD}}/\overline{\text{DEN}}$

NOTE: When two mnemonics are given for a pin (HSPD/DEN, for example) the first applies to the streaming tape interface and the second to the formatted tape interface.

Write Data Strobe: WDS

This signal is pulsed each time a data character is written onto tape. WDS samples the write data lines WDP, WD7:WD0 from the coupler and copies this information character by character into the formatter write logic. The first character should be available prior to the first write strobe pulse and succeeding characters should be set up within half a character period after the trailing edge of each write strobe.

Read Data Strobe: RDS

This signal consists of a pulse for each character of read information to be transmitted to the coupler. This signal should be used to sample the read data lines RDP, RD7:RD0.

Read Data 7:0, Parity: RD7:RD0, RDP

Each character read from tape is made available by parallel sampling the read lines with RDS. Since the data remains on the read data lines for a full character period, corresponding RDS pulses are timed to occur after approximately the center of the character period.

2.4 Q-BUS INTERFACE

The LSI-11 Bus consists of 42 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

1. Twenty-two data/address lines - <BDAL00:BDAL21>
2. Six data transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT
3. Three direct memory access control lines - BDMG, BDMR, BSACK
4. Six interrupt control lines - BEVNT, BIAK, BIRQ4, BIRQ5, BIRQ6, BIRQ7
5. Five system control lines - BDCOK, BHALT, BINIT, BPOK, BREF.

The MS four data/address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

Table 2-2
Q-Bus Connections

	A		B	
	1	2	1	2
A	BIRQ5	+5V	BDCOK	+5V
B	BIRQ6		BPOK	
C	BDAL16	GND	BDAL18	GND
D	BDAL17		BDAL19	
E		BDOUT	BDAL20	BDAL02
F		BRPLY	BDAL21	BDAL03
H		BDIN		BDAL04
J	GND	BSYNC	GND	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	GND	BIAKI	GND	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVNT	BDAL11
S		BDMGO		BDAL12
T	GND	BINIT	GND	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

2.4.1 Interrupt Priority Level

The controller is hardwired to issue level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either a LSI-11 or LSI-11/2 processor.

2.4.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U104. The selections available are determined by configuration switch SW1 as discussed in Appendix A.

2.4.3 DCOK and INIT Signals

The DCOK and INIT signals both perform a controller clear. The self-test is performed only when DC power is initially applied.

2.4.4 NPR Operations

All DMA data transfers are carried out under microprocessor control. A check is made for memory parity errors when doing a tape write operation. If an error is detected the Q-Bus parity error (UPE) is set.

3.1 COUPLER REGISTERS

This section describes and defines the TC02 registers and packet processing. In addition, programming examples and packet formats are provided to illustrate basic TC02 programming concepts.

The DEC TS11 supports only a single tape transport. Therefore, each tape transport supported by the system has a unique set of Q-Bus registers and command/message buffers in CPU memory. The Emulex TC02 supports four tape transports. Thus, the TC02 is really emulating four TS11s with their attendant registers. It is, therefore, inaccurate to refer to TC02 when discussing registers because the four register sets that the 02 contains are not related. For example, initializing one of the subsystem emulations by writing to the appropriate TSSR register does not affect the other three emulations. Also, it is not necessary (nor possible) to separate coupler command or status from transport command or status because each register and command/message buffer set is dedicated to the individual transport. Consequently, when discussing an individual emulation we will use the term transport instead of using emulation, TC02 or TS11.

Device register usage is compatible with DEC TS11 register definitions. However, some additions have been made to provide extended functions.

The eight transport registers are:

TSBA	(1)	- Q-Bus Address Register
TSDB	(1)	- Q-Bus Data Buffer
TSSR	(1)	- Status Register
XST	(5)	- Extended Status Registers

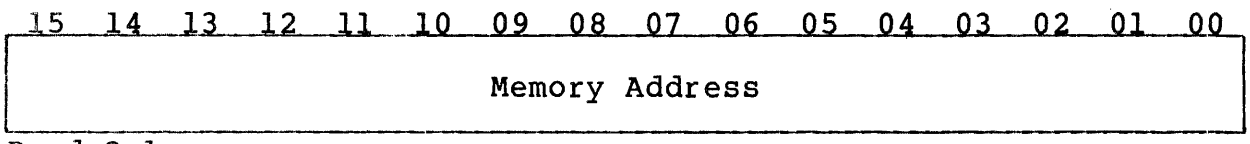
Each transport has two Q-Bus word locations used as device registers. The base address, when written to, is the data buffer register (TSDB). When read, it is the bus address register (TSBA). The second device register (base address + 2) is the status register (TSSR). Writing to the TSSR causes a subsystem initialize command, and reading the TSSR reads device status.

The TSDB register is the only register written to during normal operations. DATO or word access must be used to properly write command pointers to the TSDB. DATOB or byte access to the TSDB causes maintenance functions.

Commands are not written to the transport's Q-Bus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used by the transport to retrieve the words

in the command packet. The words of the command packet tell the transport the function to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

3.1.1 Base Address Register (TSBA)

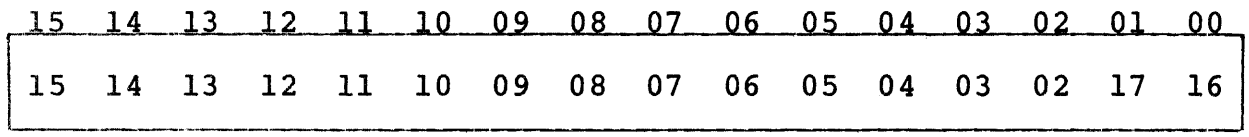


Read Only

The TSBA is a 16-bit register that is read at the transport's base address (1777XXXX). It is a reflection of the least significant 16 bits of the 18-bit TSDB register. (TSDB bits 17 and 16 are displayed in TSSR bits 09 and 08, respectively.) The contents of TSBA are valid only after the termination of a command. (A command is initiated by loading a command packet address into TSDB.) The termination may be either with or without errors. The TSBA is the base address in the read only mode and it is not cleared on power up, subsystem INIT, or bus INIT. It can also be read at any time with or without the transport unit connected.

Upon completion of a command, the TC02 deposits a message packet in a message buffer located in CPU memory. The TSBA may be read to determine the highest message buffer address plus two.

3.1.2 Data Buffer Register (TSDB)



Write Only

The TSDB is an 18-bit register that is parallel loaded from the Q-Bus at the base address. The TSDB can be loaded when the transport is bus slave by three different types of transfers from a bus master. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte). The third transfer is for normal (word) operation (DATO). This register is write-only and is not cleared at power up, subsystem initialize or bus initialize. The transport responds with SSYN anytime the TSDB is written to.

3.1.2.1 Normal Operation

A command is issued to the transport by loading an 18-bit address into the TSDB using a DATO. The address is that of a command packet located somewhere in Q-Bus address space. The address is loaded into the TSDB using the following format. Bits <15:02> of the register are loaded with bits <15:02>, respectively, from the Q-Bus. Bits 16 and 17 of the address are loaded from bits 00 and

01, respectively, from the Q-Bus. Bit 00 and bit 01 of the address are automatically loaded with zeroes by the transport logic. Loading the TSDB register initiates a fetch by the transport of the command packet at the specified address. The command defined in the packet is then executed.

3.1.2.2 Data Wraparound Using DATOB (odd)

When TSDB is loaded by a DATOB to TSDB high byte (odd address), the following happens. Bits <07:00> of the register are loaded with bits <15:08>, respectively, from the Q-Bus. Bits <15:08> of the register are loaded with bits <15:08>, respectively, from the Q-Bus. Bits 16 and 17 of the register are loaded with bits 08 and 09 respectively, from the Q-Bus. The TSDB is then loaded into TSBA. This transfer will be executed anytime a DATOB to the TSDB high byte is done. IF SSR (see TSSR bit 07) is clear, an error (RMR TSSR bit 12) occurs, but the transfer is still executed and completed. The TSSR is not affected (except for SSR bit 07, which gets cleared). To use the tape transport again, the CPU must initialize the transport (that is, write the TSSR).

3.1.2.3 Data Wraparound Using DATOB (even)

When TSDB is loaded by a DATOB to TSDB low byte (even address), the following happens. Bits <15:00> of the register are loaded with bits <15:00>, respectively, from the Q-Bus. (Most LSI-11 CPUs assert all zeroes for bits <15:08> except for a MOVB; this sign extends bit 07. See the respective processor handbook for a MOVB instruction.) Bits 16 and 17 cannot be determined. The TSDB is then loaded into the TSBA. To use the tape transport again, the CPU must initialize the transport (that is, write the TSSR).

3.1.3 Status Register (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	UPE	SPE	RMR	NXM	NBA	A17	A16	SSR	OFL	SIP	0	TC2	TC1	TC0	X

Read/Write

See Table 3-1 for definition of Termination Class (TC) Codes.

The TSSR is a 16-bit read/write register at base address 1777XXXX+2. It can be read at any time with or without the transport unit connected. It can only be updated by the transport logic; it cannot be modified from the Q-Bus except indirectly. (SPE, UPE, RMR, NXM, and SSR bits are cleared when the TSDB is written by the host CPU.)

Any write function to the TSSR is decoded as a subsystem initialize. This resets the transport and coupler no matter what state they are in and causes an automatic load sequence returning the tape to BOT if the transport is on-line.

TSSR register bits 14 through 11 and 7 are cleared only on system power up, transport power up, subsystem initialize, or at the beginning of any write command to the TSDB register. Bits 15 and 07 are under control of the transport. These may be set or cleared independently of any transport operation. Bits 10 and <06:00> are controlled by the transport and reflect the subsystem status as indicated.

The TSSR register utilizes several bits to increase its status reporting capabilities. TSSR bits <03:01> report seven termination class status codes.

On fatal errors (termination class bits equal seven), if the need buffer address is not set (NBA=0), then the message may be valid. If the need buffer address is set (NBA=1), then there was no message.

The RMR bit will not affect the error class codes because RMR may occur on a bug free system. However, RMR will set the special condition (SC). (You may have tried to perform the next command while the transport was outputting the ATTN MSG.) If RMR is seen in the TSSR, the CPU must have written the TSDB while the command was executing.

The TSSR may not reflect the current state of the hardware if ATTNs are not enabled and the message buffer is not released. (That is, the transport may be off-line while the TSSR shows on-line). To keep the TSSR up to date would violate message packet protocol.

TSSR is not cleared immediately after initialization. The microprocessor runs to complete an automatic load sequence. When tape is at BOT, TSSR updates.

Special Condition (SC) - Bit 15

When set, this bit indicates that the last command was not completed without incident. Specifically, either an error was detected or an exception condition occurred. An exception condition coud be a tape mark on read commands, reverse condition at BOT, EOT while writing, etc.

O-Bus Parity Error (UPE) - Bit 14

This bit is set by the transport when it detects a parity error in the memory data being transferred from the CPU memory. (Causes TC4 and TC5.)

Serial Bus Parity Error (SPE) - Bit 13

This bit is set by the transport when it detects a serial bus parity error on data received from the transport. (Causes TC7.)

Register Modification Refused (RMR) - Bit 12

This bit is set by the transport when a command pointer is loaded into the TSDB and subsystem ready (SSR) is not set. This bit may set on a bug free system if ATTN interrupts are enabled.

Nonexistent Memory (NXM) - Bit 11

This bit is set by the transport when trying to transfer to or from a memory location which does not exist. It may occur when fetching the command packet, fetching or storing data, or storing the message packet. (Causes TC4 and TC5.)

Need Buffer Address (NBA) - Bit 10

When set, this indicates that the transport needs a mesage buffer address. This bit is cleared during the set characteristics command if the transport gets valid data; it is always set after subsystem initialization.

Bus Address Bits 17:16 (A17, A16) - Bits <09:08>

A17 and A16 (bits 09 and 08) display the values of bits 17 and 16 in the TSBA register.

Subsystem Ready (SSR) - Bit 07

When set, this bit indicates that the transport is not busy and is ready to accept a new command pointer.

Off-Line (OFL) - Bit 06

When set, this bit indicates that the transport is off-line and unavailable for any tape motion commands.

Silo Parity Error (SIP) - Bit 05

This bit is set when the coupler detects a parity error on read data from the tape transport. (Causes TC7.)

Termination Class: TC02, TC01, TC00 - Bits <03:01>

These bits act as an offset value when an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. The code provided in this field is defined in Table 3-1. The code is expected to be utilized as an offset into a dispatch table for handling the condition. These bits are valid only when special condition (SC) is set. Refer to special conditions and errors, paragraph 3.3.4 of this manual.

Table 3-1
Termination Class Codes

TSSR Bits <03:01>	TC Code	Description
000	0	Normal termination
001	1	Attention condition
010	2	Tape status alert
011	3	Function reject
100	4	Recoverable error (tape position = one record down from start of function)
101	5	Recoverable error (tape not moved)
110	6	Unrecoverable error (tape position lost)
111	7	Fatal (Transport Data Parity) error

3.1.3.1 Bootstrap Command

The TC02 has the ability to read the boot record of bootable tapes by use of a special command. This special command does not require that a command packet be constructed.

After power-up or bus INIT, writing the TSSR Register with the value 100001 twice will cause the TC02 to space over the first record on the tape and read the second record into the CPU, starting at location 000000. The mag tape will then stop. By starting the execution of the program at location 000000, the boot record will load the desired program from the tape.

The following bootstrap program is a sample; users may write their own program if preferred.

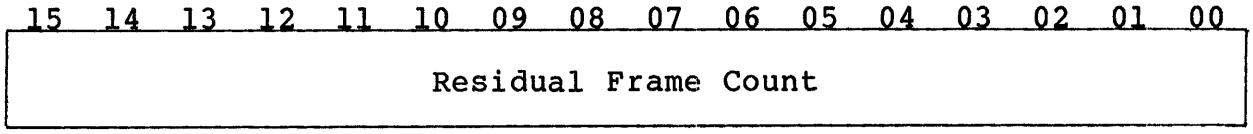
Memory Location	Content	Macro Instructions		
2000	5000	START:	CLR	R0
2002	5300	5$:	DEC	R0
2004	1376		BNE	5$
2006	12706		MOV	#1070,SP
2010	1070			
2012	12701		MOV	#172522,R1
2014	172522			
2016	12702		MOV	#100001,R2
2020	100001			
2022	10211		MOV	R2,(R1)
2024	10211		MOV	R2,(R1)
2026	22711	10$:	CMP	#122204,(R1)
2030	122204			
2032	01375		BNE	10$
2034	12704		MOV	#MESS+20,R4
2036	2062			
2040	05007		CLR	PC
2042	46523	MESS:	.WORD	46523
	00001		.END	

3.1.4 Extended Status Registers

Five additional registers are employed to provide additional status information: Residual Frame Count Register (RBPCR) and Extended Status Registers 0, 1, 2, and 3.

The Extended Status Registers are not read directly from the registers accessible at the Q-Bus interface. At the end of a command or by issuing a Get Status Command the message packet information is updated. The end message packet which results from the get status contains the extended status words. This means that a message buffer has to be defined to the subsystem before the extended status registers are available to the software.

3.1.4.1 Residual Frame Count Register (RBPCR)



Read Only

Residual Frame Count - Bits <15:00>

This word contains the octal count of residual bytes, records, tape marks for read, space records and skip tape mark commands. The contents are meaningless for all other commands.

3.1.4.2 Extended Status Register Zero (XST0)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TKM	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

Read Only

See Table 3-1 for definition of Termination Class (TC) Codes.

Tape Mark Detected (TMK) - Bit 15

This bit is set when a tape mark is detected during a read, space, or skip command and as a resut of the write tape mark or write tape mark retry commands. (Causes TC2.)

Record Length Short (RLS) - Bit 14

This bit indicates one of the following three cases. The record length was shorter than the byte count for a read operation. A space record operation encountered a tape mark or BOT before the position count was exhausted. Or, the third possibility, a skip tape marks command was terminated by encountering BOT or a double tape mark (if skip tape marks command is enabled, see LET) before exhausting the position counter. (Causes TC2.)

Logical End of Tape (LET) - Bit 13

This is set only on the skip tape marks command under two conditions: when either two contiguous tape marks are detected or when moving off BOT and the first record encountered is a tape mark. The setting of this bit will not occur unless this mode of termination is enabled through use of the set characteristics command. (Causes TC2.)

Record Length Long (RLL) - Bit 12

When set, this bit indicates that the record read was longer than the byte count specified. (Causes TC2.)

Write Lock Error (WLE) - Bit 11

When set, a TC3 indicates that a write operation was issued but the mounted tape did not contain a write enable ring. When set, TC6 indicates the WRT LOCK switch was activated during write operation.

Non-Executable Function (NEF) - Bit 10

When set, this bit indicates that the command could not be executed due to one of the following conditions: The command specified reverse tape direction but the tape was already positioned at BOT. A motion command was issued without the clear volume check (CVC) bit being set while the volume check bit was set. A write command was issued when the tape did not contain a write enable ring [Write Lock Status (WLS)]. (Causes TC3.)

Illegal Command (ILC) - Bit 09

This bit is set when a command is issued and either its command field or its command mode field contains codes not supported by the transport. (Causes TC3.)

Illegal Address (ILA) - Bit 08

This bit is set if an address greater than 18 bits in length is loaded into TCDB Register or if that register overflows. (Causes TC3.)

Capstan is Moving (MOT) - Bit 07

When set, this bit indiactes that the tape was moved during the previous operation. (Causes TC3.)

On-Line (ONL) - Bit 06

When set, this bit indicates that the transport is on-line and operable. It causes a TC1 on ATTN interrupt or a TC3 (non-executable) function if rejected because the transport was off-line.

Interrupt Enable (IE) - Bit 05

This bit reflects the state of the interrupt enable bit supplied on the last command.

Volume Check (VCK) - Bit 04

This bit is set when the transport changes state (on-line to off-line and vice versa). It is always set after initialization. (Causes TC3.)

Phase Encoded Transport (PED) - Bit 03

When set, this bit indicates that the transport is capable of reading and writing only 1600 bit/in phase encoded data. It should always be set.

Write Locked (WLK) - Bit 02

When set, this bit indicates that the mounted tape reel does not have a write enable ring installed. Therefore the tape is write protected. (Causes TC3 and TC6.)

Beginning of Tape (BOT) - Bit 01

When set, this bit indicates that the tape is positioned at the load point as denoted by the BOT refective strip on the tape. This causes TC2 if reversed in BOT, and TC3 if at BOT when a reverse command occurs.

End of Tape (EOT) - Bit 00

This bit is set whenever the tape is positioned at or beyond the EOT reflective strip. It is not reset until the tape passes over the EOT reflective strip in the reverse direction under program control. System initialization always resets this bit (status on read, TC2 on a write). Manually moving EOT mark over the EOT sensor will not set or reset the EOT bit.

3.1.4.3 Extended Status Register One (XST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	COR	0	TIG	0	0	0	0	0	IPO	0	0	0	UNC	MTE

Read Only

See Table 3-1 for Temination Class (TC) code definitions.

Data Late (DLT) - Bit 15

This bit is set when the I/O silo is full on a read or empty on a write. The conditions occur whenever the Q-Bus latency exceeds the transport's data transfer rate for a significant number of transfers. (Causes TC4.)

Correctable Data (COR) - Bit 13

This bit is set if a single track error correction condition is detected during the execution of a read or write command.

Trash in the Gap (TIG) - Bit 11

This bit is set when non-erased data is detected in a gap during a read, write, write tape mark, or erase command. It is always zero (invalid) unless SW3-8 is ON and a CDC streaming tape transport is in use. (Causes TC1 and TC4.)

Invalid Postamble (IPO) - Bit 05

This bit is set during read or write if any of the first 39 characters of the postamble are not read correctly. It is status on read. It is always zero (invalid) unless SW3-8 is ON and a CDC streaming tape transport is in use. IPO causes TC4 on a write.

Uncorrectable Data (UNC) - Bit 01

This bit is set when a parity error occurs without a corresponding dead track indication. This bit is a normal write error for any dead track. It is always zero (invalid) unless SW3-8 is ON and a CDC streaming tape transport is in use. (Causes TC3, TC4 and TC6.)

Multitrack Error (MTE) Bit - 00

This bit is set if more than one dead track occurs in the preamble or in the data field. (Causes TC4 and TC5.)

3.1.4.4 Extended Status Register Two (XST2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	SIP	0	0	0	0	0	DTP	Dead Track <07:00>							

Read Only

See Table 3-1 for Termination Class (TC) Code definitions.

Operation in Progress (OPM) - Bit 15

When set, this bit indiactes that the tape was moved during the previous operation.

Silo Parity Error (SIP) - Bit 14

Set when the transport parity checker detects a parity error on read data from tape transport. (Causes TC7.)

Dead Track Parity (DTP), Dead Track 7:0 (DT7:0) - Bits <08:00>

These bits indicate which tracks went dead, if any, during the last data transfer operation. They are always zero (invalid) unless SW3-8 is ON and a CDC streaming tape transport is in use.

3.1.4.5 Extended Status Register Three (XST3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	OPI	REV	0	DCK	NOI	LXS	RIB

Read Only

Operation Incomplete (OPI) - Bit 06

This bit is set when a read, space, or skip operation has moved 25 feet of tape without detecting any data on the tape. It is also set by a write command when the read head fails to see data transitions after four feet of tape. (Causes TC6.)

Reverse (REV) - Bit 05

This bit is set when the direction of current tape operation is reverse. For multifunction retry commands, if at least one of the commands is reverse, the bit is set.

Density Check (DCK) - Bit 03

The current operation will be done. However, note that read, space, and skip operations will complete without error (if no other errors occur) to allow tapes with a bad IDB to be read. On a write command, when a bad IDB is sensed, tape position lost will occur. (Causes TC6.)

NOTE: If you append to a tape with a bad IDB, you will not receive any DCK error until a write.

Noise Record (NOI) - Bit 02

This bit is set during a space operation when a burst of flux changes, which do not qualify as a record (but too many to ignore), are detected. (Causes TC6.)

Limit Exceeded Statically (LXS) - Bit 01

This bit is set by tension arms that have actuated their limit switches; it remains set when tension arms are returned to normal position. It can be reset only by loading tape.

Reverse Into BOT (RIB) - Bit 00

This bit is set when a read, space, skip, or reverse command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT. (Causes TC2.)

3.2 PACKET PROCESSING

The packet protocol scheme allows each TS11 emulation (transport) on the transport to provide a large amount of status and error information to the CPU while taking up only two words of Q-Bus address space. The packet protocol also prevents the transport from updating the error and status information asynchronously, that is, while the CPU is reading the error and status information.

NOTE: This section is not intended to detail all aspects of packet protocol or packet processing. It is intended to illustrate how these concepts are implemented in the transport subsystem.

To allow each transport to take up only two words of address space, we allow the CPU to define a set of locations in memory. These locations (command buffers) are used to tell the transport what operation to perform. The CPU also defines a set of locations (message buffers) in memory where the transport will put the error and status information. The CPU must give both the command buffer address and message buffer address to the transport. The CPU gives the command buffer address to the transport on every command. (The CPU writes the address of the command packet into the TSDB of the transport.) The CPU gives the message buffer address to the transport every time the CPU does a set characteristics command.

To prevent the transport from updating the message buffer while the CPU is reading that buffer, we have defined the concept of ownership. Both the command and message buffers can be owned. Each buffer may be owned by the transport or the CPU, but not by both simultaneously. Ownership of a buffer can only be transferred by the current owner.

There are four different combinations that transfer the ownership of the two buffers:

Command buffer - CPU to transport by the CPU;
Command buffer - transport to CPU by the transport;
Message buffer - CPU to transport by the CPU and
Message buffer - transport to the CPU by the transport.

The CPU transfers ownership of the command buffer to the transport by writing the address of the command packet into the TSDB. This write clears the TSSR subsystem ready (SSR) bit.

The transport transfers ownership of the command buffer to the CPU by setting the acknowledge (ACK) bit in the message buffer. When the transport outputs the message buffer, the transport sets SSR in the TSSR to indicate that the message is in the message buffer. If the message buffer does not contain the ACK bit, the CPU will know that the transport did not see the last command buffer and the CPU still owns the command buffer. The command may be reissued by the CPU.

The CPU transfers ownership of the message buffer to the transport by setting the ACK bit in the command buffer. If the command buffer does not contain the ACK bit, the transport will know that the CPU did not see the last message buffer and the transport still owns the message buffer. The transport outputs the TSSR again (with the SSR bit up) and interrupts (if IE is set) without sending out a message.

The transport transfers ownership of the message buffer to the CPU in one of two ways. The first way is used after the end of a command: the transport sets the SSR bit in the TSSR to indicate that the command is done (and interrupts if IE is set). The second way is used during an attention (ATTN). SSR will already be up because an ATTN only happens when the transport is inactive. The transport clears SSR, outputs the message, then sets SSR again and interrupts (if IE set). Note that if the CPU writes the TSDB while the SSR is clear during an ATTN, the register modification refused (RMR) error bit will be set and that command will be ignored. The ATTN message will not have the ACK bit set since the transport does not own the command buffer. Note that RMR may set in this way on a bug free system because the CPU happened to try to perform a command at the same time the transport wanted to perform an ATTN. All other settings of the RMR indicate a software bug. (The CPU tried to do a command before the previous command was finished.) If the CPU command was lost because the transport was outputting an

ATTN message, VOL CHK and INT ENB are not updated. If the CPU command was rejected (illegal command, etc.), VOL CHK and INT ENB are updated to the start of the rejected command.

When the transport is initialized, the TSSR is updated. At this time we define both the command and message buffers as belonging to the CPU. When the CPU wants to do a command (the first one must be a set-characteristics to set up the message buffer address), the CPU writes the address of the command buffer into the TSDB of the transport. This command must have the ACK bit set to give ownership of the message buffer to the transport. At this point, the transport owns both the command and message buffers.

The transport will execute the set characteristics command and send out a message to the message buffer address with the ACK bit set; this indicates that the transport has recognized the command and is finished with the command buffer. The transport will then set SSR and interrupt (if IE is set). At this point, the CPU owns both the message and command buffers again.

As you can see, the ownership of both buffers transfers simultaneously from CPU to transport and then from transport to CPU.

Now consider the case where ATTNs are enabled by the proper characteristics mode word and the transport wants to do an ATTN. An ATTN will only occur when the transport is not active. If the CPU owns both the command and message buffers, the transport must queue up the ATTN and not do anything until the CPU releases the message buffer on the next command. So when the CPU executes the next command (with the ACK bit set), the transport will output the ATTN message with the ACK bit zero; this indicates that the command was lost (except for the transfer of the message buffer ownership to the transport). The transport refuses to accept ownership of the command buffer. The CPU will then still own the command buffer (because the transport did not accept the command) and will also own the message buffer now filled with an ATTN message. If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set).

Now consider the case where the CPU wants to be notified of a change in status right away while the transport is inactive for a long period of time. To accomplish this, the transport must own the message buffer for that long period of time. Everything up to now has indicated that the transport gives up the message at the end of every command. The message buffer release command is a special command from the CPU. It tells the transport not to give ownership of the message buffer back to the CPU at the end of the command. The transport does not output a message at the end of the command but just outputs the TSSR (with the SSR bit set) and interrupts (if the proper characteristics mode word is set up). The transport then maintains ownership of the message buffer until an ATTN condition is seen. The transport then immediately clears SSR, outputs the message (with the ACK bit not set since the

transport is not responding to a command), and then sets SSR and interrupts (if IE is set). At that time the system is back to the state of the CPU owning both buffers. Another ATTN will not be done until the CPU does a command with the ACK bit set to release ownership of the message buffer containing the ATTN message.

Suppose the CPU has done a message buffer release command and wants to do another command but has not received an ATTN from the transport (so that the transport still owns the message buffer from the message buffer release command). The CPU can do a command without the ACK bit set in the command buffer. At the time of the command, the CPU does not own the message buffer so the CPU cannot release the message buffer. If the CPU does set the ACK bit, nothing will happen (except the CPU might miss an ATTN if the transport was sending out an ATTN at the same time that the CPU was doing a command).

Message packet protocol may be violated if the transport gets an error (NXM, memory parity, serial bus parity error, or I/O silo parity error) during the reading in of the message packet. When one of these errors occurs, the transport always sends out a failure message (because the packet is not reliable).

The system software should be written so it will not crash if the transport interrupts while the CPU is servicing another TC02 interrupt. This may happen, but only if the transport should receive a fatal hardware error.

3.2.1 Command Packet/Header Word

15	14 12	11 08	07 05	04 00
CTL	Device Dependent	Command Mode	Packet Format 1	Command Code
ACK	CVC OPP SWB	0 0 M M	IE 0 0	0 C C C C

The command packet header word is illustrated above and defined in paragraphs below. The command code and mode field definitions are given in Table 3-2.

Acknowledge - Bit 15

This bit is set when a command is issued and the CPU owns the message buffer. It informs the transport that the message buffer is now available for any pending or subsequent message packets. This passes ownership of the message buffer to the transport.

Device Dependent Bits/Field - Bits <14:12>

The following shows how these three bits are implemented:

Bit	Name	Definitions
14	CVC	Clear volume check
13	OPP	Opposite (reverse the execution sequence of the reread commands)
12	SWB	Swap bytes

Command Mode Field - Bits <11:08>

This bit acts as an extension to the command code and mode field and allows specification of extended device commands (seek, rewind, erase, write tape mark, etc.). Command code and mode field are detailed in Table 3-2.

Packet Format #1 Field - Bits <07:05>

The following two values are defined in this field.

Bit Values	Definition
000	One word header: interrupt disable
100	One word header: interrupt enable

Command Code Field - Bits <04:00>

Refer to Table 3-2 for definition of the three LS bits of the code.

Bits 03 and 04 of the command code field determine the format and length of command packets. The command packet formats and lengths are as follows.

Code Bits	Definition
00XXX	Four words (header, two word address, count)
01XXX	Two words (header, parameter word) or one word (header)

The swap byte bit in the command packet header word (bit 12) instructs the transport to alter the sequence of storing and retrieving bytes from the CPU's memory. When swap bytes equals one, an industry compatible sequence (beginning with an even byte) is used. When swap bytes equals zero, the swapping begins with an odd byte. (This is so only for data transferring; it is ignored otherwise.)

The following figures (Figures 3-1 and 3-2) indicate the memory positions for the bytes as they are read from or written on the tape. In these examples, the bytes of data in the record block on tape are numbered starting at zero. Byte zero is always the data byte at the beginning of the block (that is, the part of the block that is closest to BOT).

NOTE: When reading in reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

Table 3-2
Command Code and Mode Field Definitions

COMMAND CODE FIELD	COMMAND NAME	COMMAND MODE FIELD	MODE NAME
00001	Read	0000	Read next (forward)
		0001	Read previous (reverse)
		0010	Reread previous (space reverse, read forward)
		0011	Reread next (space forward, read reverse)
00100	Write Characteristics	0000	Load message buffer address and set device characteristic
00101	Write	0000	Write data (text)
		0010	Write data retry (space reverse, erase,write data)
00110	Write Subsystem Memory	0000	Not supported
01000	Position	0000	Space records forward
		0001	Space records reverse
		0010	skip tape marks forward
		0011	Skip tape marks reverse
		0100	Rewind
01001	Format	0000	Write tape mark
		0001	Erase
		0010	Write tape mark entry (space reverse, erase, write tape mark)
01011	Initialize	0000	transport initialize
01111	Get Status Immediate	0000	Get status (END message only)

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

Figure 3-1 Byte Swap Sequence, Forward

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	1	0
1002	3	2
1004	5	4
1006	7	6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	7

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 10(8)
BLOCK SIZE = 10(8) BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

SWAP BYTES = 0
BUFFER ADDRESS = 1000
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	1	0
1002	3	2
1004	5	4
1006		6

SWAP BYTES = 1
BUFFER ADDRESS = 1000
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	0	1
1002	2	3
1004	4	5
1006	6	.

SWAP BYTES = 0
BUFFER ADDRESS = 1001
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000	0	
1002	2	1
1004	4	3
1006	6	5

SWAP BYTES = 1
BUFFER ADDRESS = 1001
BYTE COUNT = 7
BLOCK SIZE = 7 BYTES

1000		0
1002	1	2
1004	3	4
1006	5	6

Figure 3-2 Byte Swap Sequence, Reverse

3.2.2 Command Packet Examples

Examples of the command packets and operational programming notes used in the transport Sybsystem are provided in this section. Refer to the figure and section number corresponding to the command packet example you are interested in.

NOTE: All four words of the command packet are always read in, even if the command takes only one word (rewind) or two words (space). Thus, the command packet must contain four words, and it must have good parity because the transport will reject the command packet on the basis of errors in the unused words.

Command Packet Example	Section Number
Get status	3.2.2.1
Read	3.2.2.2
Write characteristics	3.2.2.3
Write	3.2.2.4
Position	3.2.2.5
Format	3.2.2.6
Control	3.2.2.7
Initialize	3.2.2.8

3.2.2.1 Get Status Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FMT 1	COMMAND
ACK	CVC 0 0	0 0 0 0	IE 0 0	0 1 1 1 1
NOT USED				

MODE: 0000 = GET STATUS (END MESSAGE ONLY)

NOTE: See message packet examples for data format

The get status command packet is illustrated above. This command causes an update of the five extended status registers in the message buffer area. However, after the end of any command, the transport hardware automatically updates the extended status registers. Therefore, this command need only be used when the

transport has been left idle for some time or when a status register update is desired without performing a read, write or position tape command.

3.2.2.2 Read Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FMT 1	COMMAND
ACK	CVC 0PP SWB	X X X X	IE 0 0	0 0 0 0 1
A15	LOW ORDER BUFFER ADDRESS			A00
0	HIGH ORDER BUFFER ADDRESS	A21 A20 A19 A18 A17 A16		
BUFFER EXTENT (BYTE COUNT) (16 BIT POSITIVE INTEGER)				

NOTE: Bits <A21:A18> are used only when 22-bit addressing is enabled. See paragraph 3.3.3.

The read command packet is illustrated above. There are four modes of operation: read forward, read reverse, reread previous, and reread next. In all cases a read operation is assumed to be for a record of known length. Therefore, the correct record byte count must be known. If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, record length short (RLS) will set and a tape status alert (TSA) termination occurs. If the record is larger than the byte count, record length long (RLL) and tape status alert (TSA) will be set. Also, any read operation that encounters a tape mark does not transfer any data. In this case tape mark (TMK) and record length short (RLS) are set and a tape status alert (TSA) termination occurs.

Read reverse operations which run into BOT cause Reverse Into BOT (RIB) to set and cause a tape status alert (TSA) termination. Tape motion will stop at BOT. Read reverse while at BOT will cause a function reject (NEF) status, with no tape motion.

NOTE: When reading reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

3.2.2.3 Write Characteristics Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FMT 1	COMMAND
ACK	CVC 0 0	0 0 0 0	IE 0 0	0 0 1 0 0
A15	LOW ORDER CHARACTERISTICS DATA ADDRESS			A00
0	HIGH ORDER CHARACTER DATA ADDR	A21 A20	A19 A18	A17 A16
	BUFFER EXTENT (BYTE COUNT) (16 BIT POSITIVE INTEGER)			

MODE: 0000 = Load message buffer address ad set device characteristics

NOTE: Bits <A21:A18> are used only when 22-bit addressing is enabled. See paragraph 3.3.3.

CHARACTERISTICS DATA

A15	LOW ORDER MESSAGE BUFFER ADDRESS														A00
0	HIGH ORDER MESSAGE BUFFER ADDR									A21	A20	A19	A18	A17	A16
	LENGTH OF MESSAGE BUFFER (16 BIT POSITIVE INTERGER) (AT LEAST 14 BYTES LONG)														
0	0	0	0	0	0	0	0	ESS	ENB	EAI	ERI	0	0	0	0
	CHARACTERISTICS MODE BYTE														

NOTE: Bits <A21:A18> are used only when 22-bit addressing is enabled. See paragraph 3.3.3.

The figure above illustrates the write characteristics command packet. Its objective is to inform the transport Subsystem of the

location and size of the message buffer in CPU memory space. The message buffer must be at least seven contiguous words long and begin on a word boundary.

The write characteristics command also transfers a characteristics mode byte to the transport. This word causes specific actions for certain operational modes. The bits for this word are defined below.

If a good message buffer address has not been loaded with a write characteristics command, the need buffer address (NBA) bit in the TSSR register will be set.

Enable Skip Tape Marks Stop (ESS) - Bit 07

When this bit is set, it instructs the transport to stop during a skip tape mark command when a double tape mark (two contiguous tape marks) has been detected. In the default setting of 0, the skip tape marks command will terminate only on tape mark count exhausted or if it runs into BOT.

(ENB) - Bit 06

This bit is only meaningful if the ESS bit is set. If the transport is at BOT when a skip tape marks command is issued and the first record seen is a tape mark, then the transport will set LET and stop after the first tape mark. If the bit is clear, the transport would not set LET but count the tape mark and continue.

Enable Attention Interrupts (EAI) - Bit 05

When this bit is a zero, attention conditions, such as off-line, on-line, and microdiagnostic failure, will not result in interrupts to the CPU. If set to a one, interrupts will be generated.

NOTE: transport must own the message buffer, via message buffer release, to set attention interrupts.

Enable Message Buffer Release Interrupts (ERI) - Bit 04

If this bit is zero, interrupts will not be generated when a message buffer release command is received by the transport. Upon recognition of the command, only subsystem ready (SSR) will be reasserted. If ERI is a one, an interrupt will be generated.

3.2.2.4 Write Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FMT 1	COMMAND
ACK	CVC 0 SWB	X X X X	IE 0 0	0 0 1 0 1
A15	LOW ORDER BUFFER ADDRESS			A00
0	HIGH ORDER BUFFER ADDRESS		A21 A20 A19 A18 A17 A16	
BUFFER EXTENT (BYTE COUNT) (16 BIT POSITIVE INTEGER)				

Mode: 0000 = Write Data
0010 = Write Data retry (space rev erase, write data)

NOTE: Bits <A21:A18> are used only when 22-bit addressing is enabled. See paragraph 3.3.3.

The figure above illustrates the write command packet. There are two modes: write data and write data retry (space reverse, erase, write data). Each operation is straightforward and designed to transfer data onto tape in the forward direction only.

If a write command is executed at or beyond the EOT marker a tape status alert (TSA) termination will occur. EOT will remain set until passed in the reverse direction or a subsystem initialize.

If a write command is executed anywhere and the identification burst (IDB) was previously written bad or was not found when it left BOT, then density check (DCK) is set and tape position lost termination occurs.

3.2.2.5 Position Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FTM 1	COMMAND
ACK	CVC 0 0	X X X X	IE 0 0	0 1 0 0 0
TAPE MARK/RECORD COUNT (16 BIT POSITIVE INTEGER)				

Mode: 0000 = Space Records Forward
0001 = Space Records Reverse
0010 = Skip Tape Marks Forward
0011 = Skip Tape Marks Reverse
0100 = Rewind

The position command packet is illustrated above. This command causes tape to space records forward or reverse, skip tape marks forward or reverse, and to rewind to BOT. An exact tape mark/record count must be the second word of the packet for skip tape mark and space record commands.

A space records operation automatically terminates when a tape mark is traversed. Also, record length short (RLS) is set if the record count was not decremented to zero.

A skip tape marks command terminates when it encounters a double Tape mark and the enable skip stop mode is specified (ESS bit set) in the characteristics word. Termination will also occur if a tape mark is the first record off BOT and ESS and ENB bits are set in the characteristics word. Record length short (RLS) is set if the record count is not decremented to zero.

A space records reverse or skip tape marks reverse, which runs into BOT, sets reverse into BOT (RIB) and causes a tape status alert termination.

When a rewind command is issued, the interrupt will not occur until the tape reaches BOT in the forward direction and has begun to decelerate. Due to tape speed during rewind, the transport overshoots BOT in the reverse direction and then moves the tape forward until BOT is located before terminating the operation. Normal termination will be indicated if the operation is completed without incident. If the tape is already at BOT, the rewind will still be done to make sure the tape is positioned properly.

NOTE: If the tape is positioned between BOT and the first record and you do a space reverse or skip reverse, RIB will set and the residual frame count equals the specified count in the original command.

3.2.2.6 Format Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FTM 1	COMMAND
ACK	CVC 0 0	X X X X	IE 0 0	0 1 0 0 1
NOT USED				

MODE: 0000 = Write Tape Mark
0001 = Erase
0010 = Write Tape Mark Retry (space rev. erase, write tape mark)

The above figure illustrates the format command packet. This command can write a tape mark, rewrite a tape mark, and erase tape. In all cases, executing a format command at our beyond EOT will cause a tape status alert (TSA) termination. The EOT bit will remain set until passed in the reverse direction. A subsystem initialize can also reset the EOT bit. Also, any format command executed with density check (DCK) set will cause a tape position lost termination.

Density check is set when a invalid identification burst (IDB) is read off BOT. This occurs in a read after write mode within the first three inches of tape and is transparent to the user's operation.

The erase command will cause three inches of tape to be erased. This length is controlled automatically by the transport hardware. Successive erase commands can be used to erase more than three inches (in three inch increments).

3.2.2.7 Control Command

15	14 12	11 08	07 05	04 00
CTL	DEV. DEP.	MODE	FTM 1	COMMAND
ACK	CVC 0 0	X X X X	IE 0 0	0 1 0 1 0
NOT USED				

MODE: 0000 = Message Buffer Release
0001 = Unload
0010 = Clean Tape

The figure above illustrates the control command packet. The three modes of operation are message buffer release, unload, and clean. The message buffer release command, when executed with the ACK bit set, allows the transport to own the message buffer so it can update the status in the status in the message buffer area on an ATTN. This is beneficial when the operating system is processing data in other areas not concerned with operating the transport Subsystem and the host wants to know the current transport status.

The unload command is designed to rewind tape completely onto the supply reel. When the command is executed, termination occurs immediately; an interrupt will occur if IE is set.

The clean tape command moves ten inches of tape over the tape cleaners and returns it to the original position. Successive clean tape commands are not recommended since the tape may creep outside the interrecord gap (IRG) margins. Also, the clean tape command does not recognize BOT. (That is, you can clean tape and reverse past BOT and back again without setting status bits.)

3.2.2.8 Initialize Command

15	14	12	11	08	07	05	04	00
CTL	DEV.	DEP.	MODE		FMT 1		COMMAND	
ACK	CVC	0 0	0	0 0 0	IE	0 0	0	1 0 1 1
NOT USED								

MODE: 0000 = Transport Initialize

The initialize command packet is illustrated above. This command is not very useful, but is included for compatibility with packet protocol. A transport initialize can be done by a write to the TSSR, as this action does not need a command packet.

The transport initialize command is a no-op. It results in a message update, just like a get status, if there are no microdiagnostic or runaway errors. However, if errors are displayed, the command does the same thing as a write to the TSSR. Section 3.1.3 contains TSSR details.

3.2.3 Message Packet Header Word

15	14 12	11 08	07 05	04 00
CTL	RESERVED	CLASS CODE	PACKET FORMAT 1	MESSAGE CODE
ACK	0 0 0	0 0 C C	0 0 0	1 M M M M

Acknowledge - Bit 15

This bit is used by the transport to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set since the transport does not own the command buffer.

Reserved - Bits <14:12>

These bits are reserved for future expansion.

Class Code Field - Bits <11:08>

These bits define the class of failures found in the rest of the message buffer.

MSG Type	Class Value	Definition
ATTN	0000	On-or off-line
FAIL	0001	Other (ILC,ILA,NBA)
FAIL	0010	Write lock error or non-executable function

Packet Format #1 Field - Bits <07:05>

The single value supported by the TS12 is as follows.

Value	Definition
000	One word header

Message Code - Bits <04:00>

Term Class	Value	Definition
0,2	10000	End
3	10001	Fail
4,5,6,7	10010	Error
1	10011	Attention

3.2.4 Message Packet Example

All message packets are identical. Each message packet contains the message packet header word just described, plus a data length field word and the five extended status registers. The figure below illustrates the message packet format.

15	14 12	11 08	07 05	04 00
CTL	DEV. STAT	STD. STATUS	FMT 1	MESSAGE
ACK	0 0 0	0 0 X X	0 0 0	M M M M M
0	0 0 0	0 0 0 0	0 0 0	0 1 0 1 0
RBPCR				
XSTAT0				
XSTAT1				
XSTAT2				
XSTAT3				

MESSAGES: 10000 = END
BITS 4:0 10001 = FAIL
10010 = ERROR
10011 = ATTN

STD STATUS: FAIL MSG.
BITS 11:8 0001 = OTHER
0010 = WRITE LOCK ERROR OR NON-EXECUTABLE FUNCTION
ATTN MSG
0000 = ON OR OFF LINE

3.3 OPERATIONAL INFORMATION

The following information considers the operation and programming requirements of the transport Subsystem.

3.3.1 Q-Bus Registers

Each transport has two Q-Bus word locations used as device registers. The base address, when written to, is the data buffer register (TSDB). When read, it is the bus address register (TSBA). The second device register (base address + 2) is the status register (TSSR). Writing to the TSSR causes a subsystem initialize command, and reading the TSSR reads device status.

The TSDB register is the only register written to during normal operations. DATO or word access must be used to properly write command pointers to the TSDB. DATOB or byte access to the TSDB causes maintenance functions.

Commands are not written to the transport's Q-Bus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used by the transport to retrieve the words in the command packet. The words of the command packet tell the transport the function to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

3.3.2 Command and Message Packets

Command packets must reside on modulo - 4 address boundaries within CPU memory space. This means the starting address of the packet must be devisible by 4 (that is, octal 00, 04, 10, 14, etc.).

All four words of a command packet must exist and have good memory parity, even if all four words are not used by a command. (For instance, rewind uses only one word.)

Message packets are issued by the subsystem and are deposited into the CPU's memory space. Controlled operation of the transport requires that it be supplied a message buffer address on write characteristics command. The five extended status registers are stored in this message buffer area. The END message packet, which results at the end of any command, contains these extended status words.

3.3.3 22-Bit Memory Addressing

Twenty-two bit addressing capability is available for the TC02. The Emulex part number for the kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U107 on the TC02 PCBA.

To use the 22-bit addressing capability, the programmer must specify the 22-bit address in the command packet as indicated in the various packet examples in paragraphs 3.2.2.2, 3.2.2.3 and 3.2.2.4. Also, SW1-2 must be ON (closed).

Note that no facility is provided for specifying 22-bit command packet addresses when initiating a command using the TSDB. Consequently, command packets must be located in 18-bit address space.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an TC02 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An TC02 without the addressing option will not be damaged if power is present on those lines.

3.3.4 Special Conditions and Errors

Table 3-3 includes the meanings of the binary values within the termination classs code field in the TSSR register.

3.3.5 Status Error Handling Notes

TSSR error bits, other than the fatal class, termination class, and SC bits, are cleared by loading a command pointer into the TSDB register. SC is reset if it is due to a TSSR error (UPE,SPE,RMR,or NXM). Extended status error bits are cleared after the END message is sent.

All commands (even get status command) clear the XSTAT error bits; except XSTAT3 bits 15 through 08 (microdiagnostic error code) and bit LXS are not cleared.

If a density check condition is detected during a read, space, or skip function, the DCK bit is set, but the operation is not stopped. If DCK is the only status bit set during the operation, normal termination is reported. This allows tapes with good data but bad density check areas to be read. If a wrong density tape has been mounted, other errors will be reported and the operation will stop. Note that if only the density check area is bad, the density check indicator on the transport's operator panel lights, even though the data records might be the correct density. The DCK indicator will remain lit until BOT is encountered again or until a subsystem initialize is performed. Note that if you can begin reading a tape, get a density check condition with no other errors, then append to the tape; the write will get a termination class

Table 3-3
Termination Class Codes

TC2-0 Value	Msg Type	Offset	Meaning
0	END	00	Normal termination: This bit indicates the operation was completed without incident.
1	ATTN	02	Attention Condition: This code indicates that the transport has undergone a status change going off-line, coming on-line, or a microdiagnostic failure.
2	END	04	Tape Status Alert: This bit indicates a status condition has been encountered that has significance to the program. Bits of interest include TMK, EOT, RLS, and RLL.
3	FAIL	06	Function Reject: This bit indicates the specified function was not initiated. Bits of interest iclude OFL,VCK,BOT,WLE,ILC and ILA.
4	ERR	10	Recoverable Error: This bit indicates tape position is one record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate retry command.
5	ERR	12	Recoverable Error: This bit indicates tape position has not changed. Suggested recovery procedure is to log the error and reissue the original command.
6	ERR	14	Unrecoverable Error: This bit indicates tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers.
7	ATTN/ ERR	16	Fatal Subsystem Error: This bit indicates the subsystem is incapable of properly performing commands or at least that the subsystem's integrity is seriously questionable.

code of 6. This indicates that the tape position is lost because density check will remain set. The whole tape should be copied over so that transports depending on the IDB will be able to read the tape.

A command is not responded to while another command is in progress (result is RMR), except in the following cases.

1. A DATO (word access) to the TSSR (subsystem initialize) brings any operation in progress to an immediate halt. All subsystem parameters which had been in the subsystem's memory (VCK reset, EOT, etc) are erased. Also, if the on-line switch is ON, the transport performs an auto-load sequence and positions the tape at BOT.

2. The transport responds to any nontape motion command while performing a rewind unload (while the transport is off-line) because SSR is still up.

The transport also responds to any nontape motion commands (get status, transport initialize, set characteristics, and message buffer release) when off-line, except when in maintenance mode. (The subsystem ready command, SSR, is not asserted in this case and results in RMR.)

The following failures can occur without resulting in an interrupt, even though the specified command had interrupt enable set.

SPE The possibility exists that the transport cannot transfer valid data or command information via the serial bus to the transport. In this case the SC, TC2, TC1, and TC0 bits are not valid either.

NXM They might occur before the interrupt enable bit is fetched as
UPE part of the command packet.
BPE

Section 4
INSTALLATION

This section describes the step-by-step procedure for installation of the TC02 Tape Coupler in a Q-Bus environment. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the TC02, is covered in paragraph 4.1).

Emulex recommends that Section 4 be read in its entirety before installation is begun.

1. Inspect the TC02.
2. Prepare the tape transports.
3. Prepare the CPU.
4. Configure the TC02.
5. Install the TC02.
6. Route the transport I/O cables.
7. Run the diagnostics.

4.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in the sockets.

4.2 TAPE TRANSPORT PREPARATION

4.2.1 Transport Placement

Uncrate and install the tape transports in their racks according to the manufacturer's instructions. Position the racks in their final places before beginning the installation of the TC02. This allows the I/O cable routing and length to be accurately judged. If possible, place the racks side by side to make installation of the daisy-chained cables simpler.

4.2.2 Address Selection

Up to four tape transports may be daisy chained to one TC02. Each tape transport must be assigned a unique device number in the range 0 to 3. The address assigned to the transport determines its Q-Bus address and device name (see Table 4-1). For example, if

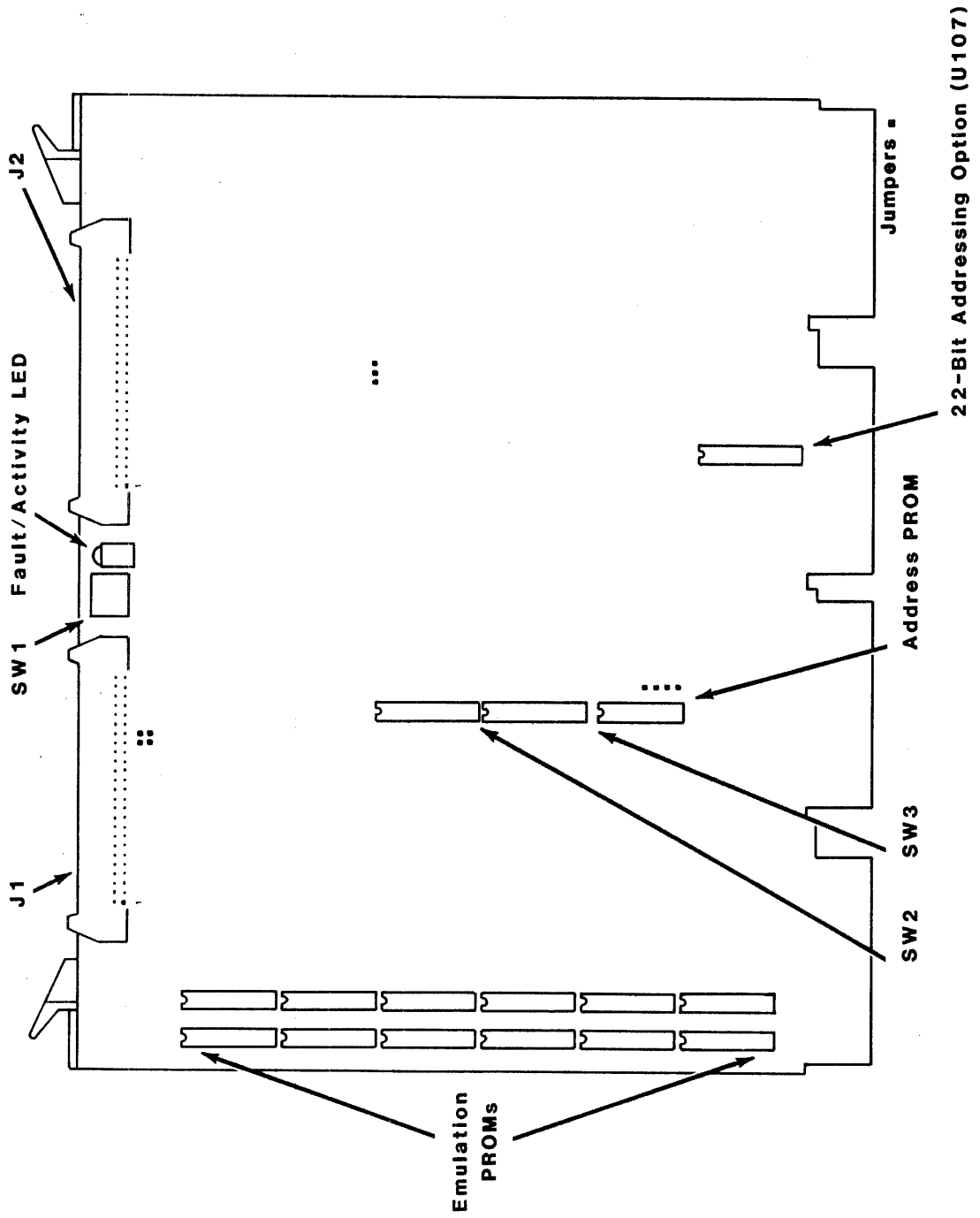


Figure 4-1 TCO2 Coupler Assembly

the address desired is 772524 (unit 1), then SW3-1 would be closed (ON). If that unit alone is to be enabled, SW3-4 would be closed (see Table 4-1, below). The transport's address must be set to one, even if it is the only transport on the coupler.

Numbers for streaming transports may be assigned irrespective of position in the daisy chain.

Formatted (start/stop) transport installations require that the formatter logic have its address set to zero. A second formatter with an address of one is not supported. The address of the host transport that contains the formatter does not have to be set to zero. Any address in the range 0 to 3 may be selected for the host and slave transports irrespective of position in the daisy chain.

Transport addresses are sometimes selected by a thumb switch on the front panel of the transport but more frequently by switches on one of the transport's PCBAs. See the specific transport's installation manual for instructions.

4.3 SYSTEM PREPARATION

4.3.1 Powering Down the System

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power light will remain lit). Slide the CPU rack out of the cabinet and remove the card rack cover. Open the rear door of the cabinet.

4.4 COUPLER SETUP

Several configuration setups must be made on the coupler before inserting it into the chassis. These are made by SW1, SW2 and SW3.

4.4.1 Coupler Modes

The TC02 functions with both streaming and formatted tape drives. The mode of the coupler is determined by the setting of a minimal number of switches. SW1-4 enables the TC02 to interface with a streaming tape transport when OFF (open), and with a formatted tape transport when ON (closed). Below is a brief description of the two types of modes in which the coupler may function.

Formatted Tape Drive Mode: When enabled to function with formatted tape drives, the coupler will read and write DEC or IBM compatible 9-track PE (1600 bpi) or 9-track NRZI (800 bpi) formats. This mode accommodates transport speeds in a range of 12.5 to 125 ips. A maximum of four tape transports may be attached to the coupler with any mix of 9-track NRZI, PE or dual density.

Streaming Tape Drive Mode: The streaming mode is media compatible with tapes created on the DEC TS11. Tapes have 9-tracks at 1600 bpi. In streaming mode, the transport speed is typically 100 ips. In non-streaming mode transport speed is typically 25 ips (check

manufacturer specs. for exact speed). The coupler shifts from non-streaming mode to streaming mode automatically if enough data to support the additional throughput is available. The shift is software transparent.

4.4.2 Coupler Address Selection

The DEC TS11 tape subsystem consists of one tape transport interfaced to the Q-Bus by a coupler. Each TS11 requires two Q-Bus addresses, one for each of its registers. The TC02, which can support up to four individual tape transports, thus emulates four TS11 subsystems. Consequently, each transport interfaced to the system by the TC02 is represented by a unique set of Q-Bus registers. There is a direct relationship between a transport's unit number and the Q-Bus base address for the subsystem it represents. The relationship between the transports and their addresses is depicted in Table 4-1.

The TC02 allows the user to select one of four address ranges. Each range includes starting addresses for four emulations (transports). The starting addresses within each range are contiguous.

The standard address range (selected by SW3-1) includes the CSR addresses fixed for TS11 type devices under VMS and other DEC operating systems. The three alternate ranges are not normally associated with the TS11. If one of the alternate ranges is selected, the autoconfigure utility will not locate or properly identify the device. In that case, the manual connect command can be used to configure the system.

Table 4-1
Q-Bus Starting Addresses

	ADDRESS RANGE					
Transport Number	SW3-1 N/A	SW3-2 J - H	SW3-2 K - H	SW3-2 L - H	Device Name	Enabling Switch
0	772520	772440	776300	777460	MS0	SW3-3
1	772524	772444	776304	777464	MS1	SW3-4
2	772530	772450	776310	777470	MS2	SW3-5
3	772534	772454	776314	777474	MS3	SW3-6

The Emulex TC02 uses switches SW3-1 and SW3-2 to select the standard or alternate range of addresses, respectively. The ranges are represented by the base address for the subsystem represented by the first tape unit (number 0). The standard starting address is 772520. SW3-1 and SW3-2 may not be turned ON at the same time.

The alternate address selected by SW3-2 varies according to the placement of a wire-wrap jumper. Table 4-2 shows the relationship of the jumper to the starting address that is selected.

Table 4-2
Alternate Q-Bus Starting Address Selection

Starting Address	Jumper Connection
772440	J to H
776300	K to H
777460	L to H

The TC02 is shipped from the factory with pins J and H jumpered together. If one of the other starting addresses is required remove the factory jumper and reconfigure as indicated.

4.4.3 Individual Transport Enabling

Each transport that is interfaced to the Q-Bus using the TC02 must be individually enabled using switches SW3-3 through SW3-6. Table 4-1 shows the relationship of the transport to its Q-Bus address and the switch which enables it. This feature is useful if a DEC TS11 is already installed in the CPU at the standard Q-Bus starting address. It is desirable to place the second tape transport (the Emulex emulation) at the next available bus address. This is done by selecting the standard Q-Bus address range on the TC02, assigning the new transport a unit number of 1 and turning SW3-4 ON. The other three enabling switches (SW3-3, SW3-5 and SW3-6) are left OFF to disable those Q-Bus addresses.

The tape transport's unit number must be set to correspond to the Q-Bus address required. That is, if an address of 772524 is required, the transport address would be set to one and SW3-4 would be closed. See paragraph 4.2.2, above.

4.4.4 Interrupt Vector Address

Each tape unit must have an individual interrupt vector address. The TS11 is assigned one fixed interrupt vector (224) under VMS and other DEC operating systems. Vectors required for additional transports are assigned from floating vector address space. See Appendix B for instructions on assigning floating vectors.

When SW2-8 is open (OFF), the address for unit zero is selected by switches SW2-1 through SW2-7. The vector addresses for units 0-3 are contiguous. Each address falls four words from the one before it. For example, if 300 is selected as the vector address for unit 0, the vector address for unit 1 will be 304, the address for unit 2 will be 310, and the address for unit 3 will be 314.

With SW2-8 closed (ON), the standard vector address of 224 is selected for unit 0. The addresses for units 1-3 are contiguous and their starting point is selected as described above. Unit one

will be in the same relationship to the switch setting as previously described; that is, the switch setting plus four. Remember, though, that the vector for unit 0 is 224 regardless of the switch settings with SW2-8 closed (ON).

Figure 4-2 shows the relationship of SW2-1 through SW2-7 to the Q-Bus bits they control.

Vector Address

Octal	2			2			4		
Binary	0	1	0	0	1	0	1	X	X
Address Bit	08	07	06	05	04	03	02	01	00
Switch Setting	ON	OFF	ON	ON	OFF	ON	OFF	X	X
Switch SW2-	7	6	5	4	3	2	1	X	X

Figure 4-2 Vector Address Selection

Some examples of vector address selection are given below. The first example is for all four drives using contiguous vectors, starting at 224.

Unit	CSR Address	Vector	Switch SW2 Setting 1 2 3 4 5 6 7 8
1	772520	224	O C O C C O C O
2	772524	230	
3	772530	234	
4	772534	240	

The second example has drive zero starting at 224 (SW2-8 ON). The remaining three drives have contiguous vectors starting at 300 for drive one. In this example, notice that only three drives have contiguous vectors (drives one through three), and the starting address set by SW2-1 through SW2-7 is 274. SW2-8 forces the drive zero vector to 224.

Unit	CSR Address	Vector	Switch SW2 Setting 1 2 3 4 5 6 7 8
1	772520	224	O C O C C O C C
2	772524	300	
3	772530	304	
4	772534	310	

4.4.5 Speed Selection for Tape Transports

The TC02 supports tape transport speeds of up to 125 ips. The coupler must however, be enabled for either 50 ips and under, or more than 50 ips. The selection is made by SW3-7. This switch sets a time limit that will cause the tape drive to stop after a read command is executed and no data is found on the tape. Setting the switch to ON (closed), enables the coupler to function with tape drives which run at 50 ips and under. Setting the switch to the OFF (open) position enables the coupler to interface to tape drives with speeds greater than 50 ips. For streaming tapes set this switch based on the lowest speed of the tape transport.

4.4.6 Options

The TC02 has several optional features which allow the user to optimize the coupler for a particular application. The options are described below. Keep in mind that some of the options apply to the streaming mode and others to the formatted mode.

4.4.6.1 Density

User may select recording densities of either 1600 (open) or 3200 (closed) bpi using SW1-3. In order to enable the 3200 bpi density, the tape transport must have 3200 bpi capability. This option is applicable only to streaming tape transports.

4.4.6.2 Interblock Gap

When in streaming mode, the length of the interblock gap determines the maximum time in which the operating system software must issue another read or write command to keep the tape drive streaming. If another command is not issued in time, the drive will halt and reposition. By lengthing the interblock gap, the maximum time in which the system has to issue another command is increased. However, longer interblock gaps also use more tape. Normal interblock gaps are .6 in. long, and the software has 2.5 msec to issue another command. The extended gap is 1.2 in. long, and that gives the operating system 8.5 msec to recommand the tape subsysytem. The extended interblock gap is enabled by closing SW2-9.

4.4.6.3 CDC Extended Status Command

When a CDC streaming tape drive is used SW2-10 can be set to the ON (closed) position to enable several status bits in XST1 and XST2 that are otherwise not emulated. These bits include TIG, IPO and UNC in XST1; and the Dead Track bits in XST2. Do not set with other than CDC transports as the results will be indeterminate.

NOTE: With Revision E and above TC02/FS firmware, switch SW2-10 must be ON (closed) for operation of CDC 92185 Group Coded Recording (GCR) tape transports. However, the TC02/FS does not support 75 ips GCR operation. Therefore, the adaptive velocity feature of GCR tape transports must be disabled in the tape transport.

4.4.6.4 22-Bit Memory Addressing

Twenty-two bit addressing capability is available as an option for the TC02. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U107 on the TC02 PCBA. See paragraph 3.3.3 for programming instructions.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a TC02 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. A TC02 without the addressing option will not be damaged if power is present on those lines.

4.5 PHYSICAL INSTALLATION

4.5.1 Slot Selection

The coupler may be placed in any slot along the Q-Bus without regard to NPR priority.

4.5.2 Mounting

The coupler board should be plugged into the Q-Bus backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly in the throat of the connector before attempting to seat the board by means of the extractor handles.

4.6 CABLING

Figure 4-3 is to be used in conjunction with the paragraphs below.

4.6.1 Cabling the TC02 Coupler to a Transport Formatter

The tape transport formatter is connected to the controller with two 50-wire cables. These cables may be ordered in various lengths from Emulex. Below is a list of the available lengths and their corresponding part numbers.

Length (feet)	Part Number
3.0	TU1211201-01
5.0	TU1211201-02
8.0	TU1211201-03
15.0	TU1211201-04
25.0	TU1211201-05
35.0	TU1211201-06
50.0	TU1211201-07

The cables are connected from J1 and J2 on the TC02 to the appropriate connector on the formatter PCBA of the transport. See Table 2-1 for the cable interface signals. Table 4-3 lists TC02 coupler to formatter connections.

Table 4-3
TC02 Coupler to Formatter Connections

Manufacturer	Model	TC02 Connector J1 to:	TC02 Connector J2 to:
CDC (Tandberg)	92180	J125	J124
CDC (Keystone)	92181 (BY3A6)	P4	P5
Cipher	F100X, F900X	P4	P5
Cipher	F880, CT-75, CT-125	P1	P2
Digi-Data	All Formatted	J4	J3
Kennedy	Formatted Start/Stop	J5	J4
Kennedy	Streamer	J1	J2
Pertec	Formatted Start/Stop	P4	P5

The plugs at the controller end of the cable are aligned by matching the arrowhead molded into the controller mounted jack with the arrowhead molded into the cable connector. Proper orientation of the transport connectors can be determined by matching the pin numbers molded into the face of the jack with the numbers etched on the card-edge over which they fit.

Some transport formatters have 100-pin connectors and require an adaptor that allows Emulex's two 50-pin connectors to be used. The adaptor must be ordered from the drive manufacturer.

4.6.2 Daisy-Chaining

Up to four tape transports may be daisy-chained from the TC02.

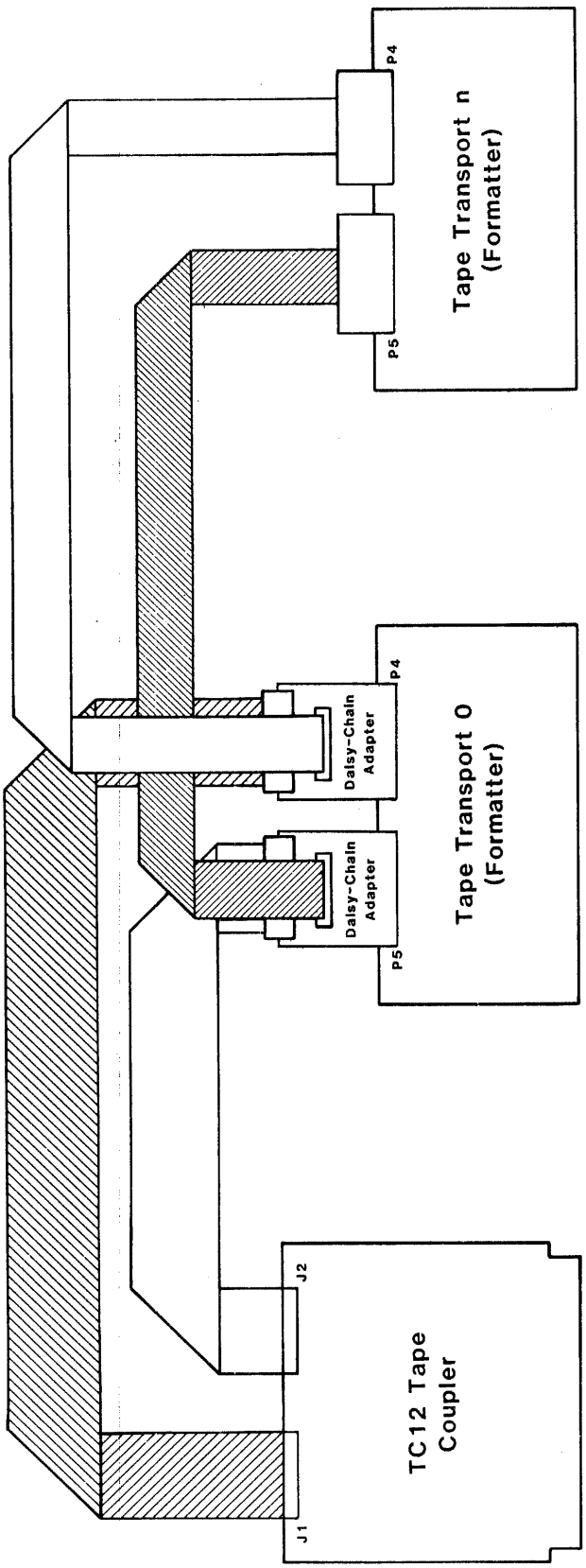


Figure 4-3 Tape Transport Cabling

4.6.2.1 Streaming Tape Transports

Streaming tape transports, all of which have integral formatters, are connected using Emulex's daisy-chain adaptor (TU1210402). Two adaptors (one per cable) are required for every additional drive beyond the first to be connected to the coupler. For example, if you want to daisy-chain three transports together, four adaptors will be required. Standard Emulex cables (see the list above) are used to cable between the drives. Termination is provided on the formatter PCBA. It may be necessary to remove or disable terminators on intermediate transports. See the transport manufacturer's manual.

4.6.2.2 Formatted Tape Transports

The formatter for formatted transports is connected to the TC02 coupler as described in paragraph 4.6.1, above. The slave transports are then daisy-chained from the formatter according to the instructions supplied by the transport's manufacturer. Emulex does not supply the cables that interconnect the transports.

Up to four drives may be daisy-chained in a formatter configured subsystem, however they must all be one of the two allowable speeds.

NOTE: The high-low switches on Kennedy formatters must also be set for the individual drive speeds. Set the switch banks which correspond to unused drives to match the speed of drive zero.

4.6.3 Grounding

For proper operation of the tape subsystem, it is very important that the transports have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between transports.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

4.7 TESTING

4.7.1 Self-Test

When power is applied to the CPU, the coupler will automatically execute a built-in self-test. This self-test is not executed with every bus INIT but only on powering-up. If the self-test has been executed successfully, the Fault LED on the front edge of the coupler board will be OFF. If the Fault LED is ON steadily the coupler did not pass its self-test and the coupler cannot be addressed from the CPU.

4.7.2 Diagnostics

The DEC TS11 diagnostics should be run. Only the Controller Repair Diagnostic (ZTSI, runs first three tests with a minor patch) and the Data Reliability Exerciser (ZTSH) need be run. The diagnostics can be loaded from an XXDP media.

The patch that needs to be applied to ZTSI is:

Location	Is	Should Be
2122	12	3

Appendix A

TC02 OPTION SWITCHES

TABLE A-1
TC02 Factory Switch Settings

Switch	Setting	Switch	Setting	Switch	Setting
SW1-1	OFF	SW2-1	OFF	SW3-1	ON
SW1-2	OFF	SW2-2	OFF	SW3-2	OFF
SW1-3	OFF	SW2-3	OFF	SW3-3	ON
SW1-4	OFF	SW2-4	OFF	SW3-4	OFF
		SW2-5	OFF	SW3-5	OFF
		SW2-6	OFF	SW3-6	OFF
		SW2-7	OFF	SW3-7	ON
		SW2-8	ON	SW3-8	OFF
		SW2-9	OFF	SW3-9	OFF
		SW2-10	OFF	SW3-10	OFF*

*For firmware revision A, switch SW3-10 must be ON.

With the factory switch settings one tape drive (MS0) is enabled with a starting address of 772520 and an interrupt vector address of 224. These factory settings enable the TC02 to interface with streaming tape drives. To enable the TC02 to interface with formatted tape drive set SW1-4 to ON (closed). The controller will still enable tape drive MS0 with a starting address of 772520 and interrupt vector of 224.

TABLE A-2
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Reset	Coupler Reset
SW1-2	Disable	Enable	22-Bit Addressing Mode
SW1-3	Disable	Enable	3200 bpi tape density[1]
SW1-4	Streaming	Formattted	Tape drive type[2]

[1]For tape drives with 3200 bpi capability only.

[2]See paragraph 1.2.2.

Note: When SW1-3 and SW1-4 are ON at the same time the streaming mode will be disabled for streaming tape drives.

TABLE A-3
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW2-1	One	Zero	Interrupt Vector Address Bit 2[2]
SW2-2	One	Zero	Interrupt Vector Address Bit 3[2]
SW2-3	One	Zero	Interrupt Vector Address Bit 4[2]
SW2-4	One	Zero	Interrupt Vector Address Bit 5[2]
SW2-5	One	Zero	Interrupt Vector Address Bit 6[2]
SW2-6	One	Zero	Interrupt Vector Address Bit 7[2]
SW2-7	One	Zero	Interrupt Vector Address Bit 8[2]
SW2-8		224	Unit 0 Interrupt Vector Address[2]
SW2-9	Disable	Enable	Long Interblock Gap Enable[4]
SW2-10	Disable	Enable	CDC extended status and GCR operation[3]

[1]All unused switches MUST BE OFF.

[2]See paragraph 4.4.3

[3]See paragraph 4.4.5.4.

[4]Streaming tape only.

TABLE A-4
OPTION SWITCH SETTINGS

Option Sw	Open	Closed	Function
SW3-1			Standard Q-Bus Address[2]
SW3-2			Alternate Q-Bus Address
SW3-3	Disable	Enable	Unit 1 enabled
SW3-4	Disable	Enable	Unit 2 enabled
SW3-5	Disable	Enable	Unit 3 enabled
SW3-6	Disable	Enable	Unit 4 enabled
SW3-7	>50 ips	0-50 ips	Tape drive type[4]
SW3-8	Disable	Enable	Inhibit on-the-fly commands
SW3-9			Not used[1]
SW3-10	2K	1K	PROM Address Range[3]

[1]All unused switches MUST BE OFF.

[2]See paragraph 4.4.1

[3]This switch should be closed (ON) for firmware revision A only, and open (OFF) for firmware revisions B and above.

[4]See paragraph 4.4.4.

Appendix B

AUTOCONFIGURE FOR VMS, RSTS/E AND RSX-11M

B.1 OVERVIEW

This appendix describes the algorithms for assignment of floating device addresses and interrupt vector addresses for VMS, RSTS/E and RSX-11M systems. Several devices have floating addresses; therefore, the presence or absence of floating devices affects the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to DEC standards, interrupt vector addresses must be assigned in a specific sequence and the presence of one type of device affects the correct assignment of interrupt vector addresses for the other devices.

B.2 DETERMINING THE CSR DEVICE ADDRESS FOR USE WITH AUTOCONFIGURE

CSR device addresses for those devices not assigned fixed numbers are selected from the floating CSR device address space (760010 - 763776) of the Q-Bus input/output (I/O) page.

Selection of the CSR device address for a floating-address device depends on the algorithm used by the SYSGEN utility during execution of the Autoconfigure routine. The algorithm is used with the appropriate SYSGEN device. SYSGEN devices are listed in Table B-1.

Table B-1. SYSGEN Device Table

Rank	Device	Registers	Rank	Device	Registers
1	DJ11	4	15	LPA11	8
2	DH11	8	16	KW11C	4
3	DQ11	4	17	Reserved	4
4	DU11	4	18	RX211	4
5	DUP11	4	19	DR11W	4
6	LK11	4	20	DR11B	4
7	DMC11/DMR11	4	21	DMP11	4
8	DZ11	4	22	DPV11	4
9	KMC11	4	23	ISB11	4
10	LPP11	4	24	DMV11	8
11	VMV21	4	25	UNA	4
12	VMV31	8	26	UDA	2
13	DWR70	4	27	DMF32	16
14	RL11	4	28	KMS11	8

Essentially, SYSGEN checks each valid CSR device address in the floating CSR device address space for the presence of a device. SYSGEN expects any devices installed in that space to be in the other address specified by the SYSGEN Device Table. Also, SYSGEN expects an eight-byte block to be reserved for each device that is not installed in the system. Each empty block tells SYSGEN to observe the next higher address on an eight-byte boundary for the next listed device.

When a device is detected, SYSGEN reserves a block of addresses for that device according to the number of registers used by that device (see Registers columns in Table B-1). SYSGEN then observes the next CSR device address space on an eight-byte boundary (the device address is always an octal number that ends in zero). If a device is present at that next address, it is assumed to be the same type of device as the previous device, and a block of bytes is reserved for that device. If SYSGEN receives no response from any device at that next address, that space is reserved to indicate there are no more devices of that type. SYSGEN then checks the next highest CSR device address space on an eight-byte boundary for the next device in the SYSGEN Device Table.

In summary, four rules govern the assignment of CSR device addresses in floating-address spaces:

a. Devices with floating CSR device addresses must be attached in the other in which they are listed in the SYSGEN Device Table.

b. The first address of a new type device must be on a 2 | N word boundary, where N is the first integer greater than or equal to LOG_2M, and M is the number of device registers. Possible boundaries are listed in the following table:

Number of Registers in Device	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5, 6, 7, 8	XXXX00, XXXX20, XXXX40, XXXX60
9 through 16	XXXX00, XXXX40

c. A gap of at least eight bytes must the register block for any installed device to indicate there are no more devices of that type.

d. An eight-byte gap must be reserved in the floating-address space for each device type that is not currently installed in the system.

B.3 DETERMINING THE INTERRUPT VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

Floating interrupt vector addresses for communications devices and other devices that interface with the Q-Bus are assigned according to a standard convention; in which the order sequence starts at 300 and proceeds to 777. The assigned priority sequence is listed in Table B-2.

Table B-2
Priority Ranking for Floating Interrupt Vector Addresses
(starting at 300_8 and proceeding upward to 777_8

Rank	Option	Number of Vectors	Octal Modulus (Address)
1	DC11	2	10[1]
1	TU58	2	10[1]
2	KL11 (extra)	2	10
2	DL11-A (extra)	2	10
2	DL11-B (extra)	2	10
3	DP11	2	10
4	DM11-A	2	10
5	DN11	1	4
6	DM11-BB--CS21/H2	1	4
7	DH11 modem control	1	4
8	DR11-A	2	10
9	DR11-C	2	10
10	PA611 (reader + punch)	4	10
11	LPD11	2	10
12	DT11	2	10
13	DX11	2	10
14	DL11-C	2	10
14	DL11-D	2	10
14	DL11-E	2	10
15	DJ11	2	10
16	DH11--CS21/H2	2	10
17	GT20	4	10
17	VSV11	4	10
18	LPS11	6	10
19	DQ11	2	10
20	KW11-W	2	10
21	DU11	2	10
22	DUP11	2	10
23	DV11+modem control	3	10
24	LK11-A	2	10
25	DWUN	2	10
26	DMC11	2	10
26	DMR11	2	10
27	DZ11	2	10
28	KMC11	2	10
29	LPP11	2	10
30	VMV21	2	10

Table B-2 (continued)

Rank	Option	Number of Vectors	Octal Modulus (Address)
31	VMV31	2	10
32	VTV01	2	10
33	DWR70	2	10
32	RL11/RLV11	1	4 (after the first)
35	RX02	1	4
36	TS11	1	4 (after the first)
37	LPA11-K	2	10
38	IP11/IP300	2	4
39	KW11-C	2	10
20	RX11	1	4 (after the first)
21	DR11-W	1	4
22	DR11-B	1	4 (after the first)
23	DMP11	2	10
22	DPV11	2	10
25	ISB11	2	10
26	DMV11	2	10
27	UNA	1	4
28	UDA	1	4
29	DMF32	8	4

[1] There is no standard configuration for systems with both DC11 and TU58.

For a given system configuration, the device with the highest floating interrupt vector address would be assigned interrupt vector address 300 (all these interrupt vector address numbers are in octal). Additional devices of the same type would be assigned subsequent interrupt vector addresses according to the numbers of interrupt vector addresses required by the device and the starting boundary assigned to that device type.

Interrupt vector addresses are assigned on the boundaries indicated in the Octal Modulus column of Table B-2. For example, if the Modulus boundary is 10, the first interrupt vector address for that device must end with zero (XX0), and if the Modulus boundary is 4, the first interrupt vector address for that device can end with a zero or a four (XX0 or XX4).

Interrupt vector address boundaries always fall on Modulo-4 (XX0 or XX4). An interrupt vector address ends only in four or zero and can never end in any other number. If the device has four interrupt vector addresses and the first must start on a Modulo-10 boundary, then if 350 is used as a starting point, the interrupt vector addresses should be 350, 354, 360 and 364.

B.4 A SYSTEM CONFIGURATION EXAMPLE

Table B-3 lists devices and addresses for a system configuration that includes devices with fixed CSR device addresses and interrupt vector addresses, and with floating CSR device addresses and interrupt vector addresses.

Table B-3. Example of CSR Device and Interrupt Vector Addresses

Controller or Tape Coupler	Interrupt Vector Address	CSR Device Address
1 DN11	300	17775200
1 DU11	310	17760040
1 DV11	320	17775000
1 DMC11	340	17760100
2 DZ11s	350	17760120
	360	17760130
2 TS11s	224	17772520
	370	17772524
3 DR11Bs	124	17772410
	400	17772430
	410	17760300
2 DMP32s	420	17760400
	460	17760440

Table B-4 lists and shows how the CSR device addresses for the floating-address devices in Table B-3 were computed, including interblock gaps (Gap).

Table B-4. Floating Address Computation

Installed	Device	Address	Installed	Device	Address
	DJ11 Gap	17760010		RL11 Gap	17760220
	DH11 Gap	17760020		LPA11 Gap	17760230
	DQ11 Gap	17760030		KWC11 Gap	17760240
--->	DU11	17760040		Reserved	17760250
	DU11 Gap	17760050		RX211 Gap	17760260
	DUP Gap	17760060		DR11W Gap	17760270
	LK11 Gap	17760070	--->	DR11B	17760300
--->	DMC11	17760100		DR11B Gap	17760310
	DMC11 Gap	17760110		DMP11 Gap	17760320
--->	DZ11	17760120		DPV11 Gap	17760330
--->	DZ11	17760130		ISB11 Gap	17760340
	DZ11 Gap	17760140		DMV11 Gap	17760350
	KMC11 Gap	17760150		UNA Gap	17760360
	LPP11 Gap	17760160		UDA Gap	17760370
	VMV21 Gap	17760170	--->	DMF32	17760400
	VMV31 Gap	17760200	--->	DMF32	17760440
	DWR70 Gap	17760210			

BLANK