

**SC72/BX
DISK CONTROLLER
TECHNICAL MANUAL
(4 AND 8 PORT VERSIONS)**



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This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with instructions in this technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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EMULEX PRODUCT WARRANTY

DISK CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex disk controller product supplied shall be free from defects in material and workmanship.

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The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adapters, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product in such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and unless otherwise stated, pay return transportation cost for such replacement. Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement.

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1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC72/BX Disk Controller, manufactured by Emulex Corporation. In addition, this manual provides diagnostic and application information.

The contents of the seven sections and two appendices in this manual are briefly outlined in the following descriptions:

- Section 1 **Introduction.** This section contains an overview of the SC72/BX disk controller and includes the specifications.
- Section 2 **General Description.** This section includes the description of physical characteristics and interfaces.
- Section 3 **Installation.** This section contains the information necessary to set-up and physically install the SC72/BX disk controller system.
- Section 4 **Programming, Operation, and Controller Registers.** This section describes programming requirements, operation techniques, and functions of words, bytes, fields, and bits contained in all registers.
- Section 5 **Commands.** This section describes all commands used by the SC72/BX disk controller system.
- Section 6 **Diagnostics.** This section describes the diagnostic programs, routines, and utilities for the SC72/BX disk controller system.
- Section 7 **Troubleshooting.** This section describes fault isolation procedures that can be used to pinpoint trouble spots.
- Appendix A **SC72/BX Configuration and Option Selection.** This appendix provides instructions for configuring the SC72/BX disk controller, and for selecting options by means of switches.
- Appendix B **Disk Drive Modifications.** This appendix provides modification instructions to move the Sector and Index signals from the A-Cable to the B-Cable.

1.1.1 RELATED DOCUMENTATION

Three other Emulex manuals are related to the SC72/BX Disk Controller:

- **PDP-11 Patch Manual (PD9950902-00).** This manual describes operating system patches which may be necessary when operating with disk drives that have nonstandard capacities.
- **TRACKR User's Manual (PD9950905-00).** This manual describes the TRACKR software which can be used to perform track replacement on RP06 emulations.
- **Disk Maintenance Utility (SXBX0D) User's Guide (PD9950904-00).** This manual describes the SXBX0D utility, which is used to prepare a new disk to contain data or to maintain the integrity of disks in use.

1.2 OVERVIEW

The SC72/BX Disk Controller is an embedded controller for the PDP-11/70 computer central processing unit (CPU), manufactured by Digital Equipment Corporation (DEC). It consists of four printed circuit board assemblies (PCBAs), and can be used to interface with any large disk drive subsystem that has a Storage Module Drive (SMD) interface. The SC72/BX disk controller is capable of emulating RM02, RM03, RM05, RM80, RP04, RP05, and RP06 DEC Massbus disk subsystems, and of operating with disk drives that have different characteristics from those used in the DEC disk subsystems. The SC72/BX disk controller provides the capability of operating with a mixture of disk drives that have storage capacities ranging upward from five megabytes.

Emulation of these disk drive systems is done by using programmable read-only memory (PROM) integrated circuits (ICs) that can be configured and selected for the wide range of disk drive capacities. One or two logical disk drive units may be mapped on each physical disk drive, and the logical number of cylinders, tracks, and sectors may be remapped to suit a different number of physical cylinders, tracks, and sectors with no correspondence between physical addresses (see subsection 1.3.6).

1.3 FEATURES

Features that enhance performance and increase versatility are described in the following subsections.

1.3.1 MICROPROCESSOR DESIGN

The SC72/BX design incorporates a unique (patent pending) 16-bit, bipolar microprocessor to perform all disk controller functions. Using the microprocessor reduces the component count, provides high reliability and easy maintainability, and enables a single set of hardware to be adapted to a wide range of emulation capabilities through the flexibility of microprogramming. The SC72/BX disk controller achieves functional capability that exceeds performance of emulated DEC controllers by providing enhancement features such as built-in self-test during power-up, built-in disk formatting, and ability to work with disk drives of various types, sizes and capacities.

1.3.2 PACKAGING

The SC72/BX disk controller is constructed on three hex-sized PCBAs and one dual-width multiple-layer PCBA which plug directly into the backplane of the PDP-11/70 CPU chassis. No cabling is required between the PDP-11/70 CPU and the SC72/BX disk controller. The SC72/BX disk controller obtains its power from the PDP-11/70 CPU.

1.3.3 SELF-TEST

The SC72/BX disk controller incorporates an internal self-test routine which is executed during power-up. This self test exercises all parts of the microprocessor, random access memory (RAM) buffer, and disk data logic circuitry. Although this self-test routine does not completely test all SC72/BX disk controller circuitry, successful execution of the self-test routine indicates the SC72/BX disk controller is probably operational. If the SC72/BX disk controller fails the self-test routine, the Fault light emitting diode (LED) on the controller is illuminated (ON) and the controller cannot be addressed from the CPU.

1.3.4 BUFFERING

The SC72/BX disk controller contains a 4K x 16-bit high-speed RAM buffer that temporarily stores the contents of the controller's device registers plus up to 14 sectors of data from the selected disk drive. Buffer operations eliminate the possibility of a data-late condition, and permit the SC72/BX disk controller to be operated at low bus priorities.

1.3.5 ERROR CORRECTION

The SC72/BX disk controller includes a 32-bit error correcting code (ECC) that is capable of correcting single error bursts up to 11 bits long, and of detecting error bursts of longer length. The SC72/BX disk controller determines the location of the error and the error pattern and passes this information to the PDP-11/70 CPU which performs the actual correction. A 16-bit cyclic redundancy check character (CRCC) is included in the header of every sector.

1.3.6 OPTION AND CONFIGURATION SWITCHES

The SC72/BX disk controller has switches in dual in-line package (DIP) switch packs that can be used to configure the SC72/BX disk controller for various disk capacities, bus addresses, interrupt vector addresses, and various firmware options. It is possible to select one of several possible combinations of disk characteristics for up to eight physical disk drives that can be handled by the SC72/BX disk controller, including a mixture of disk capacities and disk drive type codes.

1.3.7 DUAL PORT CAPACITY

The SC72/BX disk controller can operate with disk drives that have dual-port capability. This feature allows a second disk controller to have access to any system disk drive on a priority basis.

1.3.8 DUAL ACCESS CAPABILITY

The Dual Access mode is supported by the SC72/BX disk controller to provide compatibility with disk drives when the system is configured for dual-access operation. When in the Dual-Access mode, the SC72/BX disk controller sets the DPM bit in the Drive Type Register and the PGM bit in the Drive Status Register. These bits are set to allow the SC72/BX disk controller to imitate the DEC neutral state.

1.4 FUNCTIONAL COMPATIBILITY

The SC72/BX disk controller is compatible with media, address mapping, diagnostics, and operating systems to the extent described in this subsection.

1.4.1 MEDIA COMPATIBILITY

The SC72/BX disk controller is media compatible with the following DEC disk drive emulations:

- RM02 and RM03 disk packs when using a CDC 9762 disk drive or equivalent
- RM05 disk packs when using a CDC 9766 disk drive or equivalent
- RP06 disk packs when using a Memorex 677 (200 megabyte) disk drive or equivalent.

1.4.2 DISK MAPPING

The SC72/BX emulates one or two logical disk drive units per physical disk drive. The Unit Select number for any physical disk drive unit number must be in the range from 0 through 3.

When a physical disk drive has two logical disk drive units mapped onto it, the first logical disk drive unit is mapped onto the first half of the heads or cylinders, and has a Unit Select number that is the same as the Unit Select number of the physical disk drive. The second logical disk drive unit is mapped onto the second half of the heads or cylinders, and has a Unit Select number that is four greater than the Unit Select number of the physical disk drive unit; thus, 0 and 4, 1 and 5, 2 and 6, and 3 and 7 (see Appendix A, Tables A-2 and A-5).

When disk drives of different capacities are used, the mapping varies the cylinders, tracks, and/or sectors, as applicable.

1.4.3 DIAGNOSTICS

The SC72/BX disk controller executes the Emulex diagnostic SXBX0D. This diagnostic runs with RM and RP drive emulations. For details on running SXBX0D, refer to the Disk Maintenance Utility (SXBX0D) User's Guide (P/N PD9950904-00). In addition to SXBX0D, the SC72/BX executes the following standard DEC diagnostic routines:

ZRJA	-	Mechanical and Read/Write Test
ZRJB	-	Formatter
ZRJD	-	Multi-Drive Exerciser
ZRJG	-	Diskless Controller Test - Part 1*
ZRJH	-	Diskless Controller Test - Part 2*
ZRJI	-	Functional Controller Test - Part 1*
ZRJJ	-	Functional Controller Test - Part 2*
ZRMA	-	Formatter
ZRMB	-	Performance Exerciser
ZRMC	-	Functional Controller, Part 1*
ZRMD	-	Functional Controller, Part 2*
ZRME	-	Functional Controller, Part 3*
ZRMF	-	Extended Drive Test
ZRMI	-	Drive Compatibility Test

The diagnostic routine names marked with an asterisk (*) require certain patches to correct coding problems or to bypass unsupported Maintenance mode functions. All diagnostic routines require patches to run with disk drive capacities other than those in standard RM and RP disk drive emulations. Patches that are required to modify the standard DEC diagnostic routines are listed and described in Section 6 of this manual.

1.4.4 OPERATING SYSTEMS

The SC72/BX disk controller is compatible with DEC operating systems without modification when emulating any standard DEC disk drive subsystem. Patches to the operating system are required when operating with disk drives that have nonstandard capacities. These patches numerically redefine the logical disk drive capacity as related to the operating system and usually do not involve modifications to program instructions.

1.5 SPECIFICATIONS

Specifications for the SC72/BX disk controller are listed and described in Table 1-1.

Table 1-1. SC72/BX Disk Controller Specifications

Parameter	Characteristics
FUNCTIONAL Emulation	DEC RM02, RM03, RM05, RM80, RP04, RP05, and RP06
Media Compatibility	DEC RM02, RM03, RM05, and RP06 when using appropriate disk drives
Disk Drive Interface	Storage Module Drive (SMD)
Disk Drive Ports	4 with B-Board P/N SU7210402-xx 8 with B-Board P/N SU7210403-xx
Error Control	32-bit ECC for data and 16-bit CRCC for headers. Correction of single data error burst up to 11 bits long.
Sector Capacity	256 words (512 bytes)
Sectors/Track	Selectable for each disk drive
Tracks/Cylinder	Selectable for each disk drive
Cylinders/Disk Drive	Selectable for each disk drive
Disk Drive Type Code	Selectable for each disk drive
Computer Interfaces	Unibus and Cache Bus
Unibus Address	8 switch-selectable address ranges
Interrupt Vector Address	Switch-selectable from 0 to 774
Priority Level	BR5
Data Buffering	Up to 14 sectors
Data Transfer	32-bit data transfer via Cache Bus
Self-Test	Extensive internal self-test when power is first applied (Power-Up mode)

Table 1-1. SC72/BX Disk Controller Specifications (continued)

Parameter	Characteristics
FUNCTIONAL (cont'd) Indicators	A-Board: SSYN, BBUSY, SACK, and BGIN B-Board: READ, WRITE, FAULT, and DIAG. MODE
DESIGN	High-speed, bipolar microprocessor with AMD 2901 bit-slice components
PHYSICAL	
Packaging	3 DEC hex-sized PCBAs 1 DEC dual-width PCBA
Mounting	Any set of RH70 controller slots in PDP-11/70 CPU
Connectors	One 60-pin A-Cable flat-ribbon cable connector and up to eight 26-pin B-Cable flat-ribbon cable connectors
ELECTRICAL	
Unibus Interface	DEC approved line drivers and receivers
Disk Drive Interfaces	Differential line drivers and receivers. A-Cable cumulative length to 100 feet. B-Cable cumulative length to 50 feet.
Power Required	+5 Volts (V), 11 Amperes (A) maximum -15V, 1A maximum
ENVIRONMENTAL	
Operating Temperature	0° to +55° Celsius (C) - or - +32° to +131° Fahrenheit (F)
Storage Temperature	-10° to +70° C - or - +14° to +158° F
Relative Humidity	10 to 90 percent, noncondensing

BLANK

2.1 CONTROLLER ORGANIZATION

This section is divided into four subsections, as listed in the following table:

Subsection	Title
2.1	Controller Organization
2.2	Physical Description
2.3	Interfaces
2.4	Logical Disk Format

The SC72/BX disk controller is organized around a 16-bit, high-speed, bipolar microprocessor. A simplified block diagram of the functional elements in the SC72/BX disk controller is shown in Figure 2-1. The arithmetic and logic unit (ALU) and register file portion of the microprocessor are implemented with four 2901 bit-slice components. The microinstruction is 48 bits long and the control memory of 4K words is implemented with six 4K x 8-bit PROMs.

2.1.1 RAM BUFFER

The SC72/BX disk controller uses a 4K x 16-bit high-speed random access memory (RAM) buffer to temporarily store the contents of the device registers in the SC72/BX disk controller and to buffer up to 14 sectors of data.

2.1.2 A-CABLE REGISTER

The A-Cable Register (ACR) provides the storage of all signals that are sent to and from the disk drive via the A-Cable. The inputs from the selected disk drive are testable by the microprocessor.

2.1.3 DATA HANDLING

Serial data from the selected disk drive are converted to 16-bit parallel data and transferred to the RAM buffer via the microprocessor. Similarly, the data accessed from the RAM buffer by the microprocessor are serialized and sent to the selected disk

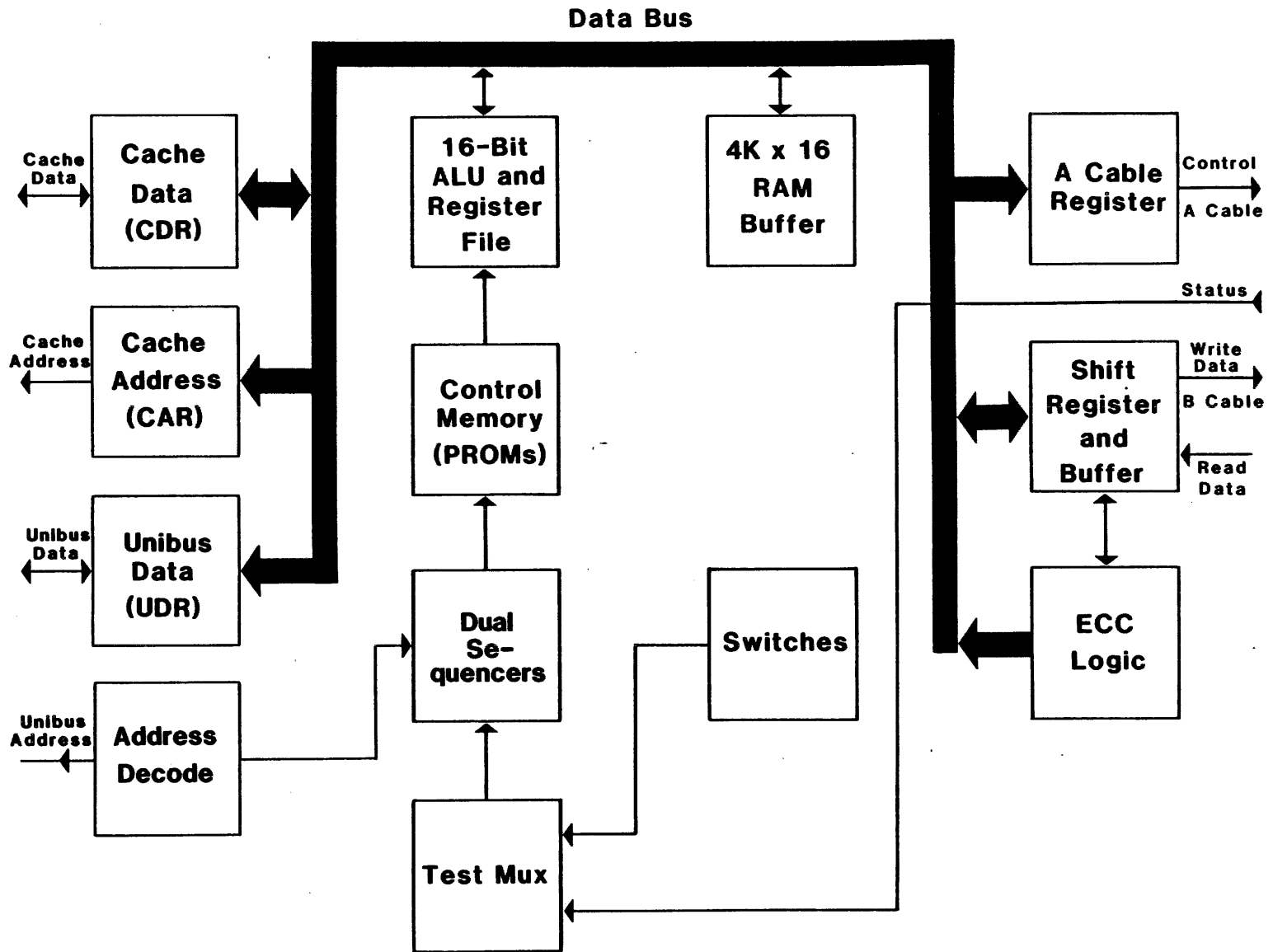


Figure 2-1. SC72/BX Disk Controller, Simplified Block Diagram

drive. The data rate is controlled by the Servo Clock pulse received from the disk drive. A 32-bit ECC Shift Register is used to generate and check the ECC logic for the data field. This same 32-bit ECC Shift Register is also used to generate the 16-bit CRCC character for the sector headers. The actual ECC polynomial operation is done independently of the microprocessor, but the error position and error pattern is determined under control of the microprocessor. Maximum serial data rate is 16 megahertz (MHz).

2.1.4 CONFIGURATION PROM

A configuration PROM is a source to the data bus. This PROM configures the maximum cylinder address, maximum track address, maximum sector address, and disk drive type code for each of the logical disk drives.

2.1.5 BUSES

The Unibus interface consists of a 16-bit bidirectional set of data lines and an 18-bit set of address lines. The Unibus interface is used for programmed input/output (I/O) and for CPU interrupts. The microprocessor responds to all programmed I/O and performs the I/O functions required for the addressed device register in the SC72/B disk controller. The microprocessor also controls all Data Transfer operations between the RAM buffer and the PDP-11/70 CPU memory via the 32-bit Cache Bus. The Cache bus address and control signal lines are on the B-Board and the data interface lines are on the C-Board (see subsections 2.2.3 and 2.3.3, and Table 2-3).

2.2 PHYSICAL DESCRIPTION

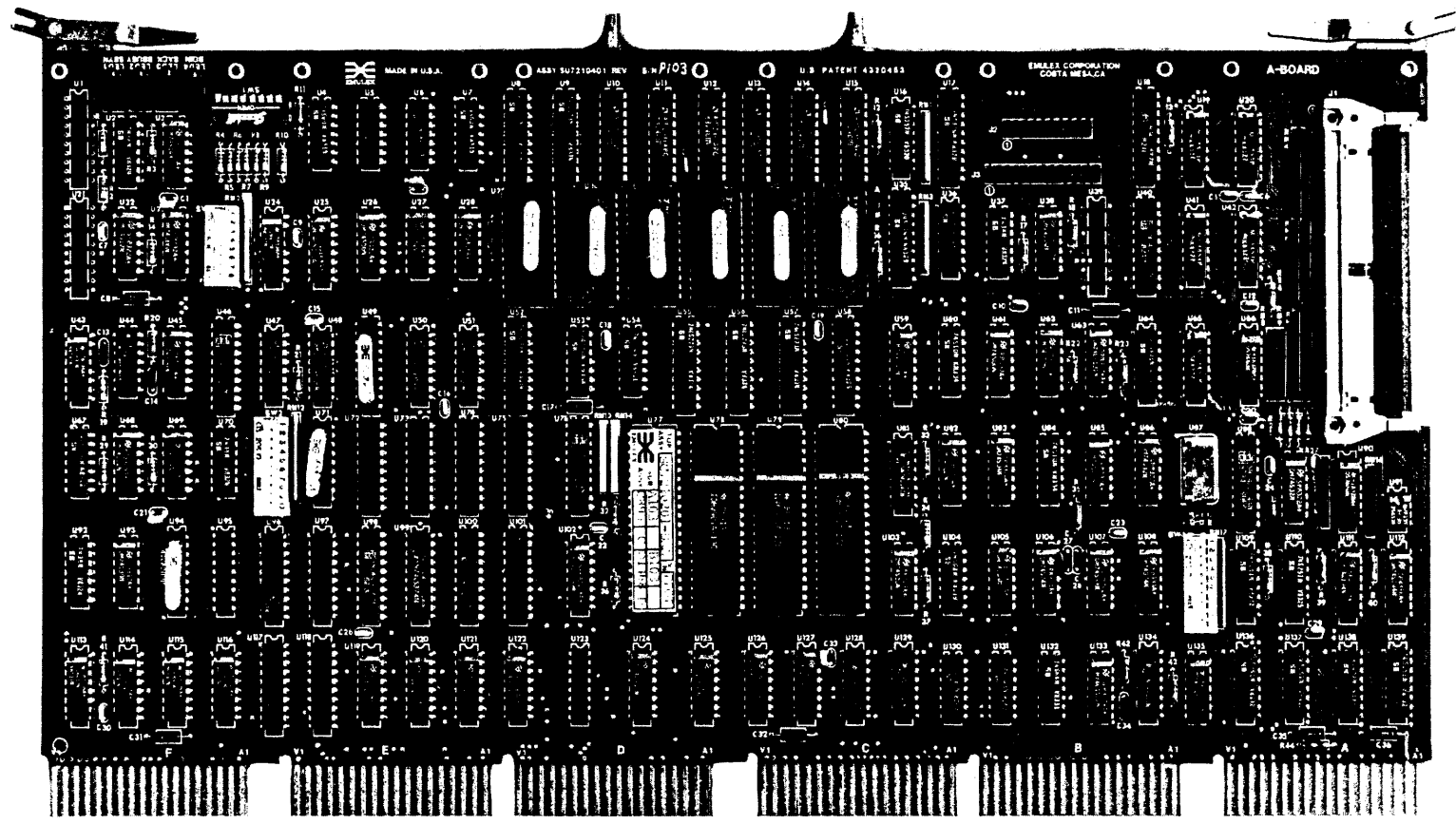
The SC72/BX disk controller consists of three hex-size PCBAs and a small interconnect PCBA; all of which plug directly into the slots in the PDP-11/70 CPU backplane that are normally allocated for a DEC RH70 disk controller, which the SC72/BX disk controller emulates.

The three hex-size PCBAs are the A-Board, the B-Board, and the C-Board; each is separately described in this subsection.

2.2.1 A-BOARD

The A-Board of the SC72/BX disk controller is Emulex Part Number (P/N) SU7210401-xx. This PCBA contains the high-speed bipolar microprocessor, the A-Cable interface and the Unibus interface, test connectors, four dual in-line package (DIP) switch packs, four LED indicators, and 10 PROMs. The A-Board is shown in Figure 2-2. It is the rear PCBA of the four-PCBA disk controller set and fits in chassis backplane slot 27, 31, 35, or 39 of the PDP-11/70 CPU. These slots are used by the BCT PCBA of the DEC RH70 controller.

The A-Board is a four-layer PCBA with power and ground planes in the inner layers and interconnection on the outer layers. The PCBA



SC7201-0191

Figure 2-2. A-Board Configuration

dimensions are 15.7 inches high by 8.7 inches wide. The 18 pins of each connector row are designated A through V from right to left, except letters G, I, O, and Q are not used. The component side is designated side 1 and the solder side is designated side 2.

2.2.1.1 A-Cable Connector

The A-Board has a 60-pin flat-cable connector that is reference designated J1. This connector is located near the top edge of the PCBA and is for the A-Cable which daisy-chains control and status information to all the disk drives in the system. Pin 1 of connector J1 is located on the edge nearest to the outside edge of the PCBA and is identified by an arrow molded into the connector body.

2.2.1.2 Test Connectors

Connectors J2 and J3 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.1.3 Switches

The four DIP switches are used to select the SC72/BX disk controller options and configuration, Unibus device register starting address and range, and interrupt vector address. These switches are listed and identified in Table 2-1.

Table 2-1. Switch Functions

Switch	PCBA	Function
SW1	A	Controller Reset/Unibus Starting Address
SW2	A	Interrupt Vector Address
SW3	A	Configuration
SW4	A	Options

2.2.1.4 Indicators

Four LED indicators at the top front edge of the PCBA show the state of the BBSY, SACK, SSYN, and BGIN Unibus signals. These same indicators are available on the BCT PCBA of the DEC RH70 controller and show Unibus hang-up problems.

2.2.1.5 Controller Freeze

When DIP switch SW1-1 is placed in the ON (CLOSED) position, the SC72/BX disk controller is "frozen" and cannot be accessed by the PDP-11/70 CPU. For Normal operation, this DIP switch must be placed in the OFF (OPEN) position.

2.2.1.6 PROMs

The A-Board has integrated circuit (IC) sockets for 10 PROMs. Six of these PROMs (U29-U34) are 4K X 8-bit data PROMs. The PROM in U4 is the auto-increment PROM for the buffer addressing scheme. The PROM in U71 is the disk drive configuration PROM. The PROMs in U94 and U95 are Unibus address decode PROMs. DIP switches SW1-4 through SW1-8 are used for address selection; i.e., switch SW1-4 selects the appropriate address decode PROM (U94 = OFF, U95 = ON) and switches SW1-5 through SW1-8 select the output of the PROM selected by switch SW1-4.

2.2.2 B-BOARD

The B-Board of the SC72/BX disk controller is Emulex P/N SU7210402-xx (four ports) or P/N SU7210403-xx (eight ports). It contains all the disk data circuitry, four or eight B-Cable disk drive interfaces, and the Cache Bus address interface. This PCBA also includes a -5 Vdc power supply for the A-Cable and B-Cable line transmitter and line receiver circuits.

The B-Board configurations are shown in Figure 2-3. Each is a two-sided, four-layer, hex-size PCBA with the same dimensions and backplane connector arrangement as used on the A-Board. The B-Board plugs into slot 26, 30, 34, or 38 of the backplane in the PDP-11/70 CPU. It occupies the same backplane that would be used by the AWR PCBA of the DEC RH70 controller.

2.2.2.1 B-Cable Connectors

The four-port version of the B-Board contains four 26-pin flat-cable connectors, reference designated J1, J2, J3, and J4. The eight-port version of the B-Board contains eight 26-pin flat-cable connectors, reference designated J1 through J8. These connectors are for the radial B-Cables to each of the four physical disk drives which may be attached to the SC72/BX disk controller. Pin 1 of these connectors is at the left end of the connector, adjacent to the reference designator, and is identified by an arrow molded into the connector body. All the B-Cable connectors are interchangeable.

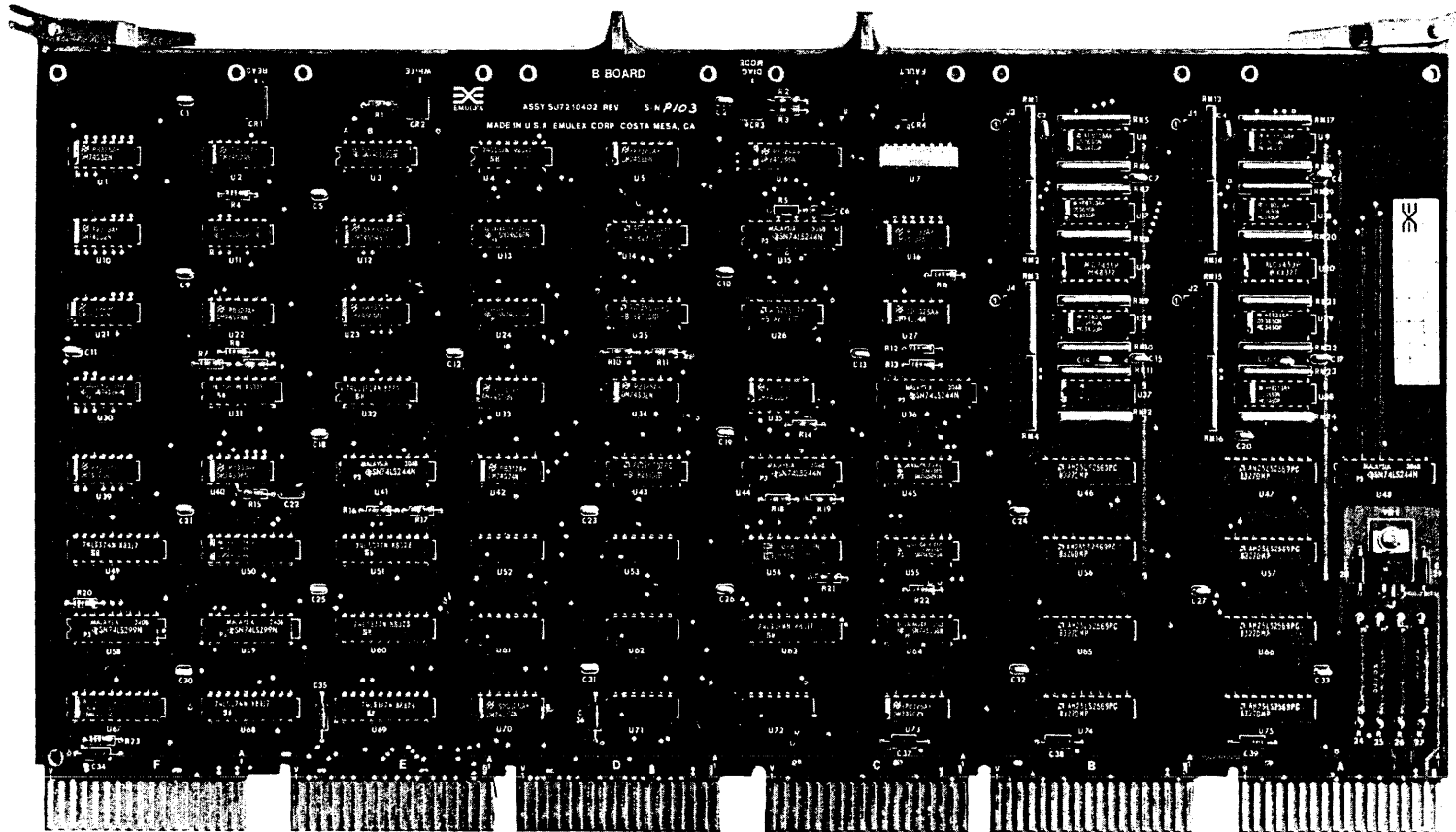


Figure 2-3. B-Board Configuration

2.2.2.2 LED Indicators

The B-Board contains four LED indicators which provide the following information:

- Fault - Indicates disk controller fault or no disk drive connected to SC72/BX disk controller
- Diagnostic Mode - Indicates disk controller in Self-Test mode
- Write - Indicates Write activity is occurring on selected disk
- Read - Indicates Read activity is occurring on selected disk.

2.2.3 C-BOARD

The C-Board of the SC72/BX disk controller is Emulex P/N SU7010406-xx. It contains the Cache Bus data interface which distributes the Cache control and status information. The C-Board is shown in Figure 2-4. The C-Board is a two-sided hex-sized PCBA with dimensions and backplane connector arrangement the same as used on the A-Board. The C-Board plugs into slot 24, 28, 32, or 3 of the backplane or expansion box in the PDP-11/70 CPU. It occupies the same backplane as would be used by the MDP PCBA of the DEC RH7 controller. There are no connectors on this PCBA.

2.2.4 CST BOARD

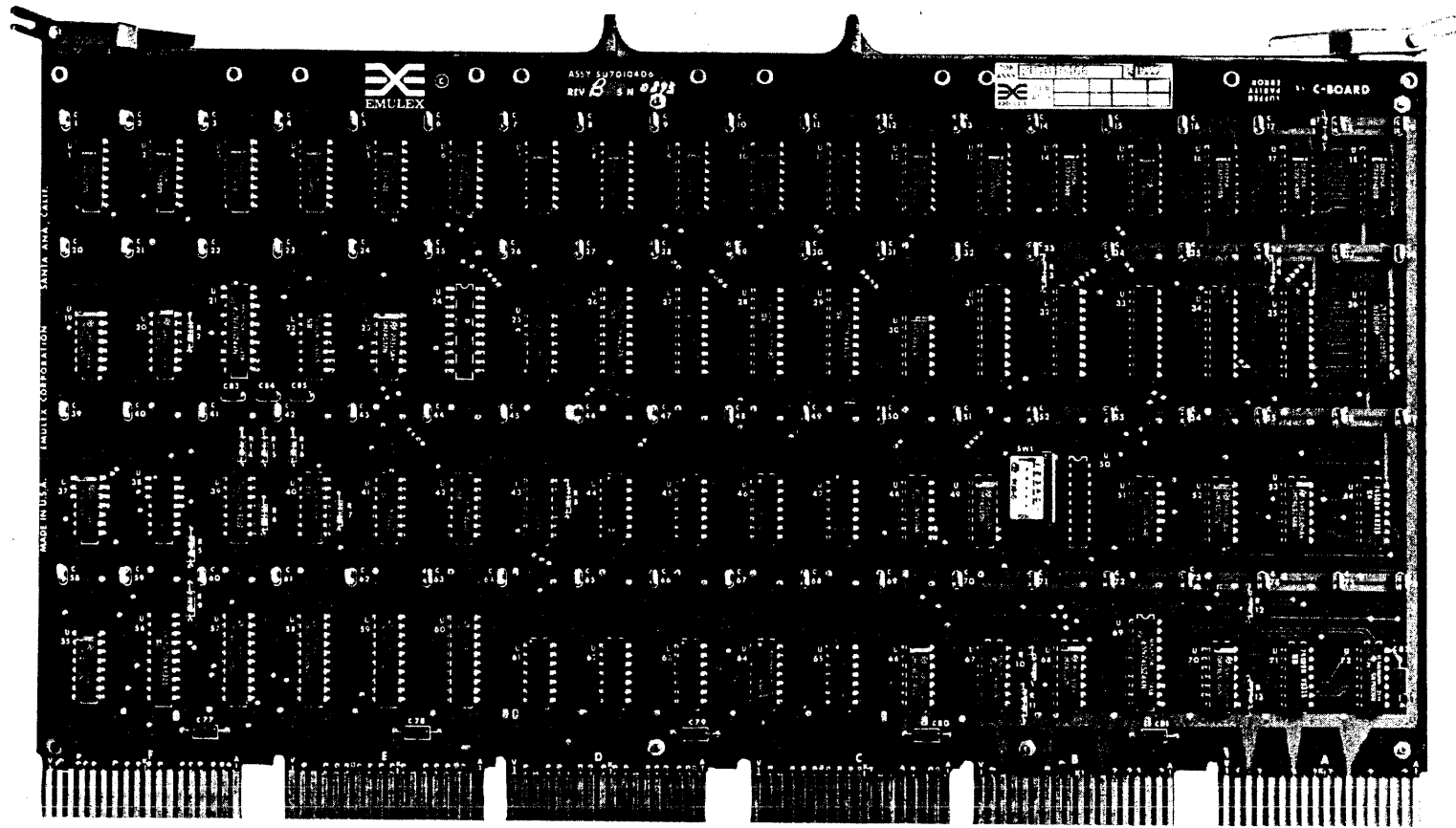
The CST PCBA of the SC72/BX disk controller is Emulex P/N SU7010404-xx. This small interconnect PCBA is used to intercept several DEC RH70 controller signals in an otherwise unused DEC RH7 controller slot and to retransmit them to one of the three Hex-sized PCBAs in the SC72/BX disk controller system. This PCBA is inserted into the D, E, and F connectors of slot 25, 29, 33, or 37 of the backplane or expansion box in the PDP-11/70 CPU. These slot connectors are normally used by the CST PCBA of the DEC RH70 controller. The CST PCBA is shown in Figure 2-5.

2.3 INTERFACES

The SC72/BX disk controller has a disk drive interface, a Unibus interface, and a Cache Bus interface. These interfaces are described in this subsection.

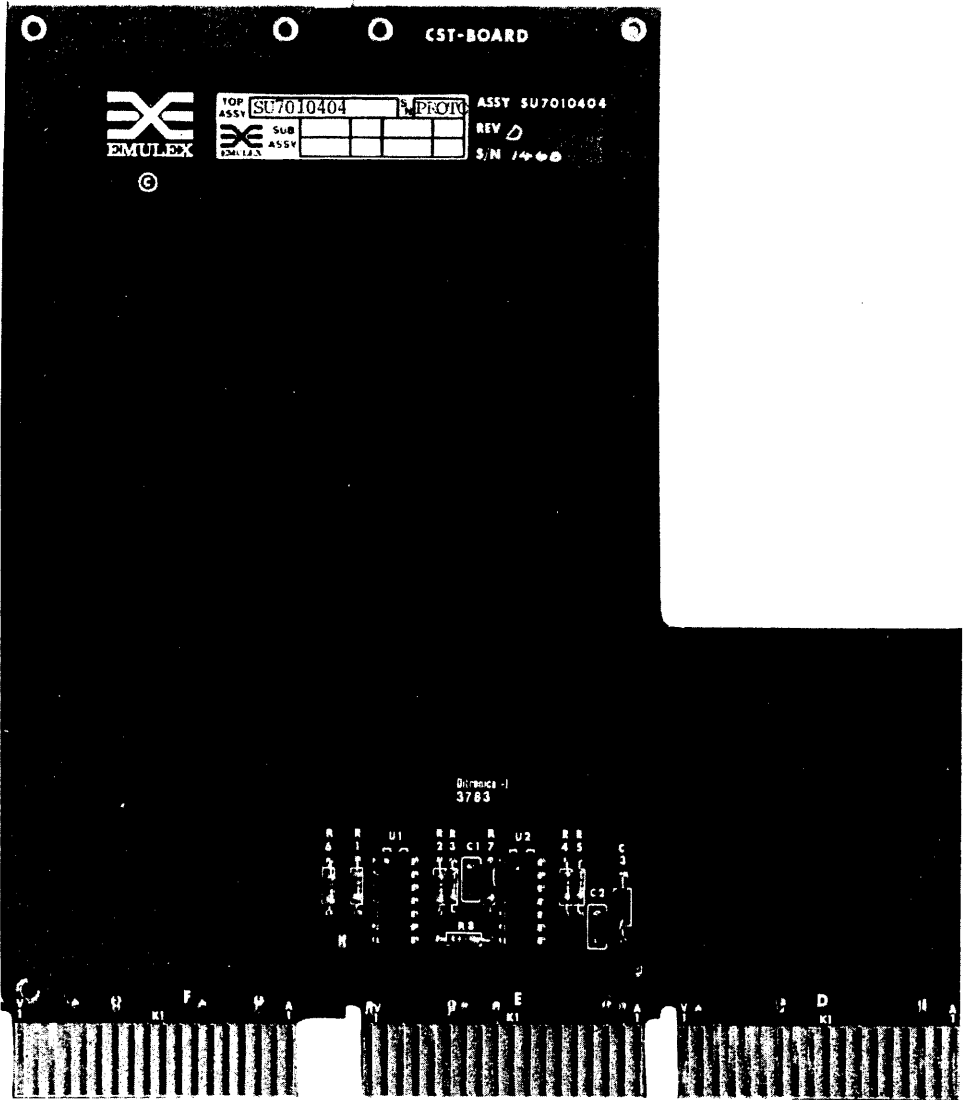
2.3.1 DISK DRIVE INTERFACE

The SC72/BX disk controller-to-disk drive interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD interface requirements (see Control Data Corporation Document No. 64712400). The SC72/BX disk controller has been tested with most disk drives that use the SMD interface and is compatible with the



SC7201-0193

Figure 2-4. C-Board Configuration



SC7201-0194

Figure 2-5. CST PCBA Configuration

electrical and timing characteristics of such disk drives. This interface requires the use of drivers and receivers and the application of A-Cables and B-Cables.

2.3.1.1 Drivers and Receivers

The line drivers for the A-Cable and B-Cables are MC3453, which are equivalent to the 75110A line drivers. The line receivers are MC3450 quad differential receivers, which are equivalent to 75108 line receivers. The lines of the A-Cable are terminated with 82 Ohms to ground and the lines of the B-Cables are terminated with 56 Ohms to ground.

2.3.1.2 A-Cable

The 60-conductor A-Cable is daisy chained to all disk drives in the system and is terminated at the last disk drive in the system. Pin assignments and descriptions of signal functions when the control tag (Tag 3) is asserted are listed in Table 2-2. The A-Cable should be a flat cable with 30 twisted pairs of wires, an impedance of 100 Ohms, and a cumulative length not more than 100 feet.

2.3.1.3 B-Cable

Each 26-conductor B-Cable is radial to all disk drives and contains the data and clock signals. Pin assignments and descriptions of signal functions when the control tag (Tag 3) is asserted are listed in Table 2-2. The B-Cable should be a 26-conductor flat cable with ground plane and drain wire, an impedance of 130 Ohms, and a cumulative length not more than 50 feet.

2.3.2 UNIBUS INTERFACE

The SC72/BX disk controller interfaces with the PDP-11/70 via the slots allocated for the DEC RH70 controller; not via an SPC slot as with a Unibus-type controller. The Unibus consists of 18 address lines and 16 bidirectional data lines, plus control signals for data and interrupt vector address transfer and for becoming bus master for sending interrupt messages. Pin assignments and descriptions of signal functions for the Unibus and Cache Bus interface are listed in Table 2-3.

2.3.2.1 Bus Request (BR) Interrupt Priority Level

The SC72/BX disk controller is hardwired for BR5 priority level. The other three Bus Grant signals are jumpered through.

2.3.2.2 Interrupt Vector Address

DIP switch SW2 sets the Interrupt Vector Address code. Bits <15:09> of the address are assumed to be zeros, so that the Interrupt Vector Address range is from zero to 774. The low-order two bits of the Interrupt Vector Address code are also assumed to be zero, since the Interrupt Vector Address must start on a double-word

Table 2-2. Pin/Signal Assignments, SC72/BX Disk
Controller-to-Disk Drive Interface

A-Cable Pins Low/High	Signal (Tag 3 Function)	From/To
22, 52	Unit Select Tag	To
23, 53	Unit Select bit 0	To
24, 54	Unit Select bit 1	To
26, 56	Unit Select bit 2	To
27, 57	Unit Select bit 3	To
1, 31	Tag 1	To
2, 32	Tag 2	To
3, 33	Tag 3	To
4, 34	Bit 0 (Write Gate)	To
5, 35	Bit 1 (Read Gate)	To
6, 36	Bit 2 (Servo Offset Plus)	To
7, 37	Bit 3 (Servo Offset Minus)	To
8, 38	Bit 4 (Fault Clear)	To
9, 39	Bit 5 (Address Mark Enable)	To
10, 40	Bit 6 (Return to Zero)	To
11, 41	Bit 7 (Data Strobe Early)	To
12, 42	Bit 8 (Data Strobe Late)	To
13, 43	Bit 9 (Release)	To
30, 60	Bit 10	To
14, 44	Open Cable Detect	To
15, 45	Fault	From
16, 46	Seek Error	From
17, 47	On Cylinder	From
18, 48	Index	From
19, 49	Unit Ready	From
20, 50	Address Mark Found	From
21, 51	Busy (Dual-Port only)	From
25, 55	Sector	From
28, 58	Write Protected	From
29	Power Sequence Hold	To
59	Power Sequence Pick	To
B-Cable Pins Low/High	Signal (Tag 3 Function)	From/To
8, 20	Write Data	To
6, 19	Write Clock	To
2, 14	Servo Clock	From
3, 16	Read Data	From
5, 17	Read Clock	From
10, 23	Seek End	From
22, 9	Unit Selected	From
12, 24	Index	From
13, 26	Sector	From

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface

A-Board Connector A				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
BS0	L	A		+5V
-5V		B		0V
BS2	L	C		—
BS7	L	D		—
BD4	L	E		—
UPROC1	L	F		—
BD2	L	H		—
BD7	L	J		—
UPROC1	H	K		—
0V		L		—
CLKU1	L	M		0V
0V		N		—
0V		P		—
0V		R		—
0V		S	H	—
0V		T	H	SECTOR
+5V		U		CERR
		V		—

A-Board Connector B				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
0V		A		+5V
0V		B		0V
0V		C		CLKD1
CKDC	L	D	L	—
0V		E		—
0V		F		—
0V		H		—
0V		J		0V
0V		K		—
0V		L		CKUC
0V		M	L	0V
0V		N		0V
0V		P		—
0V		R		—
0V		S		—
0V		T		—
0V		U		0V
0V		V	L	BUS ACL0

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

A-Board Connector C				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
CREQ	L	A		+5V
0V		B		0V
BS3	L	C		0V
0V		D		0V
0V		E		0V
0V		F		0V
BS4	L	H		—
BS6	L	J		0V
BD3	L	K		0V
0V		L	H	ZECC
0V		M	L	CLKU
BD6	L	N	H	DPF
0V		P	H	DIAGM
CLKD	L	R	H	INDEX
0V		S	H	DTICK
0V		T	H	SKEND
0V		U	H	WMODE
+5V		V	L	CLR

A-Board Connector D				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
—		A		+5V
—		B	H	TCX
DSIG	H	C		0V
CBSY	H	D	H	P23
0V		E	H	P22
0V		F	H	D21
—		H	H	CEN
—		J	H	P20
BUS BR4	L	K	H	BG7 IN
BUS BR5	L	L	H	BG7 OUT
BUS BR6	L	M	H	BG6 IN
0V		N	H	BG6 OUT
DB10	L	P	H	BG5 IN
BUS D03	L	R	H	BG5 OUT
BUS D05	L	S	H	BG4 IN
0V		T	H	BG4 OUT
BUS INTR	L	U	L	BUS BR7
+5V		V	L	BUS D07

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

A-Board Connector E				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
—		A		+5V
—		B		—
BUS D02	L	C		0V
BUS D04	L	D	L	BUS D06
BUS D08	L	E	L	BUS D10
DB 12	H	F	L	BUS D09
BUS D13	L	H	H	DB11
BUS D14	L	J	L	BUS D11
BUS D15	L	K	H	DB01
BUS D00	L	L	L	BUS D01
DB02	H	M	H	DB03
DB04	H	N	H	DB05
DB06	H	P	H	DB07
BUS DCLO	L	R	H	DB09
DB08	H	S	H	DB00
0V		T	H	DB14
BUS D12	L	U	H	DB15
+5V		V		—
A-Board Connector F				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
BUS SACK	L	A		+5V
BUS NPR	L	B		—
BUS BBSY	L	C		0V
—		D		0V
DB13	H	E	L	BUS A00
BUS A02	L	F	L	BUS A01
—		H	L	BUS A03
BUS A05	L	J	L	BUS A04
BUS A06	L	K	L	BUS A07
BUS A09	L	L	L	BUS INIT
BUS A10	L	M	L	BUS A08
BUS A12	L	N	L	BUS A11
BUS A14	L	P	L	BUS A13
BUS A16	L	R	L	BUS A15
BUS MSYN	L	S	L	BUS A17
0V		T	L	BUS C1
BUS SSYN	L	U	L	BUS C0
+5V		V		0V
—				

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

B-Board Connector A				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
—		A		+5V
-5V		B		-15V
WMODE	H	C		0V
0V		D		—
CRST	L	E		—
0V		F		—
CREQ	L	H		—
0V		J		—
0V		K		—
0V		L	L	BD3
CLR	L	M		0V
0V		N		0V
—		P		—
0V		R		—
0V		S		—
0V		T	H	SECTOR
—		U		—
+5V		V		—
B-Board Connector B				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
0V		A		+5V
0V		B		—
0V		C		0V
—		D		—
—		E		—
0V		F		—
0V		H		—
—		J		—
0V		K		0V
0V		L		—
BD3	L	M	L	CKUC
0V		N		0V
BS4	L	P		0V
0V		R		—
—		S		—
0V		T		—
0V		U	L	BS6
—		V		—

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

B-Board Connector C				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
0V		A		+5V
0V		B		0V
0V		C		0V
0V		D		0V
0V		E		0V
0V		F		0V
0V		H		0V
0V		J		0V
0V		K		0V
0V		L		0V
0V		M		—
0V		N		0V
MBC BUS A15	L	P		—
MBC BUS A13	L	R		—
MBC BUS A12	L	S		0V
0V		T	L	MBC BUS A11
BS3	L	U		0V
+5V		V		0V
B-Board Connector D				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
—		A		+5V
WMODE	H	B		0V
P21	H	C		0V
SKEND	H	D	H	P20
CEN	H	E	H	INDEX
DTICK	H	F	L	MBC BUX A09
0V		H	L	MBC BUS A10
P23	H	J	L	MBC BUS A14
P22	H	K	;	MBC BUS A08
MBC BUS A05	L	L	L	MBC BUS A07
TCK	H	M	L	MBC BUS A06
CLR	L	N		0V
MPC BUS A20	L	P	L	MBC BUS A19
DPF	H	R	H	ZECC
DIAGM	H	S	L	CLKU
0V		T	L	MBC BUS A18
		U	L	MBC BUS A17
+5V		V	L	MBC BUS A21

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

B-Board Connector E				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
BD6	L	A		+5V
DSIG	H	B		0V
MBC BUS A16	L	C		CNTLX REQ
MBC BUS CX	L	D	L	DB05
DB04	H	E	H	DB03
0V		F	L	MBC BUS A04
MBC REQ ACKN	L	H	L	MBC BUS A03
MBC BUS A02	L	J	H	DB00
DB06	H	K	H	DB07
DB01	H	L	H	DB02
DB14	H	M		0V
DB13	H	N		DB15
DB12	H	P	H	DB10
DB11	H	R	H	DB09
0V		S	L	MBC BUS A01
		T	H	DB08
		U	L	CKDC
+5V		V		

B-Board Connector F				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
---		A		+5V
---		B		0V
---		C		---
---		D		---
---		E	L	MBC BUS C1
---		F		---
0V		H		---
---		J		---
CREQ	L	K		---
CEN	H	L		---
---		M		---
CAR01	L	N		0V
---		P	L	CLK D
BD6	L	R		---
SEL ADRS CNTLX	H	S		---
0V		T		---
---		U		---
+5V		V	H	P19

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

C-Board Connector A				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
0V		A		+5V
0V		B		0V
0V		C		0V
0V		D		0V
0V		E		0V
0V		F	L	CREQ
0V		H	L	CLR
0V		J		
BS0	L	K	L	BD2
BD7	L	L		0V
0V		M		
0V		N		0V
0V		P	H	CERR
		R	L	CLKD1
AACK	L	S	L	BS7
0V		T		0V
		U		0V
+5V		V		

C-Board Connector B				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
0V		A		+5V
0V		B		0V
0V		C		0V
0V		D		0V
CRST	L	E	H	WMODE
0V		F		0V
0V		H	L	BD3
0V		J	L	BD4
BS2	L	K	H	UPROC1
0V		L	L	UPROC1
0V		M		0V
0V		N		0V
0V		P		0V
		R		0V
		S		0V
0V		T	L	CLKU1
0V		U		0V
		V		0V

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

C-Board Connector C				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
CAR01	L	A		+5V
		B		0V
CBSY	H	C		0V
CEN	H	D		0V
		E		0V
0V		F	H	MEM BYTE 3 PAR
0V		H	L	MBC BUS D00
MBC BUS D01	L	J	L	MBC BUS D02
MBC BUS D03	L	K	L	MBC BUS D04
MBC BUS D05	L	L	L	MBC BUS D06
MBC BUS D07	L	M	L	MBC BUS D08
MBC BUS D09	L	N		0V
MBC BUS D10	L	P	L	MBC BUS D11
MBC BUS D12	L	R	L	MBC BUS D13
MBC BUS D14	L	S	L	MBC BUS D15
0V		T		
MBCT0	H	U	L	MBC BUS D16
+5V		V	L	MBC BUS D17
C-Board Connector D				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
MBC BUS D18	L	A		+5V
MBC BUS D19	L	B	L	MBC BUS D20
MBC BUS D21	L	C		0V
MBC BUS D22	L	D	L	MBC BUS D23
MBC BUS D24	L	E	L	MBC BUS D25
MBC BUS D26	L	F	L	MBC BUS D27
0V		H	L	MBC BUS D28
MBC BUS D29	L	J	L	MBC BUS D30
MBC BUS D31	L	K	L	MBC BUS B1PA
MBC BUS B0PA	L	L	L	MBC BUS B2PA
MBC BUS B3PA	L	M		0V
0V		N		0V
ADRS PE	H	P		0V
MEM D00	H	R	H	MEM D01
MEM D02	H	S	H	MEM D03
0V		T	H	MEM D04
MEM D05	H	U	H	MEM D06
+5V		V	H	MEM D07

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

C-Board Connector E				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
—		A		+5V
—		B	H	MEM D08
MEM D09	H	C		0V
MEM D10	H	D	H	MEM D11
MEM D14	H	E	H	MEM D13
MEM D12	H	F	H	MEM D15
0V		H	H	MEM D19
MEM D17	H	J	H	MEM D18
MEM D16	H	K	H	MEM D20
MEM D21	H	L	H	MEM D22
MEM D23	H	M	H	MEM D24
MEM D28	H	N		0V
MEM D25	H	P	H	MEM D27
MEM D26	H	R	H	MEM D29
MEM D30	H	S	H	MEM D31
0V		T	H	MEM BYTE 1 PAR
DATA RDY CNTLX	H	U	H	SEL DATA CNTY
+5V		V	H	MEM BYTE 0 PAR
C-Board Connector F				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
DB13	H	A		+5V
DB12	H	B	H	DB05
DB10	H	C		0V
DB09	H	D	H	DB04
DB08	H	E	H	DB02
DB11	H	F	H	DB15
0V		H	H	DB01
DB14	H	J	H	DB00
BD6	L	K	H	DB03
DB07	H	L		—
DB06	H	M		—
—		N		0V
CKC	L	P		—
0V		R		—
MEM BYTE2 PAR	H	S		—
0V		T		0V
0V		U		0V
+5V		V		0V

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

CST PCBA Connector D				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
---		A		---
---		B		0V
---		C		---
---		D		---
---		E		---
---		F		---
0V		H		---
0V		J		---
---		K		0V
---		L		---
---		M		0V
---		N		---
0V		P		---
---		R		---
0V		S	L	MBC ADRS ACKN
---		T		0V
---		U		---
---		V		---

CST PCBA Connector E				
Component Side		Pin	Solder Side	
Signal	High/Low		High/Low	Signal
---		A		+5V
MBCT0	H	B		0V
0V		C		0V
---		D		0V
0V		E		---
---		F		---
---		H		---
---		J		---
---		K		0V
SELDATA CNTLX	H	L	L	AACK
---		M	L	ADRS PAR ERR
MBC TIMEOUT	H	N		0V
0V		P		0V
0V		R		---
---		S		---
0V		T		0V
---		U		---
+5V		V		---

Table 2-3. Pin/Signal Assignments, Unibus/Cache Bus Interface (continued)

CST PCBA Connector F				
Signal	Component Side High/Low	Pin	Solder Side High/Low	Signal
0V		A		
0V		B	H	ADRS PE
0V		C		0V
0V		D		
0V		E		0V
0V		F		0V
0V		H		0V
0V		J		
0V		K		0V
0V		L		
---		M		
---		N		0V
---		P		
---		R		
0V		S		0V
0V		T		0V
0V		U		
---		V		0V

address. Switch settings for the Interrupt Vector Address are described in subsection 3.5.2.

2.3.2.3 DCLO and INIT Signals

The DCLO and INIT signals both perform a Controller Clear function. The Self-Test routine is performed only when the DCLO signal has been asserted.

2.3.3 CACHE BUS INTERFACE

The Cache Bus address and control signals are on the B-Board. These signal lines allow for a 22-bit memory address and for control in writing and reading a single or double word to or from memory. The Cache Bus 32-bit data interface lines are on the C-Board.

2.4 LOGICAL DISK FORMAT

The logical disk format involves mapping the system in such a way that the software corresponds with logical disk drive unit addresses on physical disk drives. The number of logical disk drive units per physical disk drive is configured and selected by setting DIP switches (see Tables A-2, A-5, and A-8). The number of cylinders, tracks, and sectors for each disk drive can be configured by the configuration PROM.

2.4.1 SECTOR FORMAT

The media-compatible RM sector format used by the SC72/BX disk controller is shown in Figure 2-6. The RP sector format is similar, except it has two additional words in the header. Each track of 20,160 bytes is divided into the required number of sectors. The four-byte header is preceded by a preamble of 30 bytes which ends in the synchronization (sync) byte and it is followed by a two-byte cyclic redundancy check character (CRCC).

The 256-word data field is preceded by a preamble of 20 bytes which ends in the sync byte followed by four bytes of the error correction code (ECC).

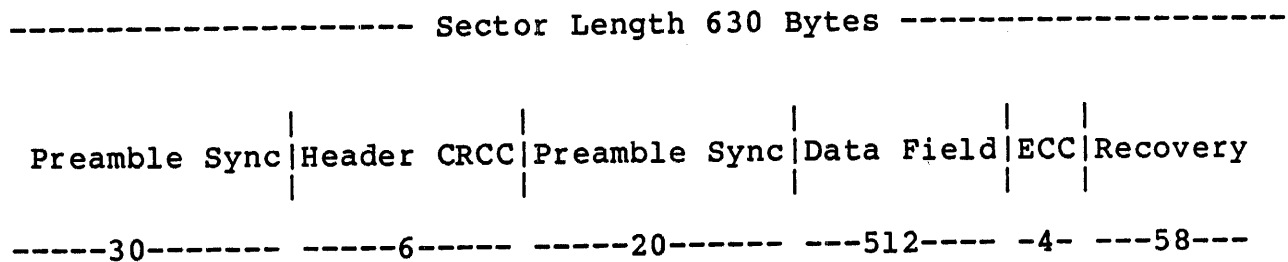


Figure 2-6. Sector Format

2.4.2 RM HEADER FORMAT

The RM header format, shown in Figure 2-7, consists of the following three words:

Word One -

This word contains the cylinder address in bits <10:00>. Bit 12 is set to logic one to identify 16-bit format to the software, and bits 14 and 15 are each set to logic one to identify a good sector. Bit 11 is cleared (reset) to logic zero. For RM80 emulations, bit 13 is the Skip Sector Flag (SSF), but it is cleared (reset) to logic zero for all other emulations.

Word Two -

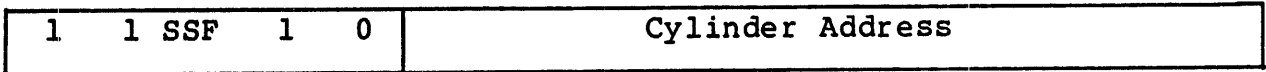
The low byte of this word contains the sector address and the upper byte of this word contains the track address. Each track on the disk drive contains the number of sectors established by the appropriate configuration switches.

Word Three -

This word contains the CRCC which is generated and checked by the logic in the SC72/BX disk controller. This word is not available to the software.

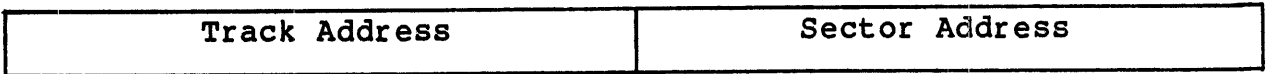
Header Word 1:

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00



Header Word 2:

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00



Header Word 3:

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

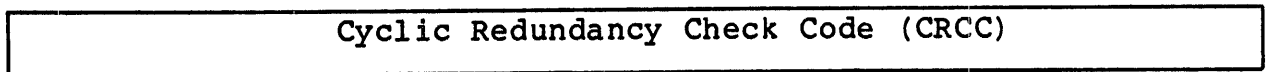


Figure 2-7. RM Header Words Format

2.4.3 RP HEADER FORMAT

The RP header format, shown in Figure 2-8, consists of the following five words:

Word One -

This word contains the cylinder address in bits <10:00>. Bit 12 is set to logic one to identify 16-bit format to the software, and the remaining bits are cleared to logic zero.

Word Two -

The low byte of this word contains the sector address and the upper byte of this word contains the track address. Each track on the disk drive contains the number of sectors established by the appropriate configuration switches.

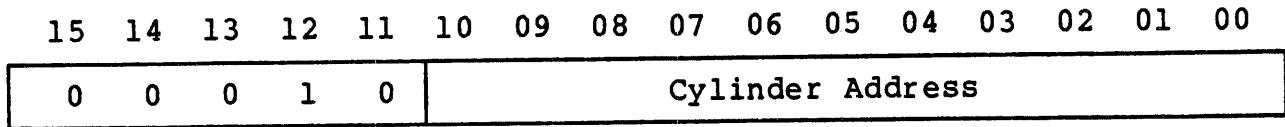
Words Three and Four -

These are user words that are not checked by the firmware unless the Replacement Track mode is enabled.

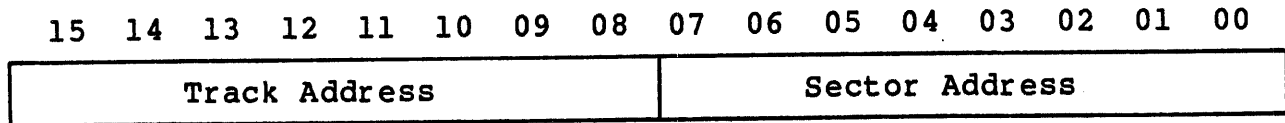
Word Five -

This word contains the CRCC which is generated and checked by the logic in the SC72/BX disk controller. This word is not available to the software.

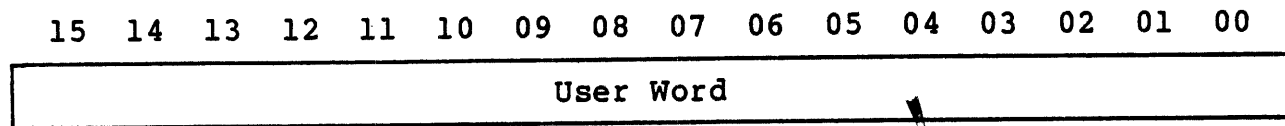
Header Word 1:



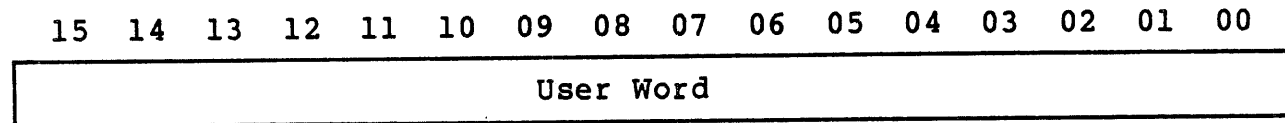
Header Word 2:



Header Word 3:



Header Word 4:



Header Word 5:

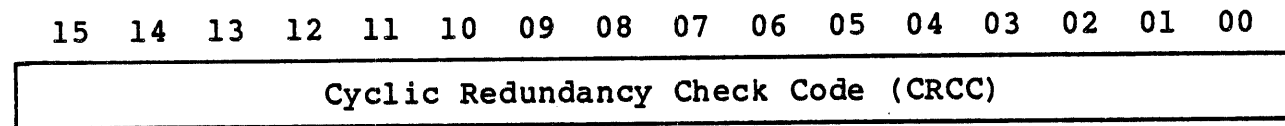


Figure 2-8. RP Header Words Format

2.4.4 HEADER FIELD HANDLING

After the disk drive reports it is on cylinder, the SC72/BX disk controller locates the desired sector by means of the sector counters. A sector counter for each disk drive is maintained in the SC72/BX disk controller circuitry. The SC72/BX disk controller compares the header with the desired track, sector, and cylinder and then checks the CRC word for errors. An error in the header field is indicated by setting the appropriate error bit in the error register (Format Error, Header Compare Error, Bad Sector Error, Skip Sector Error, or CRC Error). A header error is valid only when the sector count field of the RMLA/RPLA register and the sector field of the RMDA/RPDA register have already matched. The place where the CRC Error occurs in the header field is immaterial because the SC72/BX disk controller cannot determine its location

in the header field. Software, however, can be used to read the header and place it in the memory by issuing the Read Header and Data command. The Header Compare operation may be inhibited by setting the HCI bit in the RMOF/RPOF register to logic one.

If the actual size of the useful data information is less than 256 words (512 bytes), the remainder of the data field is filled with zeros until 256 words have been written. During disk formatting procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual sectors, or groups of sectors should not be reformatted unless absolutely necessary.

BLANK

3.1 INTRODUCTION

This section describes the step-by-step procedure for installing the SC72/BX disk controller in a PDP-11/70 CPU system. This section is divided into eight subsections, as listed in the following table:

Subsection	Title
3.1	Introduction
3.2	Inspection
3.3	Disk Drive Preparation
3.4	System Preparation
3.5	SC72/BX Disk Controller Configuration
3.6	Physical Installation
3.7	Cable Routing and RFI Suppression
3.8	Testing

3.1.1 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the SC72/BX disk controller PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI).

Each SC72/BX disk controller PCBA is a standalone unit that complies with FCC regulations and is designed to be embedded in a PDP-11/70 CPU cabinet. When properly installed, the SC72/BX disk controller system does not cause compliant computers to exceed RFI limits for Class A equipment.

There are two possible configurations in which the disk drives to be interfaced with the SC72/BX disk controller system can be installed:

- a. In the same cabinet as the DEC CPU and the SC72/BX disk controller.
- b. In an expansion cabinet that is separate from the cabinet in which the CPU and SC72/BX disk controller are installed.

To limit radiated RFI, DEC completely encloses the computer system components, that could radiate RFI, with a grounded metal shield. When installing system components, do nothing that could reduce the effectiveness of the shield. That is, when installation of the SC72/BX disk controller system [SC72/BX disk controller PCBA,

Personality Panels, Blank Panels (if any), Bulkhead Distribution Panels (if any), disk drives, and shielded cables] is complete, no gap in the shielding that would allow RFI radiation can be allowed.

Conducted RFI is generally prevented by installing a filter in the ac line between the computer system and the ac source. Most power distribution panels of current manufacture contain suitable filters.

The procedures required to maintain shield integrity and to limit radiated and conducted RFI are explained fully in subsection 3.7.

3.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

After unpacking the SC72/BX disk controller, visually inspect the entire assembly for bent or broken connector pins, damaged components, or other visual evidence of physical damage. The PROMs should be carefully examined to ensure each is firmly and completely seated in its socket. Verify that controller model or part number designation, revision level, and serial number agree with those on shipping invoice. This verification is important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

3.3 DISK DRIVE PREPARATION

Disk drive preparation involves placement, local or remote power-up control selection, sectoring, disk drive numbering, and Sector and Index signal modification.

3.3.1 PLACEMENT

Uncrate and install the disk drives as instructed in the manufacturer's technical manual. Position and level the disk drives in their final places before beginning the installation of the SC72/BX disk controller. This positioning allows the I/O cable routing and length of cables to be accurately determined. Place the disk drives side-by-side or above and below each other to simplify installation of the A-Cable daisy chain.

3.3.2 LOCAL/REMOTE

The setting of the LOCAL/REMOTE switch on the disk drive determines whether the disk drive can be powered up from the disk drive (local) or from the SC72/BX disk controller (remote). Place the

switch in the REMOTE position. With the PDP-11/70 CPU powered down, press the START switch on the front panel of each disk drive (the LED in the START switch/indicator should illuminate, but the disk drive should not spin up and become ready). When the PDP-11/70 CPU is powered up, the disk drives should spin up sequentially. This sequential spin-up prevents heavy current draw that would otherwise occur if all the disk drives were powered up at the same time. When the disk drives are in the Remote mode, they are powered down when the PDP-11/70 CPU is powered down. While the PDP-11/70 CPU is powered on, the disk drives may be powered up or down individually (to change disk media , for example) by using the START switch on the front panel of the disk drive.

3.3.3 SECTORING

The disk drives must be configured for the number of sectors per track required for the selected disk drive configuration. The procedure for entering the sector numbers differs from one manufacturer's disk drive model to the disk drive model of another manufacturer; therefore, the technical manual of the disk drive manufacturer must be referred to for instructions about how to establish proper sectoring of the disk drives.

3.3.4 DISK DRIVE NUMBERING

An address from zero to three (zero to seven for eight-port models) must be selected for each disk drive. No two disk drives in the system should be assigned the same number. To determine the number that each disk drive should be assigned, decide what particular configuration is to be used, then assign the disk drive numbers according to that configuration in Table A-2, A-5, or A-8 of Appendix A.

CDC disk drive addresses are selected by using an ID plug. Disk drives from other manufacturer's have their addresses selected by switches on one of the logic PCBAs in the disk drive. For exact procedure of disk drive numbering, refer to the manufacturer's technical manual for the disk drive.

3.3.5 SECTOR AND INDEX MODIFICATIONS

Sector and Index signals on the A-Cable may have to be moved to the B-Cable, for some installations (see subsection 3.5.3). Instructions for making such changes on commonly used disk drives are included in Appendix B.

NOTE

To prevent significant performance degradation, Emulex strongly recommends modifying the disk drive to place the Sector and Index signals on the B-Cable if the disk drive has not been delivered in that configuration.

3.4 SYSTEM PREPARATION

Power down the system and place the main AC circuit breaker at the rear of the PDP-11/70 CPU cabinet in the OFF position (the AC power indicator should remain lit). Slide the CPU card rack out of the cabinet and remove the card-rack cover.

3.5 SC72/BX DISK CONTROLLER CONFIGURATION

The SC72/BX disk controller must be configured to operate with the disk drives in the system before it is installed in the backplane or expansion box of the PDP-11/70 CPU. Components that are used in configuring and interfacing the SC72/BX disk controller are switches, PROMs and connectors located on the A-Board, and B-Board. Location of components on the A-Board, B-Board, and C-Board are shown in Figures 3-1, 3-2 and 3-3, respectively.

For functions that are assigned to the configuration switches not explained in this subsection, refer to the Appendices at the end of this manual.

3.5.1 SC72/BX DISK CONTROLLER ADDRESS SELECTION

All controllers that interface with the DEC Unibus have a block of several command and status registers through which the system can command and monitor the controller. The registers are addressed sequentially from a starting address that is assigned to that particular device type; in this system application, the device type in which the starting address is placed is the Emulex SC72/BX disk controller.

The starting address for the device registers in the SC72/BX disk controller is selected by DIP switches SW1-4 through SW1-8. The starting address range is fixed from base + 00₈ to base + 52₈. A normal starting address of 776700 is obtained by placing switch SW1-8 in the ON position. The normal starting address is the base address; all addresses are in octal. See Appendix A, subsection A.3 for a complete list of all selectable starting addresses.

3.5.2 INTERRUPT VECTOR ADDRESS

The interrupt vector address is programmed by using DIP switch pack SW2 on the A-Board. The normal interrupt vector address for the SC72/BX disk controller is 254, and this interrupt vector address is set by placing switches SW2-2, -3, -5, and -7 in the ON position, and leaving switches SW2-1, -4, -6, and -8 in the OFF position. The alternate interrupt vector address of 150 is set by placing switches SW2-3, -5, and -6 in the ON position and leaving switches SW2-1, -2, -4, -7, and -8 in the OFF position. Switches SW2-8 through SW2-1 represent Interrupt Vector Address bits 8 through 1, respectively.

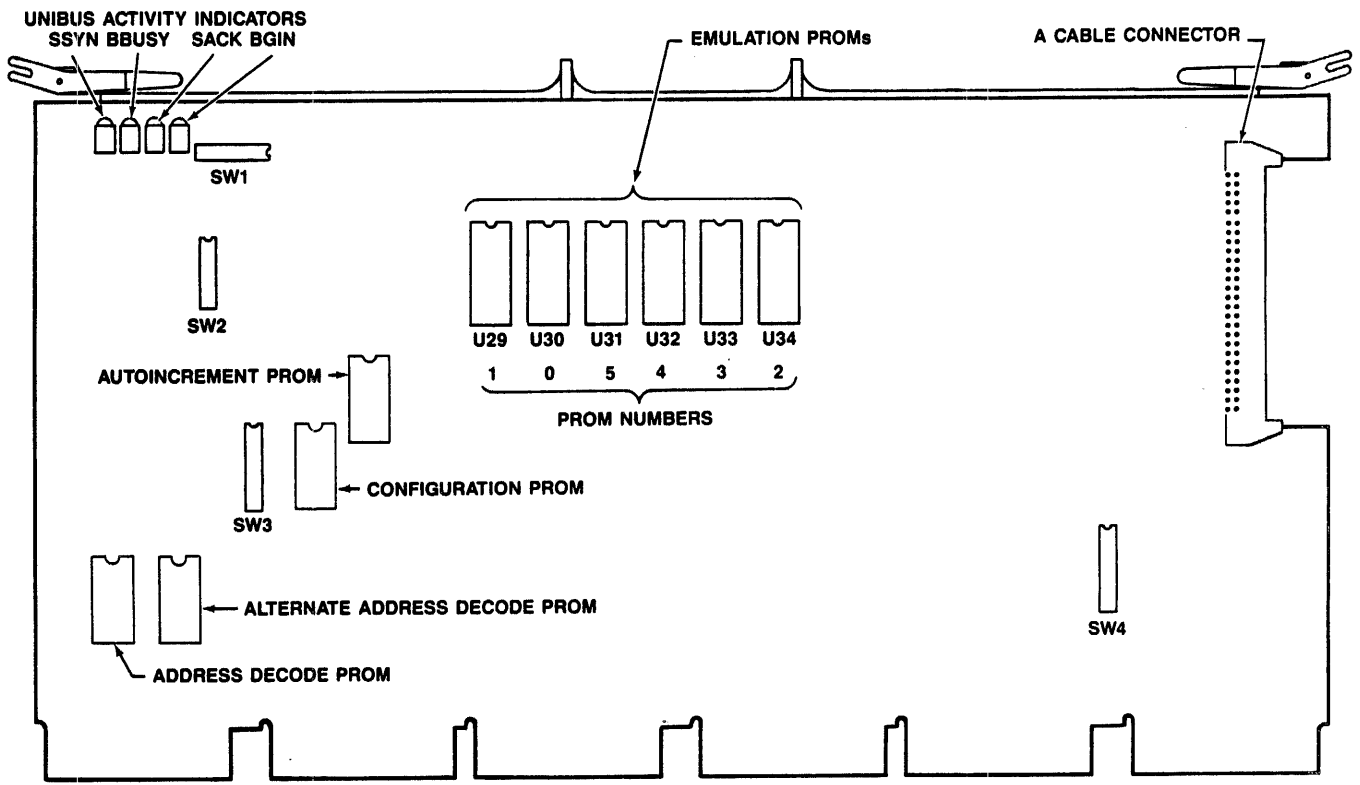


Figure 3-1. Component Locations, A-Board

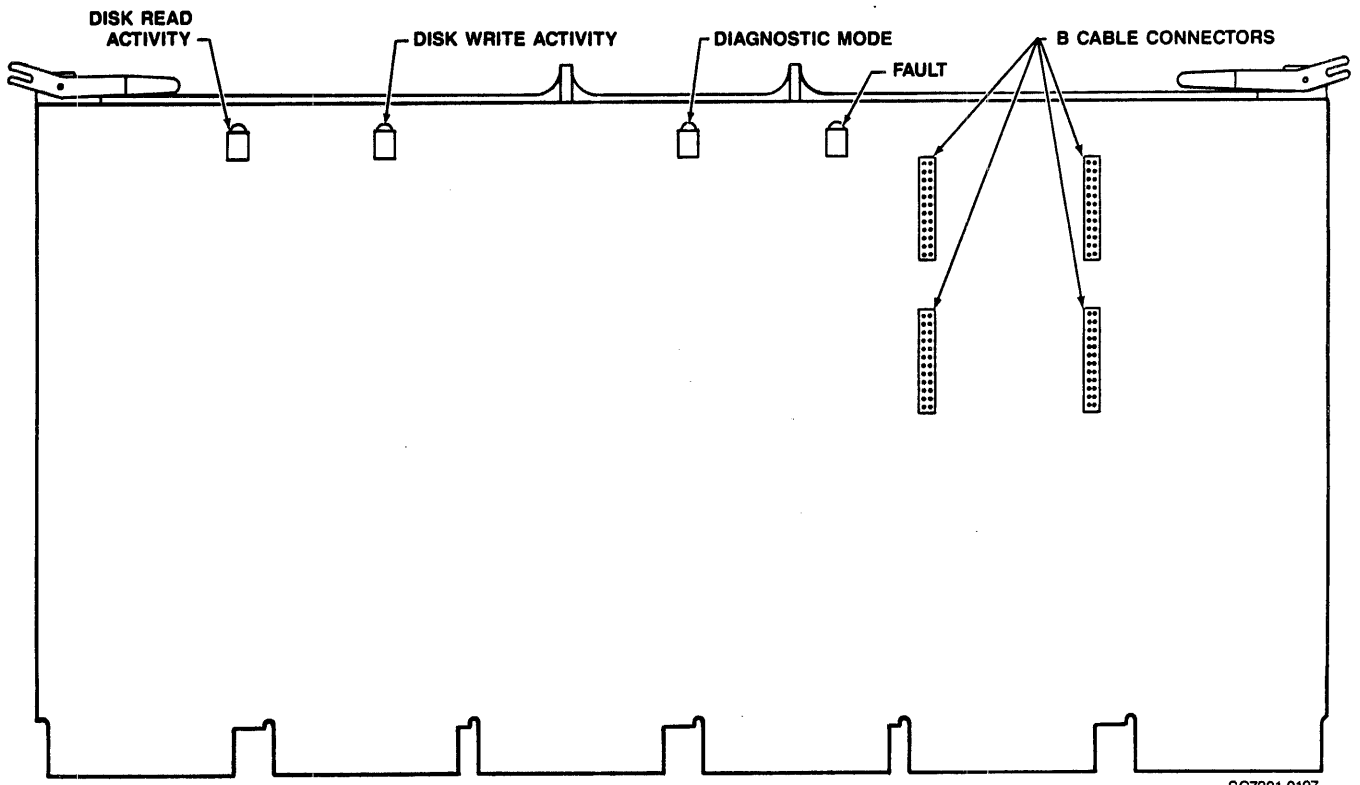
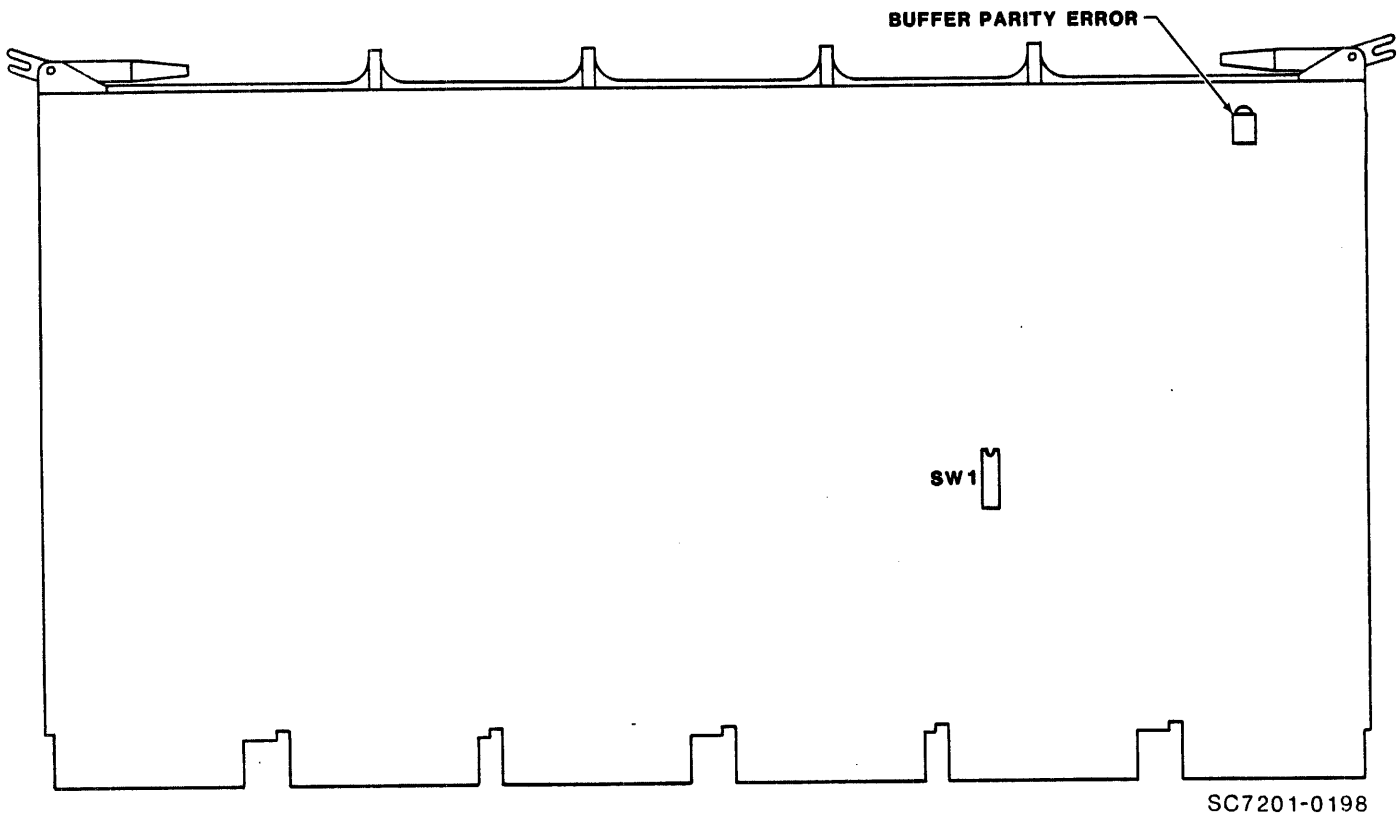


Figure 3-2. Component Locations, 4-port B-Board



SC7201-0198

Figure 3-3. Component Locations, C-Board

3.5.3 INDEX AND SECTOR PULSE SELECTION

The SC72/BX disk controller is designed to have the Index and Sector signals on the B-Cable from each physical disk drive. The signals are necessary for proper operation of the sector counters that are associated with each disk drive. RM/RP emulations require an updated sector counter which can be read by the PDP-11/70 CPU. Failure to have a valid sector count may cause incorrect operation of the rotational position-sensing software.

Depending on the disk drive manufacturer and model, the Index and Sector pulse signals may be carried on the A-Cable instead of the B-Cable. For example, standard CDC disk drives provide the Index and Sector signals on the A-Cable; however, they may be moved to the B-Cable by minor rewiring of the disk drive backplane, or this configuration may be ordered from the factory. The procedure for making this modification to several of the more commonly used disk drives is described in Appendix B. If the procedure for the disk drive in question is not covered in that appendix, it is usually described in the technical manual provided by the manufacturer of the disk drive.

Emulex disk controllers can be reconfigured to receive the signals on the A-Cable by placing switch SW4-8 in the ON (CLOSED) position. To make the most efficient use of the SC72/BX disk controller, the

disk drive must be configured to carry the Index and Sector signals on the B-Cable (see Appendix B).

3.5.4 DISK DRIVE CONFIGURATION SELECTION

The phrase "disk drive configuration selection" describes the process that is used to configure the SC72/BX disk controller to emulate a particular type of disk drive. That is, a particular set of physical disk drives are available for the system, and the configuration selection arrangements on the SC72/BX disk controller merely inform the rest of the circuitry in that disk controller what types of disk drives are to be used. Switches SW3-1 through SW3-6 on the A-Board are used to select the disk drive configuration. For ease of maintaining this manual, the table of configuration switch settings for disk drive emulation is contained in Appendix A.

3.5.5 OPTION SWITCHES

The user can select a number of options by using DIP switches on the A-Board.

3.5.5.1 Controller Reset Option

DIP switch SW1-1 allows selection of Normal operation (OFF) or Reset operation (ON) which initializes and "freezes" the SC72/BX disk controller so that it cannot respond to the CPU.

3.5.5.2 CPU Stall Option

DIP switch SW1-3 allows selection of the CPU Stall circuit for Normal operation (OFF) or for disabling the CPU Stall circuit (ON). That is, when switch SW1-3 is ON, it disables the circuit that normally activates a CPU Stall (via a Unibus NPR request) whenever a programmed I/O cycle occurs during a Cache Bus DMA cycle. Thus, it prevents a CPU status loop from excessively stalling the DMA cycle. The circuit needs to be disabled only for special circumstances that usually involve non-DEC hardware that could become confused.

3.5.5.3 Eight Port/Disk Drive Select Options

DIP switch SW3-7 allows selection of circuitry for support of four or eight physical disk drives. OFF selects the configuration for four physical disk drives, and ON selects the configuration for eight physical disk drives.

DIP switch SW4-1 allows selection of firmware that is compatible for the four-port version of the B-Board or for the eight-port version of the B-Board. OFF selects the four-port version, and ON selects the eight-port version.

Switch settings must be coordinated with PROM selection, and emulation PROMs on A-Board must be revision D or later. For details, see Appendix A.

These switches, although usually used in tandem, select two totally independent options. All four possible combinations of the two switches are legal and usable.

3.5.5.4 Hardware Sector Interleave Option

DIP switch SW4-3 allows selection of circuitry that is compatible with 2-1 hardware sector interleaving. ON position enables this option and OFF position disables this option.

3.5.5.5 Logical Disk Drive Unit Swap Option

DIP switch SW4-4 in the ON position allows logical disk drive units zero through three to be swapped with logical disk drive units four through seven. The OFF position disables the swap condition.

3.5.5.6 Replacement Track Mode Option

DIP switch SW4-5 is used with RP-only emulations. ON position enables Replacement Track mode and OFF position disables that mode. See Appendix C for details.

3.5.5.7 Dual-Port Mode Option

DIP switch SW4-6 allows selection of Single-Port or Dual-Port mode. ON position enables Dual-Port mode and OFF position enables Single-Port mode. The function of the Dual-Port mode option is described in subsection 4.2.

3.5.5.8 Dual-Access Mode Option

DIP switch SW4-7 allows support of the Dual-Access mode. ON position enables and OFF position disables this mode function. When in the Dual-Access mode, the SC72/BX disk controller sets the DPM and PGM bits in the Drive Status Register to imitate the DEC neutral state. The function of this mode is detailed in subsection 4.2.7.

3.5.5.9 Index/Sector Signals Placement Option

DIP switch SW4-8 allows Index and Sector signals to be placed on the A-Cable or the B-Cable, depending on system configuration. ON position places these signals on the A-Cable and OFF position places them on the B-Cable (see subsections 3.3.5 and 3.5.3).

3.5.5.10 Special RP06 Mapping Option

DIP switch SW4-9 allows support of special mapping when emulating dual RP06 disk drives. ON position enables this option and OFF position disables it.

3.6 PHYSICAL INSTALLATION

Physical installation of the SC72/BX disk controller involves PROM installation, RH70 slot selection and physical mounting.

3.6.1 PROM INSTALLATION/REPLACEMENT

The A-Board provides IC sockets for installation of 10 PROMs. Six of these sockets are near the top center of the A-Board when viewed from the component side and are reference designated U29 through U34. When the PROMs are installed or replaced, the ID numbers (on top of each PROM) are placed in a discontinuous sequence from the reference designators (U numbers) silkscreened on the A-Board next to each respective socket. The A-Board contains four other PROMs in IC sockets U49, U71, U94, and U95. The first address decode PROM is located in IC socket U94. The second address decode PROM (U95) is usually not installed. It is only used when the user needs an address that is not contained in the first address decode PROM. See Appendix A, Subsection A.3 for a complete list of all selectable starting addresses.

3.6.2 RH70 SLOT SELECTION

The PCBAs that comprise the SC72/BX disk controller may be placed into any of the available slot positions for the DEC RH70 controller. There are four prewired RH70 positions in the PDP-11/70 CPU. Slot RH70 A (forward disk controller position) is powered by its own power supply from the PDP-11/70 CPU backplane. Slots RH70 B and C are also powered from the same power supply. The RH70 D slot is powered by the power supply that powers the SPC Unibus slots. Figure 3-4 shows the PDP-11/70 CPU computer chassis with a single SC72/BX disk controller installed in RH70 slots 24, 25, 26, and 27. Cache Bus request priorities between RH70 positions is described on page VI-4-13 of the DEC KB 11 Processor Manual.

3.6.3 MOUNTING

Each SC72/BX disk controller PCBA should be plugged into the PDP-11/70 CPU backplane or expansion box with the component side facing in the same direction as the CPU and other modules.

- - - - -
C A U T I O N
- - - - -

Always turn off power to CPU before insertion
and/or removal of any PCBAs to avoid possible
circuit damage.

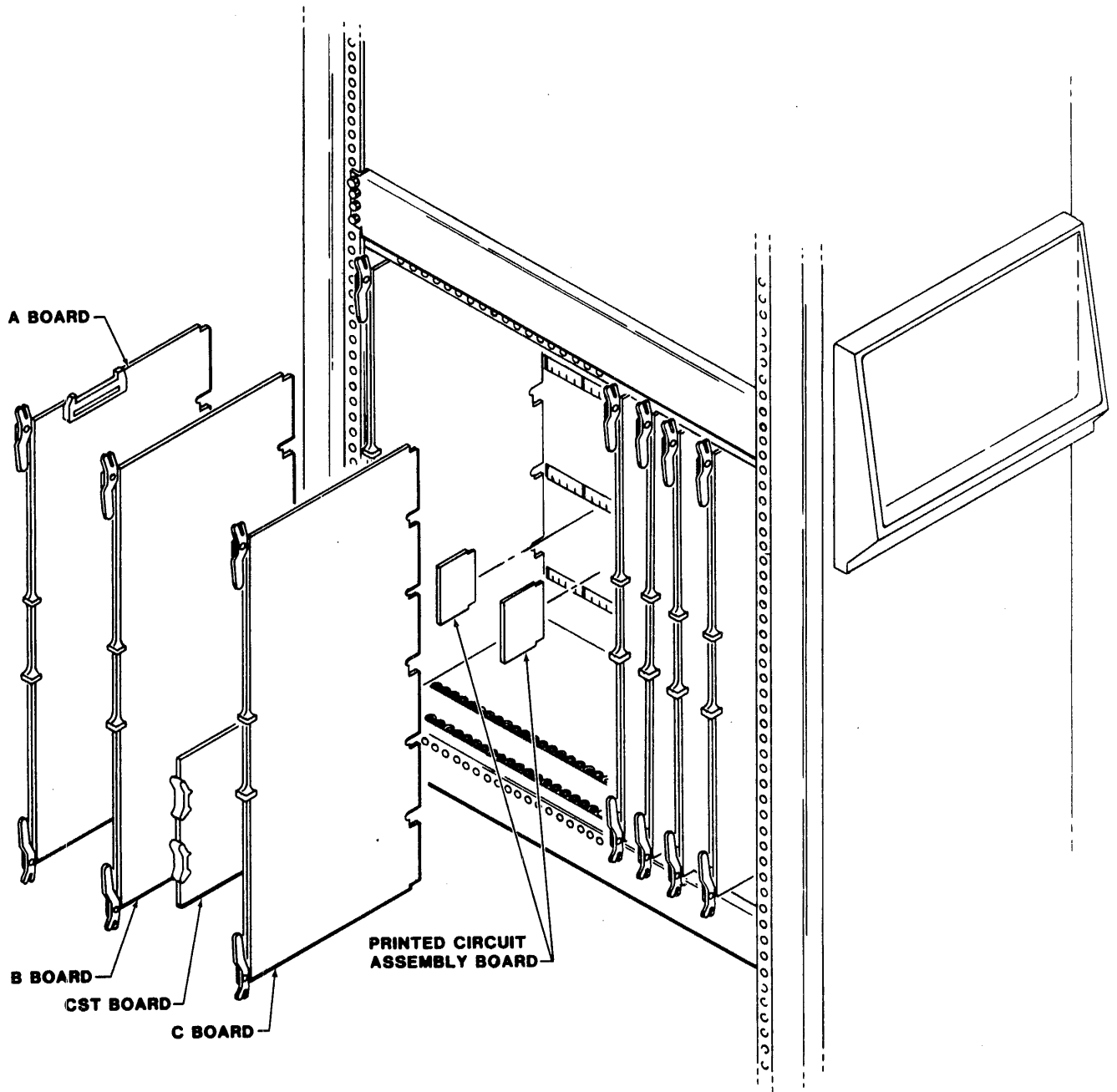
Verify each PCBA is properly aligned in the throat of the mating RH70 connector before attempting to firmly seat the PCBA by means of the extractor handle. To install the four PCBAs and interface cables, see Figure 3-5 and use the following procedure:

- a. Remove Bus Grant PCBA from RH70 slot 27, 31, 35, or 39. The selected slot is to be used for installation of the A-Board.
- b. Insert A-Board fully into selected RH70 slot.

- c. Plug A-Cable for first disk drive in system into connector J1 on top of A-Board. A-Cable should lie in cableway at top of PDP-11/70 CPU chassis underneath memory cables from CPU. Cable should pass through strain relief at rear of chassis, and pin 1 of A-Cable connector should be toward outside of chassis. Pin-1 end of A-Cable connector should be identified with an arrow molded into connector body (or some other suitable and easily recognized identification marking). If twisted-pair flat cable is used, brown-brown, followed by red-brown colored twists should be on pin-1 side of A-Cable.
- d. Insert B-Board three-quarters of proper seating depth into RH70 slot for B-Board in front of A-Board. This slot should be 26, 30, 34, or 38, as applicable, but must be slot adjacent to that in which A-Board is installed.
- e. Connect all B-Cables. B-Cables should be dressed in cableway above A-Cable, and should pass through cable strain relief at rear of PDP-11/70 CPU chassis. Pin 1 of B-Cable connector (black stripe edge of cable) should be toward outside of PDP-11/70 CPU chassis. B-Cables may be plugged into any one of the four B-Cable connectors, because they are all identical in function.
- f. Fully insert B-Board and properly dress B-Cables into cableway.
- g. Install CST PCBA into RH70 slot in front of B-Board. This slot can be 24, 28, 32, or 36, as applicable, but must be slot adjacent to that in which B-Board is installed.
- h. Install C-Board into RH70 slot in front of CST PCBA. This slot can be 25, 29, 33, or 37, as applicable, but must be slot adjacent to that in which CST PCBA is installed.
- i. Connect cables to disk drives (see subsection 3.7).

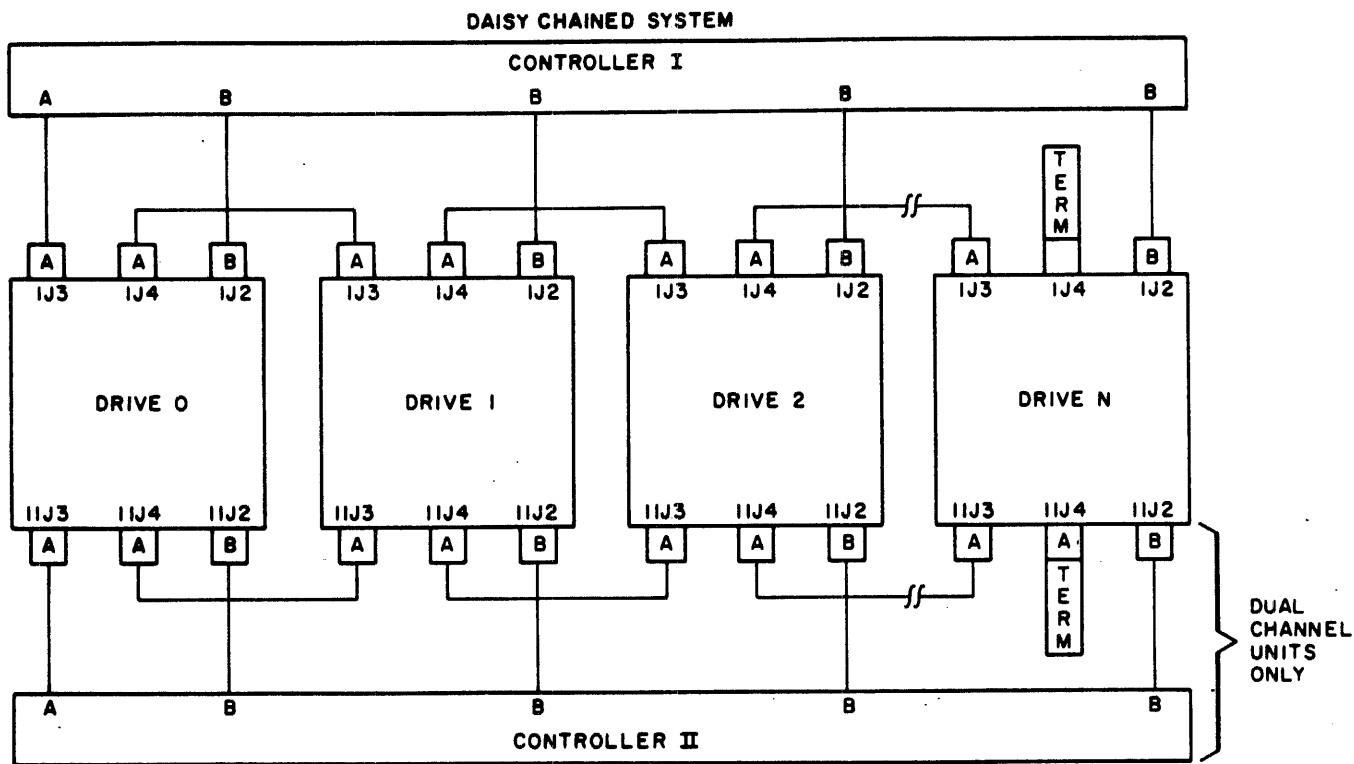
3.7 CABLE ROUTING AND RFI SUPPRESSION

Cable routing and installation is governed by requirements of the Federal Communications Commission (FCC). This subsection describes the features, use, and installation of the RFI-suppression devices, manufactured by Emulex Corporation, to meet FCC requirements for Class A equipment.



SC7201-0199

Figure 3-4. SC72/BX Disk Controller Installation Sequence



NOTES:

- 1. MAXIMUM CUMULATIVE A CABLE LENGTHS = 100 FEET**
- 2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET**

SC7201-0200

Figure 3-5. SC72/BX Disk Controller Cabling Diagram

3.7.1 EQUIPMENT CABINET

The equipment cabinet in which the computer equipment is installed should be a standard 19-inch wide EIA or RETMA equipment cabinet, completely enclosed by metal. To ensure proper shielding of all equipment in the cabinet, all outer walls of the cabinet must be free from holes, except small perforations for air exhaust are permitted.

New equipment cabinets for DEC systems have a specially fabricated rear bulkhead door or panel in which apertures have been cut. These apertures are designed for installation of blank panels or panels with slots and associated grounding bars to provide feed-through shield grounding for cables that connect equipment mounted within the cabinet and equipment mounted in other cabinets. All such apertures must be filled with one of these panels. These panels are called "Personality Panels" and are all the same size as shown in Figure 3-6.

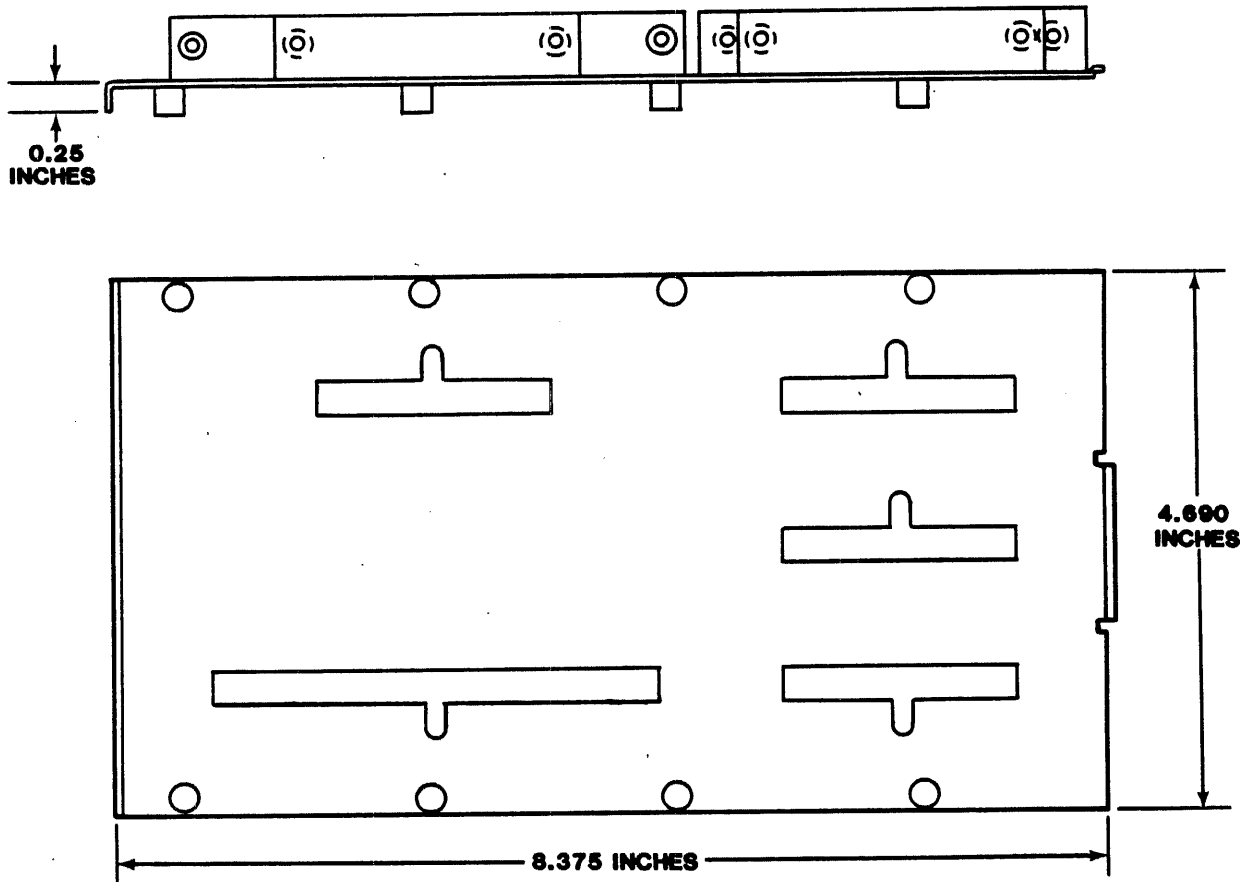
3.7.1.1 Same Cabinet

If the disk drives to be interfaced with the SC72/BX disk controller PCBA are to be mounted in the same cabinet as the CPU SC72/BX disk controller, the main concern is installing the system so that no gaps are left in the shield. The rear of the CPU cabinet is typically shielded with a bulkhead from top to bottom. The bulkhead is segmented to ease installation of different optional peripheral devices. Each segment has two apertures, each of which is covered by a blank panel. The general procedure is to remove one of the blank panels from the bulkhead segment and replace that blank panel with a Personality Panel (Emulex P/N SU1110201-xx), or to remove the entire bulkhead segment and replace it with a Bulkhead Distribution Panel (Emulex P/N CU2220301-xx). To maintain the integrity of the RFI shield, there must be no gap above or below the replacement panel after that panel is installed. If shield integrity is maintained, no other steps are necessary to ensure RFI shield compliance for the cabinet. Conducted RFI should be prevented by the line filters that are installed by DEC in the power distribution panel for the CPU cabinet.

3.7.1.2 Separate Cabinets

If the disk drives to be interfaced with the SC72/BX disk controller PCBA are mounted in a separate cabinet from that of the CPU and SC72/BX disk controller, that expansion cabinet must prevent RFI radiation by being shielded in the same way the DEC CPU cabinet is shielded. Also the cables that connect to the SC72/BX disk controller interface in the CPU cabinet must be shielded, since they are external to the shielded cabinet environment.

Emulex recommends using a hardened cabinet such as the Everest Electronic Equipment Model EH9642 with the FCC option. The Everest, like the DEC CPU cabinets, has a full-length, segmented bulkhead in the rear. One of the segments should be removed and replaced with a Bulkhead Distribution Panel or with a rack-mount panel that contains a blank panel and a Personality Panel (these components are needed to allow the shielded cable from the SC72/BX disk controller to be terminated). As in the DEC cabinet, there must be no gap above or below any rack-mounted panel when the installation is complete.



SC7201-0201

Figure 3-6. Personality Panel Dimensions

To prevent the introduction of conducted interference on the ac line that feeds the internal power supply, a power distribution panel with a line filter must be installed in the expansion cabinet. A typical adequate filter is the Model 1020 EMI Filter, manufactured by Filter Concepts Corporation and included in the Model MDP110 Power Supply manufactured by Marway Products, Incorporated.

3.7.1.3 Shielding

For older equipment-cabinet installations that lack complete metal shielding, all system cabling inside and outside the cabinet must be shielded. For new equipment cabinets that provide complete shielding, only those cables that run outside the cabinet(s) must be shielded.

3.7.1.4 Grounding

Ground returns and shielding of all cabling within the rack/cabinet must be grounded to the cabinet, and the cabinet itself must have a sure Earth ground. All cable ground returns and shielding entering the cabinet must be properly grounded, once inside the cabinet.

3.7.2 RFI-SUPPRESSION DEVICES

The RFI-suppression devices developed by Emulex consists of suitable Personality Panels, unshielded cables for connections within the equipment cabinet, and shielded/jacketed cables that are routed between the cabinets. Two Personality Panels are required; one for each end of the shielded/jacketed cable(s). The Personality Panel for Emulex disk controllers is Emulex part number (P/N) SU1110201-xx.

For older equipment cabinets that lack the bulkhead with apertures for blank panels and Personality Panels, Emulex provides a special bulkhead distribution panel (Emulex P/N CU2220301-xx) that can be mounted on the back of an equipment cabinet. Mounting requires four screws on each end, as shown in Figure 3-7. This distribution panel has apertures for the blank panels and Personality Panels.

ALL DIMENSIONS IN INCHES

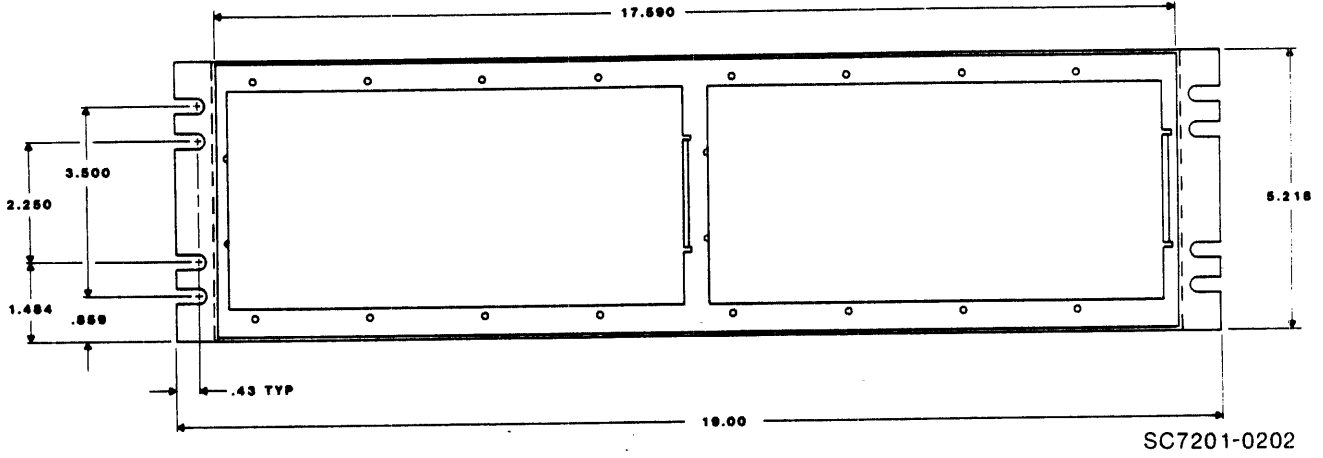


Figure 3-7. CU2220301 Bulkhead Distribution Panel

Cable details for Emulex disk controllers are listed in Table 3-1 with cable lengths expressed in feet (ft) or inches (in.), as applicable.

Table 3-1. Shielded Cables and Installation Hardware

Item	Part Number	Description	Length	Qty Rqd	Interface
1	SU7811212-01	Cable, Shielded,	4 ft	1	SMD A-Cable
	SU7811212-02	Cable, Shielded,	8 ft	1	SMD A-Cable
	SU7811212-03	Cable, Shielded,	15 ft	1	SMD A-Cable
	SU7811212-04	Cable, Shielded,	25 ft	1	SMD A-Cable
	SU7811212-05	Cable, Shielded,	35 ft	1	SMD A-Cable
	SU7811212-06	Cable, Shielded,	50 ft	1	SMD A-Cable
2	SU7811219-01	Cable, Unshielded,	2 ft	2	SMD A-Cable
	SU7811219-02	Cable, Unshielded,	4 ft	2	SMD A-Cable
	SU7811219-03	Cable, Unshielded,	6 ft	2	SMD A-Cable
	SU7811219-04	Cable, Unshielded,	8 ft	2	SMD A-Cable
	SU7811219-05	Cable, Unshielded,	10 ft	2	SMD A-Cable
3	SU7811213-01	Cable, Shielded,	4 ft	1-4	SMD B-Cable
	SU7811213-02	Cable, Shielded,	8 ft	1-4	SMD B-Cable
	SU7811213-03	Cable, Shielded,	15 ft	1-4	SMD B-Cable
	SU7811213-04	Cable, Shielded,	25 ft	1-4	SMD B-Cable
	SU7811213-05	Cable, Shielded,	35 ft	1-4	SMD B-Cable
	SU7811213-06	Cable, Shielded,	50 ft	1-4	SMD B-Cable
4	SU7811218-01	Cable, Unshielded,	2 ft	2-8	SMD B-Cable
	SU7811218-02	Cable, Unshielded,	4 ft	2-8	SMD B-Cable
	SU7811218-03	Cable, Unshielded,	6 ft	2-8	SMD B-Cable
	SU7811218-04	Cable, Unshielded,	8 ft	2-8	SMD B-Cable
	SU7811218-05	Cable, Unshielded,	10 ft	2-8	SMD B-Cable
	SU7811218-06	Cable, Unshielded,	12 ft	2-8	SMD B-Cable
	SU7811218-07	Cable, Unshielded,	15 ft	2-8	SMD B-Cable
5	SU1110201	Personality Panel		4-10	All
6	CU2220301	Bulkhead Distribution Panel (optional)		2-5	All

The items listed in Table 3-1 can be ordered from your Emulex sales representative or directly from the factory. The factory address is:

Emulex Customer Service
 3545 Harbor Boulevard
 Costa Mesa, CA 92626
 (714) 662-5600 TWX 910-595-2521

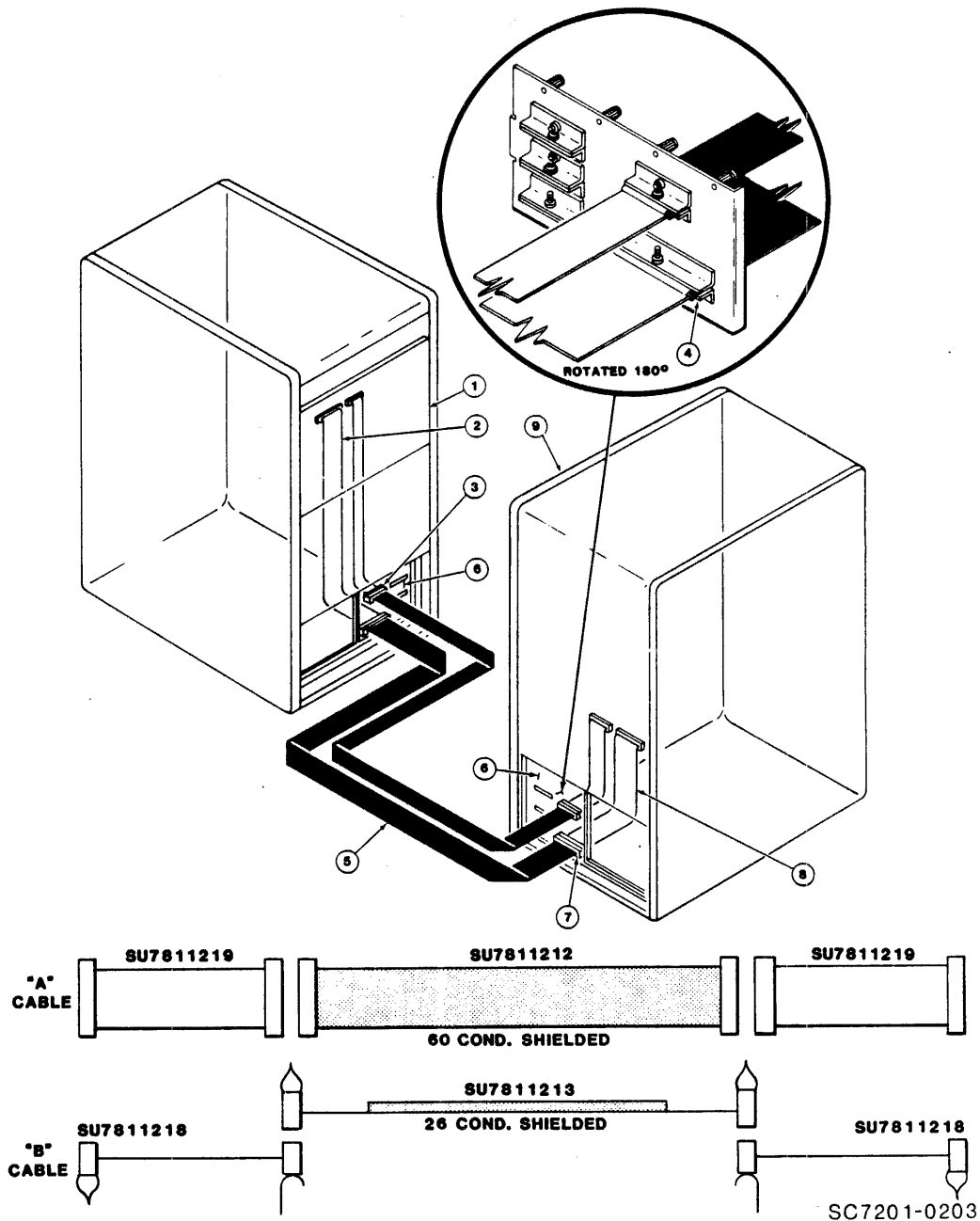
3.7.3 CABLE INSTALLATION

Emulex products are installed directly in the backplane of a CPU cabinet manufactured by DEC. If the cabinet which houses the CPU has enough room to include the peripheral(s) controlled by the Emulex product, those peripherals should be housed in the same cabinet. In such an installation, no shielded interconnect cables are required because the equipment cabinet itself provides the shielding. If the cabinet is the older type which does not provide complete shielding, the cables between the Emulex product and the interconnected equipment must be shielded, even when the cables are not routed outside the cabinet.

When peripherals controlled by the Emulex product(s) are not housed in the same equipment cabinet, the equipment must be interconnected by suitable RFI-suppression devices that ground all shielded cables entering the equipment cabinet.

To install the Emulex RFI-suppression devices, see Figures 3-6 and 3-8 and use the following procedure:

- a. Open rear bulkhead door or panel of CPU equipment cabinet.
- b. Install Emulex SC72/BX disk controller in appropriate CPU bus slots.
- c. Install appropriate Personality Panel in convenient aperture in rear bulkhead of equipment cabinet for SC72/BX disk controller and secure in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panel.
- d. Install two Personality Panels in convenient aperture in rear bulkhead of equipment cabinet for first disk drive in daisy chain and secure each in place with eight captive screws. Tighten screws finger tight. Verify no gaps are present above or below Personality Panels.
- e. Repeat step d for cable entry to and exit from cabinets for remaining disk drives to be in daisy chain.
- f. Select shielded interface cable (P/N SU7811212-xx) long enough to reach from Personality Panel for SC72/BX disk controller to Personality Panel for cable entry to first disk drive.



1. SC72/BX DISK CONTROLLER PCBAS
2. NONSHIELDED EXTENSION CABLE, SC72/BX DISK CONTROLLER - SHIELDED CABLE
3. CABLE CONNECTORS, SC72/BX DISK CONTROLLER - SHIELDED CABLE
4. CLAMP - SHIELD OF SHIELDED CABLE CLAMPED WITHIN
5. SHIELDED/JACKETED CABLE, EXTERNAL TO EQUIPMENT CABINETS
6. PERSONALITY PANELS
7. CABLE CONNECTORS, SHIELDED CABLE - PERIPHERAL DEVICE
8. NONSHIELDED EXTENSION CABLE, SHIELDED CABLE-PERIPHERAL DEVICE
9. PERIPHERAL DEVICE

Figure 3-8. RFI-Suppression Cable Installation

- g. Strip about one inch of shielded insulation from end of cable for SC72/BX disk controller to expose shield. Cut shield at each edge to allow shield to be folded back over insulation, then fold shield over insulation. Route prepared cable ends through appropriate slots in Personality Panel (see detail in Figure 3-8). Repeat this process at other end of cable.
- h. Select unshielded interface cable (P/N SU7811219-xx) long enough to reach from A-Cable connector to associated Personality Panel in cabinet bulkhead.
- i. Find arrow molded into header of cable connector for mating cable connector. Arrow identifies pin 1 of connector.
- j. Find arrow molded into header of mating connector on SC72/BX disk controller, then align arrows and connect mating connectors.
- k. Select shielded interface cable (P/N SU7811213-xx) long enough to reach from Personality Panel for SC72/BX disk controller to Personality Panel for first disk drive in daisy chain.
- l. Repeat steps g through j for this B-Cable, then repeat this B-Cable installation procedure for up to seven more B-Cables.
- m. Select unshielded interface cable (P/N SU7811219-xx) long enough to reach from A-Cable connector on SC72/BX disk controller to shielded A-Cable connector in associated Personality Panel for SC72/BX disk controller.
- n. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.
- o. Select unshielded interface cable (P/N SU7811219-xx) long enough to reach from A-Cable connector on disk drive to associated Personality Panel in rear bulkhead of disk drive cabinet.
- p. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.
- q. Select unshielded interface cable (P/N SU7811218-xx) long enough to reach from B-Cable connector on SC72/BX disk controller to shielded B-Cable connector in associated Personality Panel for SC72/BX disk controller.

- r. Find and align pin 1 identifying arrows on mating connectors at each end of unshielded interconnect cable and connect mating connectors.
- s. Select unshielded interface cable (P/N SU7811218-xx) long enough to reach from B-Cable connector on first disk drive to associated Personality Panel in rear bulkhead of disk drive cabinet.
- t. Repeat steps q through s for each of remaining B-Cables.
- u. Interconnect disk drives to be daisy chained as instructed in disk drive technical manual. Verify last disk drive in daisy chain is properly terminated. If disk drives are in separate extension cabinets, use shielded cable between cabinets as described in foregoing steps of this procedure.
- v. Close bulkhead door or panel on each equipment cabinet.

The subsystem cabling for the SC72/BX disk controller and associated disk drives is shown in Figure 3-5. B-Cables are radially connected, one to each disk drive, but the A-Cable is connected to only the first disk drive and thence to subsequent disk drives in the daisy chain by additional A-Cables between disk drives.

3.7.3.1 A-Cable

The 60-wire A-Cable should be plugged into connector J1 on the A-Board of the SC72/BX disk controller and the other end should be connected to the first disk drive. If more than one disk drive is to be used, the second disk drive is daisy-chained to the first disk drive by another A-Cable, then the third disk drive is daisy-chained to the second disk drive by another A-Cable, and the fourth disk drive is daisy-chained to the third disk drive by another A-Cable. The last disk drive on the A-Cable must have a terminator installed (see Figure 3-5). The terminator is supplied by the disk drive manufacturer. The terminator is usually plugged into one of the two A-Cable connectors on the disk drive. In some applications, a ground wire may emerge from the terminator. If such a ground wire is present, that ground wire must be connected to the disk drive chassis to provide a ground return for the resistors in the terminator. Pin 1 of the A-Cable connector on the A-Board is on the left. Pin 1 of the A-Cable connector has a notch or arrow molded on the connector body to identify the location of pin 1. Twisted-pair and flat cable have the brown-brown twist followed by the red-brown twist on the pin 1 edge of the A-Cable. The cable normally exits to the rear of the SC72/BX disk controller and through a grounding panel or bar in the PDP-11/70 CPU equipment rack. If the disk drives are mounted in the same rack as the PDP-11/70 CPU, the cables can run inside the chassis without shield grounding; otherwise, all cables between the SC72/BX disk controller and the associated disk drives must be shielded and

those shielded cables must be grounded via a grounding panel or bar at each end of the shielded cable.

NOTE

The connectors for the A-Cable and B-Cables are not keyed and can be physically reversed in the mating connector. No equipment damage should result by improper cable installation, but the system cannot operate properly.

3.7.3.2 B-Cable

Each disk drive must have a 26-wire B-Cable connected to one of the B-Cable connectors on the SC72/BX disk controller. These connectors are J1 through J4 or J8 on the B-Board of the SC72/BX disk controller. Any of these connectors can accept any B-Cable from any disk drive, because the circuitry is all the same. No extractors are used with the B-Cables. Pin 1 of the B-Cable connector has a notch or molded arrow on the connector body to identify the pin-1 location. The wire for the pin-1 edge of the B-Cable is white with a black stripe.

3.7.4 GROUND STRAP

For proper operation of the disk subsystem, the disk drives must have a good ground connection to the logic ground of the PDP-11/70 CPU chassis. The ground connection should be braid (preferably insulated) that is 1/4-inch wide or wider, or AWG No. 10 wire or larger. The grounding wire may be daisy chained between disk drives. If the disk drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the disk drive is placed in the On-Line mode with the SC72/BX disk controller. It can be connected for performing local Off-Line maintenance on the disk drive. All cables must be shielded and grounded within each equipment rack/cabinet to meet requirements of the FCC rules for Class A equipment.

NOTE

Failure to observe proper signal grounding methods generally results in marginal operation with random error conditions.

3.7.4.1 Cabling CDC and Fujitsu Drives

Certain problems may occur when Fujitsu Eagle and CDC disk drives are used on the same daisy chain string. The procedures below should be followed on any system which mixes Eagles and CDC drives on the same daisy chain:

1. Disable Tags 4 and 5 on the Eagle as described on pages 3-7 of the Fusjitsu manual.

2. Use one of the following three grounding procedures:

- A. Install CDC drives with chassis (AC) and signal (DC) grounds connected together at the drive. Refer to the system grounding section of the CDC drive manual for details.

Install grounding strap SG (DC) to FGI (AC) on the Eagle.

Install separate ground straps from each drive to the common system ground on the CPU.

- B. Install FCC-approved drive cables and attach all cable shields to the CPU and drive chassis grounds.

- C. Separate the chassis (AC) and signal (DC) grounds on each drive.

Install FCC-approved cables and attach the shield grounds to the chassis (AC) ground of each drive. Daisy chain the signal (DC) ground of each drive to the signal (DC) ground of the controller.

3. If the cable from the controller to the first drive is less than 25 feet, place the Eagles first in the daisy chain. If the cable from the controller to the first drive is more than 25 feet, place the Eagles last on the daisy chain, closest to the terminator. If the total daisy chain length is more than 50 feet, use FCC approved cables whenever possible.

3.8 TESTING

Testing involves self-test, register examination, hardware formatting, and diagnostics.

3.8.1 SELF-TEST

When power is applied to the PDP-11/70 CPU, that power is also simultaneously applied to the SC72/BX disk controller; therefore, the SC72/BX disk controller automatically executes a built-in self test whenever power is applied to the CPU. The self test is not executed with every INIT signal from the Unibus, but only at power-up time. If the self test is successful, the FAULT LED on the top edge of the B-Board becomes extinguished or flashes. The FAULT LED flashes when the SC72/BX disk controller cannot properly address one disk drive after successful self-test execution. Such flashing can occur if the A-Cable or B-Cables are not properly connected, if a disk drive is not powered with a Unit Select code plug, or if two disk drives have identical Unit Select code plug (or select switching). Steady illumination of the FAULT LED indicates the SC72/BX disk controller failed the self test and cannot be addressed from the PDP-11/70 CPU.

3.8.2 REGISTER EXAMINATION

After applying power to the PDP-11/70 CPU and observing the FAULT LED indicator is extinguished, a quick check should be made to verify the registers in the SC72/BX disk controller can be read from the computer console. The RMCS1/RPCS1 register should contain 004200 if the disk drive is available and 000200 if it is not. If the PDP-11/70 CPU has a console emulator, all registers in the SC72/BX disk controller should be examined.

3.8.3 HARDWARE FORMATTING OF DISKS

The SC72/BX disk controller can format any disk by writing headers and all-zeros data in all sectors of the addressed disk. This format does not verify the data or headers, and does not write a Bad Sector File on the last track of the last cylinder; however, with the disk drive in the On-Line and Ready mode, formatting can be performed from the front panel of the PDP-11/70 CPU by using the following procedure:

- a. Halt the PDP-11/70 CPU by placing the HALT/ENABLE switch in the down position, then press the START switch to cause an INIT operation. If halting the PDP-11/70 CPU is undesirable (console emulator in use), deposit a 40g (Controller Clear instruction) in register RMCS2/RPCS2 at address 17776710 (or base + 10 if alternate address is selected).
- b. Install a scratch pack on disk drive and perform necessary operations to make that disk drive On-Line and Ready.
- c. Deposit the disk drive Unit Select number (if other than zero) in register RMCS2/RPCS2 at address 17776710 (or base + 10 if alternate address is selected).
- d. Deposit a 0000021g (Read-In Preset command) in register RMCS1/RPCS1 at address 17776700 (or base + 00 if alternate address is selected). This deposit sets Volume Valid (bit 06 in register RMDS/RPDS).
- e. Deposit a 177777g in register RMHR/RPCC at address 17776736 (or base + 36 if alternate address is selected). This deposit enables the extended Format command.
- f. Deposit a 0000077g (Format command) in register RMCS1/RPCS1 at address 17776700 (or base + 00 if alternate address is selected). The WRITE activity LED indicator on the B-Board (see Figure 3-2) should flash as long as the disk formatting is being processed. Wait until this LED is not lit.

- g. Examine contents of register RPDS/RMDS at address 17776712 (or base + 12 if alternate address is selected) to determine if the bit 14, the ERR bit in that register, is set or cleared. The set condition of the ERR bit indicates an error has occurred on the selected disk drive. If an error that results from the Formatting operation exists, the contents of registers RMER1/RPER1, RPER2, and RMER2/RPER3 should be examined to determine the cause of the error, and the contents of registers RMDA/RPDA and RMDC/RPDC should be examined to determine how far the formatting progressed.
- h. Repeat steps b through g as often as necessary.
- i. Run the software Format program. (Patches may be required on nonstandard disk drives. See Section 6 for appropriate diagnostic modification patches (RM and RP) or run the Emulex S1B18X Format program (for RM02/RM03) or S1B28A (for RP06).

3.8.4 DIAGNOSTICS

The DEC diagnostics listed in subsection 1.4.3 should be run. Usually, only the Formatter and Performance Exerciser diagnostic routines need to be run. If the disk drive configuration does not have a capacity that matches the emulated disk drive exactly, the diagnostic routines must be patched. Section 6 of this manual lists the patches that may be made to the DEC RM and RP diagnostics. If the Formatter diagnostic routine is run on an unformatted disk, it reports five errors while trying to read the Bad Sector File before it proceeds.

Emulex has diagnostics available which automatically size the formatting to the selected type of disk drive, and therefore never need patching.

If the disk drive has a capacity (size) different from that of the DEC disk for the selected Drive Type Code (see Appendix A, Table A-2, A-5, or A-8), the operating system must be patched. RSTS/E and RSX-11M patches are included in the Emulex patch document.

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4.1 PROGRAMMING INFORMATION

This subsection provides information about clearing the SC72/BX disk controller, handling interrupt conditions, termination of Data Transfer operations, and the functions made available when the Ready (RDY) bit in register RPCS1/RMCS1 bit position 07 is set. This subsection is divided into three subsections, as listed in the following table:

Subsection	Title
4.1	Programming Information
4.2	Dual Controller Operation
4.3	Controller Registers

4.1.1 CLEARING THE CONTROLLER

Clearing the SC72/BX disk controller may be accomplished by one of three methods, as applicable:

- a. Controller Clear - performed by writing a one-bit into the CLR bit position (register RPCS2/RMCS2, bit 05) or by issuing the Unibus Initialize (INIT) command. Either of these actions causes clearing (resetting) and/or setting of the following register bits (as applicable):

RP Disk Drives

Reset RPCS1 bits <15:12>, <10:08>, 06:00>; RPCS2 bits <15:07>, <05:00>; RPBA bits <15:00>. Sets RPCS2 bit 06 and RPCS1 bit 07.

In all RP disk drive emulations: Reset all bits in registers RPER1, RPER2, RPER3, RPDA, RPEC1, and RPEC2; RPAS ATA bit; RPOF bits <07:00>; RPDA ATA, ERR, and LST bits; RPMR bits <15:09> and <07:00>. Sets RPMR bit 08.

RM Disk Drives

Reset RMCS bits <15:12>, <10:08>, <06:00>; RMCS2 bits <15:07>, <05:00>; RMBA bits <15:00>. Sets RMCS2 bit 06 and RMCS1 bit 07.

In all RM disk drive emulations: Reset all bits in registers RMER1, RMER2, RMEC2, and RMDA; RMA ATA bit; RMDS ATA, ERR, and LST bits; RMMR1 bits <15:04> and <02:00>. Sets RMMR1 bit 03.

- b. Error Clear - performed by writing a one-bit into the TRE bit position (register RPCS1/RMCS1 bit 14). Setting this bit causes the following register bits to be cleared:

RPCS1/RMCS1 bit 14, and RPCS2/RMCS2 bits <15:08>. Also clears the SC bit (RPCS1/RMCS1 bit 15) if contents of register RPAS/RMAS equals zero.

- c. Drive Clear - Drive Clear is a command (Function Code 11). When this command is issued to the disk drive that is selected by Unit Select code U2 through U0, the following register bits are cleared and/or set (as applicable):

RP Disk Drives

Reset RPDS ATA and ERR bits; RPAS ATA bit; RPMR bits <15:09> and <07:00>; RPOF bits <07:00>; all bits in registers RPER1, RPER2, RPER3, RPEC1, and RPEC2. Sets RPMR bit 08.

RM Disk Drives

Reset RMDS ATA and ERR bits; RMA ATA bit, RMMR1 bits <15:04> and <02:00>; all bits in registers RMER1, RMER2, and RMEC2. Sets RMMR1 bit 03.

4.1.2 INTERRUPT CONDITIONS

The SC72/BX disk controller generates an interrupt whenever there is present one or more of the following conditions:

- a. Termination of a Data Transfer operation if Interrupt Enable (IE) bit 06 in register RPCS1/RMCS1 is set when the SC72/BX disk controller becomes ready.
- b. Assertion of Attention Active bits (RPDS/RMDS bit 15, and RPAS/RMAS bits <07:00>) or occurrence of set Special Condition (SC) bit (RPCS1/RMCS1 bit 15) while SC72/BX disk controller is not busy and IE (bit 06 in register RPCS1/RMCS1) is set.

- c. Program writes a one into bits RDY and IE (RPCS1/RMCS1 bits <07:06>, respectively) at the same time.

NOTE

Writing a one into RDY and IE in register RPCS1/RMCS1 can be done by Read-Modify-Write instructions (BIS, etc.) which then sets the IE bit properly.

4.1.3 DATA TRANSFER TERMINATIONS

Any Data Transfer operation which has been successfully started may be terminated in one of the following ways:

- a. Normal Termination - Word count overflows to zero and the SC72/BX disk controller becomes Ready at the end of the current sector.
- b. Controller Error - An error occurs in register RPCS2/RMCS2 bits <15:08>. Any of these errors sets the TRE bit (RPCS1/RMCS1 bit 14) which terminates the Data Transfer immediately and places the SC72/BX disk controller in the Ready mode.
- c. Drive Error - The ERR bit (register RPDA/RMDS bit 14) and at least one bit in register RPER1/RMER1, RPER2, and/or RPER3/RMER2 is set. The TRE bit is also set and the SC72/BX disk controller is placed in the Ready mode. The ATA bits (RPDS/RMDS bit 15 and RPAS/RMAS bits <07:00>) for the disk drive that is performing the Data Transfer operation also become asserted.
- d. Program-Caused Abort - The program can cause an abort of any operation by executing a Controller Clear or a Reset instruction. Status and error information is lost when a program-caused abort is done, and the SC72/BX disk controller and selected disk drive become Ready immediately.

4.1.4 READY BITS

The RDY bit (RPCS1/RMCS1 bit 07) is the Ready indicator for the SC72/BX disk controller. When RDY is set to logic one, the SC72/BX disk controller is ready to accept a Data Transfer command. RDY is reset when the SC72/BX disk controller is performing a commanded Data Transfer operation. The DRY bit (RPDS/RMDS bit 07) is the Ready indicator for the selected disk drive and is the complement of the GO bit (RPCS1/RMCS1 bit 00). To successfully initiate a Data Transfer command, both these bits must be asserted. A command that does not involve transfer of data (Seek, Drive Clear, etc.) may be issued to a disk drive at any time DRY is asserted (set to one) regardless of the state of the RDY bit.

When a Data Transfer command is successfully initiated, both RDY and DRY become negated (reset). When a command that does not involve data transfer is successfully initiated, only the DRY bit is reset.

Assertion of the RDY bit after execution of a Data Transfer command does not occur until the DRY bit is set and the SC72/BX disk controller is done with the operation. RDY is asserted when the last memory cycle is completed (or at the time of an abort condition) and the last of the data has been transferred.

If any command, except Drive Clear, is issued to a disk drive that has asserted the ERR bit (RPDS/RMDS bit 14), that command is ignored by the disk drive. If a Data Transfer command is issued to a disk drive which has asserted the ERR bit, the disk drive does not execute the command and the Missed Transfer (MXF, RPCS2/RMCS2 bit 09) error bit is set.

4.2 DUAL CONTROLLER OPERATION

Disk drives that use an SMD interface may be equipped with a Dual Port option which allows two disk controllers (usually on separate computers) to access the disk drive(s). The SC72/BX disk controller supports this type of operation as a standard feature. Most of the Dual Port functions of the DEC controller that is being emulated are supported by the SC72/BX disk controller, and those which are not should be transparent to a properly written program for Dual Port disk drives.

4.2.1 DUAL PORT CHANNELS

The two disk drive ports are identified as Channel I and Channel II. Each channel has a disable switch which disables the port and prevents the computer from having access to that port. Access to the disk drive in Dual Port operation is switched back and forth between the two disk controllers under program control of the two computers which are involved. Table 4-1 summarizes the responses of the registers in the SC72/BX disk controller to different conditions that can occur during operation in the Dual Port mode.

4.2.2 UNSEIZED STATE

The disk drive is in the unseized state when it is not connected to either SC72/BX disk controller. The PDP-11/70 CPU must issue a request for the SC72/BX disk controller to seize the disk drive. This request is made in one of two ways:

- a. Writing into any disk drive register, including Read-only registers.
- b. Writing a one-bit into the appropriate ATA bit position (see subsection 4.3.9) in the RPAS/RMAS register for the disk drive.

4.2.3 SEIZED STATE

The disk drive is seized when it is logically connected to one of the SC72/BX disk controllers. At that time, the DVA bit (RPCS1/RMCS1 bit 11) is set to indicate the disk drive is ready to communicate with the SC72/BX disk controller which has seized that disk drive. If the disk drive is seized by the other SC72/BX disk controller, the DVA bit is reset and all the disk drive registers are read as zeros and any attempted Write operation to a register is ignored. Any attempt to seize a disk drive which is busy with the other port causes the request to be remembered and acted upon when that disk drive is released by the other SC72/BX disk controller.

4.2.4 RETURNING TO THE UNSEIZED STATE

The disk drive is released and returned to the unseized state by issuing a Release command. In addition, a one-second timer in the SC72/BX disk controller times out and releases the disk drive if one of the events described in paragraph 4.2.2 for seizing the disk drive is not performed periodically to keep resetting the timeout timer. Furthermore, reading the contents of register RPCS1/RMCS1 when the disk drive is already seized resets the timer back to the one-second interval.

Table 4-1. Register Access with Dual Port Operation of SC72/BX Disk Controller

Disk Drive State During SC72/BX Disk Controller Action	SC72/BX Disk Controller Response with Respect to Action Occurring on Channel I
<u>Read Contents of RPCS1/RMCS1</u>	
Disk Drive Not Seized	Reads only common portion of RPCS1/RMCS1 register contents. Disk drive portion of register RPCS1/RMCS1 is read as all zeros. No Request flag is set.
Disk Drive Seized by Channel I	Bit 11 (DVA) of register RPCS1/RMCS1 set to logic one condition; contents of disk drive and common portions of register RPCS1/RMCS1 are read. SC72/BX disk controller resets timer to one second interval.
Disk Drive Seized by Channel II	Reads only common portion of RPCS1/RMCS1 register contents. Disk drive portion of register RPCS1/RMCS1 is read as all zeros. No Request flag is set.

Table 4-1. Register Access with Dual Port Operation of SC72/BX Disk Controller (continued)

Disk Drive State During SC72/BX Disk Controller Action	SC72/BX Disk Controller Response with Respect to Action Occurring on Channel I
<u>Read Contents of Any Other Disk Drive Register</u>	
Disk Drive Not Seized	Reads all zeros.
Disk Drive Seized by Channel I	Reads register contents.
Disk Drive Seized by Channel II	Reads all zeros.
<u>Write to RPCS1/RMCS1 Register</u>	
Disk Drive Not Seized	Function code is attempted if GO bit (RPCS1/RMCS1 bit 00) set. Port Request flag is set. Operation Incomplete (OPI) error is usual result.
Disk Drive Seized by Channel I	Loads function code. (Switches to unseized condition if function code is a Release command).
Disk Drive Seized by Channel II	Function code attempted if GO bit equals one. Port Request flag is set. OPI error is usual result.
<u>Write Into Any Other Disk Drive registers, Except RMCS1/RPCS1</u>	
Disk Drive Not Seized	Write command is ignored and Port Request flag is set.
Disk Drive Seized by Channel I	Loads the register. Resets timer duration to one second.
Disk Drive Seized by Channel II	Write command is ignored and Port Request flag is set.

When the SC72/BX disk controller detects a previously busy disk drive become not busy, it checks the status of its Request flag. If the disk drive had been previously requested while busy on the other port, the SC72/BX disk controller seizes the disk drive, sets the DVA bit and sets the appropriate ATA bit, which causes an interrupt message to be sent to the PDP-11/70 CPU if the IE bit

(RPCS1/RMCS1 bit 06) is set. If the PDP-11/70 CPU does not respond to the Attention Active (ATA) signal within one second, the disk drive is released, but the ATA bit remains set.

4.2.5 DEC COMPATIBILITY

The SC72/BX disk controller differs from the equivalent DEC RH70 controller in three important areas:

- a. There is no neutral state. Since the SC72/BX disk controller does not have instantaneous access to all disk drives at the same time (a limitation of the daisy-chained A-Cable and the microprocessor organization of the SC72/BX disk controller), then if the disk drive is not currently seized, the SC72/BX disk controller assumes it is busy at the other port. The DEC RH70 controllers can switch from neutral to seized state within the time required to perform a single Read or Write operation on a disk drive register. In that situation, no ATA bits are set in the RPDS/RMDS and/or RPAS/RMAS registers, and the disk drive appears to have been already seized.
- b. The Release command is not instantaneous because the SC72/BX disk controller requires a few microseconds to execute the command. During this command execution time, the disk drive appears to the PDP11/70 CPU to be in the unseized state.
- c. During a Data Transfer operation, the timeout timers do not operate and the disk drives cannot be polled to determine if they are or are not busy. Because of this condition, no disk drives are seized or released during execution of a Data Transfer operation.

The software driver should not issue a Release command and then attempt to save the current status of a disk drive because the Release command immediately sets the disk drive in the unseized state. To allow the other SC72/BX disk controller time to poll the disk drive, the PDP-11/70 CPU should not communicate with any of the registers in the released disk drive until it is required to seize the disk drive again.

4.2.6 DUAL-PORT DISK DRIVES IN SINGLE-PORT MODE

When using an operating system which does not have Dual-Port disk drive software support, advantages may still be achieved by using Dual-Port disk drives while operating the SC72/BX disk controller in the Single-Port mode. This operating condition allows for a nondynamic operation between two PDP-11/70 CPUs. In such an operating condition, the SC72/BX disk controller does not logically release the disk drive; i.e., in effect, the disk drive is seized by both SC72/BX disk controllers at the same time.

The one-second timeout timer (and Release command) operate exactly as described in subsection 4.2.4. Even when a disk drive is released, it still appears (to the releasing disk controller) to be in the seized condition. No ATA signal is generated when the other disk controller detects the disk drive is not busy. If a command is issued to a SC72/BX disk controller while a disk drive is busy on the other port, the SC72/BX disk controller waits indefinitely until that disk drive becomes not busy before executing whatever command it has been issued.

The mode of operation eliminates the need for manually switching the disk drive from one SC72/BX disk controller to another.

4.2.7 DUAL ACCESS MODE

The SC72/BX disk controller supports the Dual Access mode to provide compatibility with software that is configured for Dual Access operations.

The Dual Access mode is enabled by setting switch SW4-7 in the ON position. When in the Dual Access mode, the SC72/BX disk controller sets the Dual Port Mode (DPM) bit (bit 11 in register RPDT/RMDT) and the Programmable (PGM) bit (bit 09 in register RPDS/RMDS) to imitate the DEC neutral state.

When bits DPM and PGM are set, the operating system attempts to seize a disk drive by simply writing a command to it. If the disk drive is not busy, the command is executed. If the disk drive is already busy on its other port, the SC72/BX disk controller simply waits until that disk drive is released and then seizes the disk drive and commands it to perform the requested operation.

The choice of disk controller made by the operating system depends on whether the disk controller is or is not currently executing a command, and what type of command (if any) is being executed. A disk controller that is executing a Data Transfer command can not accept another Data Transfer command, but a disk controller that is executing a Positioning or Housekeeping command may be issued any command that is applicable to a non-busy disk drive.

The first time the SC72/BX disk controller detects a disk drive, it is ignored for one second. This one-second delay occurs once for each disk drive on the SC72/BX disk controller interface. The delay prevents the SC72/BX disk controller from detecting erroneous status information when power is applied to the disk drive after the SC72/BX disk controller has been powered up. For a disk drive in Dual Port mode, the delay (or stall) prevents the other PDP-11/70 CPU from accessing that disk drive until the time delay (stall) has been completed. The Dual Access option switch bypasses the stall in all instances. For proper system operation with the Dual Access switch option activated (SW4-7 ON), all disk drives must have power applied before either SC72/BX disk controller is powered up.

Setting the Dual Port option switch overrides the Dual Access option, except for the one-second stall override.

4.3 CONTROLLER REGISTERS

The SC72/BX disk controller has 22 device registers. These registers are used to interface the SC72/BX disk controller with the disk drives in the system and with the PDP-11/70 CPU of the computer. The registers are loaded (written into) and/or their contents are read under program control. These activities initiate selected commands to the disk drives and monitor status and error conditions that may be present on the disk drives. Most registers can be written into with word or byte operations.

The SC72/BX disk controller can emulate both RP and RM types of disk drives when certain configurations are selected. Each physical disk drive can support any type of logical disk drive unit, and when a physical disk drive has two logical disk drive units assigned to it, each logical disk drive unit is usually the same type and capacity. Many registers, described in this subsection, are therefore capable of being RP or RM registers; but not both RP and RM simultaneously. Those registers that lack this duality in emulation are so indicated by a single (unslashed) identifying mnemonic and their descriptions are not further subdivided into additional subsections with lower-level sideheads. The second-level sidehead includes the numerical address which is common to both registers described. For example, subsection 4.3.2 lists address 17776700 as the address which pertains to both registers RPCS1 and RMCS2. Whether an RP or RM register is activated depends on the disk drive configuration setup by the user (see Appendix A, Tables A-2, A-5, and A-8).

4.3.1 COMMON FEATURES

Registers RPWC/RMWC, RPBA/RMBA, RPCS2/RMCS2, RPDB/RMDB, and bits <15:12> and <10:06> of register RPCS1/RMCS1 are common to all disk drives. Loading and reading of these register contents is independent of the disk drive unit selected. A separate set of the other registers and bits 11 and <05:00> of register RPCS1/RMCS1 exists for each of the disk drives. Loading and reading of these register contents depends on the disk drive selected by the Unit Select code number in register RPCS2/RMCS2. In addition, the eight ATA bits in register RPAS/RMAS are each associated with an individual disk drive. Any attempt to write into the disk drive registers (except RPAS/RMAS) while the GO bit for that disk drive is asserted causes a Register Modification Refused error and the register is not modified.

4.3.2 CONTROL/STATUS REGISTER ONE (RPCS1/RMCS1) 17776700

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

SC	TRE	0	0	DVA	0	A17	A16	RDY	IE	F4	F3	F2	F1	F0	GO
----	-----	---	---	-----	---	-----	-----	-----	----	----	----	----	----	----	----

---Common To---	---Common To-----
All Disk Drives	All Disk Drives

Register RPCS1/RMCS1 can be read from or written to by program control. It is used to store the Function Code of the current command to the disk and to store information about the operational status of the SC72/BX disk controller. Setting the GO bit causes the SC72/BX disk controller to recognize the Function Code in the register and to initiate the operation for the corresponding disk drive. The actual start of command execution does not begin when the Function Code is written into this register. Command execution begins when the SC72/BX disk controller has finished any previous operation and polls through register RPCS1/RMCS1 for the disk drive in search of a command that needs initiation.

Special Condition (SC) - Bit 15

This Read-only bit is set as long as the TRE bit in RPCS1/RMCS1 or any of the ATA bits for the addressed disk drive are set. This bit also causes an Interrupt message to be sent to the PDP-11/70 CPU if the IE bit (RPCS1/RMCS1 bit 06) is set.

Transfer Error (TRE) - Bit 14

This Read/Write bit is set by RMCS2/RPCS2 error bits (WCE, DLT, UPE, NED, NEM, PGE, MXF, or by a disk drive operational error during a Data Transfer operation. Writing a one into this bit position causes the Transfer Error bits (WCE, etc.) to be cleared. They are also cleared at the start of every Data Transfer operation.

Drive Available (DVA) - Bit 11

This Read-only bit is set when the disk drive is seized by the SC72/BX disk controller. When not in the Dual Port mode, the disk drive is seized as long as it is powered up.

Extended Bus Address (A17, A16) - Bits <09:08>

These bits comprise part of the upper extension of register RPBA/RMBA. They represent a two-bit counter that is incremented by one every time register RPBA/RMBA overflows. These bits cannot be altered if the state of the RDY bit is zero; therefore, no error occurs when an alteration is attempted.

NOTE

These bits are replicated in register RPBAE/RMBAE. Writing in these bit positions in either register RPCS1/RMCS1 or RPBAE/RMBAE affects both registers.

Ready (RDY) - Bit 07

This Read-only bit is reset (0) when the SC72/BX disk controller starts to execute a Data Transfer command (Function Codes 51 through 77), and it is set when execution of that Data Transfer command is terminated.

Interrupt Enable (IE) - Bit 06

When IE is set, an Interrupt message can be generated by the SC72/BX disk controller when RDY is asserted at the end of a Data Transfer operation or when any ATA bit is asserted. IE is automatically reset when the Interrupt message is accepted by the PDP-11/70 CPU. When a zero is written into the IE bit position by the program, any pending Interrupt messages are cancelled (disabled). An Interrupt Request message is generated by writing a one into both the IE and RDY bit positions in register RPCS1/RMCS1 at the same time. This IE bit is the same as the IE bit in register RPCS3/RMCS3.

Function Code (F4 through F0) - Bits <05:01>

These bits and the GO bit in this RPCS1/RMCS1 register comprise the Function (command) Code which determines the instructions to be performed by the SC72/BX disk controller and selected disk drive. The Function Codes are represented by an octal number that includes the GO bit. The Function Codes and their meanings are listed in the following table:

Function Code	Meaning	Function Code	Meaning
01	No Operation	53	Write Check Header and Data Command
03	Unload Command (RP-only)	55	Physical Write Check Header and Data Command*
05	Seek Command	61	Write Data Command
07	Recalibrate Command	63	Write Header and Data Command
11	Drive Clear Command	65	Physical Write Header and Data Command*
13	Release Command	71	Read Data Command
15	Offset Command		
17	Return-to-Centerline Command		
21	Read-In Preset Command		
23	Pack Acknowledge Command		

Function Code	Meaning	Function Code	Meaning
31	Search Command	73	Read Header and Data Command
37	Transparent ECC Correction Command*	75	Physical Read Header and Data Command*
41	Word Count Equals Sector Count Command*	77	Format Command*
51	Write Check Data Command		

* Extended (see subsection 5.5).

Go (GO) - Bit 00

This GO bit must be set to cause the SC72/BX disk controller to respond to a command. The GO bit is reset after command termination.

4.3.3 WORD COUNT REGISTER (RPWC/RMWC) 17776702

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Two's Complement Word Count

Register RPWC/RMWC is loaded with the two's complement of the number of data words to be transferred to or from the Main Memory. Register RPWC/RMWC is incremented by one after each word is transferred, and it can accommodate 65,536 words. Register RPWC/RMWC is not cleared by Initialize (INIT) or Controller Clear (CLR) RPCS2/RMCS2 bit 05.

4.3.4 UNIBUS ADDRESS REGISTER (RPBA/RMBA) 17776704

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Memory Address

Register RPBA/RMBA is initially loaded (written into) with the low-order 16 bits of the memory address for a Data Transfer operation. The low-order bit (00) is always forced to zero state. Register RPBA/RMBA is incremented by two after transfer of a word to or from the memory, unless the BAI bit (RPCS2/RMCS2 bit 03) is set. This RPBA/RMBA register is cleared by INIT or CLR.

4.3.5 DISK ADDRESS REGISTER (RPDA/RMDA) 17776706

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Track Address

Sector Address

Register RPDA/RMDA is used to address the sector and track on the selected disk where a Data Transfer operation is to be performed. Register RPDA/RMDA can be loaded only as a word. It is incremented each time a sector of data is transferred; therefore, consecutive sectors or blocks of data are automatically addressed when the word count indicates that more than one sector or block of data are to be transferred. At the end of a Data Transfer operation, register RPDA/RMDA contains the address of the sector that follows the last sector involved in the Data Transfer operation.

Register RPDA/RMDA contains a sector counter that provides up to 256 sectors per track. It also contains a track counter which is incremented by one every time the sector counter overflows its maximum count. When the sector address and the track address reach their maximum counts, they are reset to zero and the content of register RPDC/RMDC is incremented by one. The Invalid Address Error (IAE) bit (RPER1/RMER1 bit 10) is set if the address in register RPDA/RMDA is not valid when a Data Transfer, Seek, or Search command function is initiated. The maximum track and sector addresses are obtained from the selected configuration (see Appendix A, Tables A-2, A-5, and A-8).

4.3.6 CONTROL/STATUS REGISTER TWO (RPCS2/RMCS2) 17776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
-															
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0
-															

Register RPCS2/RMCS2 can be read from or written to under program control. It is used to store the current disk drive Unit Select code and the operational status of the SC72/BX disk controller. Register RPCS2/RMCS2 can also initiate a Controller Clear operation. All bits of this register, except bit 06, are cleared by an INIT or a CLR condition.

Data Late (DLT) - Bit 15

Normally, this Read-only bit cannot be set because of the 14-sector buffer in the SC72/BX disk controller. It can be set by accessing registers RPDB/RMDB without the appropriate status bit (RPCS2/RMCS2 bit 07 or 06) set to logic one state.

Write Check Error (WCE) - Bit 14

This Read-only bit is set when the SC72/BX disk controller is performing a Write Check operation and a word read from the selected disk does not match the corresponding word in memory. When the mismatch occurs, disk reading terminates and the WCE bit is set. The memory address, displayed in register RPBA/RMBA, is the address of the double word that follows the word which did not match (if bit BAI in this register is not set). The mismatched data word on the disk is displayed in register RPDB/RMDB.

Bus Parity Error (UPE) - Bit 13

This Read-only bit is set if a Parity error occurs in the memory while the SC72/BX disk controller is performing a Write command or a Write Check command. When the error occurs, register RPBA/RMBA contains the address of the double word that follows that word in which the Parity error occurred (if bit BAI in this register is not set).

Nonexistent Drive (NED) - Bit 12

This Read-only bit is set when the program reads from or writes to a device register that is associated with a disk drive (selected by bits U2, U1, and U0) which is not recognized because there exists one or more of the following conditions:

- a. The disk drive has the wrong Identification Code plug
- b. The disk drive has not been powered up
- c. The addressed disk drive is nonexistent.

Nonexistent Memory (NEM) - Bit 11

This Read-only bit is set when the SC72/BX disk controller is performing an NPR Data Transfer operation and the memory does not respond within 10 microseconds. The Memory Address displayed in register RPBA/RMBA is the address of the double word that follows the memory location that is causing the error.

Program Error (PGE) - Bit 10

This Read-only bit is set when the program attempts to initiate a Data Transfer operation while the SC72/BX disk controller is currently performing a Data Transfer operation.

Missed Transfer (MXF) - Bit 09

This Read-only bit is set if a Data Transfer operation cannot be executed; i.e., register RPDS/RMDS ERR bit 14 set to logic one state.

Massbus Data Bus Parity (MDPE) - Bit 08

This Read-only bit is always reset to logic zero state.

Output Ready (OR) - Bit 07

This Read-only bit is set when a word that can be read by the program is present in register RPDB/RMDB. Any attempt to read the contents of register RPDB/RMDB before OR is asserted causes a DLT error.

Input Ready (IR) - Bit 06

This Read-only bit is always set to the logic one state.

Controller Clear (CLR) - Bit 05

When a logic one state is written into this Write-only bit position, the SC72/BX disk controller is initialized. This bit is always read as a zero.

Parity Test (PAT) - Bit 04

This Read/Write bit has no effect on any operation of the SC72/BX disk controller. (It is used only for diagnostic compatibility.)

Bus Address Increment Inhibit (BAI) - Bit 03

When this Read/Write bit is set, the SC72/BX disk controller does not increment registers RPBA/RMBA during execution of a Data Transfer operation. If set, BAI causes all data words to be read from or written into the same memory location.

Unit Select (U2, U1, and U0) - Bits <02:00>

These Read/Write bits select one of eight disk drives for communicating with the PDP-11/70 CPU. The Unit Select bits can be changed at any time without interfering with the current operations. Unit Select bit codes are listed in the following table:

		Bit			
		02	01	00	
		U2	U1	U0	Unit
-					-
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	1	0	0	0	4
	1	0	0	1	5
	1	1	0	0	6
	1	1	0	1	7
-					-

4.3.7 DRIVE STATUS REGISTER (RPDS/RMDS) 17776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
-	ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0 OFM
-															-

This Read-only register contains various status indicator bits for the disk drive selected by the Unit Select number in register RPCS2/RMCS2.

Attention Active (ATA) - Bit 15

An Attention condition sets the ATA bit in this register and in the Attention Summary register (RPAS/RMAS). This bit is cleared by the INIT or CLR signals, by loading a command with the GO bit (RPCS1/RMCS1 bit 00) set, or by loading a one-bit in register RPAS/RMAS, in the bit position correlating to the Unit Select number of the particular disk drive. This last-mentioned method of clearing the ATA bit does not clear the error-indicator bits in any register.

An Attention condition is caused by one or more of the following conditions:

- a. An error bit set in the Error registers
- b. Completion of a Positioning operation
- c. Change of state of the MOL bit (RPDS/RMDS bit 12)
- d. Dual Port mode of operation with the disk drive presently available if previously not available
- e. Correct sector identification for the Search command
- f. Completed execution of the Unload command. (RP only).

Error (ERR) - Bit 14

Set (or asserted) when one or more of the errors in Error registers RPER1/RMER1, RPER2, or RMER2/RPER3 for a selected disk drive is set. While ERR is asserted, all commands, except Drive Clear are not accepted by the SC72/BX disk controller.

Positioning In Progress (PIP) - Bit 13

Set when one of the following Positioning commands is accepted: Seek, Offset (RP disk drives only), Return-To-Centerline (RP disk drives only), Recalibrate, and Search. Also set during execution of Implied Seek and Mid-Transfer Seek operations that are executed as part of a Data Transfer command. For RM02/03/05 disk drive emulations, set if MOL bit equals logic zero state. Cleared when the moving function is completed at the time that bits DRY and ATA are set.

Medium On-Line (MOL) - Bit 12

Set when the Unit Ready line from the disk drive is asserted. Setting this bit indicates the disk drive is up to speed, the heads are positioned over the recording tracks, and no Fault condition exists within the disk drive. Cleared when the spindle is powered down or when the disk drive goes off line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the Write Protected line from the disk drive is asserted (enabled by a switch located on the disk drive): A Write command to a disk drive when WRL is set causes the Write-Lock Error (WLE) bit (RPER1/RMER1 bit 11) to be set. For RM80 disk drive emulations, WRL is set if MOL is in the logic zero state.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been written to or read from. Cleared when a new Write command to register RPDA/RMDA is received.

When LST is set, register RPDA/RMDA is reset to all zeros and register RPDC/RMDC increments by one to the first illegal cylinder address. If register RPWC/RMWC does not contain all zeros, the operation is aborted, causing status bit AOE (RPER1/RMER1 bit 09) to be set. Set AOE bit indicates the desired cylinder register overflowed during a Read or Write operation.

Programmable (PGM) - Bit 09

Set when Dual Port or Dual Access operation is enabled.

Drive Present (DPR) - Bit 08

Set if the SC72/BX disk controller has seized the addressed disk drive. Reset when the other SC72/BX disk controller has seized the addressed disk drive. DPR status is a reflection of the DVA bit (RPCS1/RMCS1 bit 11).

Drive Ready (DRY) - Bit 07

Set at completion of every command execution. Cleared at initiation of every command execution. When set, DRY indicates the disk drive is ready to accept a command. If a mechanical movement command was initiated, the ATA bit is also set when DRY is set. This bit is the complement of the GO bit used by the disk drive.

Volume Valid (VV) - Bit 06

Set by Pack Acknowledge or Read-In Preset command. Cleared whenever the disk drive cycles up from the OFF state. When reset, VV indicates the disk drive has been off line and that a disk pack may have been changed.

Offset Mode (OFM) - Bit 00

This bit is enabled only with RM disk drive emulations. Set by Offset command to indicate a Read operation is to be done with the heads in the Offset position as determined by the condition of bit

OFS (RMOF bit 07). Cleared by any one of the following commands: Read-In Preset, Return-To-Centerline, Recalibrate, Write, or Mid-Transfer Seek.

4.3.8 ERROR REGISTER ONE (RPER1/RMER1) 17776714

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF
-----	-----	-----	-----	-----	-----	-----	------	-----	-----	-----	-----	-----	-----	-----	-----

Register RPER1/RMER1 is a Read/Write register for storing the error status of the disk drive which has its Unit Select number stored in register RPCS2/RMCS2. Register RPER1/RMER1 contents can be written only as a word. Any attempt to write a byte causes an entire word to be written. If the program attempts to write into this register while the disk drive is busy, the RMR error bit (RPER1/RMER1 bit 02) is set, and the contents of register RPER1/RMER1 are not otherwise modified. Writing zeros into the bit positions of this register should not be used as the normal method of clearing errors; use the Drive Clear command instead.

Data Check (DCK) - Bit 15

Set during a Read operation when the ECC hardware detects an ECC error. The Read operation terminates when the contents of the current sector being read are transferred. If the Error Correction Code Inhibit (ECI) bit (RMOF/RPOF bit 11) is not set, the SC72/BX disk controller goes into the Error Correction process, and the RDY bit is not set until the end of that process. If the ECI bit is set, the Error Correction process is inhibited and the Data Transfer operation terminates immediately.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the Unsafe and Seek Incomplete error conditions in register RMER2/RPER3. When UNS is set, correct results on any commanded operation cannot be guaranteed. Some faults must be cleared by manual intervention at the addressed disk drive.

Operation Incomplete (OPI) - Bit 13

Set when a Read or Write command that involves a header search cannot find the addressed physical sector within three Index pulses. Also set during a Search operation when a sector count match is not made within three Index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. Also set if a Sector pulse occurs before the end of the Sector's data

field has been reached. When DTE is set, the GO bit is cleared and the RDY bit is set.

Write Lock Error (WLE) - Bit 11

Set when a Write command is issued to a Write-Locked disk drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in register RPDC/RMDC or RPDA/RMDA is invalid and a Seek, Search, or Data Transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when register RPDC/RMDC overflows during a Read or Write operation. Setting this bit indicates the address has exceeded the cylinder address limit. When AOE is set, the SC72/BX disk controller terminates the operation when the last sector of the last cylinder has been read from or written into.

Header CRC Error (HCRC) - Bit 08

Set when a CRC error is detected in the header. If a CRC error is detected during attempted execution of a Read or Write command, the SC72/BX disk controller does not complete the Read or Write operation and no data are transferred. If a CRC error is detected during attempted execution of a Read Header and Data command, or a Write Check Header and Data command, the contents of the entire sector are transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header which are read at the sector whose count is equal to the desired sector field of register RPDA/RMDA do not match the contents of registers RPDC/RMDC and RPDA/RMDA. If the HCE bit is set during execution of a Read or Write command, the SC72/BX disk controller does not perform any Data Transfer operation. If the HCE bit is set during attempted execution of a Read Header and Data command, or a Write Check Header and Data command, the entire sector is transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the Error Correction procedure indicates the error was a noncorrectable ECC error. When ECH is set, the DCK bit (RPER1/RMER1 bit 15) is also set.

Write Clock Fail (WCF) - Bit 05

This bit position normally contains a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in register RPOF/RMOF does not match bit 12 in word one of a sector's header. If FER is set, then bit HCE may or may not be set.

Parity Error (PAR) - Bit 03

This bit position normally contains a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when an attempt is made to write into any disk drive register, except register RPMR/RMMR1 or RPAS/RMAS, when the DRY bit (RPDS/RMDS bit 07) is in logic zero state. The disk drive continues to execute the command that is currently in progress.

Illegal Register (ILR) - Bit 01

This bit position normally contains a zero unless written into.

Illegal Function (ILF) - Bit 00

Set when the Function Code in register RPCS1/RMCS1 is illegal and the GO bit is set.

4.3.9 ATTENTION SUMMARY REGISTER (RPAS/RMAS) 17776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	ATA	ATA	ATA	ATA	ATA	ATA	ATA
									7	6	5	4	3	2	1

Register RPAS/RMAS can be read from or written into at any time. It allows the program to examine the Attention status of all disk drives by using only one Register Read operation. It also provides a means of resetting the Attention logic in a selected group of disk drives. The eight low-order bits of this register correlate to the ATA bits in register RPDS/RMDS of the disk drive that has the same Unit Select number as the bit position (ATA number) in this register.

The ATA bit in a disk drive can be reset by loading a one into the bit position that correlates to the Unit Select number of the disk drive. Loading a zero into the correlating bit position in this register has no affect upon the disk drive. For a program to use register RPAS/RMAS without losing status information, the program must use MOV instructions for all Write instructions to the register. An instruction that performs a Read-Restore operation (such as BIS) may cause bits that became asserted during the Read-Restore operation to be lost.

A persistent error, just like any error condition, causes the affected ATA bit that represents the selected disk drive to become reasserted. When such an event occurs, the attempts by the SC72/BX disk controller to clear the error cannot bring about the cleared error condition.

4.3.10 LOOK-AHEAD REGISTER (RPLA/RMLA) 17776720

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	Sector Counter						0	0	0	0	0	0

Register RPLA/RMLA contains the disk drive sector counter which always counts from zero to the maximum sector count selected in the disk drive . It is used to present the angular position of the disk, relative to the Read/Write heads for the disk whose logical disk drive unit number appears in register RPCS2/RMCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays.

4.3.11 DATA BUFFER REGISTER (RPDB/RMDB) 17776722

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data Buffer															

Register RPDB/RMDB provides a maintenance tool to check the data paths through the SC72/BX disk controller. The Output Ready (OR) and Input Ready (IR) (RPCS2/RMCS2 <07:06>, respectively) status indicator bits are provided so the programmer can determine when words can be read from or written to register RPDB/RMDB.

Register RPDB/RMDB is used as an access to the Silo Buffer for a DEC RH70 controller emulation. The SC72/BX disk controller has no Silo Buffer. All Write commands to this register are ignored. If a Write Check Error (WCE) occurs (RPCS2/RMCS2 bit 14 set), the data word read from the disk is placed in register RPDB/RMDB and the OR bit in register RPCS2/RMCS2 is set. Reading the contents of register RPDB/RMDB resets the OR bit in register RPCS2/RMCS2. Any further attempts to read the contents of register RPDB/RMDB creates a Data Late (DLT) error (RPCS2/RMCS2 bit 15 set).

4.3.12 MAINTENANCE REGISTERS 17776724

The Maintenance registers for RP and RM disk drive emulations are RPMR and RMMR1, respectively, but both use the same address.

4.3.12.1 Maintenance Register (RPMR)

The Maintenance mode is not supported for RP disk drive emulations, except if bit zero is set in the logic one state no Seek operations occur and all Data Transfer operations are bypassed.

4.3.12.2 Maintenance Register 1 (RMMR1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	MUR	MOC	MSER	MDF	0	0	MWP	0	0	DMD

Register RMMR1 is a Read/Write register that allows a program to simulate various signals from the disk for diagnostic testing of the SC72/BX disk controller. The DMD bit in this register must be set before any other bit has an effect on the SC72/BX disk controller. This register may be written into as a word or as a byte. Writing to register RMMR1 can occur at any time, regardless of the status of the disk drive. A Drive Clear or Controller Clear command resets all bits in this register to the zero state, except bit 03 which is always set.

Maintenance Unit Ready (MUR) - Bit 09

Set by a diagnostic program to simulate the Unit Ready signal from the disk drive.

Maintenance On Cylinder (MOC) - Bit 08

Set by a diagnostic program to simulate the On Cylinder signal from the disk drive.

Maintenance Seek Error (MSER) - Bit 07

Set by a diagnostic program to simulate the Seek Error signal from the disk drive.

Maintenance Drive Fault (MDF) - Bit 06

Set by a diagnostic program to simulate the Fault signal from the disk drive.

Maintenance Write Protect (MWP) - Bit 03

Set by a diagnostic program to simulate the Write Protect signal from the disk drive.

Diagnostic Mode (DMD) - Bit 00

Set by the diagnostic program to reconfigure the disk drive into the Maintenance mode. None of the other bits in this register have any affect on the SC72/BX disk controller unless the DMD bit is set to logic one state. Before a disk drive can be placed in the Maintenance mode, it must first be ready and not busy. No positioner motion is initiated for a Seek, Home, Search, or Implied Seek command, and all Data Transfer commands are ignored.

4.3.13 DRIVE TYPE REGISTER (RPDT/RMDT) 17776726

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Disk Drive Type Code							

Register RPDT/RMDT provides information about the type of disk drive that is selected.

Moving-Head (MOH) - Bit 13

Always set to indicate the disk drive is a moving-head device.

Dual Port Mode (DPM) - Bit 11

Set indicates the disk drive is operating in the Dual Port mode as enabled by switch SW4-6, or in Dual Access mode as enabled by switch SW4-7.

Drive Type Code - Bits <07:00>

These bits code an octal number that specifies the type of selected disk drive. The octal number and corresponding disk drive type are listed in the following table:

20 = RP04	21 = RP05	22 = RP06		
24 = RM03	25 = RM02	26 = RM80	27 = RM05	

4.3.14 SERIAL NUMBER REGISTER (RPSN/RMSN) 17776730

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW4	SW4	SW4	SW4	SW4	SW4	SW4	SW4	Firmware Rev. Port Number							
-8	-7	-6	-5	-4	-3	-2	-1								

Register RPSN/RMSN was provided to distinguish a particular disk drive from similar disk drives attached to the DEC controller by means of a four-decade serial number. In the SC72/BX disk controller, it consists of the controller port number to which the disk drive is attached, the firmware revision level, and the eight SW4 DIP switch settings (A-Board).

4.3.15 OFFSET REGISTER (RPOF/RMOF) 17776732

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
X	0	0	FMT	ECI	HCI	SSEI	0	OFS	X	OFS	OFS	X	X	X	X
			16					7		5	4				

Register RPOF/RMOF contains a format-select bit, three inhibit bits, the disk drive offset direction bit, and two offset function bits. The offset direction bit determines if a Read operation is to be done with the heads and/or PLO advanced or retarded from the normal centerline position on the particular track addressed. Bit 07 is not exclusive to RP disk drives, but bits 05 and 04 are.

- a. In RP disk drive emulations, the status of bits OFS5 and OFS4 determines the actual offset. Bits <12:10> are cleared by a Read-In Preset command. Bits <07:00> are reset by the INIT signal and the Drive Clear command. Bits marked 'X' are Read/Write bits that have no affect on operation of the SC72/BX disk controller and can therefore be set to logic one state or reset to logic zero state.
- b. In RM disk drive emulations, bits <15:00> are cleared by a Read-In Preset command. Bit SSEI is used only in RM80 disk drive emulations.

Format Bit (FMT16) - Bit 12

Set for 16-Bit mode and reset for 18-Bit mode. When reset, the SC72/BX disk controller operates with two fewer sectors per track; i.e., if track has 32 sectors in 16-Bit mode, it has 30 sectors in 18-Bit mode. The state of this bit should always be logic one because the SC72/BX disk controller handles only the 16-bits/word format.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit Header Compare and CRC Check. With HCI set, the SC72/BX disk controller depends only on the sector count for sector identification. Emulex recommends the HCI bit should be reset during performance of a Write operation.

Skip-Sector Error Inhibit (SSEI) - Bit 09

For RM80 disk drive emulations only. Set to inhibit Skip-Sector errors during a Data Transfer operation. When set, the disk drive operates with one extra sector per track. Reset whenever a Data Transfer command increments the contents of register RMDA to a new track address. This bit cannot be set unless bit FMT16 is already set.

Offset Direction (OFS7) - Bit 07

The state of this bit is established under software control to select the direction of positioner or Phase-Locked Oscillator (PLO) offset. Logic one state retards the heads and logic zero state

advances the heads. Information about the amount of offset, with respect to track width, that is provided by the disk drive should be available in the disk drive technical manual provided by the disk drive manufacturer.

PLO Offset Enable (OFS5) - Bit 05

Set enables the data strobe advance/retard. This bit is functional with RP disk drive emulations only. There is no PLO offset with RM disk drive emulations.

Positioner Offset Enable (OFS4) - Bit 04

Set enables the positioner offset. This bit is functional with RP disk drive emulations only. In RM disk drive emulations, positioner offset is implied.

4.3.16 DESIRED CYLINDER REGISTER (RPDC/RMDC) 17776734

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Desired Cylinder Address

Register RPDC/RMDC contains the address of the cylinder to which the positioner is to move the heads on the disk drive. It is cleared by the Read-In Preset command. After an Initial Load operation, the value in register RPDC/RMDC is incremented by one whenever register RPDA/RMDA is reset to zero during execution of a Data Transfer operation. When register RPDC/RMDC is incremented, and register RPWC/RMWC contents are not equal to zero, a Mid-Transfer Seek operation is initiated by the SC72/BX disk controller.

The Invalid Address Error (IAE) bit (RPER1/RMER1 bit 10) is set if this register contains a Cylinder Address greater than the largest addressable cylinder when the GO bit (RPCS1/RMCS1 bit 00) is asserted.

4.3.17 CURRENT CYLINDER REGISTER AND HOLDING REGISTER 17776736

The Current Cylinder register is used in RP disk drive emulations and the Holding register is used in RM disk drive emulations. Both registers have the same address.

4.3.17.1 Current Cylinder Register (RPCC)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

Current Cylinder Address

Register RPCC is a Read-only register that reflects the current cylinder address of the selected disk drive. The Current Cylinder Address contained in this register should be equal to the contents of register RPDC at the end of a Seek operation. Register RPCC can, however, be used for other functions:

- a. The configured size (capacity) of the selected disk drive can be read if the register has been written into with one of the following values:

100027 = Maximum Cylinder Address
 100030 = Maximum Track Address
 100031 = Maximum Sector Address (FMT16 bit **MUST** be set)

- b. Writing a 177777g into the register can enable execution of several extended commands (see subsection 5.5) when the Function Codes for those commands are loaded into register RPCS1. The enabled condition remains set until either execution of the Data Transfer command is ended or some data other than 177777g is loaded into register RPCC.

4.3.17.2 Holding Register (RMHR)

15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
---	---	---	---	---	---	---	---	---	---	---	---	---	---	---	---

Register RMHR is a Read-only register that always returns all zeros when read, except when there occurs the following conditions:

- a. The configured size (capacity) of the selected disk drive can be read if the register has been written into with one of the following values:

100027 = Maximum Cylinder Address
 100030 = Maximum Track Address
 100031 = Maximum Sector Address (FMT16 bit **MUST** be set)

- b. Writing a 177777g into the register can enable execution of several extended commands (see subsection 5.5) when the Function Codes for those commands are loaded into register RMCS1. The enabled condition remains set until some data other than 177777g is loaded into register RMHR.

4.3.18 ERROR REGISTER TWO AND MAINTENANCE REGISTER TWO 17776740

The Error register, supported at this address, is used only with RP disk drive emulations. The Maintenance register, supported at this address, is used only with RM disk drive emulations.

4.3.18.1 Error Register Two (RPER2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	PLU	0	IXE	0	MDS	DCU	0	0	0	0	0	0	0	0

Register RPER2 is a Read/Write register that contains status information about the performance of that disk drive whose Unit Select number is encoded in register RPCS2. This register may be written only as a word. If any bit is set in this register, the ERR bit (RPDS bit 14) is also set. Writing zeros into this register should not be used as the normal way of clearing set error bits; the Drive Clear command or Controller Clear command should be used instead. If the program attempts to write into this register while the disk drive is busy, the RMR bit (RMER1 bit 02) is set and the Write command is ignored.

PLU Unsafe (PLU) - Bit 13

Set if the SC72/BX disk controller does not detect at least 16 Servo Clock pulses within 3.0 microseconds.

Index Error (IXE) - Bit 11

Set when the SC72/BX disk controller detects more than 128 Sector pulses without an Index pulse, when the system is configured with the Sector and Index pulses on the B-Cable.

Multiple Drive Select (MDS) - Bit 09

Set if more than one disk drive responds to a logical disk drive unit address on the A-Cable.

DC Power Unsafe (DCU) - Bit 08

Set if the -5Vdc power supply to the cable drivers and receivers is not within the voltage tolerance limits.

4.3.18.2 Maintenance Register Two (RMMR2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
11777 ₈															

Register RMMR2 is a Read-only register that returns a 11777₈ when read while the disk drive is connected and selected via the contents of register RMCS2.

4.3.19 ERROR REGISTER THREE AND ERROR REGISTER TWO 17776742

Error Register Three supports RP disk drive emulations only, and Error Register Two supports RM disk drive emulations only. Both registers use the same address.

4.3.19.1 Error Register Three (RPER3)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OCYL	SKI	OPE	0	0	0	0	0	0	ACL	0	0	URW	0	0	0

Register RPER3 is a Read/Write register that contains status information about the electromechanical performance of the disk drive whose Unit Select number is encoded in register RPCS2. This register is to be written only as a word. If any bit is set in this register, the ERR bit (RPDS bit 14) is also set, and in some instances the UNS bit (RPER1 bit 14) is also set. Writing zeros into this register should not be used as the normal way of clearing set error bits. A Drive Clear command or a Controller Clear command should be used instead. If the program attempts to write into this register while the disk drive is busy, the RMR bit (RPER1 bit 02) is set and the Write command is ignored.

Off-Cylinder (OCYL) - Bit 15

Set if an Off-Cylinder error indication occurs at the completion of a Seek operation. Set condition of this bit sets the UNS bit (RPER1 bit 14).

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the disk drive. Also sets the UNS bit (RPER1 bit 14). The SC72/BX disk controller automatically issues a Fault Clear signal and a Return-To-Zero (RTZ) signal to the disk drive when a Seek error is detected. The error is posted at the completion of the RTZ function.

Operator Plug Error (OPE) - Bit 13

Set whenever the Identification Address plug for the disk drive is removed and then reinstalled.

AC Power Unsafe (ACL) - Bit 06

Set if an ACLO signal is received from the Unibus.

Unsafe to Read or Write (URW) - Bit 03

Set if a Fault status indication is received from the disk drive. Also sets the UNS bit (RPER1 bit 14). The SC72/BX disk controller automatically issues a Fault Clear command and a Return-to-Zero (RTZ) command to the disk drive when a Fault status indication is

received from the disk drive. The error is posted at the completion of the RTZ function.

4.3.19.2 Error Register Two (RMER2)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	DCU	DVC	ACU	SSE	0	DPE	0	0	0

Register RMER2 is a Read/Write register that contains status information about the electromechanical performance of that disk drive whose Unit Select number is encoded in register RMCS2. This register may be written as either a word or a byte. If any bit is set in this register, the ERR bit (RMDS bit 14) is also set, and in some instances the UNS bit (RMER1 bit 14) is set. Writing zeros into this register should not be used as the normal way of clearing set error bits. A Drive Clear command or a Controller Clear command should be used instead. If the program attempts to write into this register while the disk drive is busy, the RMR bit (RMER1 bit 02) is set and the Write command is ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the SC72/BX disk controller detects a zero in bit 14 or 15 of the first header word and the HCI bit (RMOF bit 10) is in the logic zero state.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the disk drive. Also sets the UNS bit (RMER1 bit 14). The SC72/BX disk controller automatically issues a Fault Clear signal and a Return-To-Zero (RTZ) signal to the disk drive whenever a Seek Error is detected. The error is posted at the completion of the RTZ function.

Operator Plug Error (OPE) - Bit 13

Set whenever the Identification Address plug for the disk drive is removed and then reinstalled.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a disk drive while the MOL bit (RMDS bit 12) is in the logic zero state. Also set whenever any command, except Read-In Preset or Pack Acknowledge is issued to a disk drive while the VV bit (RMDS bit 06) is in the logic zero state.

Loss of Sector Clock (LSC) - Bit 11

Set when the SC72/BX disk controller detects more than 128 Sector pulses without detecting an Index pulse, while system is configured with Sector and Index pulses on the B-Cable.

Loss of Bit Clock (LBC) - Bit 10

Set if the SC72/BX disk controller does not detect at least 16 Servo Clock pulses within three microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one disk drive responds to a logical disk drive unit address on the A-Cable. This bit cannot be set by a programmed instruction.

DC Power Unsafe (DCU) - Bit 08

Set if the -5Vdc power supply to the cable drivers and receivers is not within proper voltage tolerances. This bit cannot be set by a programmed instruction.

Device Check (DVC) - Bit 07

Set if a Fault status indication is received from the disk drive. Also sets the UNS bit (RMER1 bit 14). The SC72/BX disk controller automatically issues a Fault Clear instruction and a Return-To-Zero (RTZ) instruction to the disk drive whenever a Fault status is detected. The error is posted at the completion of the RTZ function.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO signal is received from the Unibus.

Skip-Sector Error (SSE) - Bit 05

For RM80 disk drive emulations only. Set whenever bit 13 of Header Word One is set and the SSEI bit (RMOF bit 09) is reset. This error indicates the sector has been skipped and the data resides in the next sector.

Data Parity Error (DPE) - Bit 03

This bit position normally contains a zero unless written into.

4.3.20 ECC POSITION REGISTER (RPEC1/RMEC1) 17776744

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

Register RPEC1/RMEC1 is a Read-only register that contains the position of the error pattern as determined by the ECC Error Correction procedure. The error position is the number of bit positions from the beginning of the data field in the sector to (and including) the right-most bit position of the error pattern that is stored in register RPEC2/RMEC2. If the detected error is

not correctable by using the ECC Error Correction procedure, bit ECH (RPER1/RMER1 bit 06) is set.

4.3.21 ECC PATTERN REGISTER (RPEC2/RMEC2) 17776746

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

Register RPEC2/RMEC2 is a Read-only register that contains the 11-bit error correction pattern obtained from the ECC Error Correction procedure. A one in any bit position in the Error Pattern indicates a bit of the data in memory from the last read sector which is in error. The Error Pattern may straddle two 16-bit words in memory. The bit displacement to the right-most bit of the Error Pattern is determined by the bit count in register RPEC1/RMEC1. The actual correction is done by an exclusive-OR of the Error Pattern and the data in memory.

4.3.22 BUS ADDRESS EXTENSION REGISTER (RPBAE/RMBAE) 17776750

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	
0	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16

Register RPBAE/RMBAE contains the upper six bits of the memory address which is combined with the lower 16 bits in register RPBA/RMBA to form the complete 22-bit address. The six-bit field is incremented each time register RPBA/RMBA overflows. Bits A17 and A16 are replicated in register RPCS1/RMCS1 bits <09:08>, respectively. Writing in either register bit positions affects both registers.

4.3.23 CONTROL/STATUS REGISTER THREE (RPCS3/RMCS3) 17776752

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
APE	DPE	DPE	WCE	WCE	DBL	0	0	0	IE	0	0	IP3	IP2	IP1	IP0
	HI	LO	HI	LO											

Register RPCS3/RMCS3 can be read from or written to by program control. It is used to store cache status information and the Inverted Parity check bits.

Address Parity Error (APE) - Bit 15

Set if a Parity error is detected on the address portion of the Cache bus interface.

Data Parity Errors (DPE HI and DPE LO) - Bits <14:13>

Set if Parity error is detected in data read from memory when performing a Write or Write Check command. When either of these bits is set, the UPE bit (RPCS2/RMCS2 bit 13) is also set.

Write Check Errors (WCE HI and WCE LO) - Bits <12:11>

Set if data fails to compare between memory and the disk when performing a Write Check command. When either of these bits are set, the WCE bit (RPCS2/RMCS2 bit 14) is also set.

Double Word (DBL) - Bit 10

Set if the last Data Transfer operation to memory was a double-word operation.

Interrupt Enable (IE) - Bit 06

When set (IE equals one), an Interrupt request may be sent to the PDP-11/70 CPU (see subsection 4.1.2). This bit is also replicated in bit 06 of register RPCS1/RMCS1. Writing into this bit position in either register RPCS1/RMCS1 or RPCS3/RMCS3 affects both registers. Cleared when the Interrupt Vector Address is requested by the PDP-11/70 CPU. If the program writes a zero into the IE bit position, pending Interrupt requests are cancelled.

Inverted Parity (IP3 through IP0) - Bits <03:00>

These bits are used to invert and test Cache Bus parity. Setting any one of these bit positions causes the corresponding byte to have its parity logic inverted during Write and Write Check operations. The bit states correlate to the four-byte Cache bus Data Transfer operations as listed in the following table:

Bit	Parity Logic
IP0	Even word, even byte
IP1	Even word, odd byte
IP2	Odd word, even byte
IP3	Odd word, odd byte

If a Data Parity Error (DPE) or a Write Check Error (WCE) occurs during a 32-bit Cache Bus Data Transfer operation (DBL equals one), register RPBA/RMBA is then either plus two or plus four bytes ahead of the word that caused the error, and register RPWC/RMWC must have been incremented once or twice after the error occurred. The user must examine the contents of register RPCS3/RMCS3 to determine the actual address of the error. The address of the error is established by the following conditions:

- a. If DBL equals zero, the contents of register RPBA/RMBA equals the actual address plus two.

- b. If DBL equals one and either WCE LO or DPE LO equals one, the contents of register RPBA/RMBA equals the actual address plus four.
- c. If DBL equals one and either WCE HI or DPE HI equals one, contents of register RPBA/RMBA equals actual address plus two.

BLANK

5.1 INTRODUCTION

The disk drive is selected by the Unit Select code bits in register RPCS2/RMCS2. Operations to be performed by the selected disk drive are specified by the Function Code bits in register RPCS1/RMCS1. (The function code for the command is enclosed in parenthesis after the subsection sidehead.) Initiation of the specified disk drive operation is begun when the GO bit in register RPCS1/RMCS1 is asserted (set). Commands and corresponding Function Codes (always odd because the GO bit must be asserted to execute the command) are described in this section. This section is divided into six subsections, as listed in the following table:

Subsection	Title
5.1	Introduction
5.2	Data Transfer Commands
5.3	Positioning Commands
5.4	Housekeeping Commands
5.5	Optional Commands
5.6	Automatic Skip-Sector Feature

Some commands are divided into two descriptions; one describes its function with RP disk drive emulations, and one describes its function with RM disk drive emulations. Commands so divided can be distinguished by the fourth-level sidehead format.

5.2 DATA TRANSFER COMMANDS

Data Transfer commands involve transfer of information to or from the disk and are designated by Function Codes 51 through 77.

All Data Transfer commands have Seek and Search (for sector) functions implied. When the addressed cylinder number does not equal the current cylinder number during execution of the Data Transfer command, a Seek command is issued to position the heads at the addressed cylinder. The SC72/BX disk controller then searches the addressed track for the addressed sector. When the addressed sector is found, a match of the sector header must be made before the Data Transfer operation is started. Three commands do not require sector header matching before the Data Transfer operation is started: Write Header and Data command, Read Header and Data command, and Write Check Header and Data command. If the Header Compare Inhibit (HCI) bit in register RPOF/RMOF bit position 10 is set, the header is not compared or checked; i.e., the Data Transfer

operation is started, based on the pre-recorded sector pulses, as is done in executing the Write Header and Data command. Header errors are not reported when the HCI bit is set. If a header error is detected while the HCI bit is cleared, the Data Transfer operation is aborted. The Read Header and Data command aborts only the transfer of data that follows the sector that caused the error. The Write Check Header and Data command operates like the Read Header and Data command.

Desired cylinder, track, and sector addresses are updated after transfer of the contents of a sector has been completed. At the end of the Data Transfer operation, the SC72/BX disk controller and disk are prepared to transfer the contents of the next sequential sector. This preparation (set up) allows multiple sector Data Transfer operations and spiral Data Transfer operations across tracks and cylinders. When the specified cylinder address changes during a Data Transfer operation, the Implied Seek operation is performed and is called a Mid-Transfer Seek operation.

The header size is two words for RM disk drive emulations, and four words for RP disk drive emulations. In all sectors, the data field capacity (size) is 256 words.

Six types of Data Transfer commands are described in this subsection.

5.2.1 WRITE CHECK DATA COMMAND (51)

This command reads data from the selected disk drive and compares that data, on a word-by-word basis, with the data obtained from memory. If the data comparison fails, the WCE error status bits are set and the command is terminated immediately (see subsections 4.3.6 and 4.3.23).

5.2.2 WRITE CHECK HEADER AND DATA COMMAND (53)

This command reads the contents of the header field and data field from the selected disk drive and compares those contents, on a word-by-word basis, with data obtained from memory. If the header or data comparison fails, the WCE error status bits are set and the command is terminated immediately.

5.2.3 WRITE DATA COMMAND (61)

This command writes 256 words, obtained from memory, into the data field of the selected sector. A two-word ECC is appended to each sector. If the word count in register RPWC/RMWC goes to zero while the data field in the sector is being written, the rest of the sector is filled with zeros. After data have been transferred to the data field of that sector, the word count in register RPWC/RMWC is checked, and if that word count is not zero, the Data Transfer operation is continued to the data field of the next sector; otherwise the Write Data command is terminated.

5.2.4 WRITE HEADER AND DATA COMMAND (63)

This command causes words obtained from memory to be written into the header field and the data field of the selected sector. A one-word CRC is appended to each header field, and a two-word ECC is appended to each data field. If the word count in register RPWC/RMWC goes to zero while the sector is being written, the rest of the sector is filled with zeros. After data have been transferred to the header and data fields of that sector, the word count in register RPWC/RMWC is checked, and if that word count is not zero, the Data Transfer operation is continued to the header and data fields of the next sector; otherwise the Write Header and Data command is terminated.

5.2.5 READ DATA COMMAND (71)

This command reads the contents of the 256-word data field from the selected sector and transfers that data to memory. When transfer of data from that sector has been completed, the ECC is checked to verify that data read from the disk was free from errors. If a data error occurred, and the ECI bit in register RPOF/RMOF is reset, the ECC correction procedure is initiated to determine whether the error is or is not correctable. When the ECC correction procedure is finished, the Read Data command is terminated to allow software to apply the correction information. If no data errors occurred, the word count in register RMWC is checked; if not zero, the Read Data operation is repeated by continuing on to read the contents of the next sector. If the word count in register RPWC/RMWC goes to zero during the reading of data from any addressed sector, the rest of the sector contents are not transferred.

5.2.6 READ HEADER AND DATA COMMAND (73)

This command causes the contents of the header field and the data field in the selected sector to be transferred to memory. When the Data Transfer operation from that sector has been completed, the ECC is checked to verify that data read from the disk was free from errors. If a data error occurred, and the ECI bit in register RPOF/RMOF is reset, the ECC correction procedure is initiated to determine whether the error is or is not correctable. When the ECC correction procedure is finished, the Read Header and Data command is terminated to allow software to apply the correction information. If no data errors occurred, the word count in register RPWC/RMWC is checked; if not zero, the Read Header and Data operation is repeated by continuing on to read the contents of the header and data fields in the next sector. If the word count in register RPWC/RMWC goes to zero during the reading of data from any addressed sector, the rest of the sector contents are not transferred.

5.3 POSITIONING COMMANDS

Positioning commands cause mechanical movement to position the heads over the disk pack. They require miliseconds for completion. When a Position command is initiated, the SC72/BX disk controller sets the PIP bit and resets the DRY bit (RPDS/RMDS bits 13 and 07,

respectively). When a commanded Positioning operation is completed, the SC72/BX disk controller resets the PIP and GO bits, and sets the DRY and ATA bits.

Six types of Positioning commands are described in this subsection.

5.3.1 UNLOAD COMMAND (03)

This command is valid for RP disk drive emulations only. The command is intended to cause the disk drive to retract its heads and stop the spindle motion. This operation cannot be executed with disk drives that use the SMD-type interface, so the command is simulated. A three-second cycle-down/cycle-up event sequence is generated in the SC72/BX disk controller. At the end of the event sequence, the SC72/BX disk controller resets the GO bit, resets the VV bit, sets the MOL, DRY, and ATA bits and performs a Drive Clear function. The MOL bit is reset for the duration of the cycle-down/cycle-up event sequence.

5.3.2 SEEK COMMAND (05)

This command causes the heads to be moved to the cylinder address specified by the contents of register RPDC/RMDC. When the SC72/BX disk controller detects the Seek command while the GO bit is set, it sends the cylinder address to the corresponding disk drive. Any attempt to Write into register RPDC/RMDC while the Seek command is being executed causes the RMR error status bit in register RPER1/RMER1 to be set. The contents of register RPDC/RMDC are not modified. When the commanded Seek operation is completed, the ATA and DRY bits in register RPDS/RMDS are set and the GO bit in register RPCS1/RMCS1 is reset. If the disk drive is unable to complete the commanded Seek operation within 500 milliseconds, or if it has moved the head carriage to a position outside the recording field, the disk drive asserts the Seek Error signal and the SC72/BX disk controller sets the SKI error status bit in register RPER2/RMER2 and the ERR, ATA, and DRY bits in register RPDS/RMDS. The SC72/BX disk controller automatically issues a Fault Clear instruction and a Return-To-Zero instruction to the disk drive so that the Drive Clear command can clear the error condition.

5.3.3 RECALIBRATE COMMAND (07)

This command causes the selected disk drive to position its heads over cylinder zero. A Return-To-Zero instruction is automatically performed with each Head Load operation sequence, and whenever a Fault or Seek Error signal is detected. This command also clears the OFM bit (RMDS bit 00).

5.3.4 OFFSET COMMAND (15)

The Offset command functions differ for RP and RM disk drive emulations.

5.3.4.1 Offset Command for RP Disk Drive Emulations

The Offset command causes the positioner to be offset by an incremental amount from the centerline of the addressed track and/or it causes the data strobe to be advanced or retarded by a small amount when the next Read operation is to be executed. This Offset operation offers additional data recovery attempts beyond the capability provided by the ECC Error Correction procedure. An Offset command uses the contents of register RPOF to determine the offset condition. When the Offset operation is done, the ATA bit is set to indicate that a Read command can be issued. The actual offset is simulated during this time, and instead occurs at the beginning of the Read command.

Register RPOF contents, except bits FMT16, ECI, and HCI, are cleared and the disk drive leaves the Offset state by any one of the following methods:

- a. Seek to another cylinder by means of a Seek command or Mid-Transfer Seek operation.
- b. A Write command.
- c. A Return-To-Centerline command.

5.3.4.2 Offset Command for RM Disk Drive Emulations

This Offset command causes the OFM bit (RMDS bit 00) to be set. Subsequent Read operations are done with the heads offset from the centerline of the track in the direction specified by the state of bit OFS7 (RMOF bit 07). This operation offers additional data recovery attempts beyond the capabilities provided by the ECC Error Correction procedure when an ECC error is detected. If an ECC hard error occurs, both the advanced and retarded offset positions should be used to allow greater opportunity for error recovery. When the Offset command is done, the ATA bit is set to indicate that a Read command should be issued to the cylinder and track for recovery of the data.

The OFM bit (RMDS bit 00) is cleared by any one of the following methods:

- a. Seek to another cylinder by means of an Implied Seek operation or a Mid-Transfer Seek operation.
- b. A Write command.
- c. A Return-To-Centerline command.

- d. A Recalibrate command.
- e. A Read-In Preset command.

5.3.5 RETURN-TO-CENTERLINE COMMAND (17)

The Return-To-Centerline command functions differ for RP and RM disk drive emulations.

5.3.5.1 Return-To-Centerline Command for RP Disk Drive Emulations

This command is used to clear bits <07:00> in register RPOF and to set the ATA bit in register RPDS. This command is simulated. The actual return-to-centerline function occurred at the completion of the Read command.

5.3.5.2 Return-To-Centerline Command for RM Disk Drive Emulations

This command is used to clear the OFM bit (RMDS bit 00) and the OFS7 bit (RMOF bit 07), and to set the ATA bit in register RMDS.

5.3.6 SEARCH COMMAND (31)

The Search command causes the SC72/BX disk controller to perform a Seek operation for the desired cylinder and then compare the contents of the sector counter with the desired sector address stored in register RPDA/RMDA. If the comparison matches, the ATA bit is set and an Interrupt message is sent to the PDP-11/70 CPU if the IE bit (RPCS1/RMCS1 bit 06) is set. If the comparison is not made before three Index pulses have been received by the SC72/BX disk controller, the Search command is incomplete and the OPI bit (RPER1/RMER1 bit 13) is set.

5.4 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place the disk drive logic into a known or Initialized state. They usually require only a few microseconds for execution. Five types of Housekeeping commands are described in this subsection.

5.4.1 NO OP COMMAND (01)

This command performs no operation, except to clear the ATA bit.

5.4.2 DRIVE CLEAR COMMAND (11)

The Drive Clear command functions differ for RP and RM disk drive emulations.

5.4.2.1 Drive Clear Command for RP Disk Drive Emulations

This command clears the ATA and ERR bits in RPDS; the ATA bit in RPAS; bits <15:09> and <07:00> in RPMR; bits <07:00> in RPOF; and

bits <15:00> in RPER1, RPER2, RPER3, RPEC1, and RPEC2. It sets bit 08 in RPMR.

5.4.2.2 Drive Clear Command for RM Disk Drive Emulations

This command clears the ATA and ERR bits in RMDS; the ATA bit in RMDS; bits <15:04> and <02:00> in RMMR1; and bits <15:00> in RMER1, RMER2, and RMEC2. It sets bit 03 in RMMR1.

5.4.3 RELEASE COMMAND (13)

This command performs a Drive Clear operation and releases the disk drive for use by the other port.

5.4.4 READ-IN PRESET COMMAND (21)

The Read-In Preset command functions differ for RP and RM disk drive emulations.

5.4.4.1 Read-In Preset Command for RP Disk Drive Emulations

This command sets the Volume Valid (VV) bit (RPDS bit 06), and clears the following register bits: ATA in RPDS; FMT16, HCI, and ECI in RPOF; and bits <15:00> in RPDC and RPDA.

5.4.4.2 Read-In Preset Command for RM Disk Drive Emulations

This command sets the Volume Valid (VV) bit (RMDS bit 06), and clears the following register bits: OFM and ATA in RMDS, and <15:00> in RMDC, RMDA, and RMOF.

5.4.5 PACK ACKNOWLEDGE COMMAND (23)

This command sets the VV bit (RPDS/RMDS bit 06) for the selected disk drive. This command, or a Read-In Preset command, **MUST** be issued before any Data Transfer command or Positioning command can be issued to a disk drive that has gone off-line. The reset of the VV bit identifies disk pack changes to the CPU.

5.5 EXTENDED COMMANDS

Extended commands can be enabled only by writing a 177777g into register RPCC/RHMR. They remain enabled until either of two events occur:

- a. A Data Transfer command is terminated.
- b. Some data other than 177777g is written into register RPCC/RMHR.

Four types of Extended commands are described in this subsection.

5.5.1 TRANSPARENT ECC CORRECTION COMMAND (37)

This command enables the SC72/BX disk controller to correct ECC errors during a Read operation before the data is transferred to memory. This command can be used with a Read command or a Read Header and Data command. It also has limited use with a Write command. Reading continues with the next sector if the data in that sector is correctable. If the data cannot be corrected, then the Data Transfer operation terminates with the bad sector and an uncorrectable Read Error is flagged in the normal manner. When the Read operation is done, the number of errors corrected during execution of the current Data Transfer command is stored in register RPEC2/RMEC2. All bits in register RPEC2/RMEC2 are reset to the zero state at the start of every Read command. When this command is not enabled, Read Errors are handled in the normal manner and register RPEC2/RMEC2 is not cleared before an attempt to execute a Read command.

A cumulative corrected error count is maintained for each disk drive. This error count may be read by writing a 100023₈ into register RPCC/RMHR and then reading the contents of register RPCC/RMHR. This cumulative error counter is cleared only when the SC72/BX disk controller is powered up.

This Function Code (37) can be set during a Write operation but it is not used during that Write operation unless the emulated disk drive is an RM80 configuration (see Automatic Skip-Sector Feature, subsection 5.6). Function Code 37 enables Transparent ECC Correction only for the disk drive selected by the Unit Select code in register RPCS2/RMCS2. Bit 14 of register RPOF/RMOF reflects the status of the Transparent ECC Correction mode; when set, it indicates the Transparent ECC Correction command is enabled. Bit 14 of register RPOF/RMOF is cleared at the end of any Data Transfer operation. It is also cleared at the start of any Write Check operation because the SC72/BX disk controller does not support this function during a Write Check operation.

5.5.2 WORD COUNT EQUALS SECTOR COUNT COMMAND (41)

Enabling this command causes register RPWC/RMWC to contain the number of sectors to be transferred instead of the number of words to be transferred. This command can be used with the Read operation, Read Header and Data operation, Write operation, and Write Header and Data operation. The SC72/BX disk controller does not support this command for a Write Check operation. Transfer of partial sector contents cannot be done by using this command.

When this command is not enabled, register RPWC/RMWC contains a word count. Regardless of whether register RPWC/RMWC contains a word count or a sector count, the count is always negative.

Function Code 41 is enabled only for that disk drive whose Unit Select number matches the Unit Select code stored in register RPCS2/RMCS2. Bit 13 of register RPOF/RMOF reflects the status of

the Word Count Equals Sector Count mode; when set, it indicates the function is enabled. This bit is cleared at the end of any data Transfer operation. It is also cleared at the start of any Write Check operation because the SC72/BX disk controller does not support this function during a Write Check operation.

Usually, this command is intended for transfer of very long bursts of data through single Unibus I/O ports.

5.5.3 PHYSICAL READ/WRITE/WRITE CHECK HEADER AND DATA COMMANDS

Three separate Function Codes can be optionally selected and entered in the Function Code bit positions of register RPCS1/RMCS1 so that users can write their own custom-formatted programs to take advantage of the Track Replacement featured offered on RP04/05/06 disk drive emulations. RP04/05/06 disk drive emulations have two extra words in the header which the SC72/BX disk controller can use to specify an alternate track address and cylinder address in place of the current (assumed defective) address. Users who wish to use the commands available with this option should ask Emulex for details about how this option is used.

5.5.4 FORMAT COMMAND (77)

Format command functions differ for RP and RM disk drive emulations.

5.5.4.1 Format Command for RP Disk Drive Emulations

This Format command executes a Return-To-Zero instruction, clears registers RPDC and RPDA, sets the FMT16 bit in register RPOF, and formats the entire disk pack in standard format. In each sector, the FMT16 bit is set in Header Word One, Header Words Three and Four contain all zeros, and the data field of the sector contains all zeros. When the formatting is completed, register RPDC contains the last cylinder number plus one, and the LST bit in register RPDS is set.

5.5.4.2 Format Command for RM Disk Drive Emulations

This Format command executes a Return-To-Zero instruction, clears registers RMDC and RMDA, sets the FMT16 bit in register RMOF, and formats the entire disk pack in standard format. In each sector, bits <15:14> and the FMT16 bit are set in Header Word One, and the data field of the sector contains all zeros. When the formatting is completed, register RMDC contains the last cylinder number plus one, and the LST bit in register RMDS is set.

5.6 AUTOMATIC SKIP-SECTOR FEATURE

This feature functions with Read Data and Write Data commands only. It enables automatic execution of the Skip-Sector function which is standard in RM80 disk drive emulations. If a Skip-Sector Error

(SSE) is detected while either the Transparent ECC Correction mode (Function Code 37) or the Word Count Equals Sector Count mode (Function Code 41) is enabled, the firmware sets the Skip-Sector Error Inhibit (SSEI) bit (RMOF bit 09), increments the number of usable sectors per track by one (to gain access to the Skip-Sector), increments the contents of register RMDA by one, and continues the Data Transfer operation with the data contents of the next sector.

As in the Normal mode of operation, the SSEI bit is reset if the end of the track is reached; therefore, multiple SSE errors can occur and all are skipped.

To ensure proper operation of this feature, the SSEI bit (RMOF bit 09) must be reset immediately before execution of any Read Data or Write Data operation. On that sector which is being skipped, the firmware ignores all other header errors, except a CRC error. The event sequences of this feature comply with the standard requirements of DEC RM80 formatter and disk drive emulations.

6.1 INTRODUCTION

This section describes the modifications in DEC RM and RP diagnostics which are required to run them on the SC72/BX disk controller. Once modified, these diagnostics can be run on any current and future configurations generated for the emulations covered in this manual. Note that the Emulex diagnostic SXBX0D runs with RM and RP emulations and requires no modification. For details on running SXBX0D, refer to the Disk Maintenance Utility (SXBX0D) User's Guide (P/N PD9950904-00).

Part one of the modifications includes all known programming errors, and all modifications required to bypass unsupported portions of the DEC Maintenance mode. Part two of the modification lists patches for the self-sizing requirements.

The patches listed and described in this section are supported by all revision levels of the SC72/BX disk controller.

This section is divided into three subsections, as listed in the following table:

Subsection	Title
6.1	Introduction
6.2	RM Diagnostics
6.3	RP Diagnostics

6.2 RM DIAGNOSTICS

This subsection describes modifications for seven diagnostic routines used in the Self-Sizing mode with RM disk drive emulations.

6.2.1 CZRMAC0 - RM03/RM02 FORMATTER

Product Code: AC-9252C-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	12632	10011	1
2.	23630	13746	12746
3.	27154	1750	1503
4.	27512	10164	110164
5.	31602	10164	110164
6.	32772-32774	5702, 1426	4737, 34676
	32776-33000	4737, 34676	5702, 1424

- | <u>Item</u> | <u>Explanation</u> |
|-------------|---|
| 1. | This modification alters the number of tracks that must be formatted before a bad sector file can be written. Since the format OP code does not write a bad sector file, and since the Performance Exerciser does not run without one, this modification allows any size Format or Verify operation to create a bad sector file. If the number is not altered, then the entire disk pack must be formatted before a bad sector file can be written. |

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
30044	4037	406
11260-11262	11237, 4	113737, 31472
11266-11270	12737, 1466	13737, 31470
11510-11512	22737, 151466	23737, 31466
11520-11522	22737, 2000	23737, 31464
12530-12532	12702, 1466	13702, 31470
12560-12562	12737, 5	13737, 5660
12612-12614	62737, 5	63737, 5660
15200-15202	22737, 1466	23737, 31470
15210-15212	122737, 4	123737, 31472
15402-15404	122737, 1466	123737, 31470
15410-15412	112737, 4	113737, 31472
16410-16412	22737, 4	23737, 31472
16430-16432	22737, 1466	23737, 31470
16440-16442	122737, 4	123737, 31472
16502-16504	22737, 1467	23737, 5652
20070-20072	12737, 1466	13737, 31470
20076-20100	12737, 4	13737, 31472
27176-27200	22705, 20024	122705, 24
27204-27206	22705, 24024	122705, 27
27220-27222	22705, 20025	122705, 25
27226-27230	22705, 24025	122705, 25
10734-10740	12737, 1466, 1320	104412, 13703, 26644
10742-10746	132762, 3, 26526	13702, 1220, 10263
10750-10752	1003, 12737	10, 4737
10754-10756	1466, 1320	31320, 104413

The following subroutine must be inserted where indicated. It replaces a rotational position sensing routine the formatter does not need because the formatter formats only one disk drive at a time. The contents of the existing routine are not shown.

Locations: 31320-31452

Contents: 62703, 36, 12713, 100027, 11304, 12713, 100030, 11305, 12713, 100036, 10437, 1320, 10537, 1324, 12703, 31464, 105023, 110523, 10413, 52723, 150000, 10423, 10523, 5204, 5205, 10437, 5652, 10537, 5660, 10437, 5666, 10537, 5674, 10437, 5704, 10537, 5712, 10437, 5730, 10537, 5736, 10437, 5754, 10537, 5762, 207.

6.2.2 CZRMBO - RM03/RM02 PERFORMANCE EXERCISER

Product Code: AC-A994B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	11134-11136	400, 46116	100000, 46144
2.	32144	13746	12746
3.	35130	1750	1503
4.	35466	10164	110164
5.	37556	10164	110164
6.	41036-41040	5702, 1426	4737, 34676
	41042-41044	4737, 34676	5702, 1424

All of the items for Part 1 modifications are unidentified program bugs.

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
4440	57512	60410
4472	57512	60410
6364-6366	22760, 1465	26060, 106
13534-13540	123727, 1415, 5	240, 4737, 60304
13554-13560	23727, 1412, 151466	240, 4737, 60230
16654-16656	62705, 5	66005, 112
16672-16676	20527, 4, 101402	26005, 112, 3002
16700-16702	162705, 5	16005, 112
22614-22616	112766, 4	116066, 112
25442-25446	10004, 62704, 2	10046, 4737, 60064
25664	12737	402
25762-25764	16403, 55252	4737, 60206
26214-26220	12737, 1466, 40674	240, 4737, 60262
26222-26226	112737, 4, 46073	240, 4737, 60326
35152-35154	22705, 20024	122705, 24
35160-35162	22705, 24024	122705, 27
35174-35176	22705, 20025	122705, 25
35202-35204	22705, 24025	122705, 25

The following subroutines must be added to the end of the program at the indicated locations.

Locations: 60064-60204

Contents: 10146, 111001, 13704, 34620, 4037, 35050, 401, 403,
 105761, 34512, 1375, 105761, 34472, 3424, 62704, 36,
 6301, 6301, 62701, 60350, 12714, 100027, 11421, 11400,
 5300, 10037, 1446, 12714, 100030, 11421, 11437, 1444,
 12714, 100036, 12601, 16604, 2, 12600, 62704, 2, 200.

Locations: 60206-60346

Contents: 16403, 55252, 13763, 1444, 16, 13763, 1444, 24, 207,
5046, 111016, 6316, 6316, 67716, 60350, 13646, 52716,
150000, 5216, 22637, 1412, 207, 5046, 111016, 6316,
6316, 62716, 60350, 13637, 46074, 207, 5046, 111016,
6316, 6316, 62716, 60352, 123637, 1415, 207, 5046,
111016, 6316, 6316, 62716, 60352, 113637, 46073, 207.

Those users operating disk drives with more than 80 megabyte capacity also require the patches in the following list. The Performance Exerciser limits the number of allowable bad sectors on any disk drive to 16, even though the Bad Sector File can handle 126. The patches in the following list allow the program to run with 126 or fewer bad sectors. The first two patches in the list move the base address of the buffer. These locations have already been patched, and the "From" column reflects these patches.

<u>Location</u>	<u>From</u>	<u>To</u>
4440	60410	70410
4472	60410	70410
17202	20	176
17206	62702	16002
20274	12701	16001
20300	60001	240
20304	20	176
25504	14	22
25510	162	154
25716	122	126
26166	62701	16001
26174	40	400
26344	62701	16001
26352	40	400
43146	0	60410
43452	0	61410
43756	0	62410
44262	0	63410
44566	0	64410
45072	0	65410
45376	0	66410
45702	0	67410

6.2.3 CZRMCB0 - RM03/RM02 FUNCTIONAL TEST - PART 1

Product Code: AC-A9997B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	25024, 25026	4737, 43216	137, 25622
2.	10730	40001	0
3.	13062	1012	412
4.	26600	1007	407
5.	27014	1011	411
6.	35570	1406	406
7.	45152	4	10
8.	60000	7	1405
9.	66074	13746	12746
10.	10356-10362	5007, 110102, 1	11102, 105002, 240

<u>Item</u>	<u>Explanation</u>
1.	This modification bypasses an OPI test to comply with DEC hardware ECOs #7634-0004, 7684-0007, and 7684-0009.
2.	This modification is required only on very fast processors. It changes a Drive Clear test to run in Normal mode instead of Maintenance mode.
3.	This modification bypasses a "loss of bit clock" test which is run in Maintenance mode.
4.	This modification bypasses an "RMR" test which, as written, can be run only in the Maintenance mode.
5.	This modification bypasses a Massbus Parity Error test. Since there is no Massbus on the Emulex SC72/BX disk controller, there is no Massbus Parity to test.
6.	This modification bypasses a test of register RMLA that is done in the 18-Bit Address mode.
7-10.	Unidentified program bugs.

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
7634	24024	20024
7654	24025	20027
7732-7734	12706, 1100	4737, 104106
27500-27502	12737, 1466	13737, 104400
30522-30524	22726, 1000	23726, 104400
31372-31374	12737, 1466	13737, 104400
32022-32024	12737, 1466	13737, 104400
32240-32242	22737, 1466	23737, 104400
32730-32732	12737, 2400	13737, 104410
33224	3400	37400
33250-33252	12737, 2400	13737, 104410
33344-33346	12737, 1467	13737, 104402
33636	2000	4000
33662-33664	12737, 1467	13737, 104402
36364	633	40
36370	634	41
36754	634	40
36760	633	41
37436-37440	12737, 2400	13737, 104410
37700	4000	40000
37724-37726	12737, 2400	13737, 104410
40032-40034	12737, 1467	13737, 104402
40304	2000	4000
40330-40332	12737, 1467	13737, 104402
51114	177770	177700
51134-51140	23727, 51702, 240	23737, 51702, 104412
51150-51152	162737, 5	163737, 104412
51224-51226	22737, 1467	23737, 104402
51340-51342	22737, 1467	23737, 104402
51600	176000	170000
52236-52242	23727, 1432, 1466	23737, 1432, 104400
52304-52310	123727, 1405, 4	123737, 1405, 104404
57730-57736	23727, 1432, 1466	23737, 1432, 104400
577776-60002	123727, 7, 4	123737, 1405, 104404

The following subroutine must be inserted where indicated. The previous contents of the locations should be all zeros.

Locations: 104106-104174

Contents: 13700, 1276, 062700, 36, 12701, 104400, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10011, 207.

6.2.4 CZRMDB0 - RM03/4M02 FUNCTIONAL TEST - PART 2

Product Code: AC-B000B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	40452	4	10
2.	63360	13746	12746

Both of the above modifications correct unidentified program bugs.

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
7656	24024	20024
7674	24025	20027
7732-7734	12700, 1100	4737, 101550
17514-17516	12737, 2037	13737, 102514
20374-20376	12737, 1466	13737, 102500
22272-22274	22737, 2000	23737, 102506
22300	103402	101402
23014-23016	22737, 1466	23737, 102500
23076-23100	12737, 1466	13737, 102500
23104-23106	12737, 2037	13737, 102514
23374-23376	12737, 1466	13737, 102500
23402-23404	12737, 2037	13737, 102514
24406-24410	12737, 2400	13737, 102510
25066	3400	37400
25126-25130	12737, 1467	13737, 102502
25614	1777	3777
34714	5737	0
36766-36770	122763, 4	123763, 102504
44414	177770	177700
44434-44440	23727, 45202, 240	23737, 45202, 102512
44450-44452	162737, 240	163737, 102512
44474-44500	23727, 45200, 5	23737, 45200, 102506
44510-44512	162737, 5	163737, 102506
44524-44526	22737, 1467	23737, 102502
44640-44642	22737, 1467	23737, 102502
45100	176000	170000
45536-45542	23727, 1434, 1466	23737, 1434, 102500
45604-45610	123727, 1407, 4	123737, 1407, 102506
53764-53766	22737, 1466	23737, 102500
54002-54004	122737, 4	123737, 102504

The following subroutine must be inserted where indicated. The previous contents of the locations should be all zeros.

Location: 101550-10646

Contents: 13700, 1276, 62700, 36, 12701, 102500, 12710, 100027,
11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221,
105021, 116121, 177775, 12710, 100036, 16100, 177776,
6200, 6200, 6200, 10021, 112721, 37, 116111, 177767,
207.

6.2.5 CZRMEB0 - RM03/RM02 FUNCTIONAL TEST - PART 3

Product Code: AC-B003B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	31032	42702	52702
2.	30070, 30072	404, 240	402, 0
	30076, 30100	137, 30470	5237, 1336
3.	30416, 30420	404, 240	402, 0
	30424, 30426	137, 30470	5237, 1336
4.	44472	4	10
5.	67364	13746	12746

- | <u>Item</u> | <u>Explanation</u> |
|-------------|---|
| 1. | This modification reverses a DEC patch that eliminated Bus-Address-Increment-Inhibit mode in a Write test. The DEC controller gets Data Late errors in this mode; the Emulex SC72/BX disk controller does not. |
| 2. | This modification increments the saved contents of register RMDA after attempting a Write operation with the ERR bit in register RMDS set. The DEC controller increments register RMDA during the illegal attempt to perform a Write operation; the Emulex SC72/BX disk controller does not. The modification allows a subroutine to pass the test. |
| 3. | Same as Item 2, except this modification is for an attempted Read operation with the ERR bit in register RMDS set. |
| 4-5. | Unidentified program bugs. |

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
7632	24024	20024
7652	24025	20027
7706-7710	12706, 1100	4737, 111760
20040-20042	12737, 1466	13737, 112100
20444-20442	12737, 1466	13737, 112100
22076-22100	12737, 2037	13737, 112114
32604-32610	23727, 1434, 1400	23737, 1434, 112100
32710-32712	12737, 2037	13737, 112114
36722-36724	22737, 2037	23737, 112114
41000-41002	12737, 2000	13737, 112116
41006-41010	12737, 1466	13737, 112100
42012-42014	12737, 2012	13737, 112120
42426-42430	112737, 4	123737, 112104
42446-42450	22737, 1466	23737, 112100
42516-42520	122737, 4	123737, 112104
42536-42540	22737, 1466	23737, 112100
43006-43010	122763, 4	123763, 112104
50434	177770	177700
50454-50460	23727, 51222, 240	23737, 51222, 112112
50470-50472	162737, 240	163737, 112112
50514-50520	23727, 51220, 5	23737, 51220, 112106
50530-50532	162737, 5	163737, 112106
50544-50546	22737, 1467	23737, 112102
50660-50662	22737, 1467	23737, 112102
51120	176000	170000
51556-51562	23727, 1434, 1466	23737, 1434, 11210
51624-51630	123727, 1407, 4	123737, 1407, 112104
60004-60006	22737, 1466	23737, 112100
60022-60024	122737, 4	123737, 112104

The following subroutine must be added to the test at:

Locations: 111760-112052

Contents: 13700, 1276, 62700, 36, 12701, 112100, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116121, 177767, 10521, 116121, 177776, 112721, 12, 116111, 177776, 207.

6.2.6 CZRMFB0 - EXTENDED DRIVE TEST

Product Code: AC-B0006B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	21464	13746	12746
2.	27722-27726	5737, 4322, 1011	32737, 100000, 4350
	27730-27734	32737, 100000, 4350	1405, 12737, 177777
	27736-27742	1405, 12737, 177777	1446, 137, 30370
	27744-27750	1446, 137, 30370	5737, 4322, 1401
3.	37246	1750	1503
4.	37604	10164	110164
5.	41674	10164	110164
6.	43064-43066	5702, 1426	4737, 44770
	43070-43072	4737, 44770	5702, 1424

All these items are unidentified bugs.

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
1774	400	1466
2040	400	1466
2176	144	100*
37270-37272	22705, 20024	122705, 24
37276-37300	22705, 24024	122705, 27
37312-37314	22705, 20025	122705, 25
37320-37322	22705, 24025	122705, 25
17574-17576	20127, 1466	20137, 1574
17602-17604	20227, 4	20237, 1602
17022-17026	22700, 5, 3365	23700, 1602, 2365
17222-17224	122737, 4	123737, 1602
20312-20314	122737, 5	123737, 1602
20320	3370	2370
33530-33534	122702, 5, 3003	123702, 1602, 2003

* Required on disk drives that have fewer than 100 logical cylinders (see last entry in "To" column of Part 2 Modifications).

The following subroutine must be inserted where indicated. It replaces an existing subroutine of similar function that is no longer needed. The contents of the existing routine are not listed in this manual; only the contents of the new subroutine are listed.

Locations: 26632-27004

Contents: 104412, 113704, 1102, 6304, 16401, 1620, 13704, 1450,
62704, 36, 12702, 1566, 5003, 12122, 6237, 1566,
103002, 12122, 401, 5022, 5203, 20327, 14, 1405, 20327,
3, 1363, 24242, 761, 12714, 100027, 11405, 12703, 1574,
5713, 1412, 21327, 1466, 1407, 21327, 1465, 1002, 5305,
402, 20513, 2001, 10513, 12714, 10030, 11437, 1602,
104413, 207.

6.2.7 CZRMIB0 - DRIVE COMPATIBILITY TEST

Product Code: AC-B015B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	21000	13746	12746

This item in this Modification is an unidentified program bug.

This test has no Part 2 Modifications. It is not practical to rewrite this test; to rewrite it would require allocating an indeterminate amount of buffer space near the beginning of the test. The test uses cylinders 000-800 (but not all of them), and tracks zero through four. Any configuration with 801 or more cylinders and five or more tracks is compatible with this test.

6.3 RP DIAGNOSTICS

This subsection describes modifications for seven diagnostic routines used with RP disk drive emulations.

NOTE

Unlike RM disk drives, RP disk drives do not have a Self-Sizing mode.

6.3.1 DZRJA-B-D - RP04/RP05/RP06 MECHANICAL AND READ/WRITE TEST

Product Code: MAINDEC-11-DZRJA-A-D

MODIFICATIONS (Part 1)

There are no Modifications for Part 1 of this diagnostic program.

MODIFICATIONS (Part 2)

All of the following locations are changed from '1456' to 'C-1':

1614, 1616, 1620, 1672, 1740, 2004, 2026, 2050, 2072, 2112, 2132,
2170, 2220, 2260, 2312, 2336, 2404, 2450, 2472, 2514, 2536, 2556,
2576, 2634, 2664, 2724, 2756.

6.3.2 CZRJBB0 - RP04/RP05/RP06 FORMATTER PROGRAM

Product Code: AC-9185B-MC

MODIFICATIONS (Part 1)

There are no Modifications for Part 1 of this diagnostic program.

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
3352	1456	C-1

6.3.3 CZRJDC0 - RP04/RP05/RP06 MULTIDRIVE EXERCISER

Product Code: AC-9195C-MC

MODIFICATIONS (Part 1)

There are no Modifications for Part 1 of this diagnostic program.

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
16676	1457	C
25504	1456	C-1

6.3.4 CZRJGB0 - RP04/RP05/RP06 DISKLESS CONTROLLER TEST - PART 1

Product Code: AC-9208B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	5714, 5716	5737, 1700	5777, 173760
2.	10776	4537	406
3.	11052, 11062	104200, 104200	4200, 4200
4.	11140, 11150	10, 10	0, 0
5.	11310, 11330	1642, 176174	1632, 176702
6.	11364, 11400	5, 401	1, 1
7.	11542, 11560, 11562	1644, 1747, 176706	1634, 177776, 176704
8.	11620	4037	474
9.	12564	177777	0
10.	12734, 12746	4276, 4276	4200, 4200
11.	13010, 13022	17437, 17437	0, 0
12.	13064, 13076	116000, 116000	16000, 16000
13.	13664	17437	0
14.	14004	4276	4200
15.	14022	116000	16000
16.	14202, 14204	4737, 42614	137, 15444
17.	16352, 16354	12706, 1000	137, 41064
18.	12520	177777	175777

ItemExplanation

1. This Modification fixes an unidentified program error. The purpose of the instruction is to test for the presence of an RH70 controller versus an RH11 controller. It does this by testing for the existence of an RH70 register whose address is in location 1700g. As written, however, the program checks for the existence of location 1700g, not the existence of the location whose address is in 1700g. This fix corrects the instruction.
2. This Modification branches around a portion of the test that only works in Maintenance mode.
- 3-7,
and
9-15. These Modifications alter bits in the expected results of certain registers, after various register operations, to reflect their expected status when the SC72/BX disk controller is not in Maintenance mode.
8. This Modification branches around a portion of the test that can only be run in Maintenance mode.
- 16-17. These Modifications jump around Maintenance mode Read/Write tests. These tests can only be run in Maintenance mode.
18. This Modification allows for either a 10-bit or 11-bit cylinder address register.

NOTE

This test assumes the SC72/BX disk controller is being tested after a system power-up. Certain registers which are not cleared by a Bus Init signal are assumed to contain all zeros, as would be the situation in Power-Up mode.

MODIFICATIONS (Part 2)

There are no Modifications to Part 2 of this diagnostic program.

6.3.5 CZRJHB0 - RP04/RP05/RP06 DISKLESS CONTROLLER TEST - PART 2

Product Code: AC-9213B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	21250, 21252	5737, 15020	5777, 173544
2.	24170	15010	15014
3.	26756	177677	175777
4.	30650, 30652	4037, 45702	137, 44132
5.	30646	31154	44132

<u>Item</u>	<u>Explanation</u>
1.	This Modification fixes an unidentified program error. It is exactly the same error as outlined in Modification 1 of the Diskless Controller Test - Part 1, Item 1.
2.	This Modification corrects a program error to ensure all the controller registers are tested.
3.	This Modification corrects a program error to test the status of the PSEL bit (the bit under test) instead of the IE bit (which is not under test).
4-5.	These Modifications jump around those data I/O tests that can be run only in Maintenance mode.

MODIFICATIONS (Part 2)

There are no Modifications to Part 2 of this diagnostic program.

6.3.6 CRZJIB0 - RP04/RP05/RP06 FUNCTIONAL CONTROLLER TEST - PART 1

Product Code: AC-9218B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	6526, 6530	5737, 2340	5777, 173606
2.	12744	1005	1003
3.	17732, 20410	30500, 30500	10500, 10500
4.	21344, 21474	20400, 20400	400, 400
5.	22430, 22724	30500, 30500	10500, 10500
6.	23014	11600	16000
7.	33656, 34356	30500, 30500	10500, 10500
8.	41210-41216	240, 240, 240, 240	32777, 200, 141104, 1774
9.	42300-42304	240, 32777, 100	4737, 400, 30377
	400-406	402, 0, 406, 0	12703, 100, 5303
	410-414	412, 0, 416	1376, 12703, 100, 207
10.	15472	177777	17437
11.	15506	177777	175777

- | <u>Item</u> | <u>Explanation</u> |
|-------------|---|
| 1. | This Modification fixes an unidentified program error. it is exactly the same error as outlined in Modification 1 of the Diskless Controller Test - Part 1, Item 1. |
| 2. | This Modification changes a branch to bypass a Maintenance mode test. |
| 3-5, 7. | These modifications remove the "PIP" bit from a test of RPDS. The "PIP" bit sets during these tests, but not as quickly as in the DEC controller. |
| 6. | This test Modification removes the sign change bit from a test of RPOF. Since there is no hardware signal from an SMD disk drive available to the controller to indicate a phase change in the PLO, this bit is not implemented. |
| 8. | This Modification changes a Maintenance mode Seek operation to a Normal mode Seek operation. |
| 9. | This modification inserts a timeout loop into the program between the loop that waits on some bit becoming set and the routine that tests for IE equals zero, thus indicating the Interrupt request occurred and was serviced. This same timeout loop exists in Part 2 of the functional test. The use of Maintenance mode in certain parts of this test may have eliminated the need for the timeout in this test. |

- | <u>Test</u> | <u>Explanation</u> |
|-------------|---|
| 10. | This test Modification allows for either a 10-bit or a 16-bit Disk Address register. |
| 11. | This test Modification allows for either a 10-bit or an 11-bit Cylinder Address register. |

MODIFICATIONS (Part 2)

There are no Modifications to Part 2 of this diagnostic program.

6.3.7 CZRJJB0 - RP04/RP05/RP06 FUNCTIONAL CONTROLLER TEST - PART 2

Product Code: AC-9223B-MC

MODIFICATIONS (Part 1)

<u>Item</u>	<u>Location</u>	<u>From</u>	<u>To</u>
1.	6412, 6414	5737, 2240	5777, 173622
2.	15342, 15352	177702, 2410	177672, 2370
3.	15366, 15370	200, 0	0, 1
4.	15404, 15414, 15430	177774, 2574, 200	177672, 2370, 0
5.	21446, 21456, 21512	3402, 0, 200	3400, 177777, 0
6.	23132, 23142	177502, 2574	177400, 2370
7.	23110, 23120	177410, 2410	177400, 2370
8.	26622, 26630	204, 102, 1200	0, 0, 1000, 0
	26636, 26644	100	
9.	26706, 26714, 26734	2164, 177774, 100	2370, 17762, 0
10.	27366, 27270	13700, 2270	137, 27646
11.	33566	25	1000

- | <u>Item</u> | <u>Explanation</u> |
|--------------|---|
| 1. | This Modification fixes an unidentified program error. It is exactly the same error as outlined in Modification 1 of the Diskless Controller Test - Part 1, Item 1. |
| 2-4 and 5-9. | These Modifications alter the expected contents of RPBA, RPWC, and the IR and OR bits in RPCS2 at the completion of an aborted Write test to compensate for the lack of a SILO buffer. The SC72/BX disk controller does not alter the values of those registers if the Write command cannot be done. The DEC controller does. |
| 10. | This Modification jumps around a Maintenance mode test. |
| 11. | This Modification increases a stall timer to compensate for the delay between the detection of an error and the setting of the Interrupt Enable (IE) bit. This Modification is required on CPUs that include a cache memory. |

MODIFICATIONS (Part 2)

<u>Location</u>	<u>From</u>	<u>To</u>
11706	11456	10000+C-1
11770	1456	C-1
12256	1456	C-1
17366	11457	10000+C
17444	1457	C
21156	11456	10000+C-1
21240	11457	10000+C
21316	1456	C-1
21576	1457	C
21606	1456	C-1
21704	11456	10000+C-1
22012	1456	C-1
22244	1457	C

NOTE

"C" equals the number of logical cylinders per disk drive.

BLANK

7.1 OVERVIEW

This section describes preventive maintenance and servicing procedures for maintaining optimum performance of the SC72/BX disk controller system. This section is divided into four subsections, as listed in the following table:

Subsection	Title
7.1	Overview
7.2	Preventive Maintenance
7.3	Service
7.4	Fault Isolation

7.2 PREVENTIVE MAINTENANCE

The regularly scheduled maintenance checks, cleaning procedures, component replacement procedures and adjustment procedures detailed in the separately supplied system component technical manuals should be accomplished at the prescribed intervals. There are no adjustments or calibrations required in servicing the SC72/BX disk controller. Emulex recommends the diagnostic software programs be used in the system checkout. The diagnostic programs should be run at regularly scheduled intervals to verify correct system operation.

NOTE

When any circuit component has been replaced, the diagnostics should be run and all pertinent circuit characteristics should be checked before the system is returned to normal operation.

Preventive maintenance of the SC72/BX disk controller system also includes three periodic verifications:

- a. Proper seating of all four PCBAs of the SC72/BX disk controller in the CPU backplane or expansion box.
- b. Proper seating of cables in connectors.
- c. Proper seating of PROMs in their respective IC sockets.

These verifications should be made about once a year or whenever physical location of components of the SC72/BX disk controller is changed.

7.3 SERVICE

The components of the Emulex SC72/BX disk controller have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory. Corrective maintenance should not normally be required. Except for setting DIP switches, no adjustments or alignments are required. If a malfunction does occur, as indicated by Fault Isolation procedures, and a component is not working properly, the entire SC72/BX disk controller should be returned to the factory or to an Emulex-authorized repair center for service. Emulex products are not designed to be repaired in the field.

If any or all PCBAs of the SC72/BX disk controller are to be returned, Emulex recommends that a description of the symptoms and operating environment be included with the returned unit to expedite troubleshooting. Figure 7-1 shows a configuration record sheet to be filled in. The depicted configuration shows component locations, PROMs, DIP switch settings and cable connections for each PCBA, as applicable.

Before returning the SC72/BX disk controller (or any PCBA thereof) to Emulex, whether it is or is not under warranty, request the factory or the factory representative to provide return-shipment instructions and a Return Materials Authorization (RMA) number.

DO NOT RETURN A PRODUCT OR COMPONENT TO EMULEX
WITHOUT AUTHORIZATION

A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii notify:

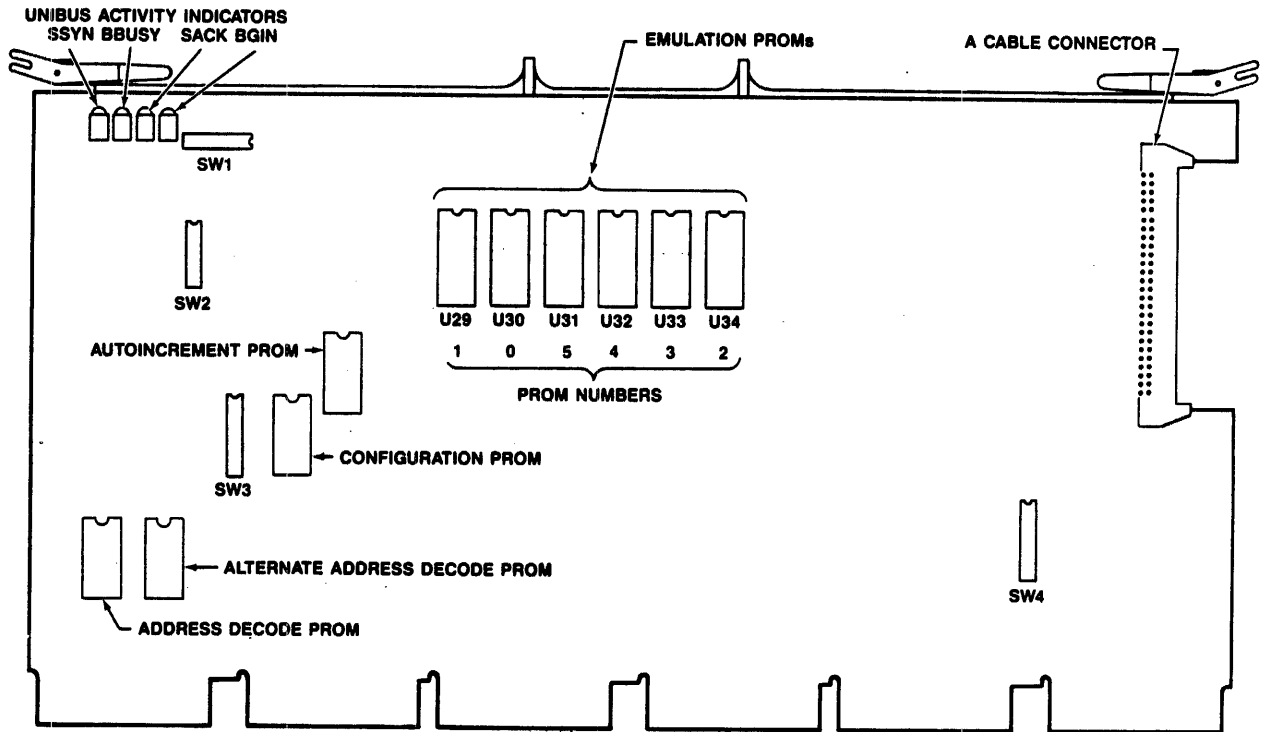
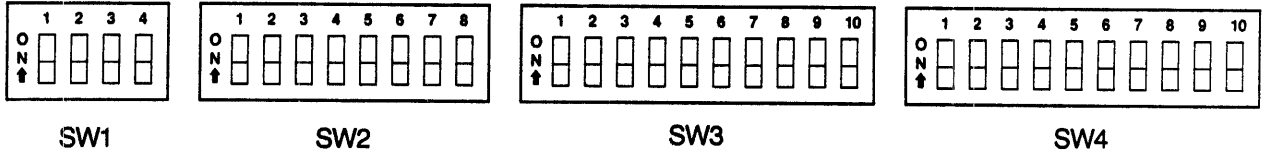
Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, Ca 92626
(714) 662-5600 TWX 910-595-2521

Outside of the United states, notify the distributor from whom the product or component was initially purchased.

After notifying Emulex and receiving an RMA, package the product (preferably by using the original packing material) and send the product **POSTAGE PAID** to the address provided by the Emulex representative. The sender must also insure the package.

CONFIGURATION REFERENCE SHEET

Serial Numbers: A _____ B _____ C _____ Cst _____



Emulation PROM: From _____ to _____, Rev _____
 Configuration PROM: _____
 Address Decode PROM: _____
 Alt. Address Decode PROM: _____

Use Pencil

SC7202-0204

Figure 7-1. Configuration Sheet SC72/BX Disk Controller (SH 1 of 4)

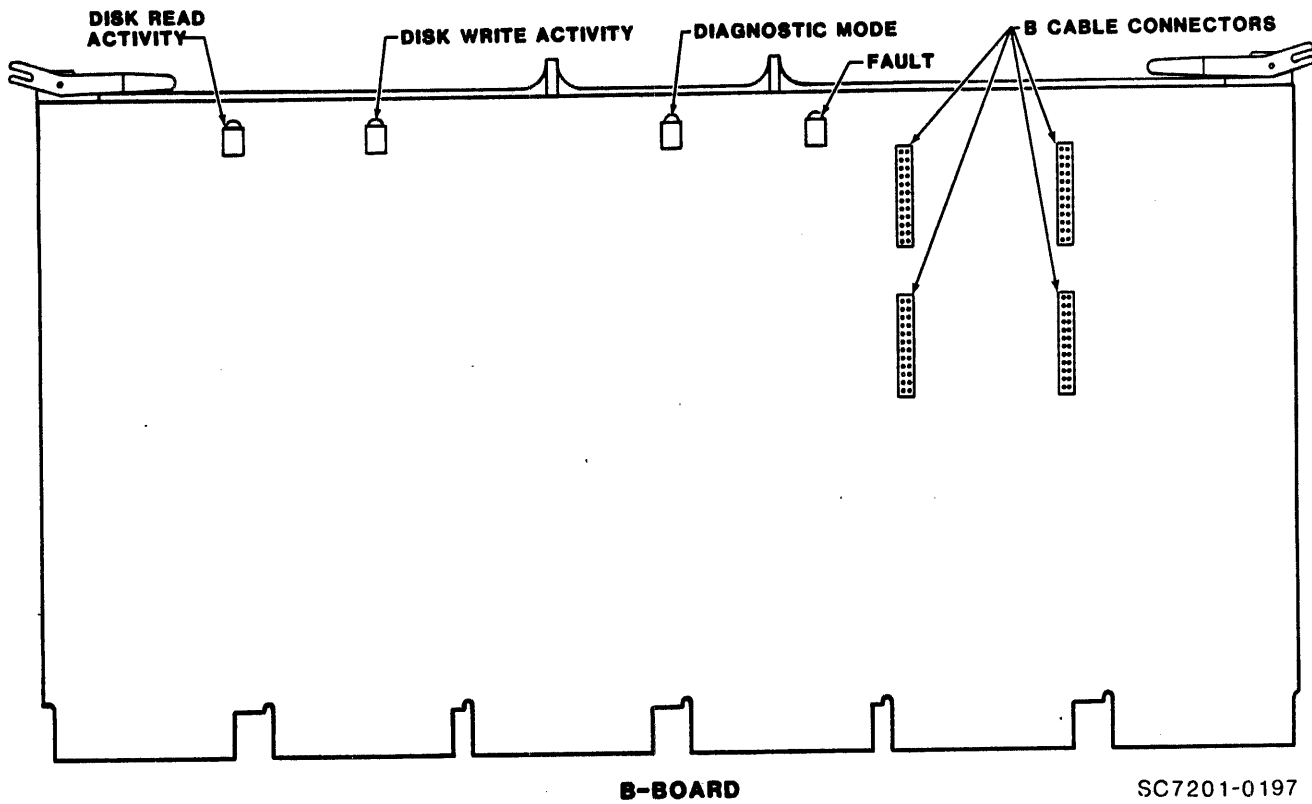


Figure 7-1. Configuration Sheet SC72/BX Disk Controller (SH 2 of 4)

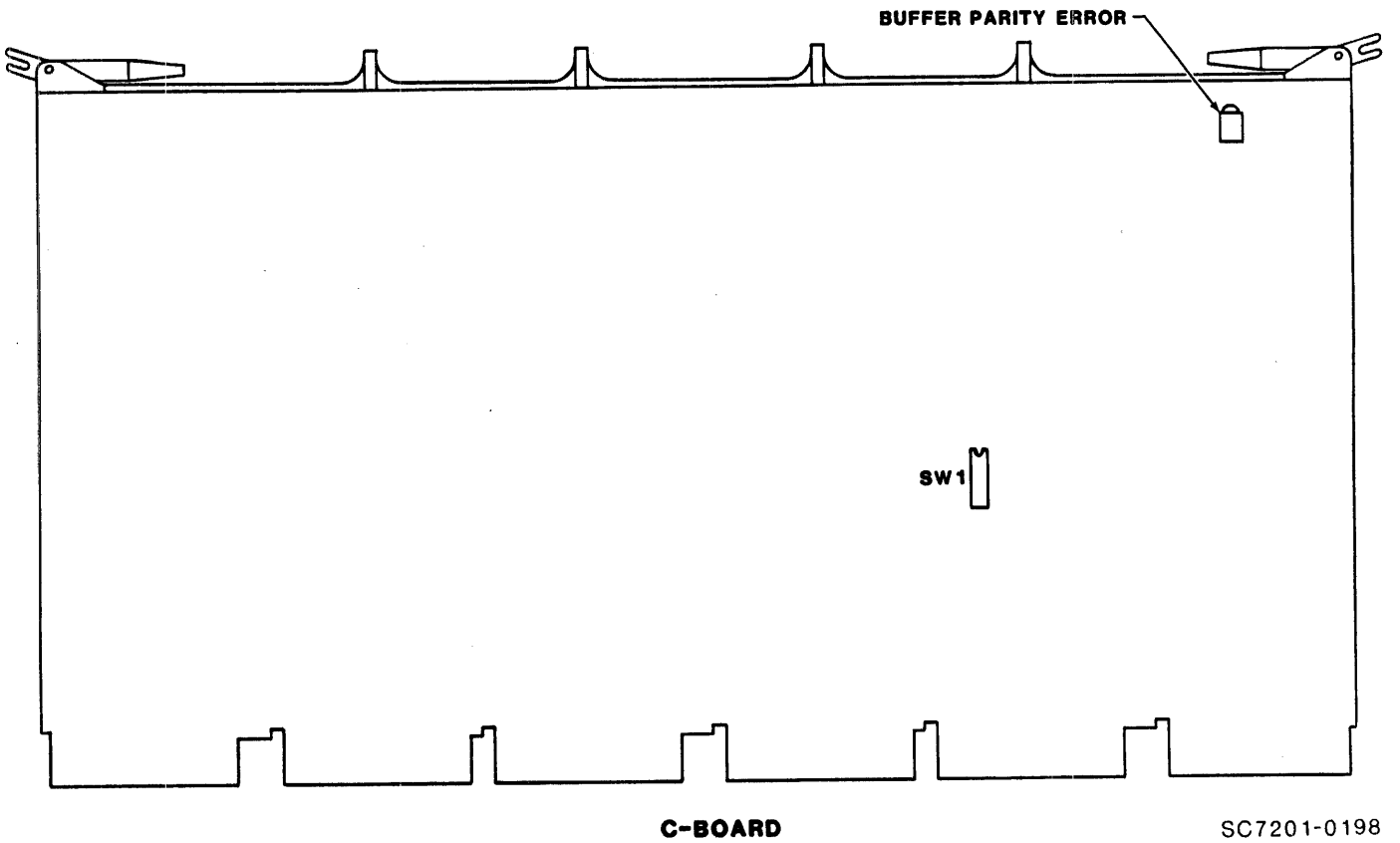
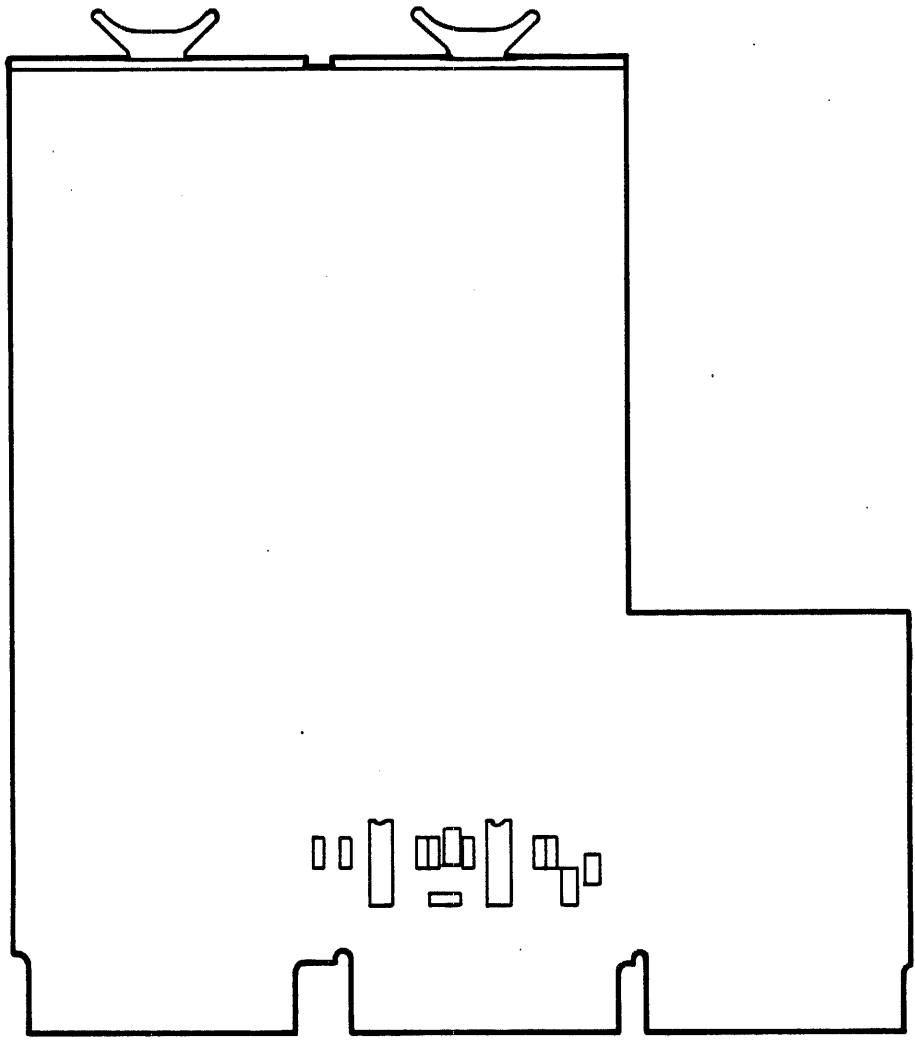


Figure 7-1. Configuration Sheet SC72/BX Disk Controller (SH 3 of 4)



SC7201-0205

Figure 7-1. Configuration Sheet SC72/BX Disk Controller (SH 4 of 4)

7.4 FAULT ISOLATION

The ensuing suggested fault isolation procedures are general in nature, based on established troubleshooting techniques, and should be used primarily as a guide. Following these procedures can aid in determining whether the equipment failure is a result of operator error or equipment malfunction, speed location of a failed circuit component, and minimize down time caused by equipment malfunctions.

7.4.1 ISOLATING THE PROBLEM

In troubleshooting electronic equipment, the problem can usually be attributed to any of three sources:

- a. Operator error
- b. Adverse environmental factor(s)
- c. Equipment malfunction.

Operator error is a more prevalent source of equipment problems than most operators care to admit. Operating procedures should always be investigated and eliminated **BEFORE** assuming any other source of malfunction exists. The symptoms should not be systematically investigated for environmental or electromechanical symptoms of malfunction until all possibility of human error has been eliminated.

7.4.2 OPERATING PROCEDURE CHECK

A system malfunction, appearing to be caused by circuit failure, is often found to be the result of improper operation or application of the equipment. When a problem is observed, the operating procedures being used with the malfunctioning unit and its associated units must therefore be thoroughly checked to ensure they are being correctly performed.

7.4.3 MANUAL OPERATIONS CHECK

A check must be made to determine if manual operations such as cleaning, servicing, or troubleshooting were performed on the equipment or related equipment before the first observed abnormal operation. Recently performed manual operations are suspect and should be double-checked to ensure that they were properly executed. Emulex recommends the following checks:

- a. Verify recently changed procedures correctly performed
- b. Verify adjustment settings properly made
- c. Verify tightness of system connector installations
- d. Verify that any parts temporarily removed or disconnected were properly and securely replaced; this check should

include proper seating of PCBAs in slots of CPU backplane or expansion box

- e. Verify that no accidentally loosened or damaged components are evident. Tighten any loose components and replace any obviously damaged components.

7.4.4 VISUAL INDICATOR CHECKS

If the malfunction persists after double-checking all recent manual operations, visually check the status of all operating controls and indicators in the system. Visual indicators include the following items:

- a. Switches and indicator lights on PCBAs and operator control panels (OCPs)
- b. Busses
- c. Switches and/or indicators mounted out of sight on internal chassis or PCBAs
- d. Printed data outputs
- e. Signals monitored at test points by using meters, oscilloscopes, etc.

Correct any observed control-setting errors. Attempt to determine possible causes of erroneous indication.

7.4.5 POWER CIRCUIT CHECK

The effects of power supply malfunctions are normally widespread, which makes diagnosis of the problem difficult. Error indications tend to appear throughout the equipment and are difficult to localize. These symptoms, however, can sometimes be used as an indication that the cause of the problem is basic and pertains to the power circuits.

7.4.5.1 Fuses

Verify that all fuses in the power circuits are of the proper type and rating, and that none have blown. This check should include any fuses (or circuit breakers) internally mounted and not readily accessible from the front or rear of the major units of the system. Remove any blown fuse and replace with new fuse of the same type and rating.

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C A U T I O N
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Fuses with higher ratings or faster blow time limits than those removed must **NEVER** be installed. Determine cause of fuse failure and correct problem **BEFORE** replacing failed fuse.

7.4.5.2 Voltage Levels

Verify that power of the proper frequency and amplitude is being supplied to the equipment. If the primary input power is correct, check the output levels from all internal power supplies. All such outputs must be within required specifications (see applicable technical manuals for the equipment) and not subject to slow or intermittent drifting. If the problem is cyclic or intermittent; i.e., appears for a period of time and then disappears, check the power supplies for extreme sensitivity to variations in ambient temperature (heat or cold).

7.4.6 ELECTRONIC CIRCUIT CHECKS

When the possibility of operator error has been eliminated, and the existing symptoms have been thoroughly analyzed but the cause of the problem cannot be found, then attempt to determine if the problem is repeatable, continuous, or intermittent. The identical operation should be repeated several times to determine the types and number of failures.

If repeating the operation fails to sufficiently isolate the location of the malfunctioning circuit area, all the diagnostic programs should be run to determine if the symptoms appear under all conditions.

The power supply voltages, as well as the AC line voltage at the input, should be checked first to determine if they are within specification. The basic timing circuits should then be checked. Problems in either of these areas are difficult to diagnose, since these circuits affect operation of all other circuits. These timing circuits, in turn, make error indications intermittent and problem isolation difficult. Varying the environment (power supply voltages, heat, mechanical shock, etc.) may sometimes cause an intermittent problem to occur more often so that it can be investigated effectively.

- - - - -
C A U T I O N
- - - - -

The +5V should only be varied $\pm 5\%$ in margin tests. The IC chips used are rated from +4.75V to +5.25V.

7.4.6.1 Circuit Divisions

When attempting fault isolation in electronic systems, it is best to divide the system into troubleshooting areas, with each system unit being considered as a separate area. Then each functional section of each unit (power circuits, amplifier circuits, servo circuits, digital circuits, analog circuits, etc.) should be considered as a separate area. In this way, each area can be individually evaluated, and those not involved in the problem can be eliminated from consideration. The source of the problem is thus isolated into ever smaller areas until only the actual problem area remains.

Most electronic equipment operates from an interwoven network of circuits. Malfunctions or improper operating procedures originating in one area of the equipment often cause failure symptoms within that area and other related areas. These symptoms are the foremost troubleshooting aids available and should be used to their fullest extent. In many instances, a malfunction can be isolated to a particular area by completely analyzing the symptoms.

7.4.7 NOISE PROBLEM CHECKS

Many times, equipment failures occur which are extremely intermittent and seem to appear at random intervals. The cause of these symptoms can often be traced to the power ON/OFF switching of heavy machinery or high-powered electrical devices in the immediate area. Such events can cause extreme noise signals on the primary AC power input lines and a sudden variation in line voltage may be reflected in the DC operating voltages which can result in an equipment failure. Therefore, when extremely intermittent failures are encountered, an attempt must be made to reference these failures to a simultaneous outside occurrence which might have a bearing on the problem.

Individual power supplies within the equipment must be checked for excessive ripple in output levels. Checks must also be performed for noise bursts caused by the combination of loose electrical connections and mechanical shock or vibration. In some situations, individual components may also be found to be sensitive to mechanical shock or vibration even though all connections are secure.

7.4.8 FAULT ISOLATION GUIDE

Table 7-1 is a Fault Isolation Guide that should be used as a diagnostic aid for the isolation of faults in the SC72/BX disk controller system. It lists possible symptoms, probable cause of the malfunction, and corrective actions.

Table 7-1. SC72/BX Disk Controller Fault Isolation Guide

Symptom	Probable Cause	Remedy
CPU powered up, FAULT LED indicator lit.	Self Test Failure.	Verify SC72/BX disk controller PCBAs are properly seated in CPU backplane slots; reseal if necessary. Defective unit. Return SC72/BX disk controller to factory. Switch SW1-1 ON but should be OFF. Place switch SW1-1 in OFF position.
Data Transfer operation attempted but appropriate activity LED indicator (WRITE or READ) not lit.	A-Cable or B-Cable reversed in connector(s). A-Cable or B-Cable for addressed disk drive not connected. Addressed disk drive does not have Ready status. Wrong Device Address coded in configuration DIP switches.	Check cable connections and reverse if pins of connectors not properly matched. Connect cables to addressed disk drive. Perform operations on disk drive that are needed to produce Ready status condition, then retry operation. Encode correct address in configuration DIP switch pack.
Unable interrupt CPU.	Wrong Interrupt Vector Address in configuration DIP switches.	Encode correct Interrupt Vector Address in configuration DIP switch pack.
Operation or event occurring in which an applicable LED indicator should be steadily lit or flashing, but LED does not respond.	Circuit to LED is open. LED burnt out.	Check continuity of LED circuit. Replace LED or return PCBA to factory.

Table 7-1. SC72/BX Disk Controller
 Fault Isolation Guide (continued)

Symptom	Probable Cause	Remedy
DIP switch set to produce a specific condition or event, but condition or event does not occur.	Circuit to switch open. Switch defective.	Check continuity of switch circuit. Replace switch or return PCBA to factory.

A.1 INTRODUCTION

To allow the SC72/BX disk controller user maximum flexibility in disk drive selection, the SC72/BX disk controller supports a wide variety of disk drive types. This appendix provides the switch-setting information which makes possible this selective flexibility.

A.2 CONTROLLER CONFIGURATION

The SC72/BX disk controller is capable of supporting a wide variety of disk drives. Switches SW3-1 through SW3-6 select the various configurations that are supported, and a list of these disk drive types and capacities are described in Tables A-1, A-4, and A-7. Tables A-2, A-5, and A-8 list the proper switch settings for each of the various disk drive configurations.

Tables A-1 and A-2, and Tables A-4 and A-5, are for system configurations with four physical disk drives (switch SW3-7 OFF). These tables also can be used for certain system configurations with eight physical disk drives (switch SW3-7 ON). (See paragraph A.2.3.3 for more information.) Tables A-7 and A-8 are for system configurations with eight physical disk drives (switch SW3-7 ON).

A.2.1 PHYSICAL VERSUS LOGICAL DISK DRIVE UNIT NUMBERING

A primary feature of the SC72/BX disk controller is its ability to emulate eight DEC disk subsystems by using four physical disk drives. This emulation is accomplished by mapping two logical disk subsystems onto one disk drive which contains twice as much capacity as the standard DEC subsystem. If this emulation is used, the mapping of logical disk drive units onto physical disk drive units is done as listed in the following table:

Physical Disk Drive Unit Number	Logical Disk Drive Unit Number
0	0 and 4
1	1 and 5
2	2 and 6
3	3 and 7

This mode of operation is possible only when operating with the configuration for four physical disk drives (switch SW3-7 OFF). When the configuration for eight physical disk drives is selected (switch SW3-7 ON), only one logical disk drive unit is allowed to be mapped on each of the eight (possible) physical disk drives.

The physical/logical assignments for specific disk drive unit configurations can be found by comparing the PHYSICAL disk drive column with the LOGICAL disk drive column in Tables A-2, A-5, and A-8.

A.2.1.1 Disk Drive Unit Number Assignment

The disk drives must be assigned a distinct physical disk drive unit number. This physical disk drive unit number may be determined after the logical configuration to use has been decided. The physical disk drive unit number for each disk drive must correlate to the physical disk drive unit number listed in Table A-2, A-5, or A-8. Thus, for configuration number 04 in Table A-2, physical disk drive unit number 0 would be an 823-cylinder, 19-track disk drive; physical disk drive unit number 1 would be an 823-cylinder, 19-track disk drive; physical disk drive unit number 2 would be an 842-cylinder, 40-track disk drive; and physical disk drive unit number 3 would be an 842-cylinder, 40-track disk drive.

A.2.2 SECTORING FUJITSU 2351A DISK DRIVES

To allow the Fujitsu 2351A disk drive to function properly with the SC72/BX disk controller, some alterations must be made to the sector select switch settings found in the Fujitsu technical manual.

To configure the Fujitsu 2351A for 48 sectors, the jumpers at location BC7 must be set such that bit one is jumpered 2-3 (instead of 3-4), bit 2 is jumpered 6-7 (instead of 5-6), and all other jumpers are set as instructed in the Fujitsu technical manual.

A.2.3 CONFIGURATION SELECTION FOR FOUR-DISK DRIVE AND EIGHT-DISK DRIVE VERSIONS

The SC72/BX emulates five different DEC disk subsystems, the RM02, RM03, RM05, RM80, and RP06. The unformatted capacity, in megabytes (Mb), of each of these subsystems is listed in the following table:

Emulation	Capacity in Mb
RM02	80
RM03	80
RM05	300
RM80	160
RP06	200

Essentially, there are two different types of disk drive configurations:

- With the first type, each emulated DEC disk drive subsystem exists on one physical disk drive. With the eight-disk drive configuration selected, this is the the only type that is possible.
- In the second type, two emulated logical disk drive units are mapped onto one physical disk drive unit.

These two types of disk drive mapping may be combined when the four-disk drive configuration is selected.

To determine the configuration switch settings which are compatible with the system that is being used, use the following procedure:

NOTE

For the four-disk drive configuration, refer to Tables A-1 and A-2 or Tables A-4 and A-5. For the eight-disk drive configuration, refer to Tables A-7 and A-8. (See also paragraph A.2.3.3.)

1. Locate, in Table A-1, A-4, or A-7, the type and capacity of each disk drive that is being used. Note the number that is assigned to each type of physical disk drive intended to be used in the system.
2. Scan down the KEY column in Table A-2, A-5, or A-8 until the KEY number appropriate to the intended disk drive is located. Check the corresponding emulation in the LOGICAL disk drive type column. If the emulation is not one that is required, continue to scan the KEY column in search of the required emulation.
3. After finding a suitable match for physical disk drive unit 0, check the KEY and LOGICAL disk drive type column for matching physical disk drive units 1 through 3 or 1 through 7 for that configuration row. It is not necessary to use all of the disk drive ports.
4. When an entire suitable configuration match has been located by using the tables, set the configuration switches as indicated in Table A-2, A-5, or A-8.
5. Three PROMs come with the SC72/BX:
 - 897, a four port PROM, stored at U71 on the A-Board. (See Table A-2.)
 - C03, an alternate four port PROM, stored at U21 on the A-Board. (See Table A-5.)
 - C00, an eight port PROM, stored at U50 on the C-Board. (See Table A-8.)

The PROM you use should be placed in the socket at location U71 on the A-Board. The other two PROMs should be stored at locations U21 and U50.

A.2.3.1 Configuration PROMs

The SC72/BX is shipped with three configuration PROMs. Two are for use with the four-port B-Boards (Emulex PROMs P/N 897 and P/N C03); the other is for use with the eight-port B-Boards (Emulex PROM P/N C00).

A.2.3.2 PROM Locations

One configuration PROM is installed in IC socket U71 on the A-Board, one is stored at U21 on the A-board, and the third is stored in the spare socket at U50 on the C-Board. For proper operation, the desired configuration PROM must be installed in IC socket U71 on the A-Board.

A.2.3.3 Configuration PROM Selection

The four-port configuration PROMs may be used with either the four-port or the eight-port B-Board. In this configuration, the associated configuration switches have the following functions:

1. Switch SW3-7 OFF - Use the four-port configuration Tables A-1 and A-2 or Tables A-4 and A-5 as they stand.
2. Switch SW3-7 ON - Use the four-port configuration Table A-2 or A-5 as defined in the following instruction:
 - a. Switch SW3-1 OFF - Disk drives 0-3 are configured per entry in Table A-2 or Table A-5. Disk drives 4-7 are configured per the next sequential entry in the same table; e.g., for configuration 40, disk drives 0-3 are as shown for configuration 40, and disk drives 4-7 are as shown for configuration 41.
 - b. Switch SW3-1 ON - Disk drives 4-7 are a repeat of configuration shown for disk drives 0-3. If a configuration is selected which maps two logical disk drives per physical disk drive and switch SW4-1 is ON (to indicate that an eight-port B-Board is in use) then each physical disk drive contains only one logical disk drive.
3. The eight-port configuration PROM can be used only in conjunction with an eight-port B-Board. Such switch settings are listed in the eight-port configuration Table A-8.

Table A-1
Drives Supported (PROM No. 897)

Mfg.	Model	Key	Physical			Configurations
			Cyl	Trk	Sec	
Ampex	330	1024-16	1024	16	32	16,17,40
Ampex	9380	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
Ampex	93160	1645-05	1645	5	32	34,35,36
APS	4830*	823-10	823	10	64	04,12-15,20-23,32, 33,43
CDC	9448-96	823-06	823	6	32	20,22
CDC	9715-340	711-24	711	24	32	56,57
CDC	9715-515	711-24A	711	24	44	72,73
CDC	9715-515	711-24B	711	24	50	74-77
CDC	9730-80	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
CDC	9730-160	823-10A	823	10	32	01-03,10,21,23,51,53
CDC	9730-160	1646-05	823	10	32	45,46
CDC	9762	823-05	823	5	32	00-02,07,10,13-15, 25,36,42,64,65,70,71
CDC	9766	823-19	823	19	32	04,12-15,20-23,32, 33,43,57,62,63,66,67
CDC	9766	823-19A	823	19	22	72,73
CDC	9771	1024-16	1024	16	64	62-65
CDC	9771	1024-16A	1024	16	84	66-71
CDC	9775	842-40	842	40	32	04-07,11
CDC	9775	1684-19	842	38	32	47
Century	T82RM	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
Century	T302RM	823-19	823	19	32	04,12-15,20-23,32, 33,43,57
Century	T306	823-19	823	19	32	04,12-15,20-23,32, 33,43,57
Century	T306	815-19	815	19	22	60
Fujitsu	2280	823-05	823	5	32	00-02,07,10,13-15, 25,36,42
Fujitsu	2284	823-10A	823	10	32	01-03,10,21,23,51,53
Fujitsu	2294	1024-16	1024	16	32	16,17,40
Fujitsu	2312	589-07	589	07	32	24,25
Fujitsu	2351A	842-20	842	20	44	41-44,53,55
Fujitsu	2351A	842-20A	842	20	48	26,27
Memorex	677	815-19	815	19	22	52,55
Memorex	677-30	823-19	823	19	32	04,12-15,20-23,32, 33,43,57
NEC	D2351	760-19	760	19	62	61
Priam	3350	561-03	561	3	32	37
STC	8775	1124-30	1124	30	32	30-32
Techstor	160	700-12	700	12	32	50

Notes on next page

Notes for Table A-1:

*Set sector size to 630 bytes/sector (switch count equals 629) and enable the track length compatibility switch located on the slog board. This makes the drive look like a CDC 9766.

Table A-2
Four Physical Disk Drive Configurations (PROM No. 897¹)

CONF. NO.	SW-3						PHYSICAL KEY Unit		LOGICAL Unit(s) = Dr Type		Rev
	6	5	4	3	2	1					
00	O	O	O	O	O	O	823-05	0	0	= RM02	A
							823-05	1	1	= RM02	A
							823-05	2	2	= RM02	A
							823-05	3	3	= RM02	A
01	O	O	O	O	O	C	823-05	0	0	= RM02	A
							823-05	1	1	= RM02	A
							823-10	2	2,6	= RM02/RM02	A
							823-10	3	3,7	= RM02/RM02	A
02	O	O	O	O	C	O	823-05	0	0	= RM02	A
							823-10	1	1,5	= RM02/RM02	A
							823-10	2	2,6	= RM02/RM02	A
							823-10	3	3,7	= RM02/RM02	A
03	O	O	O	O	C	C	823-10	0	0,4	= RM02/RM02	A
							823-10	1	1,5	= RM02/RM02	A
							823-10	2	2,6	= RM02/RM02	A
							823-10	3	3,7	= RM02/RM02	A
04	O	O	O	C	O	O	823-19	0	0	= RM05	A
							823-19	1	1	= RM05	A
							842-40	2	2,6	= RM05	A
							842-40	3	3,7	= RM05	A
05	O	O	O	C	O	C	823-19	0	0	= RM05	A
							842-40	1	1,5	= RM05/RM05	A
							842-40	2	2,6	= RM05/RM05	A
							842-40	3	3,7	= RM05/RM05	A
06	O	O	O	C	C	O	842-40	0	0,4	= RM05/RM05	A
							842-40	1	1,5	= RM05/RM05	A
							842-40	2	2,6	= RM05/RM05	A
							842-40	3	3,7	= RM05/RM05	A
07	O	O	O	C	C	C	823-05	0	0	= RM02	A
							823-10	1	1,5	= RM02/RM02	A
							823-19	2	2	= RM05	A
							842-40	3	3,7	= RM05/RM05	A

¹PROM #897 requires Revision B or above firmware.

Table A-2, cont.

CONF. NO.	SW-3					PHYSICAL KEY Unit		LOGICAL Unit(s) = Dr Type		Rev
	6	5	4	3	2	1				
10	O	O	C	O	O	O	823-10	0	0,4 = RM02/RM02	A
							823-10	1	1,5 = RM02/RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-05	3	3 = RM02	A
11	O	O	C	O	O	C	842-40	0	0,4 = RM05/RM05	A
							842-40	1	1,5 = RM05/RM05	A
							842-40	2	2,6 = RM05/RM05	A
							823-19	3	3 = RM05	A
12	O	O	C	O	C	O	823-19	0	0 = RM05	A
							823-19	1	1 = RM05	A
							823-19	2	2 = RM05	A
							823-19	3	3 = RM05	A
13	O	O	C	O	C	C	823-05	0	0 = RM02	A
							823-05	1	1 = RM02	A
							823-05	2	2 = RM02	A
							823-19	3	3 = RM05	A
14	O	O	C	C	O	O	823-05	0	0 = RM02	A
							823-05	1	1 = RM02	A
							823-19	2	2 = RM05	A
							823-19	3	3 = RM05	A
15	O	O	C	C	O	C	823-19	0	0 = RM05	A
							823-19	1	1 = RM05	A
							823-19	2	2 = RM05	A
							823-05	3	3 = RM02	A
16	O	O	C	C	C	O	1024-16	0	0 = RM05	A
							1024-16	1	1 = RM05	A
							1024-16	2	2 = RM05	A
							1024-16	3	3 = RM05	A
17	O	O	C	C	C	C	1024-16	0	0 = RM05	A
							1024-16	1	1 = RM05	A
							1024-16	2	2 = RM05	A
							823-19	3	3 = RM05	A
20	O	C	O	O	O	O	823-06	0	0,4 = RM03/RM02*	A
							823-06	1	1,5 = RM03/RM02*	A
							823-06	2	2,6 = RM03/RM02*	A
							823-19	3	3 = RM05	A
21	O	C	O	O	O	C	823-10	0	0,4 = RM02/RM02	A
							823-10	1	1,5 = RM02/RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-19	3	3 = RM05	A
22	O	C	O	O	C	O	823-19	0	0 = RM05	A
							823-06	1	1,5 = RM03/RM02*	A
							823-06	2	2,6 = RM03/RM02*	A
							823-19	3	3 = RM05	A
23	O	C	O	O	C	C	823-19	0	0 = RM05	A
							823-10	1	1,5 = RM02/RM02	A
							823-10	2	2,6 = RM02/RM02	A
							823-10	3	3,7 = RM02/RM02	A

Table A-2, cont.

CONF. NO.	SW-3					PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s) = Dr Type	
24	O	C	O	C	O	O	589-07	0	0 = RM02	A
							589-07	1	1 = RM02	A
							589-07	2	2 = RM02	A
							589-07	3	3 = RM02	A
25	O	C	O	C	O	C	589-07	0	0 = RM02	A
							589-07	1	1 = RM02	A
							589-07	2	2 = RM02	A
							823-05	3	3 = RM02	A
26	O	C	O	C	C	O	842-20	0	0 = RM02*	A
							842-20	1	1 = RM02*	A
							842-20	2	2 = RM02*	A
							842-20	3	3 = RM02*	A
27	O	C	O	C	C	C	842-20	0	0 = RM80*	A
							842-20	1	1 = RM80*	A
							842-20	2	2 = RM80*	A
							842-20	3	3 = RM80*	A
30	O	C	C	O	O	O	823-19	0	0 = RM05	A
							1124-30	1	1,5 = RM05/RM05	A
							1124-30	2	2,6 = RM05/RM05	A
							1124-30	3	3,7 = RM05/RM05	A
31	O	C	C	O	O	C	1124-30	0	0,4 = RM05/RM05	A
							1124-30	1	1,5 = RM05/RM05	A
							1124-30	2	2,6 = RM05/RM05	A
							1124-30	3	3,7 = RM05/RM05	A
32	O	C	C	O	C	O	1124-30	0	0,4 = RM05/RM05	A
							1124-30	1	1,5 = RM05/RM05	A
							1124-30	2	2,6 = RM05/RM05	A
							823-19	3	3 = RM05	A
33	O	C	C	O	C	C	823-19	0	0 = RM02*	A
							823-19	1	1 = RM02*	A
							823-19	2	2 = RM02*	A
							823-19	3	3 = RM02*	A
34	O	C	C	C	O	O	1645-05	0	0,4 = RM02/RM02	A
							1645-05	1	1,5 = RM02/RM02	A
							1645-05	2	2,6 = RM02/RM02	A
							1645-05	3	3,7 = RM02/RM02	A
35	O	C	C	C	O	C	823-05	0	0 = RM02	A
							1645-05	1	1,5 = RM02/RM02	A
							1645-05	2	2,6 = RM02/RM02	A
							1645-05	3	3,7 = RM02/RM02	A
36	O	C	C	C	C	O	1645-05	0	0,4 = RM02/RM02	A
							1645-05	1	1,5 = RM02/RM02	A
							1645-05	2	2,6 = RM02/RM02	A
							823-05	3	3 = RM02	A
37	O	C	C	C	C	C	561-03	0	0 = RM02*	A
							561-03	1	1 = RM02*	A
							561-03	2	2 = RM02*	A
							561-03	3	3 = RM02*	A

Table A-2, cont.

CONF. NO.	SW-3					PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s) = Dr Type	
40	C	O	O	O	O	O	1024-16	0	0 = RM05*	A
							1024-16	1	1 = RM05*	A
							1024-16	2	2 = RM05*	A
							1024-16	3	3 = RM05*	A
41	C	O	O	O	O	C	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							842-20	3	3,7 = RP06/RP06	A
42	C	O	O	O	C	O	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							823-05	3	3 = RM02	A
43	C	O	O	O	C	C	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							823-19	3	3 = RM05	A
44	C	O	O	C	O	O	842-20	0	0 = RP06*	A
							842-20	1	1 = RP06*	A
							842-20	2	2 = RP06*	A
							842-20	3	3 = RP06*	A
45	C	O	O	C	O	C	823-10	0	0 = RM02*	A
							823-10	1	1 = RM02*	A
							823-10	2	2 = RM02*	A
							823-10	3	3 = RM02*	A
46	C	O	O	C	C	O	823-10	0	0 = RM03*	A
							823-10	1	1 = RM03*	A
							823-10	2	2 = RM03*	A
							823-10	3	3 = RM03*	A
47	C	O	O	C	C	C	842-40	0	0 = RM05*	A
							842-40	1	1 = RM05*	A
							842-40	2	2 = RM05*	A
							842-40	3	3 = RM05*	A
50	C	O	C	O	O	O	700-12	0	0 = RM02*	A
							700-12	1	1 = RM02*	A
							700-12	2	2 = RM02*	A
							700-12	3	3 = RM02*	A
51	C	O	C	O	O	C	823-10	0	0 = RM80	A
							823-10	1	1 = RM80	A
							823-10	2	2 = RM80	A
							823-05	3	3 = RM02	A
52	C	O	C	O	C	O	842-20	0	0,4 = RP06/RP06	A
							842-20	1	1,5 = RP06/RP06	A
							842-20	2	2,6 = RP06/RP06	A
							815-19	3	3 = RP06	A

Table A-2, cont.

CONF. NO.	SW-3					PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s) = Dr Type	
53	C	O	C	O	C	C	823-10	0	0,4 = RM03	B
							823-10	1	1,5 = RM03	
							842-20	2	2,6 = RP06	
							842-20	3	3,7 = RP06	
54	C	O	C	C	O	O	823-10	0	0 = RM80	C
							823-10	1	1 = RM80	
							823-10	2	2 = RM80	
							823-10	3	3 = RM80	
55	C	O	C	C	O	C	842-20	0	0,4 = RP06/RP06	D
							842-20	1	1,5 = RP06/RP06	
							815-19	2	2 = RP06	
							815-19	3	3 = RP06	
56	C	O	C	C	C	O	711-24	0	0 = RM05	D
							711-24	1	1 = RM05	
							711-24	2	2 = RM05	
							711-24	3	3 = RM05	
57	C	O	C	C	C	C	711-24	0	0 = RM05	D
							711-24	1	1 = RM05	
							711-24	2	2 = RM05	
							823-19	3	3 = RM05	
60	C	C	O	O	O	O	842-20	0	0,4 = RP06	E
							842-20	1	1,5 = RP06	
							842-20	2	2,6 = RP06	
							815-19	3	3 = RP06	
61	C	C	O	O	O	C	760-19	0	0,4 = RP06/RP06*	K
							760-19	1	1,5 = RP06/RP06*	
							760-19	2	2,6 = RP06/RP06*	
							760-19	3	3,7 = RP06/RP06*	
62	C	C	O	O	C	O	823-19	0	0 = RM05	G
							823-19	1	1 = RM05	
							1024-16	2	2,6 = RM05/RM05	
							1024-16	3	3,7 = RM05/RM05	
63	C	C	O	O	C	C	1024-16	0	0,4 = RM05/RM05	G
							1024-16	1	1,5 = RM05/RM05	
							823-19	2	2 = RM05	
							823-19	3	3 = RM05	
64	C	C	O	C	O	O	1024-16	0	0,4 = RM05/RM05	G
							1024-16	1	1,5 = RM05/RM05	
							823-05	2	2 = RM03	
							823-05	3	3 = RM03	
65	C	C	O	C	O	C	823-05	0	0 = RM03	G
							823-05	1	1 = RM03	
							1024-16	2	2,6 = RM05/RM05	
							1024-16	3	3,7 = RM05/RM05	

Table A-2, cont.

CONF. NO.	SW-3						PHYSICAL KEY Unit		LOGICAL Unit(s) = Dr Type		Rev
	6	5	4	3	2	1					
66	C	C	O	C	C	O	823-19	0	0	= RM05	G
							823-19	1	1	= RM05	G
							1024-16A	2	2,6	= RM05/RM05*	G
							1024-16A	3	3,7	= RM05/RM05*	G
67	C	C	O	C	C	C	1024-16A	0	0,4	= RM05/RM05*	G
							1024-16A	1	1,5	= RM05/RM05*	G
							823-19	2	2	= RM05	G
							823-19	3	3	= RM05	G
70	C	C	O	O	O		823-05	0	0	= RM03	G
							823-05	1	1	= RM03	G
							1024-16A	2	2,6	= RM05/RM05*	G
							1024-16A	3	3,7	= RM05/RM05*	G
71	C	C	O	O	C		1024-16A	0	0,4	= RM05/RM05*	G
							1024-16A	1	1,5	= RM05/RM05*	G
							823-05	2	2	= RM03	G
							823-05	3	3	= RM03	G
72	C	C	O	C	O		823-19A	0	0	= RP06	H
							823-19A	1	1	= RP06	H
							711-24	2	2,6	= RP06	H
							711-24	3	3,7	= RP06	H
73	C	C	O	C	C		711-24	0	0,4	= RP06	H
							711-24	1	1,5	= RP06	H
							823-19A	2	2	= RP06	H
							823-19A	3	3	= RP06	H
74	C	C	C	O	O		711-24A	0	0	= RM05*	H
							711-24A	1	1	= RM05*	H
							823-05	2	2	= RM03	H
							823-05	3	3	= RM03	H
75	C	C	C	O	C		711-24A	0	0	= RM05*	H
							711-24A	1	1	= RM05*	H
							823-19	2	2	= RM05	H
							823-19	3	3	= RM05	H
76	C	C	C	C	O		823-05	0	0	= RM03	J
							823-05	1	1	= RM03	J
							711-24A	2	2	= RM05*	J
							711-24A	3	3	= RM05*	J
77	C	C	C	C	C		823-19	0	0	= RM05	H
							823-19	1	1	= RM05	H
							711-24A	2	2	= RM05*	H
							711-24A	3	3	= RM05*	H

*Non-Standard drive size. This size is not supported by DEC software or diagnostics. See Table A-3 for actual size.

#Requires option switch SW4-9 to be closed

C = closed/on, O = open/off

Table A-3
Non-Standard Drive Sizes (PROM No. 897)

Config.	Drive Type and Description
37	This RM02 is a 3 track, 561 cylinder drive
45	This RM02 is a 5 track, 1646 cylinder drive
50	This RM02 is a 12 track, 700 cylinder drive
33	This RM02 is a 19 track, 823 cylinder drive
26	This RM02 is a 20 track, 842 cylinder, 48 sector drive
46	This RM03 is a 5 track, 1646 cylinder drive
20	This RM03 is 164 cylinders mapped on a 9448 cartridge
22	This RM03 is 164 cylinders mapped on a 9448 cartridge
40	This RM05 is a 16 track, 1024 cylinder drive
66	This RM05 is a 16 track, 1024 cylinder, 42 sector drive
67	This RM05 is a 16 track, 1024 cylinder, 42 sector drive
70	This RM05 is a 16 track, 1024 cylinder, 42 sector drive
71	This RM05 is a 16 track, 1024 cylinder, 42 sector drive
47	This RM05 is a 19 track, 1684 cylinder drive
74-77	This RM05 is a 24 track, 711 cylinder, 50 sector drive
27	This RM80 is a 20 track, 842 cylinder, 48 sector drive
61 ¹	This RP06 is a 19 track, 760 cylinder, 30 sector drive
44	This RP06 is a 19 track, 1772 cylinder drive

¹SW4-9 must be ON (enables mapping two RP06's onto a 19-head drive).

Table A-4
Drives Supported (PROM No. C03)

Mfg.	Model	Key	Physical			Configurations
			Cyl	Trk	Sec	
Ampex	9380	823-05	823	5	32	1
CDC	9715-340	711-24	711	24	32	1,7,10,11,12,34,35
CDC	9715-515	711-24A	711	24	50	32
CDC	9720	1217-10	1217	10	50	42
CDC	9730-80	823-05	823	5	32	1
CDC	9730-160	823-10	823	10	32	0,3,4,7,10,15,16 23,24,34,35,41
CDC	9762	823-05	823	5	32	1
CDC	9766	823-19	823	19	32	5,6,11,12,17, 20,25,26
CDC	9766	823-19A	823	19	22	2,13,14,21,22, 30,31
CDC	9771	1024-16	1024	16	64	0,27
CDC	9775	842-40	842	40	32	36,37,40
Century	AMS 513	845-19	845	19	44	13,14
Century	AMS 513	845-19A	845	19	50	15,16,17,20
Century	AMS 571	941-19	941	19	44	21,22
Century	AMS 571	941-19A	941	19	54	23,24,25,26
Century	T82 RM	823-05	823	5	32	1
Century	T302 RM	823-19	823	19	32	5,6,11,12,17, 20,25,26
Century	T306	823-19	823	19	32	5,6,11,12,17, 20,25,26
Fujitsu	2280	823-05	823	5	32	1
Fujitsu	2284	823-10	823	10	32	0,3,4,7,10,15,16, 23,24,34,35,41
Fujitsu	2298	1024-16	1024	16	64	0,27
Fujitsu	2298	1024-16A	1024	16	68	3,4,5,6
Fujitsu	2351A	842-20	842	20	44	2,30,31
Fujitsu	2351A	842-20A	842	20	48	36,37,40
Memorex	677-30	823-19	823	19	32	5,6,11,12,17, 20,25,26
Priam	807-23	1552-11	1552	11	32	33

Table A-5
Four Physical Disk Drive Configurations (PROM No. C03¹)

CONF. NO.	SW-3						PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s)	= Dr Type	
00	O	O	O	O	O	O	823-10	0	0,4	= RM03/RM03	A
							823-10	1	1,5	= RM03/RM03	A
							1024-16	2	2,6	= RM05/RM05	A
							1024-16	3	3,7	= RM05/RM05	A
01	O	O	O	O	O	C	711-24	0	0	= RM05	A
							711-24	1	1	= RM05	A
							823-05	2	2	= RM02	A
							823-05	3	3	= RM02	A
02	O	O	O	O	C	O	842-20	0	0,4	= RP06/RP06	A
							842-20	1	1,5	= RP06/RP06	A
							842-20	2	2,6	= RP06/RP06	A
							823-19A	3	3	= RP06	A
03	O	O	O	O	C	C	823-10	0	0,4	= RM03/RM03	A
							823-10	1	1,5	= RM03/RM03	A
							1024-16A	2	2,6	= RM05*/RM05*	A
							1024-16A	3	3,7	= RM05*/RM05*	A
04	O	O	O	C	O	O	1024-16A	0	0,4	= RM05*/RM05*	A
							1024-16A	1	1,5	= RM05*/RM05*	A
							823-10	2	2,6	= RM03/RM03	A
							823-10	3	3,7	= RM03/RM03	A
05	O	O	O	C	O	C	823-19	0	0	= RM05	A
							823-19	1	1	= RM05	A
							1024-16A	2	2,6	= RM05*/RM05*	A
							1024-16A	3	3,7	= RM05*/RM05*	A
06	O	O	O	C	C	O	1024-16A	0	0,4	= RM05*/RM05*	A
							1024-16A	1	1,5	= RM05*/RM05*	A
							823-19	2	2	= RM05	A
							823-19	3	3	= RM05	A
07	O	O	O	C	C	C	823-10	0	0,4	= RM03/RM03	A
							823-10	1	1,5	= RM03/RM03	A
							711-24	2	2	= RM05*	A
							711-24	3	3	= RM05*	A
10	O	O	C	O	O	O	711-24	0	0	= RM05*	A
							711-24	1	1	= RM05*	A
							823-10	2	2,6	= RM03/RM03	A
							823-10	3	3,7	= RM03/RM03	A
11	O	O	C	O	O	C	823-19	0	0	= RM05	A
							823-19	1	1	= RM05	A
							711-24	2	2	= RM05*	A
							711-24	3	3	= RM05*	A
12	O	O	C	O	C	O	711-24	0	0	= RM05*	A
							711-24	1	1	= RM05*	A
							823-19	2	2	= RM05	A
							823-19	3	3	= RM05	A

¹PROM #C03 requires Revision B or above firmware.

Table A-5, cont.

CONF. NO.	SW-3					PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s) - Dr Type	
13	O	O	C	O	C	C	823-19A	0	0 = RP06	A
							823-19A	1	1 = RP06	A
							845-19	2	2,6 = RP06/RP06	A
							845-19	3	3,7 = RP06/RP06	A
14	O	O	C	C	O	O	845-19	0	0,4 = RP06/RP06	A
							845-19	1	1,5 = RP06/RP06	A
							823-19A	2	2 = RP06	A
							823-19A	3	3 = RP06	A
15	O	O	C	C	O	C	823-10	0	0,4 = RM03/RM03	A
							823-10	1	1,5 = RM03/RM03	A
							845-19A	2	2 = RM05*	A
							845-19A	3	3 = RM05*	A
16	O	O	C	C	C	O	845-19A	0	0 = RM05*	A
							845-19A	1	1 = RM05*	A
							823-10	2	2,6 = RM03/RM03	A
							823-10	3	3,7 = RM03/RM03	A
17	O	O	C	C	C	C	823-19	0	0 = RM05	A
							823-19	1	1 = RM05	A
							845-19A	2	2 = RM05*	A
							845-19A	3	3 = RM05*	A
20	O	C	O	O	O	O	845-19A	0	0 = RM05*	A
							845-19A	1	1 = RM05*	A
							823-19	2	2 = RM05	A
							823-19	3	3 = RM05	A
21	O	C	O	O	O	C	823-19A	0	0 = RP06	A
							823-19A	1	1 = RP06	A
							941-19	2	2,6 = RP06/RP06	A
							941-19	3	3,7 = RP06/RP06	A
22	O	C	O	O	C	O	941-19	0	0,4 = RP06/RP06	A
							941-19	1	1,5 = RP06/RP06	A
							823-19A	2	2 = RP06	A
							823-19A	3	3 = RP06	A
23	O	C	O	O	C	C	823-10	0	0,4 = RM03/RM03	A
							823-10	1	1,5 = RM03/RM03	A
							941-19A	2	2 = RM05*	A
							941-19A	3	3 = RM05*	A
24	O	C	O	C	O	O	941-19A	0	0 = RM05*	A
							941-19A	1	1 = RM05*	A
							823-10	2	2,6 = RM03/RM03	A
							823-10	3	3,7 = RM03/RM03	A
25	O	C	O	C	O	C	823-19	0	0 = RM05	A
							823-19	1	1 = RM05	A
							941-19A	2	2 = RM05*	A
							941-19A	3	3 = RM05*	A
26	O	C	O	C	C	O	941-19A	0	0 = RM05*	A
							941-19A	1	1 = RM05*	A
							823-19	2	2 = RM05	A
							823-19	3	3 = RM05	A
27	O	C	O	C	C	C	(Do not select)		A	

Table A-5, cont.

CONF. NO.	SW-3						PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s)	Dr Type	
30	O	C	C	O	O	O	842-20	0	0,4	= RP06/RP06	A
							842-20	1	1,5	= RP06/RP06	A
							823-19A	2	2	= RP06	A
							823-19A	3	3	= RP06	A
31	O	C	C	O	O	C	823-19A	0	0	= RP06	A
							823-19A	1	1	= RP06	A
							823-19A	2	2	= RP06	A
							823-19A	3	3	= RP06	A
							711-24A	0	0	= RM02*	A
32	O	C	C	O	C	O	711-24A	1	1	= RM02*	A
							711-24A	2	2	= RM02*	A
							711-24A	3	3	= RM02*	A
							1552-110	0	0	= RM05	B
33	O	C	C	O	C	C	1552-110	1	1	= RM05	B
							1552-110	2	2	= RM05	B
							1552-110	3	3	= RM05	B
							823-10	0	0	= RM02*	C
34	O	C	C	C	O	O	823-10	1	1	= RM02*	C
							711-24	2	2	= RM05*	C
							711-24	3	3	= RM05*	C
							711-24	0	0	= RM05*	C
35	O	C	C	C	O	C	711-24	1	1	= RM05*	C
							823-10	2	2	= RM02*	C
							823-10	3	3	= RM02*	C
							842-20A	0	0	= RM03*	C
36	O	C	C	C	C	O	842-20A	1	1	= RMO3*	C
							842-40	2	2	= RMO5*	C
							842-40	3	3	= RMO5*	C
							842-20A	0	0	= RM03*	C
37	O	C	C	C	C	C	842-40	1	1	= RM05*	C
							842-40	2	2	= RM05*	C
							842-40	3	3	= RM05*	C
							842-40	0	0	= RMO5*	C
40	C	O	O	O	O	O	842-40	1	1	= RMO5*	C
							842-40	2	2	= RM05*	C
							842-20A	3	3	= RMO3*	C
							823-10	0	0	= RM03*	C
41	C	O	O	O	O	C	823-10	1	1	= RM03*	C
							823-10	2	2	= RM03*	C
							823-10	3	3	= RM03*	C
							1217-10	0	0	= RM05*	D
42	C	O	O	O	C	O	1217-10	1	1	= RM05*	D
							1217-10	2	2	= RM05*	D
							1217-10	3	3	= RM05*	D
							1217-10	0	0	= RM05*	D

*Non-standard drive size. This size is not supported by DEC software or diagnostics. See Table A-6 for actual size.

Table A-6
Non-Standard Drive Sizes (PROM NO. C03)

Config.	Drive Type and Description
32 34,35	This RM02 is a 711 cylinder, 24 track, 50 sector drive. This RM02 is an 823 cylinder, 10 track, 32 sector drive.
41	This RM03 is an 823 cylinder, 10 track, 32 sector drive.
36,37, 40	This RM03 is an 842 cylinder, 20 track, 48 sector drive.
10,12, 34,35	This RM05 is a 711 cylinder, 24 track, 32 sector drive.
36,37 40	This RM05 is an 842 cylinder, 40 track, 32 sector drive.
15,16, 17,20	This RM05 is an 845 cylinder, 19 track, 50 sector drive.
23,24, 25,26	This RM05 is a 941 cylinder, 19 track, 54 sector drive.
3,4,5,6	This RM05 is a 1024 cylinder, 16 track, 34 sector drive.
42	This RM05 is a 1217 cylinder, 10 track, 50 sector drive.

Table A-7. Drives Supported (PROM No. C00)

Mfr.	Model	Key	Physical Cyl Trk Sec			Configurations
Ampex	9380	823-05	823	5	32	01, 02, 02A, 07, 07A
CDC	9715-340	711-24	711	24	32	09
CDC	9730-80	823-05	823	5	32	01, 02, 02A, 07, 07A
CDC	9762	823-05	823	5	32	01, 02, 02A, 07, 07A
CDC	9766	823-19	823	19	32	01, 01A, 02, 05, 05A, 09, 09A
Century	315	823-19A	823	19	22	08, 08A
Century	T82RM	823-05	823	5	32	01, 02, 02A, 07, 07A
Century	T300	815-19	815	19	32	0A, AA
Century	T302RM	823-19	823	19	32	01, 01A, 02, 05, 05A, 09, 09A
Memorex	677	815-19	815	19	22	05, 06, 06A
Fujitsu	2280	823-05	823	5	32	01, 02, 02A, 07, 07A
Fujitsu	2351A	842-20	842	20	44	00, 00A
Fujitsu	2351A	842-20A	842	20	48	03, 03A, 04, 04A, 07, 07A, 0B, 0BA

Table A-8. Eight Physical Disk Drive Configurations (PROM No. C00)

CONF. No.	SW3-n						PHYSICAL		LOGICAL		Rev
	6	5	4	3	2	1	KEY	Unit	Unit(s)=	Dr Type	
00	O	O	O	O	O	O	842-20	0-7	0-7 =	RP06*	A
00A	O	O	O	O	O	C	842-20	0-7	0-7 =	RP06*	A
01	O	O	O	O	C	O	823-05	0-3	0-3 =	RM03	A
							823-19	4-7	4-7 =	RM05	A
01A	O	O	O	O	C	C	823-19	0-7	0-7 =	RM05	A
02	O	O	O	C	O	O	823-19	0-3	0-3 =	RM05	A
							823-05	4-7	4-7 =	RM03	A
02A	O	O	O	C	O	C	823-05	0-7	0-7 =	RM03	A
03	O	O	O	C	C	O	842-20A	0-3	0-3 =	RM05*	A
							842-20A	4-7	4-7 =	RM80*	A
03A	O	O	O	C	C	C	842-20A	0-7	0-7 =	RM80*	A
04	O	O	C	O	O	O	842-20A	0-3	0-3 =	RM80*	A
							842-20A	4-7	4-7 =	RM05*	A
04A	O	O	C	O	O	C	842-20A	0-7	0-7 =	RM05*	A
05	O	O	C	O	C	O	815-19	0-3	0-3 =	RP06	A
							823-19	4-7	4-7 =	RM05	A
05A	O	O	C	O	C	C	823-19	0-7	0-7 =	RM05	A
06	O	O	C	C	O	O	815-19	0-7	0-7 =	RP06	B
06A	O	O	C	C	O	C	815-19	0-7	0-7 =	RP06	B
07	O	O	C	C	C	O	842-20A	0-5	0-5 =	RM05*	E
							823-05	6,7	6,7 =	RM02	E
07A	O	O	C	C	C	C	842-20A	0,1,4,5	0,1,4,5	RM05*	
							823-05	2,3,6,7	2,3,6,7	RM02	
08	O	C	O	O	O	O	823-19A	0-7	0-7 =	RP06	C
08A	O	C	O	O	O	C	823-19A	0-7	0-7 =	RP06	C
09	O	C	O	O	C	O	711-24	0-3	0-3 =	RM05	E
							823-19	4-7	4-7 =	RM05	E
09A	O	C	O	O	C	C	823-19	0-7	0-7 =	RM05	E
0A	O	C	O	C	O	O	815-19	0-7	0-7 =	RM02*	F
0AA	O	C	O	C	O	C	815-19	0-7	0-7 =	RM02*	F
0B	O	C	O	C	C	O	842-20A	0-7	0-7 =	RM02*	G
0BA	O	C	O	C	C	C	842-20A	0-7	0-7 =	RM02*	G

* Expanded or nonstandard configurations.

Table A-9
Non-Standard Drive Sizes (PROM NO. C00)

Config.	Drive Type and Description
0A,AA	This RM02 is an 815 cylinder, 19 track, 32 sector drive.
3,4,4A, 7,7A	This RM05 is an 842 cylinder, 20 track, 48 sector drive.
3,3A,4	This RM80 is an 842 cylinder, 20 track, 48 sector drive.
00,0A	This RP06 is an 842 cylinder, 20 track, 44 sector drive.
0B,0BA	This RM02 is an 842 Cylinder, 20 Track, 48 sector drive.

A.3 USER-SELECTABLE OPTIONS

The SC72/BX has several options which the user can select by means of switches in four DIP switch packs. The switches and their functions are listed and described in Table A-10.

Table A-10. Switches for User-Selectable Options

Switch(es)	State	Function
SW1-1	ON	Controller Reset; "frozen" and unable to respond to CPU. ¹
	OFF	Normal operation enabled. ¹
SW1-2	---	Not Used
SW1-3	ON	Disables a circuit that normally activates a CPU stall (via a Unibus NPR request) whenever a programmed I/O cycle occurs during a Cache Bus DMA cycle. It prevents a CPU status loop from excessively stalling the DMA cycle. The circuit needs to be disabled only for special circumstances (that usually involve non-DEC hardware that gets confused). ²
	OFF	Enables the CPU stall circuit for Normal operations. ²
SW1-4 through SW1-8	---	Device Address selection (SW1-8 ON is standard Device Address) ³
SW2-1 through SW2-8	---	Interrupt Vector Address select (bits 1 through 8) ⁴

continued on next page

Table A-10, cont.

Switch(es)	State	Function
SW3-1 through SW3-6 SW3-7	---	Disk drive configuration select (PROMs) ⁵
	OFF	4-drive configuration selected ⁶
	ON	8-drive configuration selected ⁶
SW3-8 through SW3-10	---	Not Used
SW4-1	ON	8-port B-Board in use ⁶
	OFF	4-port B-Board in use ⁶
SW4-2	---	Not Used
SW4-3	ON	Enables 2-1 hardware sector interleaving ⁷
	OFF	Disables 2-1 hardware sector interleaving ⁷
SW4-4	ON	Enables swap of logical disk drive units 0-3 with logical disk drive units 4-7 ⁸
	OFF	Disables swap of logical disk drive units 0-3 with logical disk drive units 4-7 ⁸
SW4-5	ON	Enables Replacement Track mode (RP-only) ⁹
	OFF	Disables Replacement Track mode (RP-only) ⁹
SW4-6	ON	Enables Dual-Port mode ¹⁰
	OFF	Disables Dual-Port mode ¹⁰
SW4-7	ON	Enables Dual-Access mode ¹¹
	OFF	Disables Dual-Access mode ¹¹
SW4-8	ON	Places Index and Sector signals on A-Cable ¹²
	OFF	Places Index and Sector signals on B-Cable ¹²
SW4-9	ON	Enables special RP06 mapping ¹³
	OFF	Disables special RP06 mapping ¹³
SW4-10	---	Not Used

¹ See subsection 3.5.5.1.

² See subsection 3.5.5.2.

³ See Table A-11.

⁴ See subsection 3.5.2.

⁵ See Tables A-2, A-5, and A-8.

⁶ See subsection 3.5.5.3.

⁷ See subsection 3.5.5.4.

⁸ See subsection 3.5.5.5.

⁹ See subsection 3.5.5.6.

¹⁰ See subsection 3.5.5.7.

¹¹ See subsection 3.5.5.8.

¹² See subsection 3.5.5.9.

¹³ See subsection 3.5.5.10.

Device Address selection is done with DIP switch SW1. When switch SW1-4 is open, the Address Decode PROM in IC socket U94 is selected. When switch SW1-4 is closed, the Address Decode PROM in IC socket U95 is selected. (Normally, no Address Decode PROM is installed in IC socket U95, so that IC socket is empty.) Switches SW1-5 through SW1-8 select one of four Base Address ranges available in the selected Address Decode PROM. Only ONE switch in the group SW1-5 through SW1-8 must be closed or the SC72/BX disk controller responds to multiple sets of Device Addresses. Switch positions for Device Address selection are listed in Table A-11.

Table A-11. Device Address Selection

Switch SW1-n					Controller Base Address	PROM No.	IC Socket
4	5	6	7	8			
O	O	O	O	C	1776700	992A	U94
O	O	O	C	O	1776300	992A	U94
O	O	C	O	O	1776600	992A	U94
O	C	O	O	O	1776400	992A	U94
C	O	O	O	C			U95
C	O	O	C	O			U95
C	O	C	O	O			U95
C	C	O	O	O			U95

C = CLOSED, O = OPEN

Interrupt Vector Address selection is done with DIP switches SW2-1 through SW2-8. Switch positions for the standard Interrupt Vector Address are listed in Table A-12, and some alternates are listed in Table A-13.

Table A-12. Standard Interrupt Vector Address Selection

Octal	2			5			4		
Binary	0	1	0	1	0	1	1	0	0
Address Bit	08	07	06	05	04	03	02	01	00
Switch Setting	OFF	ON	OFF	ON	OFF	ON	ON	OFF	X
Switch SW2-	8	7	6	5	4	3	2	1	X

Table A-13. Alternate Interrupt Vector Address Selection Example

Interrupt Vector Address	SW2-n							
	8	7	6	5	4	3	2	1
150	0	0	1	1	0	1	0	0
354	0	1	1	1	0	1	1	0
270	0	1	0	1	1	1	0	0

1 = closed/on, 0 = open/off

Appendix B
DISK DRIVE MODIFICATIONS

B.1 INTRODUCTION

This appendix provides modification instructions to move the Sector and Index signals, for commonly used disk drive emulations, from the A-Cable to the B-Cables.

The titles of the following subsections represent the Control Data Corporation (CDC) model numbers for disk drive types that can be modified.

Trident and Fujitsu disk drive models that are usable with the system already have Sector and Index signals on both the A-Cable and B-Cables.

B.2 CDC 9766

Remove (Channel I)

Sector + J4-55
Sector - J4-25
Index + J4-48
Index - J4-18

Remove (Channel II)

Sector + J4-55
Sector - J4-25
Index - J4-48
Index - J4-18

Move Wire (Channel I)

	<u>Origin</u>	<u>From</u>	<u>To</u>
Sector +	PA01-5B	J3-55	J2-26
Sector -	PA01-5A	J3-25	J2-13
Index +	PA01-6B	J3-48	J2-24
Index -	PA01-6A	J3-18	J2-12

Move Wire (Channel II)

	<u>Origin</u>	<u>From</u>	<u>To</u>
Sector +	PA03-5B	J3-55	J2-26
Sector -	PA03-5A	J3-25	J2-13
Index +	PA03-6B	J3-48	J2-24
Index -	PA03-6A	J3-18	J2-12

To rework FTVV Transmitter PCBA in location A01 (CHANNEL I) and A03 (CHANNEL II), use the following procedure:

- a. Locate the jumper at center-bottom of PCBA (viewed from connector on right side).
- b. Remove jumper and reinsert in position that is one set of holes lower; i.e., from center hole to hole below original jumper.

- c. Remove the letter "F" from the PCBA type designation FTVV and mark "G" in its place so that the PCBA type identification becomes GTVV.

NOTE

On later models of the 9766 disk drive, CDC will ship disk drive units that include an enhancement feature which allows easy switch-over to the B-Cable by using the following simplified procedure:

Cut cable tie that secures PD90 to I/O cable and plug PD90 into JD90 pins 13 and 14 (Channel I) and pins 11 and 12 (Channel II), as indicated on top of connector.

B.3 CDC 9775

To rework CFAX Transmitter-Receiver PCBA in location A04 (Channel I) and B04 (Channel II), use the following procedure:

- a. View PCBA with connector toward right and locate four jumper wires to left of I/O connectors and above terminator ground lug.
- b. Remove bottom end of jumper wires from holes in which they are soldered, and move each to hole directly above hole from which wire was removed.
- c. Locate small jumper wire to right of third IC from connector edge of PCBA on bottom row of ICs. Remove and relocate this jumper wire so that it connects top and middle holes instead of original connection of bottom and middle holes on PCBA. This step ungates the Sector pulse and Index pulse driver.
- d. Remove letter "C" from PCBA type designation CFAX and mark letter "D" in its place so that PCBA identification becomes DFAX.

B.4 CDC 9762

Remove (Channel I)

B01-06B to JA82-18B
B01-06A to JA82-18A
B01-05B to JA82-25B
B01-05A to JA82-25A

Add (Channel I)

B01-06B to JA82-43B
B01-06A to JA82-44A
B01-05A to JA82-45B
B01-05A to JA82-45A

Remove (Channel II)

B03-06B to JA83-18B
B03-06A to JA83-18A
B03-05B to JA83-25B
B03-05A to JA83-25A

Add (Channel II)

B03-06B to JA83-43B
B03-06A to JA83-44A
B03-05B to JA83-45B
B03-05A to JA83-45A

To rework FTVV Transmitter PCBA in location B01 (Channel I) and B03 (Channel II), use the following procedure:

- a. View PCBA with connector toward right and locate jumper wire at center-bottom of PCBA.
- b. Remove jumper wire and reinsert one set of holes in lower row; i.e., from center hole to hole below that in which original jumper wire was located.
- c. Remove letter "F" from PCBA type designation FTVV and mark a "G" in its place so that PCBA identification becomes GTVV.

NOTE

On later models of the 9762, CDC will ship disk drive units that include an enhancement feature which allows easy switch-over to the B-Cable by using the following simplified procedure:

Remove jumper plug from B07 on back panel of logic chassis.

B.5 CDC 9730

To rework CFAX Transmitter-Receiver PCBA in location A04 (Channel I) and B04 (Channel II), use the following procedure:

- a. View PCBA with connector toward right and locate four jumper wires to left of I/O connectors and above terminator ground lug.
- b. Remove bottom end of jumper wires from holes in which they are soldered, and move each to hole directly above hole from which wire was removed.

- c. Locate small jumper wire to right of third IC from connector edge of PCBA on bottom row of ICs. Remove and relocate this jumper wire so that it connects top and middle holes instead of original connection of bottom and middle holes on PCBA. This step ungates the Sector pulse and Index pulse driver.
- d. Remove letter "C" from PCBA type designation CFAX and mark letter "D" in its place so that PCBA identification becomes DFAX.

C.1 SC72/BX TRACK REPLACEMENT

The SC72/BX track replacement mode can be enabled for RP06 emulations by setting option switch SW4-5 ON. This feature works only with RP06 emulations.

Track replacement mode uses words 3 and 4 of the RP06 header to hold the disk address of the replacement track. If SW4-5 is ON and there is both a non-zero value in header word 4 and a good header CRC, the SC72/BX will use word 3 as the cylinder address of the replacement track and bits 0-7 of word 4 as the track address for the replacement track. Bit 8 of word 4 is used as a steering bit for those drives that have two logical tracks mapped onto one physical track.

If the first sector encountered has a bad header CRC, then the SC72/BX will look at subsequent sectors until it finds one with a good header CRC. If that sector has a non-zero value in word 4 then track replacement mode is activated. If not, then the original sector is considered to be a bad sector on an unreplaced track. This feature requires that all sectors on a track contain replacement information, and that those drives that have two logical tracks per physical have the entire physical track replaced.

Emulex has a program called TRACKR that can do the track replacement for a series of drives. In order to use TRACKR, the drive must have spare cylinders at the end of the drive and the emulation must be a standard size RP06 with either one or two logical units per physical drive. This program can be used in either of two modes.

In the first mode, the contents of the bad sector file created by the Emulex RM/RP formatter is used to determine the tracks that must be replaced. Because only the Emulex formatter and the DEC VAX formatter write a bad sector file on an RP06 drive, the drive must have been formatted with one of these formatters if this mode is used.

In the second mode, manual entry of the bad tracks is used to determine the tracks that must be replaced.

Both of these modes can be used at the same time. The Emulex RM/RP formatter is described in the Disk Maintenance Utility (SXBX0A) User's Guide (Emulex part number PD9950904-00). The TRACKR program is described in the Track Replacement Utility User's Guide (Emulex part number PD9950905-00).

With option switch SW4-5 ON, the following alterations to normal operations occur:

1. Track replacement is activated for all RP drives.
2. WRITE HEADER PLUS DATA commands are rejected for all RP drives and a DTE error is generated.
3. Firmware Format commands are rejected for all drives, and a DTE error is generated.

Note that none of the DEC RP04/05/06 diagnostics will run with switch SW4-5 on. Some can be made to run with additional patches. Emulex suggests that all diagnostics be run with the SW4-5 OFF, and that track replacement mode be activated only after the entire subsystem has been verified operational.



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