QT12 TAPE CONTROLLER

TECHNICAL MANUAL

3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600 TWX 910-595-2521

QT1251001-00 Rev B
May 1987

WARNING

This equipment generates, uses, and can radiate radio-frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

CABLING

In configurations where the cables that connect the controller and its tape transport run outside of the CPU cabinet (in which the controller is installed), the cables must be shielded. See Cabling, subsection 2.6.

The information in this manual is for information purposes and is subject to change without notice.

Emulex Corporation assumes no responsibility for any errors that may appear in the manual.

Printed in U.S.A.

TABLE OF CONTENTS

Section	Title	Page
ONE	**GENERAL DESCRIPTION**	
1.1	INTRODUCTION	1-1
1.2	SUBSYSTEM OVERVIEW	1-1
1.3	PHYSICAL CHARACTERISTICS	1-2
1.4	SUBSYSTEM MODELS AND OPTIONS	1-2
1.5	FEATURES	1-4
1.6	LIMITATIONS	1-4
1.7	COMPATIBILITY	1-5
1.7.1	MEDIA COMPATIBILITY	1-5
1.7.2	SOFTWARE COMPATIBILITY	1-5
1.7.3	HARDWARE COMPATIBILITY	1-5
1.8	SPECIFICATIONS	1-6
TWO	**INSTALLATION**	
2.1	OVERVIEW	2-1
2.2	INSPECTION	2-1
2.3	PLANNING YOUR INSTALLATION	2-1
2.3.1	MAINTAINING FCC CLASS A COMPLIANCE	2-1
2.3.2	CONFIGURATION OPTIONS	2-2
2.3.3	TAPE TRANSPORT CONFIGURATION	2-2
2.3.4	PHYSICAL LOCATION	2-2
2.4	QT12 TAPE CONTROLLER CONFIGURATION	2-2
2.4.1	TAPE CONTROLLER BASE ADDRESS SELECTION	2-5
2.4.2	INTERRUPT VECTOR ADDRESS SELECTION	2-5
2.4.3	INTERRUPT PRIORITY LEVEL	2-6
2.4.4	EXTENDED FEATURES	2-7
2.4.5	DRIVE TYPE AND SIZE	2-7
2.4.6	DIAGNOSTIC ENABLE	2-7
2.4.7	BLOCK MODE DMA	2-8
2.4.8	TAPE RETENSION	2-8
2.4.9	SPARE	2-8
2.5	QT12 TAPE CONTROLLER INSTALLATION	2-8
2.6	CABLING	2-9
2.6.1	RFI SUPPRESSION	2-9
2.6.1.1	DEC BA23	2-10
2.6.1.2	Other Computers	2-10
2.6.2	STANDARD CABLING	2-13
2.6.3	GROUNDING	2-14
THREE	**TROUBLESHOOTING**	
3.1	OVERVIEW	3-1
3.2	SERVICE	3-1
3.3	POWER-UP SELF-DIAGNOSTIC	3-2
FOUR	**COUPLER REGISTERS AND PROGRAMMING**	
4.1	OVERVIEW	4-1
4.2	CONTROLLER REGISTERS	4-1
4.2.1	DATA BUFFER REGISTER (TSDB)	4-1

.2 BUS ADDRESS REGISTER (TSBA) 4-2
.3 STATUS REGISTER (TSSR) 4-3
.4 EXTENDED DATA BUFFER REGISTER (TSDBX) 4-5
.5 RESIDUAL BYTE/RECORD/FILE COUNT REGISTER (RBPCR) . 4-6
.6 EXTENDED STATUS REGISTER 0 (TXST0) 4-7
.7 EXTENDED STATUS REGISTER 1 (TXST1) 4-9
.8 EXTENDED STATUS REGISTER 2 (TXST2) 4-10
.9 EXTENDED STATUS REGISTER 3 (TXST3) 4-11
.10 EXTENDED STATUS REGISTER 4 (TXST4) 4-12
COMMAND PROCESSING 4-13
.1 COMMAND PACKET FORMAT 4-14
.2 COMMAND SET 4-15
.2.1 Read Command 4-16
.2.2 Write Characteristics Command 4-17
.2.3 Write Command 4-20
.2.4 Position Command 4-21
.2.5 Format Command 4-22
.2.6 Control Command 4-22
.2.7 Initialize Command 4-23
.2.8 Get Status Command 4-23
.3 BUFFER OWNERSHIP AND CONTROL 4-24
.4 MESSAGE PACKET FORMAT 4-24
.4.1 Message Packet Header Word 4-25
.4.2 Data Field Length Word 4-26

'E **SOFTWARE**

OVERVIEW 5-1
LIMITATIONS..... 5-1
DEC DIAGNOSTICS 5-1
EMULEX DIAGNOSTICS 5-1
RT-11 5-2
.1 BACKUP UTILITY PROGRAM (BUP) 5-2
.2 DEVICE UTILITY PROGRAM (DUP) 5-2
.3 PERIPHERAL INTERCHANGE PROGRAM (PIP) 5-2
.4 SOURCE AND BINARY COMPARE UTILITIES (SRCCOM and BINCOM) 5-2
.5 MAKING A BOOTABLE RT-11 TAPE 5-3
RSX-11M 5-3
.1 BACKUP AND RESTORE UTILITY (BRU) 5-4
.1.1 Creating a Bootable BRU Tape 5-4
.1.2 Restoring a Bootable BRU Tape 5-4
.2 DISK SAVE AND COMPRESS UTILITY (DSC) 5-4
RSTS/E 5-4
.1 SAVE AND RESTORE UTILITY (SAV/RES) 5-4
.2 BACKUP UTILITY (BACKUP) 5-4
.3 PERIPHERAL INTERCHANGE PROGRAM PIP 5-5
MicroVMS..... 5-5
.1 COPY UTILITY (COPY)..... 5-5
.2 STANDALONE BACKUP UTILITY..... 5-5
.3 BACKUP UTILITY (BACKUP)..... 5-5
.4 EXCHANGE UTILITY..... 5-6

SIX TECHNICAL DESCRIPTION

6.1 OVERVIEW	6-1
6.2 QT12 BLOCK DIAGRAM	6-1
6.2.1 MICROENGINE	6-1
6.2.2 LSI-11 BUS INTERFACE	6-3
6.2.3 TAPE TRANSPORT INTERFACE	6-5
6.3 TAPE FORMAT	6-7
APPENDIX A RELATED DOCUMENTATION	A-1
APPENDIX B QT12 BOOTSTRAP PROGRAM	B-1
APPENDIX C GLOSSARY	C-1
C.1 OVERVIEW	C-1
C.2 DEFINITIONS	C-1

LIST OF FIGURES

Figure 1-1. QT12 Tape Controller..... 1-3
Figure 2-1. QT12 Configuration Reference Sheet..... 2-3
Figure 2-2. QT12 Tape Controller Configuration Jumper Locations..... 2-4
Figure 2-3. CU2220301 Bulkhead Distribution Panel..... 2-11
Figure 2-4. RFI-Suppression Cable Installation..... 2-12
Figure 2-5. Connector Pin Definitions..... 2-14
Figure 4-1. Command Packet Header Word..... 4-14
Figure 4-2. Read Command Packet..... 4-17
Figure 4-3. Write Characteristics Command Packet and Characteristics Data..... 4-18
Figure 4-4. Write Command Packet..... 4-21
Figure 4-5. Position Command Packet..... 4-22
Figure 4-6. Format Command Packet..... 4-22
Figure 4-7. Control Command Packet..... 4-23
Figure 4-8. Initialize Command Packet..... 4-23
Figure 4-9. Get Status Command Packet..... 4-24
Figure 4-10. Message Packet..... 4-25
Figure 6-1. QT12 Tape Controller Block Diagram..... 6-2
Figure 6-2. QT12 Tape Controller QIC-24 Tape Format..... 6-8

LIST OF TABLES

Table 1-1.	Basic QT12 Subsystem Contents	1-2
Table 1-2.	QT12 Software Options	1-4
Table 1-3.	QT12 Tape Coupler Specifications	1-6
Table 2-1.	Base Address Configuration	2-5
Table 2-2.	Interrupt Vector Configuration: Standard Address	2-6
Table 2-3.	Interrupt Priority Level Configuration	2-6
Table 2-4.	Drive Type and Size Configuration	2-7
Table 2-5.	Shielded Cables and Installation Hardware	2-13
Table 3-1.	Flowchart Symbol Definitions	3-2
Table 4-1.	Status Register Bit Definitions	4-3
Table 4-2.	Termination Class Codes	4-5
Table 4-3.	Extended Data Buffer Register Bits	4-6
Table 4-4.	TXST0 Bit Definitions	4-7
Table 4-5.	TXST1 Bit Definitions	4-10
Table 4-6.	TXST2 Bit Definitions	4-11
Table 4-7.	TXST3 Bit Definitions	4-12
Table 4-8.	TXST4 Bit Definitions	4-13
Table 4-9.	Command Packet Header Word Bit Definitions	4-14
Table 4-10.	Command Code and Command Mode Field Definitions	4-15
Table 4-11.	Characteristics Mode Word Bit Definitions	4-19
Table 4-12.	Message Packet Header Word Bit Definitions	4-25
Table 4-13.	Data Field Length Word Bit Definitions	4-26
Table 6-1.	LSI-11 Bus Interface Pin Assignments	6-5
Table 6-2.	Input/Output Pin Assignments	6-6

EMULEX PRODUCT WARRANTY

CONTROLLER WARRANTY:Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adapters, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product is such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and, unless otherwise stated, pay return transportation cost for such replacement.

Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement. THE EXPRESSED WARRANTIES SET FORTH IN THIS AGREEMENT ARE IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, AND ALL OTHER WARRANTIES ARE HEREBY DISCLAIMED AND EXCLUDED BY EMULEX. THE STATED EXPRESS WARRANTIES ARE IN LIEU OF ALL OBLIGATIONS OR LIABILITIES ON THE PART OF EMULEX FOR DAMAGES, INCLUDING BUT NOT LIMITED TO SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES ARISING OUT OF, OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THE PRODUCT.

RETURNED MATERIAL: Warranty claims must be received by Emulex within the applicable warranty period. A replaced product, or part thereof, shall become the property of Emulex and shall be returned to Emulex at Purchaser's expense. All returned material must be accompanied by a RETURN MATERIALS AUTHORIZATION (RMA) number assigned by Emulex.

1.1 INTRODUCTION

This manual provides information related to the capabilities, design, installation, and use of the Emulex QT12 Tape Controller. The manual contains six sections and three appendices:

Section 1	**General Description.** This section contains an overview of the QT12 Tape Controller.
Section 2	**Installation.** This section contains the information necessary to plan your installation and to install the QT12.
Section 3	**Troubleshooting.** This section describes fault isolation procedures for maintaining optimum performance of the QT12.
Section 4	**Controller Registers and Programming.** This section describes the registers and command packets.
Section 5	**Software.** This section describes diagnostic and operating system software compatible with the QT12.
Section 6	**Technical Description.** This section describes QT12 architecture and interfaces.
Appendix A	**Related Documentation.** This section provides complete references and ordering information for related manuals.
Appendix B	**QT12 Bootstrap Program.** This appendix provides code for use in bootstrapping a QT12 tape.
Appendix C	**Glossary.** Defines technical terms used in this document.

1.2 SUBSYSTEM OVERVIEW

The QT12 is an intelligent, microprocessor-based tape controller that emulates the Digital Equipment Corporation (DEC) TSV05 subsystem, within the constraints of the streaming cartridge drive. It interfaces with standard QIC-02 compatible drives, and provides cost-effective backup for small system or tabletop applications.

1.3 PHYSICAL CHARACTERISTICS

The QT12 is located on a single dual-height printed circuit board assembly (PCBA). The PCBA plugs directly into any LSI-11 bus slot and into connectors A and B of the backplane (or connectors C and D of a serpentine backplane), from which it draws its power. A 50-conductor flat ribbon cable connects the QT12 to the QIC-02 type tape drive.

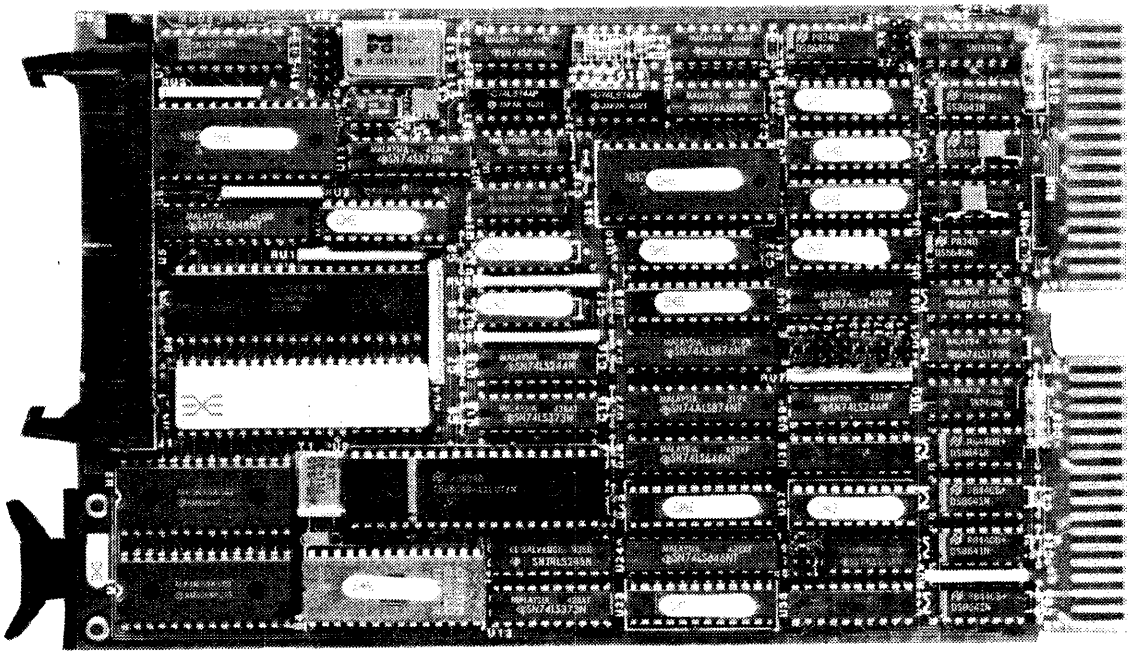
1.4 SUBSYSTEM MODELS AND OPTIONS

The QT12 Tape Controller is pictured in Figure 1-1. A single model is offered.

Table 1-1 lists part numbers for the QT12 and other items included with it. Table 1-2 lists and describes available software options.

Table 1-1. Basic QT12 Subsystem Contents

Item	Qty	Description	Part Number	Comment
1	1	QT12 Tape Controller	1200032	
2	1	QT12 Technical Manual	QT1251001	
3	1	QT12 Board Level Cabling Kit	QT1213003	Optional
4	1	QD01/QT12 Board Level Cabling Kit	QD0113004	Optional



QT1201-0709

Figure 1-1. QT12 Tape Controller

Table 1-2. QT12 Software Options

Part Number	Description
VX9951804	QT12/TC03 TS11 Emulation Installation Diagnostic (IQT12) for DEC MicroVAX I and II.
PX9951805	QT12 Logic and Data Reliability Diagnostic (T1QX3A) for DEC LSI-11 systems.
VD9951803	MicroVMS TS11 Software Driver (TSDRIVER), which makes your QT12 compatible with MicroVMS.

1.5 FEATURES

The principal features of the QT12 Tape Controller are summarized in the following table. For details regarding these features, refer to the subsections, figures, or tables indicated.

Feature	Reference
Dual-height board	Figure 1-1
Optional configuration jumpers	Table 2-1; Subsection 2.4
Internal micro-diagnostics	Subsection 3.4
Block mode DMA support	Subsection 2.4.7
Twenty-two-bit addressing capability	Subsection 2.4.4
DEC TSV05/TS11 compatibility	Subsections 1.2, 1.7, 2.4.4
Interface capability with low-cost QIC-02 streaming cartridge drives	Subsections 1.7, 2.4.5
Record buffering	Subsection 6.2.1

1.6 LIMITATIONS

The major limitation imposed by QIC-02 drives is their inability to overwrite existing files. This limitation prevents the QT12 from implementing any function that implies a destructive write. See Table 4-10 for supported functions. The drive contains imbedded automatic verification rewrite logic, so neither the Write Data Retry command nor the Write Tape Mark Retry command is necessary.

Most of the available 0.25-inch cartridge tape drives inhibit any attempt to overwrite previously recorded data, because of the unsaturated recording method and the lack of a track erase head. An erase bar is available to write on track 0 while simultaneously erasing the full width of the tape. In normal use, the operating system software does not implement destructive writes. The QT12 incorporates a pseudo-overwrite feature which allows a rewrite of the tape controller buffer before the data is actually sent out to the tape drive. This feature allows proper operation of most DEC software (see Section 5, SOFTWARE).

Positioning functions are implemented to the extent that they allow proper operation of DEC operating systems and utilities. See Table 4-10 for supported functions.

The QT12 cannot be used with 300-foot tapes, because these do not function reliably with streaming cartridge tape transports. The QT12 measures tape length and rejects 300-foot tapes with a Function Reject error condition. QT12 can use the DC300XL tapes which are 450 feet long or DC600A tapes which are 600 feet long.

1.7 COMPATIBILITY

1.7.1 MEDIA COMPATIBILITY

The DEC TSV05 subsystem is based on industry standard 0.5-inch nine-track tape, recorded at 1600 bits per inch (bpi) in various formmats. The most common format, ANSI standard, provides a convenient means of interchange with DEC and other available systems.

Major manufacturers of QIC-02 compatible drives, with which the QT12 is compatible, use 0.25-inch cartridge tapes and record in QIC-24 format (subsection 6.3).

NOTE

Emulex strongly recommends using only certified error-free tape cartridges. When an error is encountered, the QIC-02 controller on the tape drive will exhaustively attempt to recover from the error by rereading a block of data. Some operating systems drivers will time-out during this recovery period. Use of certified tapes will minimize this possibility.

1.7.2 SOFTWARE COMPATIBILITY

The QT12 Tape Controller is designed to operate with the basic utilities in DEC's RT11, RSTS, RSX-11M, and MicroVMS operating

systems. These utilities include PIP, BRU, DSC, BACKUP and others. In addition, the new utility BUP (RT11) is supported. The QT12 is compatible with DEC's TSV05 packet protocol. For more information regarding software restrictions, see Section 5.

1.7.3 HARDWARE COMPATIBILITY

The QT12 Tape Controller is compatible with DEC LSI-11, LSI-11/2, LSI-11/23, LSI-11/73, and MicroVAX I and II processors. The board plugs directly into any standard Q-22 LSI-11 backplane.

The QT12 interfaces with most standard QIC-02 compatible 5.25-inch full height or half height streaming drives. The following drives have been tested with the QT12 and are presently supported:

Archive model 5945L-2
Cipher Data model 540CT
Kennedy model 6510
Tandberg Data model 3309
Wangtek model 5099EG24

1.8 SPECIFICATIONS

Table 1-3 contains the general specifications for the QT12 Tape Controller.

Table 1-3. QT12 Tape Controller Specifications

Parameter	Characteristics
FUNCTIONAL	
Emulation	TSV05
Number of Tape Transports Supported	One
Tape Transport Interface	QIC-02
Media Compatibility	QIC-02 compatible 0.25-inch cartridge tapes, QIC-24 format.
Priority Level	Standard - BRQ5 Alternate - BRQ4
Data Buffering	32 x 512 bytes
Self-Test	Extensive internal self-test on power-up
(Continued)	

Table 1-3. QT12 Tape Controller Specifications (Cont'd)

Indicator	Single LED remains ON to indicate successful completion of power-up self diagnostics.
PHYSICAL	
Size:	Single dual-height, standard length module
Connectors:	1. Standard Q-22 LSI-11 bus edge connector using A and B rows (or C and D rows in a serpentine backplane). 2. One 50-pin right-angle flat cable connector, located at the handle end of the module, for interface to industry-standard QIC-02 drives. **Maximum cable length is three meters.**
Jumpers:	BERG 76264-101 pin jumpers or #30 wire wrap jumpers used to select address, vector, interrupt priority, block mode control, extended features, and various drive characteristics.
ELECTRICAL	
Power	+5 volts (VDC) ± 5 percent at 3 amperes (A) maximum
LSI-11 Bus Interface	Adheres to DEC Q-22 specification, but does not generate or check parity. Uses only A and B rows (or C and D rows in a serpentine backplane). Receives the following LSI-11 bus signals: BDAL00-BDAL21, BDIN, BDOUT, BSYNC, BRPLY, BWTBT, BBS7, BIRQ4, BIRQ5, BIRQ6, BIAKI, BDMGI, BSACK, BINIT, BREF. Drives the followng LSI-11 bus signals: BDAL00-BDAL21, BDIN, BDOUT, BSYNC, BRPLY, BWTBT, BBS7, BIRQ4, BIRQ5, BIAKO, BDMR, BDMGO, BSACK.
(Continued)	

Table 1-3. QT12 Tape Controller Specifications (Cont'd)

Tape Transport Interface	Does not interface the following LSI-11 bus signals: BHALT, BDCOK, BPOK, BEVNT. Adheres to ANSI X3T9.6183-20 specifications, QIC-02 device level interface for streaming cartridge tape drives. Transmitter: Signal assertion = 0 to 0.8 VDC Minimum drive capability = 24 milliamperes (mA) (sink) at 0.50 VDC Signal non-assertion = 2.5 to 5.25 VDC Signal type = Tristate Receiver: Signal assertion = 0 to 0.8 VDC Input load (maximum) = 0.4 mA at 0.4 VDC Signal non-assertion = 2.0 to 5.25 VDC Hysteresis = 0.2 VDC Receives the following signals: CB7-CB0, ACK, RDY, EXC, DIR. Transmits the following signals: CB7-CB0, ONL, REQ, RST, XFR. Does not interface to the following signal: CBP.

(Continued)

Table 1-3. QT12 Tape Controller Specifications (Cont'd)

ENVIRONMENTAL	
Temperature:	5 to 50 degrees Celsius (41 to 122 degrees Fahrenheit)
Humidity:	10 to 90 percent (non-condensing)
PERFORMANCE	
Transfer rate:	Burst 200K bytes/second Average 86.7K bytes/second
Capacity:	Limits established by drive characteristics and tape length. (Not compatible with 300-foot tapes.) The DC300XL tape has an approximate capacity of 45 unformatted MBytes or 91,000 data blocks. The DC600A tape has an approximate capacity of 60 unformatted MBytes or 120,000 data blocks.
RELIABILITY	
MTBF	32,300 hours
MTTR	0.5 hour

BLANK

Section 2
INSTALLATION

2.1 OVERVIEW

This section describes the step-by-step procedure for installation of the QT12 Tape Controller in an LSI-11 bus environment. The section is divided into eight subsections, as listed in the following table:

Subsection	Title
2.1	Overview
2.2	Inspection
2.3	Planning Your Installation
2.4	Configuration
2.5	Installation
2.6	Tape Transport Preparation
2.7	Cabling
2.8	Testing

2.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, inspect the shipping container. Report any indication of damage to the carrier company in accordance with instructions on the form included in the container.

Unpack the QT12 and inspect it for bent or broken connector pins, damaged components, or other damage. Examine the PROMs to ensure that each is properly seated in its socket. Verify that the model or part number designation, revision level, and serial number agree with those on the shipping invoice. This verification is important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

2.3 PLANNING YOUR INSTALLATION

2.3.1 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the QT12 Tape Controller PCBA with DEC computers that comply with FCC Class A limits for radiated and conducted radio-frequency interference (RFI). When properly installed, the QT12 complies with FCC regulations for Class A equipment.

When you have finished installing the QT12 Tape Controller system--QT12, personality panels, blank panels (if any), bulkhead distribution panels (if any), tape transports, and shielded cables--

there must be no gap in the shielding which would allow RFI radiation. Subsection 2.6.1 explains the procedures required to maintain shield integrity and to limit radiated RFI.

2.3.2 CONFIGURATION OPTIONS

The QT12 is shipped with standard options configured, such as device address, interrupt vector, interrupt priority level, and operation mode. These assignments can be modified by means of jumpers, as explained in subsection 2.4. During installation, you should record the subsystem configuration on the configuration reference sheet (Figure 2-1). This information will aid in troubleshooting.

The QT12 supports only a single cartridge tape transport, so planning the subsystem configuration should be a relatively simple matter. You should decide on the available options **before** installing the board in the CPU backplane, because the jumpers are not accessible after the board is in place.

2.3.3 TAPE TRANSPORT CONFIGURATION

The tape transport must also be configured prior to installation. Configuration of supported cartridge tape drives is a simple procedure; for instructions, refer to the manufacturer's technical manual. Subsection 2.4.4 of this document explains selection of transport speed.

2.3.4 PHYSICAL LOCATION

Unpack and install the cartridge tape transport as instructed in the manufacturer's manual. Position and level it in its final place before beginning installation of the QT12, so that I/O cable routing and length requirements can be determined accurately. Maximum cable length is three meters.

Use common sense when selecting a location for the QT12 subsystem. For example, it should not be exposed to heat, direct sunlight, vibration, or other unfavorable environmental conditions.

2.4 QT12 TAPE CONTROLLER CONFIGURATION

When delivered, the QT12 is configured for operation with standard nine-track QIC-02 interface tape drives. Alternate options are selected by means of jumpers (Figure 2-2; Table 2-1). See subsection 1.8 for jumper requirements.

QT12 CONFIGURATION REFERENCE SHEET

GENERAL INFORMATION

1. Host Computer Type _____
2. Host Computer Operating System _____
   Version _____
3. Tape Drive manufacturer & Model No. _____

QT12 SETUP RECORD

1. Controller Top Assembly Number _____
2. Serial Number _____
3. Warranty Expiration Date _____
4. LSI-11 Bus Address _____
5. Vector Address _____
6. Tape Drive Configuration Selections: _____
   _____
7. Jumper Settings:

OUT (1)	JUMPER	IN (0)	FUNCTION	FACTORY STATUS	REFERENCE
NA	E1 - E2	NA	Not Used	NA	
Disable	E5 - E6	Enable	Retension tape when tape is installed	IN (Enabled)	2.4.8
Disable	E7 - E8	Enable	Diagnostic Enable	OUT (Disabled)	2.4.6
1	E9 - E10	0	Address Select Bit 0	IN (0)	2.4.1
1	E11 - E12	0	Address Select Bit 1	IN (0)	2.4.1
Disable	E13 - E14	Enable	Spare	IN (Enabled)	2.4.9
Disable	E15 - E16	Enable	Extended Features	IN (Enabled)	2.4.4
QIC-24	E17 - E18	QIC-11	Drive Size	OUT (QIC-24)	2.4.5
9 Track	E19 - E20	4 Track	Drive Type	OUT (9 Track)	2.4.5
1	E21 - E22	0	Interrupt Vector Bit 7	OUT (1)	2.4.2
1	E23 - E24	0	Interrupt Vector Bit 6	IN (0)	2.4.2
1	E25 - E26	0	Interrupt Vector Bit 5	IN (0)	2.4.2
1	E27 - E28	0	Interrupt Vector Bit 4	OUT (1)	2.4.2
1	E29 - E30	0	Interrupt Vector Bit 3	IN (0)	2.4.2
1	E31 - E32	0	Interrupt Vector Bit 2	OUT (1)	2.4.2
Disable	E33 - E34	Enable	Interrupt Priority Level 5	IN (Enabled)	2.4.3
Disable	E35 - E36	Enable	Interrupt Priority Level 4	OUT (Disabled)	2.4.3
Disable	E37 - E38	Enable	Block Mode DMA	OUT (Disabled)	2.4.7

QT1201-0836

Figure 2-1. QT12 Configuration Reference Sheet

STEP	REFERENCE SUBSECTION
1. Unpack and inspect the controller	2.2
2. Configure theQT12 by selecting jumper locations	2.4
a. Tape controller base address	2.4.1
b. Interrupt vector address	2.4.2
c. Interrupt priority level	2.4.3
d. Extended features	2.4.4
e. Drive type and size	2.4.5
f. Diagnostic Enable	2.4.6
g. Block Mode DMA	2.4.7
3. Install the QD12 controller in the LSI-11 Bus	2.5
4. Cabling	2.6
a. Verify cabling needs meet standards for RFI suppression	2.6.1
b. Standard cabling	2.6.2
c. Grounding	2.6.3
5. Power up self-diagnostic	3.4

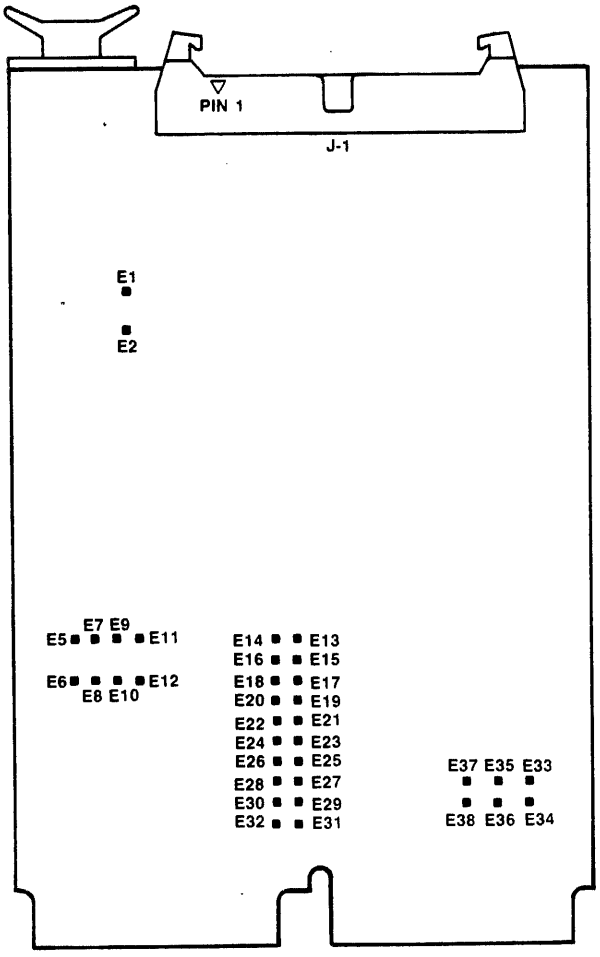


Figure 2-2. QT12 Tape Controller Configuration Jumper Locations

2.4.1 TAPE CONTROLLER BASE ADDRESS SELECTION

The **base address** serves to distinguish the QT12 from other devices on the LSI-11 bus. The QT12 is shipped with its address set to 172520 octal. Any change in base address selection requires a corresponding change in system software. Three alternate device addresses are jumper selectable (Table 2-1):

172524_8
172530_8
172534_8

DEC has reserved the base address range 172520 through 172536 for TS11/TSV05-type devices. The autoconfigure utilities for all recent DEC operating systems automatically detect a tape controller in this address range and connect it to the system. For details, consult the system generation reference manual for your operating system.

Table 2-1. Base Address Configuration

Option	Jumpers E11 - E12	Jumpers E9 - E10
Standard Address* 172520_8	IN	IN
Alternate Address 1 172524_8	OUT	IN
Alternate Address 2 172530_8	IN	OUT
Alternate Address 3 172534_8	OUT	OUT

* Factory status

2.4.2 INTERRUPT VECTOR ADDRESS SELECTION

The **interrupt vector** is a storage location that contains the starting address of a procedure to be executed when a given interrupt occurs. The QT12 is shipped with the interrupt vector preset to 224 octal. Jumpers can be used to select alternate vector assignments in the range 0 through 374 octal, as shown by the example in Table 2-2. Any change in interrupt vector selection requires a corresponding change in system software.

Table 2-2. Interrupt Vector Configuration: Standard Address

	Vector Address								
Octal		2			2			4	
Binary	0	1	0	0	1	0	1	X	X
Address Bit	08	07	06	05	04	03	02	01	00
Jumper Status	-	OUT	IN	IN	OUT	IN	OUT	X	X
Jumper	- -	E21- E22	E23- E24	E25- E26	E27- E28	E29- E30	E31- E32	- -	- -

2.4.3 INTERRUPT PRIORITY LEVEL

The QT12 supports the four-level device interrupt priority scheme that is required for compatibility with the LSI-11/23, but only two levels can be selected: 4 or 5 (Table 2-3). The controller is shipped with the priority level set to 5, as required for MicroVAX I and II, LSI-11/23, and LSI-11/73 systems. For LSI-11 and LSI-11/2 systems, set the priority level to 4.

The controller asserts interrupt requests and monitors higher-level request lines during interrupt arbitration. The level 4 request is always asserted by the QT12, regardless of its priority, in order to maintain compatibility with LSI-11 and LSI-11/2 processors.

Table 2-3. Interrupt Priority Level Configuration

	Jumpers	
Option	E33 - E34	E35 - E36
Interrupt Priority Level 5*	IN	OUT
Interrupt Priority Level 4	OUT	IN
* Factory status		

2.4.4 EXTENDED FEATURES

The Extended Features mode of operation includes 22-bit addressing and other functions and status. The QT12 is shipped with this option enabled. To disable it, remove jumper E15-E16. The Extended Features mode includes the following features:

- The QT12 generates a 22-bit address compatible with DEC's TSV05 subsystem. With this mode disabled, it generates an 18-bit address compatible with the DEC TS11.
- Bit 05 of the Extended Characteristics word (subsection 4.3.2.2) is used to select tape transport speed, which is also reflected in bit 15 of TXST4.
- The Write Retry Count field in TXST4 (subsection 4.2.10) can be examined in the message terminating the command **after** the Write operation. This field will always be zero, however, because streaming drives deal with errors automatically.

2.4.5 DRIVE TYPE AND SIZE

The QT12 interfaces with one QIC-02 drive, which is configured as physical drive 0. The factory configuration is for standard QIC-24 format nine-track drives only, but QIC-11 format and four-track drives are jumper selectable options (Table 2-4).

Table 2-4. Drive Type and Size Configuration

Drive Type/Size	Jumpers E17 - E18	Jumpers E19 - E20
QIC-24*	NA	OUT
QIC-11	NA	IN
Nine-track*	OUT	NA
Four-track	IN	NA

* Factory status

2.4.6 DIAGNOSTIC ENABLE

When this option is selected, the the QT12 operates its self-diagnostics continuously and all other controller operations are suspended (subsection 3.4). The QT12 is shipped with this option disabled. To enable it, install jumper E7-E8.

2.4.7 BLOCK MODE DMA

The QT12 is shipped with the Block Mode DMA option disabled. If your system has block mode memory, enable this feature by installing jumper E37-E38. MicroVAX II does not support block mode memory.

2.4.8 TAPE RETENSION

System loading causes many repositions of the tape cartridge. The tape becomes too tight, resulting in I/O errors and subsystem position errors. Retensioning the tape, running the tape from front to back at high speed, redistributes tape tension and helps avoid errors. If at any time it is suspected that the tape has become too tight and is causing errors, remove the tape cartridge and reinsert it. This will cause the tape to be retensioned. The process takes approximately two to four minutes to complete.

2.4.9 SPARE

Factory test jumpers E13-E14 must be IN (enabled).

2.5 QT12 TAPE CONTROLLER INSTALLATION

Power down the system and place the main AC circuit breaker at the rear of the cabinet in the OFF position. (The AC power indicator may remain lighted without indicating a potential hazard.)

WARNING

TO AVOID POSSIBLE INJURY AND EQUIPMENT DAMAGE, YOU MUST TURN OFF THE POWER BEFORE BEGINNING INSTALLATION.

The QT12 may be assigned to any backplane slot, because it uses the LSI four-level interrupt scheme to perform distributed interrupt arbitration. There must be no unused slots, however, between the CPU and the QT12.

CAUTION

Some manufacturers of LSI-11 bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing a QT12 in such a system will cause damage to the QT12.

To install the QT12 in the CPU cabinet, use the procedure appropriate to your system. See also subsection 2.6 for cabling instructions.

For MicroVAX or MicroPDP Installation:

1. Remove the rear cover from the chassis to expose the patch panel. The rear cover is held on by snap pads. Grasp the cover at the top and bottom, and pull straight back.

2. Loosen the captive screws from the patch panel using a standard screwdriver.

3. Remove the patch panel.

4. Find the flat-ribbon cable that connects the CPU module to the patch panel. For easier board installation, you may disconnect the CPU flat-ribbon cable from the patch panel.

5. Do not replace the patch panel until the installation has been verified.

For LSI-11 Series Installation:

1. Remove the cover door or panel of the CPU cabinet and select a slot for the QT12. Be sure to preserve DMA continuity.

2. Do not replace the cover until the installation has been verified.

For all systems, continue with the following steps:

1. Insert the QT12 into the selected slot, with the component side facing the same direction as the other boards.

2. Connect the socket connector of the tape drive cable (subsection 2.6.2) to the appropriate header at the edge of the QT12 board, aligning pin 1 (red) on the cable with the connector arrow (Figure 2-2). If RFI-suppression devices are required, see subsection 2.6.1 for further instructions.

3. Place the Run/Halt switch on the CPU to the Halt position, and turn on the CPU.

4. Verify that the green LED on the QT12 board edge is illuminated, indicating successful completion of the power-up micro-diagnostics.

5. If the standard address has been selected (subsection 2.4.1), open the TSDB register by entering 172520_8 via console ODT. The processor will display the contents of the TSDB register, which at this point is typically 377_8.

6. Open the TSSR register (location 172522_8 if the standard address was selected) by using console ODT. The contents of this location should be 002200_8.

7. Run the appropriate Emulex diagnostics (Section 1, Table 1-2 to verify operation of the subsystem.

2.6 CABLING

2.6.1 RFI SUPPRESSION

RFI-suppression devices are required if the CPU cabinet does not provide complete shielding, or if the tape transport and tape controller are housed in separate cabinets. If your cabinet provides complete shielding and the tape transport and QT12 are in the same cabinet, **skip this subsection** and proceed to subsection 2.6.2.

2.6.1.1 DEC BA23

Emulex provides RF suppression devices for a number of QT12 configurations. Two complete cabling kits (see Table 1-1, Page 1-2) are available for use with the QT12 when installed in DEC BA23 cabinets. See your salesman for further details.

2.6.1.2 Other Computers

For cabinets other than the DEC BA23, Emulex provides these generic RF suppression devices. Emulex RFI-suppression devices include personality panels (CU22 panel), unshielded cables for connections within the equipment cabinet, and shielded cables that are routed between the cabinets (Table 2-5). For older equipment panels that lack the bulkhead with apertures for blank panels and personality panels, Emulex provides a special bulkhead distribution panel (Figure 2-3, Table 2-5).

To install the Emulex RFI-suppression device, see Figure 2-4, and use the following procedure.

1. Install the personality panel in a convenient aperture in the rear bulkhead of the CPU cabinet. (If the cabinet has the older type of equipment panel, replace it with the bulkhead distribution panel.) Finger-tighten the eight captive screws and verify that no gaps remain.

2. Install two personality panels in convenient apertures in the rear bulkhead of the equipment cabinet that contains the tape transport. Tighten and check as in Step 1.

3. Select a shielded extension cable long enough to reach from the CPU cabinet to the tape transport cabinet. Maximum cable length is three meters.

4. Strip about 1 inch of insulation from one end of the cable. Cut the shield at each edge and fold it back over the insulation. Route the prepared cable end through the appropriate slot in the personality panel, and clamp the exposed shielding securely in the personality panel (see Figure 2-4). Repeat for the other end of the cable.

5. Select an unshielded interface cable long enough to reach from connector J1 on the QT12 to the associated personality panel in the cabinet bulkhead.

6. Align the arrow on the cable connector (pin 1) with the arrow on connector J1. Push the connectors firmly together.

7. Select an unshielded interface cable (P/N TU1211203) long enough to reach from the connector on the tape transport to the associated personality panel on the rear bulkhead of the tape transport cabinet.

8. Find and align the arrows that identify pin 1 on the mating connectors at each end of the unshielded interface cable, and connect the mating connectors.

9. Close the bulkhead door or panel on each equipment cabinet.

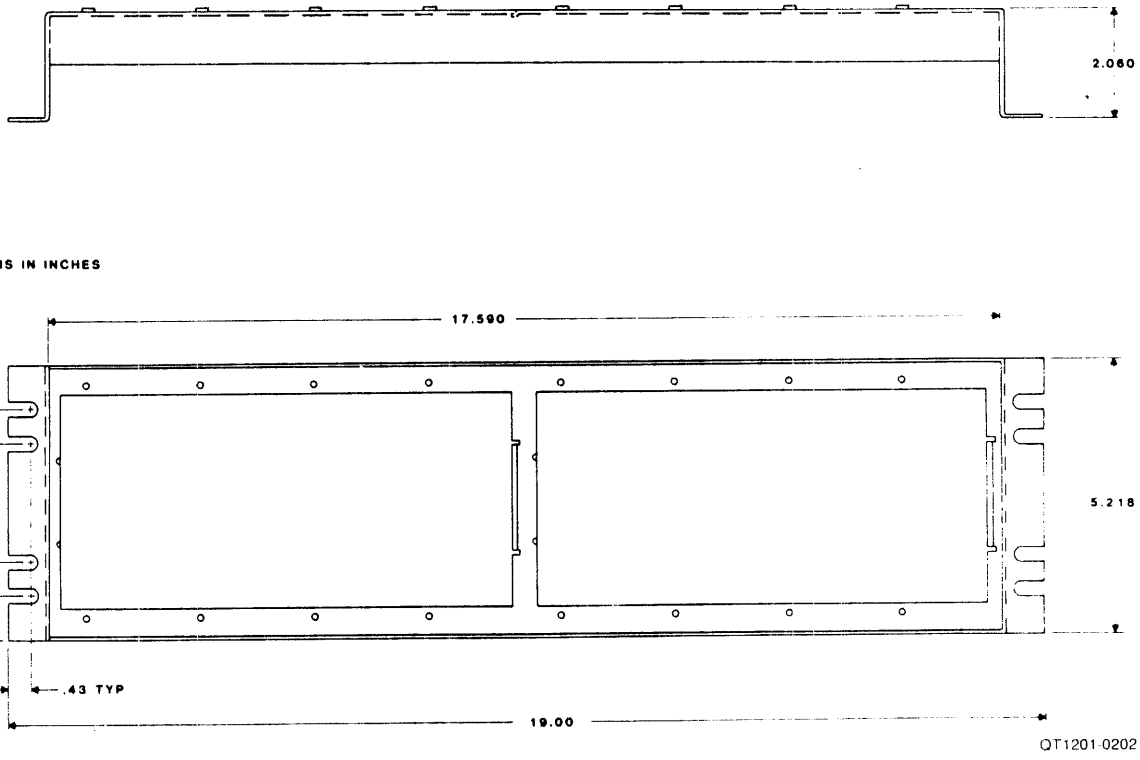


Figure 2-3 CU220301 Bulkhead Distribution Panel

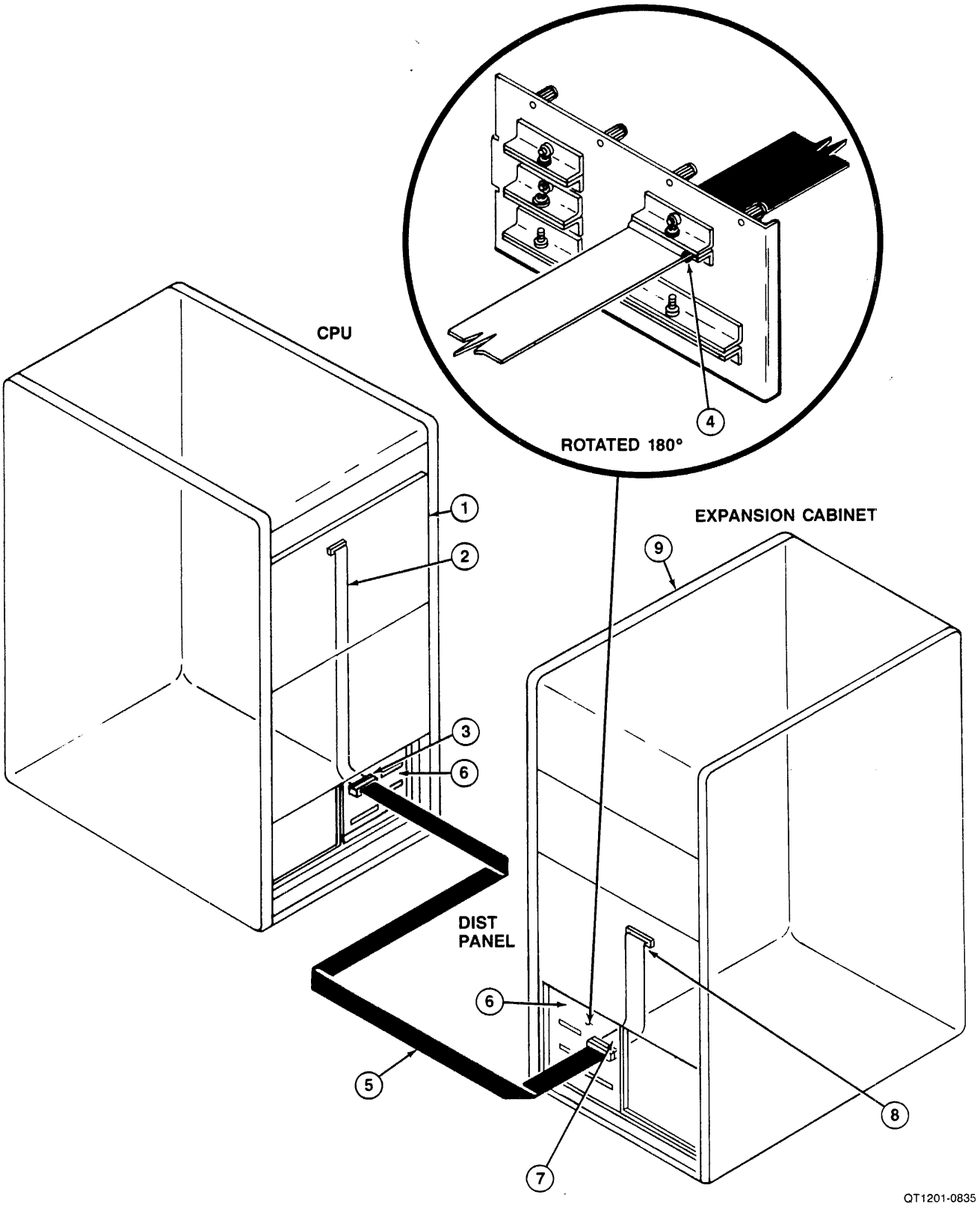


Figure 2-4. RFI-Suppression Cable Installation

Table 2-5. Shielded Cables and Installation Hardware

Part Number	Description	Length
QU1220101	CU22 Panel with 50-conductor flat-ribbon cable and connector	8 feet
QU1220102	Patch Panel with 50-conductor flat-ribbon cable and connector	1 foot
PU0611216-02	50-conductor flat-ribbon cable	10 feet
CU2220301	Bulkhead Distribution Panel (Optional)	

The items in Table 2-5 can be ordered from your Emulex sales representative or directly from the factory:

Emulex Customer Service
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

2.6.2 STANDARD CABLING

A 50-conductor ribbon cable connects the QT12 Tape Controller to any QIC-02 interface compatible drive, as explained in subsection 2.5, Step 5. If you purchase the optional cable from an independent source, use the following materials or equivalent:

Quantity	Description	Manufacturer	Part No.
1 each	50-pin socket connector	3M	3425-3000
1 each	50-pin edge connector	3M	3415-0001
As needed	50-conductor ribbon cable	3M	3365-50

Figure 2-5 illustrates the pinout of connector J1. The signals named in the figure are discussed in subsection 6.2.3.

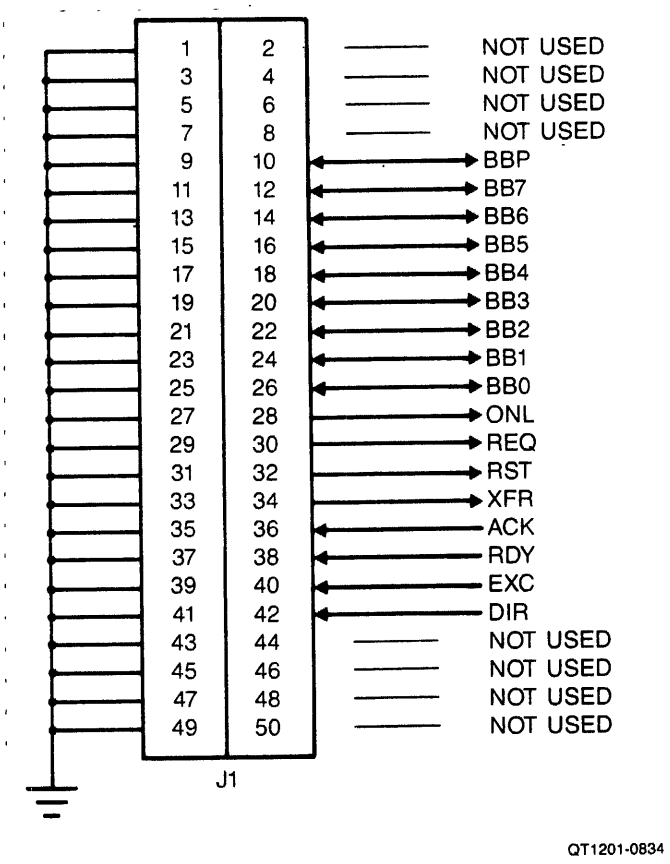


Figure 2-5. Connector Pin Definitions

2.6.3 GROUNDING

The tape transport must have a sure ground connection to the chassis ground of the computer. This connection should be made with metal braid at least 0.25 inch wide (preferably insulated), or with AWG no. 10 wire or larger. Failure to observe proper grounding methods can result in marginal operation with random error conditions.

3.1 OVERVIEW

This section describes testing and servicing procedures for maintaining optimum performance of the QT12 Tape Controller:

Subsection	Title
3.1	Overview
3.2	Service
3.4	Power-up Self-diagnostic

3.2 SERVICE

Your Emulex QT12 Tape Controller has been designed to give years of trouble-free service, and it was thoroughly tested before leaving the factory. If the QT12 should fail to work properly, however, it must be returned to the factory for service.

Locate the Configuration Reference Sheet (Figure 2-1), which contains information that technical support personnel will need to help you efficiently. Then contact Emulex or its representative for instructions and a Return Materials Authorization (RMA) number. In the continental United States, Alaska, and Hawaii, contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, Ca 92626
(714) 662-5600 TWX 910-595-2521

Outside the United States, notify the distributor from whom the subsystem was purchased.

After you have obtained the RMA, package the product (preferably using the original packing material), insure the package, and send it **postage paid** to the address provided by the Emulex representative.

NOTE

Do not return a product to Emulex without authorization. A product or component returned for service without an authorization will be returned to the owner at the owner's expense.

3.3 POWER-UP SELF-DIAGNOSTIC

The QT12 incorporates a set of internal diagnostics to verify proper functioning. These tests include:

- Proper microprocessor operation
- Condition code testing
- Register tests
- ALU operation test
- RAM verification
- Instruction tests

If the diagnostic enable jumper is removed (subsection 2.4.6), these internal diagnostics execute only once during the power-up cycle. Opon successful completion of the self test, the green LED at the edge of the board is turned on. With the jumper installed, the QT12 operates the self-diagnostics continuously and all other controller operations are suspended. The LED is turned off at initiation of the self-test and turns on upon successful completion of each pass of the diagnostics. If an error occurs, the diagnostics will loop on the failing test until successfully completed.

In addition to these built-in diagnostics, Emulex supplies installation diagnostic software (Table 1-2).

4.1 OVERVIEW

This section defines bit functions in the QT12 registers and explains command packet formats and processing. The section is divided into three subsections, as listed in the following table:

Subsection	Title
4.1	Overview
4.2	Controller Registers
4.3	Command Packet Processing

In bit descriptions, the prefixes **A** and **P** signify memory address bit(s) and command pointer bit(s) respectively.

4.2 CONTROLLER REGISTERS

The QT12 has four device registers, which occupy only two LSI-11 bus word locations:

- Data Buffer Register (TSDB)
- Bus Address Register (TSBA)
- Status Register (TSSR)
- Extended Data Buffer (TSDBX)

The TSDB and TSBA registers are both located at the LSI-11 base address (see subsection 2.4.1). When written to, the base address is TSDB; when read, it is TSBA. The TSSR register is located at the base address plus 2.

Six additional QT12 registers are contained in the message packet in system memory:

- Residual Byte/Record/File Count Register (RBPCR)
- Extended Status Registers 0 through 4 (TXSTO through TXST4)

The contents of these six registers are not accessible at the LSI-11 bus interface. A message buffer (subsection 4.3) must be defined to the subsystem before these registers are available to the software.

4.2.1 DATA BUFFER REGISTER (TSDB)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
P15	P14	P13	P12	P11	P10	P09	P08	P07	P06	P05	P04	P03	P02	P17	P18

TSDB is an 18-bit write-only register that is parallel loaded from the LSI-11 bus. TSDB can be loaded without the tape transport connected, because all controller functions reside within the controller.

The TSDB register can be loaded from the LSI-11 bus by four different transfers from the CPU; however, three transfers are for use in maintenance mode, which the QT12 does **not** support. The fourth, DATO, is the normal word output transfer used to specify a command pointer (subsection 4.3).

DATO loads TSDB with the 18-bit address of a command packet as follows:

1. Bits <15:02> of the register are loaded with bits <15:02> from the LSI-11 bus.

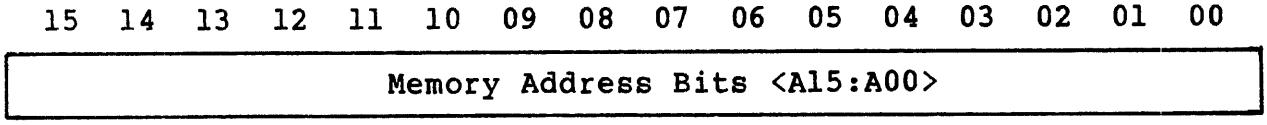
2. Bits 01 and 00 of the register are loaded with bits 17 and 16 from the LSI-11 bus.

3. Bits 01 and 00 of the address are automatically loaded with zeros by the logic in the tape transport.

TSDB is not cleared at power-up, subsystem initialize, or bus initialize. If 22-bit addressing is enabled, however, the four-bit extension to TSDB is cleared by initialize or after being used once. Consequently, these four bits must be reloaded (before TSDB) if extended addressing is to be used on subsequent command pointers.

The host CPU writes into TSDB to initiate an operation; a 16-bit portion of TSDB is used as a word buffer register. The QT12 responds whenever TSDB is written to, but it is loaded only if the SSR bit in the TSSR register is set. Writing into TSDB clears SSR; if SSR is clear, the RMR bit in TSSR is set (subsection 4.2.3).

4.2.2 BUS ADDRESS REGISTER (TSBA)



The bus address register (TSBA) is a read-only register located at the first I/O register address. It serves as a command and message pointer and also as a data pointer. Whenever TSDB is written, TSBA is parallel loaded with its low-order 16 bits. Thus the contents of TSBA reflect the 18- or 22-bit memory address used by the QT12 to access system main memory. Bits 01 and 00 are always zero, specifying a modulo-4 address. This register is **not** modified by initialize.

TSDB bits 17 and 16 are displayed in status register (TSSR) bits 09 and 08 respectively. If the Extended Features jumper is in (subsection 2.4.4), the high byte of TSSR is loaded with TSDB bits <21:18>. These bits are ignored if the Extended Features option is disabled.

4.2.3 STATUS REGISTER (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	0	SCE	RMR	NXM	NBA	A17	A16	SSR	OFL	FC1	FC0	TC2	TC1	TC0	0

TSSR is a 16-bit read/write register that can be updated only by the QT12; it cannot be modified directly from the LSI-11 bus. It can be read to examine major system status, or written to cause a hardware initialize of the QT12. Table 4-1 defines TSSR bits.

Table 4-1. Status Register Bit Definitions

Bit	Name	Significance
15	Special Condition (SC)	When set, indicates that the last command was not completed correctly (error or exception condition). Also set by RMR and NXM. Cleared by Initialize or by loading a command pointer into TSDB.
14	Not used	Always zero.
13	Sanity Check Error (SCE)	Set when the QT12 detects an internal RAM failure.
12	Register Modification Refused (RMR)	Set when TSDB is loaded with a command pointer but SSR is not set. Causes SC to be set, but no termination class code. Cleared by loading a command pointer into TSDB.
11	Nonexistent Memory (NXM)	Set when a DMA transfer is attempted to a nonexistent memory location (does not respond within 20 usec).

(Continued on next page)

Table 4-1. Status Register Bit Definitions (Cont'd)

Bit	Name	Significance
10	Need Buffer Address (NBA)	When set, indicates that the QT12 needs a message buffer address. Cleared by Write Characteristics command with valid address.
09-08	Address Bits (A17, A16)	Display TSBA bits 17 and 16.
07	Subsystem Ready (SSR)	When set, indicates that the QT12 is ready to accept a new command pointer. Cleared by writing to TSDB and by initialize. Set by the QT12 upon successful completion of internal micro-diagnostics.
06	Offline (OFL)	When set, indicates that the tape transport is offline and unavailable for tape motion commands.
05-04	Fatal Termination Class Code (FC01, FC00)	Used to indicate the type of fatal error which has occurred. Valid only when SC is set and termination class code = 7 (all bits set). Code — Meaning 00 — Internal diagnostic failure. See error code byte (high byte of TXST3). For the QT12 to accept further commands, initialize must be issued. 01 — Reserved (not used)
03-01	Termination Class Codes (TC02, TC01, TC00)	Acts as a word offset value whenever an error or exception condition occurs on a command. See Table 4-2 for definitions.
00	Not used	Always zero.

Table 4-2. Termination Class Codes

TC Code	Message Type Code (Octal)	Definition
0	END (20)	Normal Termination. The operation was completed without incident.
1	ATTN (23)	Attention Condition. The tape drive has changed status by going offline or coming online.
2	END (20)	Tape Status Alert (TSA). A status condition occurred which may affect the program. TMK, EOT, and RLL in the Extended Status registers may provide more information.
3	FAIL (21)	Function Reject. The specified function was not initiated. TSSR bit OFL and Extended Status Register bits VCK, BOT, WLE, ILC, and ILA may provide more information.
4	ERROR (22)	Recoverable Error. The tape position is one record beyond where it was when the function was initiated.
5	ERROR (22)	Recoverable Error. The tape position has not changed.
6	ERROR (22)	Unrecoverable Error. The tape position has been lost.
7	ERROR (22)	Fatal Subsystem Error. The subsystem cannot perform properly. See FC codes (Table 4-1) for more information.

4.2.4 EXTENDED DATA BUFFER REGISTER (TSDBX)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BT				P21	P20	P19	P18								

TSDBX is a write-only byte register that is used to specify the most significant four bits of the 22-bit address of the command sequence to be performed. It is loaded by a byte-access (DATOB) cycle addressed to the high byte of TSSR with SSR set. If the extended features jumper is disabled when TSDBX is written, only the Boot bit (bit 15) is examined; the other bits are ignored.

Once TSDBX has been written, bits <11:08> are transferred to TSBA bits <21:18> for use as a command pointer. Writing TSDB with the low-order 18 bits of the command pointer starts operation, causing the command packet to be fetched, and then clears TSDB. If bit 15 is set, SSR remains clear until the boot sequence is complete or until an error occurs. If bit 15 is clear, the command pointed to by the 22-bit TSDB is retrieved and command processing begins.

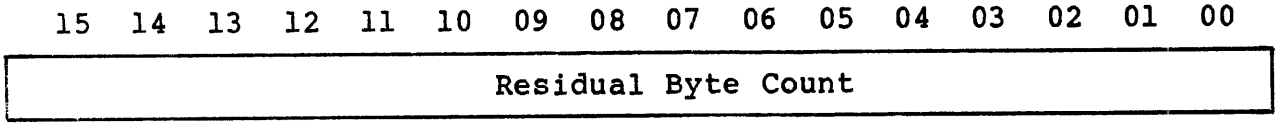
When TSDBX is written, the SSR bit is not cleared. Therefore, RMR should be checked before TSDB is written.

TSDBX bits are defined in Table 4-3.

Table 4-3. Extended Data Buffer Register Bits

Bit	Name	Significance
15	Boot Command (BT)	When this bit and SSR are set, the tape rewinds to BOT, the first record is skipped, and the first 512 bytes of the second record are transferred to host memory, starting at location 0.
14-12	Reserved	
11-08	Command Pointer Bits (P21, P20, P19, P18)	When TSDBX is written, if SSR is set and the extended features jumper is enabled, the data are loaded into TSBA bits <21:18>. TSDBX is cleared after TSDB is written and by initialize. If the extended features option is disabled, bits <21:18> are ignored.

4.2.5 RESIDUAL BYTE/RECORD/FILE COUNT REGISTER (RBPCR)



The RBPCR is available as the third word of the message packet (subsection 4.3.4). It contains a nonzero value whenever the count specified in a command exceeds the number of bytes transferred or records skipped:

Function	RBPCR Definition
Read	Value represents the number of bytes by which the tape record was shorter than the expected length.
Space Records or Skip Tape Marks	Value represents the difference between the number of records or tape marks actually skipped and the specified number.

4.2.6 EXTENDED STATUS REGISTER 0 (TXSTO)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TMK	RLS	LET	RLL	WLE	NEF	ILC	ILA	MOT	ONL	IE	VCK	PED	WLK	BOT	EOT

TXSTO is the fourth word of the message packet, which is updated by the QT12 upon completion of a command. The error bits are cleared by any command. Table 4-4 defines each of the bits in this register.

Table 4-4. TXSTO Bit Definitions

Bit	Name	Significance
15	Tape Mark Detected (TMK)	Set whenever a tape mark is detected during a Read, Space, or Skip command. Also set by the Write Tape Mark command.
14	Record Length Short (RLS)	Set if (1) the record length is shorter than indicated by the byte count on a Read operation; (2) a tape mark or BOT is encountered during a Space Record operation before the position count is exhausted; or (3) a Skip Tape Marks command is terminated by BOT or a double tape mark (if this mode is enabled) prior to exhausting the position count.
13	Logical End of Tape (LET)	If enabled by the Write Characteristics command, this bit is set when two contiguous tape marks are encountered, or when the first record after BOT is a tape mark.

(Continued on next page)

Table 4-4. TXSTO Bit Definitions (Cont'd)

Bit	Name	Significance
12	Record Length Long (RLL)	Set when the record read is longer than the byte count specified.
11	Write Lock Error (WLE)	Set when a Write operation is attempted on a write-protected tape.
10	Non-executable Function (NEF)	Set when a command cannot be executed because: (1) the command specifies reverse tape direction, but the tape is already at BOT; (2) a motion command is issued when bit 04 (Volume Check) is set or bit 06 (Online) is clear; (3) a command other than Get Status or Drive Initialize is issued when the transport is offline; or (4) a Write command is issued when the tape is not write enabled.
09	Illegal Command (ILC)	Set when a command is issued and the command code or command mode field contains codes not supported by the QT12.
08	Illegal Address (ILA)	Set when a command specifies an address containing more than the correct number of bits, or an odd address when an even one is required.
07	Motion (MOT)	Set when the tape is moving, indicating that the transport is asserting Formatter Busy or Rewinding status.
06	Online (ONL)	When set, indicates that the transport is online and operable. A change in this bit can cause a TC code of 1. If ONL is clear and a motion command is issued, NEF is set (TC code 3).

(Continued on next page)

Table 4-4. TXSTO Bit Definitions (Cont'd)

Bit	Name	Significance
05	Interrupt Enable (IE)	Reflects the state of the Interrupt Enable bit supplied by the last command.
04	Volume Check (VCK)	When set, indicates that the transport has been powered down or has gone offline (TC code 3). Cleared by the CVC bit in the command header word.
03	Phase-encoded Drive (PED)	Always set.
02	Write Locked (WLK)	When set, indicates that the mounted cartridge has its file protect tab toward Safe. The tape is therefore write protected.
01	Beginning of Tape (BOT)	When set, indicates that the tape is positioned at the load point, as denoted by the BOT hole on the tape.
00	End of Tape (EOT)	Set whenever the tape is positioned beyond either a calculated logical end of tape or the end of tape hole, whichever is sooner. Because the controller is operating in buffered mode, buffering is terminated when the logical EOT is encountered before the physical EOT. When the buffer empties, this bit is set.

4.2.7 EXTENDED STATUS REGISTER 1 (TXST1)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT		COR	0	0	0	0	RBP	0	0	0	0	0	0	UNC	0

TXST1 is the fifth word of the message packet, which is updated by the QT12 upon completion of a command or on an attention (ATTN). The error bits are cleared by any command. Table 4-5 defines bits in this register. In the DEC TS11, bits <12:09>, <07:02>, and 00 indicate various errors associated with the drive.

Table 4-5. TXST1 Bit Definitions

Bit	Name	Significance
15	Data Late (DL)	Set when the buffer becomes full on a Read and the drive attempts to transfer another byte, or when the buffer becomes empty on a Write and the drive requests another transfer. These conditions are the result of latency on the LSI-11 bus.
14	Not used	
13	Correctable Data (COR)	Set to indicate that a correctable data error occurred during a Read or Write. Always zero; the streaming drive automatically handles Read or Write errors.
12-09	Not used	Always zero.
08	Read Bus Parity Error (RBP)	Always zero. The QT12 does not implement bus parity on the drive interface.
07-02	Not used	Always zero.
01	Uncorrectable or Hard Error (UNC)	Set to indicate that the drive encountered an uncorrectable error during the previous command.
00	Not used	Always zero.

4.2.8 EXTENDED STATUS REGISTER 2 (TXST2)

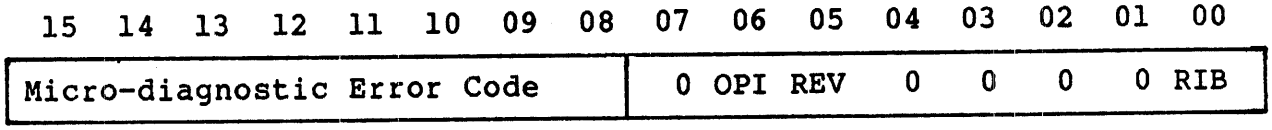
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OPM	0	0	0	0	0	0	0	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0

TXST2 is the sixth word of the message packet, which is updated by the QT12 upon completion of a command. Note that the lower byte of this register has meaning only for Write Characteristics and Get Status commands. The error bits are cleared by any command. Table 4-6 defines the bits in this register.

Table 4-6. TXST2 Bit Definitions

Bit	Name	Significance
15	Operation in Progress (OPM)	When set, indicates drive is busy.
14-08	Not used	Always zero.
07-00	Revision Level (RL)	In response to a Write Characterstics command, this field displays the following information: Bits — Definition 07 — Extended Features jumper 06 — Buffer Enable jumper 05-00 — Microcode revision level In response to all other commands, bits <02:00> display the unit number of the currently selected drive.

4.2.9 EXTENDED STATUS REGISTER 3 (TXST3)

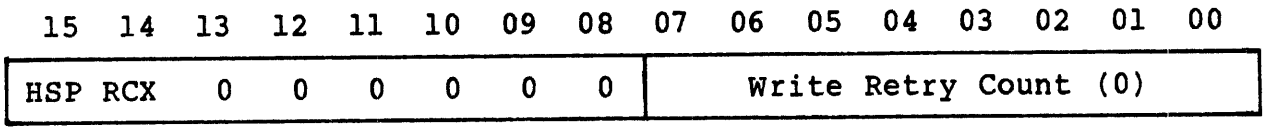


TXST3 is available as the seventh word of the message packet. Table 4-7 defines bits in this register.

Table 4-7. TXST3 Bit Definitions

Bit	Name	Significance
15-08	Micro-Diagnostic Error Code (MDE)	The QT12 encodes this field to indicate a failure detected by the internal micro-diagnostics.
07	Not used	Always zero.
06	Operation Incomplete (OPI)	Set whenever a Read, Space, or Skip command moves tape without detecting data for a specified period of time.
05	Reverse (REV)	Set when the current operation causes reverse tape motion.
04-01	Not used	Always zero.
00	Reverse Into BOT (RIB)	Indicates that a reverse motion encountered a BOT. Tape motion is halted.

4.2.10 EXTENDED STATUS REGISTER 4 (TXST4)



TXST4 is available as the eighth word of the message packet. For this word to be updated on completion of a command, the Extended Features option must be enabled. The error bits are cleared by any command. Table 4-8 defines bits in this register.

Table 4-8. TXST4 Bit Definitions

Bit	Name	Significance
15	High Speed (HSP)	Set when buffered high speed mode is selected.
14	Retry Count Exceeded (RCX)	Indicates that the QT12 could not successfully output the record within the specified number of retries. Always zero, because streaming drives deal with errors automatically.
13-08	Reserved	Always zero.
07-00	Write Retry Count (WRC)	Indicates that the QT12 initiated the displayed number of retries in order to write the previous buffered record. Always zero, because streaming drives deal with errors automatically.

4.3 COMMAND PROCESSING

Command packet protocol enables a TS11 emulation to provide a large amount of tape transport status and error information to the CPU while using only two words of LSI-11 address space. The command protocol used by the QT12 is largely identical to that of the DEC TSV05 subsystem.

The CPU communicates with the QT12 by means of buffers in CPU memory. First, the CPU writes a four-word **command packet** into a **command buffer.** It passes the location of this command buffer to the QT12 by writing a **command pointer,** containing the LSI-11 bus address of the command packet, to the TSDB register (subsection 4.2.1). From there, the address is copied to the TSBA register, from which it can be read (subsection 4.2.2).

The command pointer must be on a modulo-4 boundary (octal 0, 4, 10, etc.) due to the address limitations of the TSBA register. The command pointer, located in words 2 and 3 of the command packet, is sometimes called the **data pointer register** (DPR).

When the QT12 has executed the command, it responds by depositing a **message packet,** which contains error and/or status information, into a **message buffer.** The QT12 interrupts (if the IE bit is set; see Table 4-4) and then indicates it is ready to execute another command by setting the SSR bit in the TSSR register.

4.3.1 COMMAND PACKET FORMAT

All four 16-bit words of the command packet are read in, but fewer may be required, depending upon the type of command and the amount of information it needs for execution.

Every command packet begins with a command packet **header word.** Its format (Figure 4-1, Table 4-9) is the same for all commands; the information that it contains distinguishes one command from another. Words 2 and 3, as previously noted, contain the command pointer. Word 4, sometimes also called the **positive byte count register** (BCR), indicates the number of bytes, records, or files needed for execution of the command.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl	Device Dep.			Mode				Format			Command				
ACK	CVC	OPP	SWB	0	m	m	m	IE	0	0	0	c	c	c	c

Figure 4-1. Command Packet Header Word

Table 4-9. Command Packet Header Word Bit Definitions

Bit	Name	Significance
15	ACK (Acknowledge)	When the CPU owns the message buffer, it sets this bit when it issues a command. This informs the QT12 that the message buffer is available for use, and thus passes ownership of the message buffer to the QT12.
14	CVC (Clear Volume Check)	The Volume Check condition results when the drive changes from offline to online status. Set CVC clears the Volume Check condition, thus allowing tape operations to be executed.
13	OPP (Opposite)	This bit is ignored.
12	SWB (Swap Byte)	This bit is ignored and assumed to be 0, thus forcing the standard DEC method of retrieving bytes from memory, in which the first byte in a word is the least significant byte (bits <7:0>).

(Continued on next page)

Table 4-9. Command Packet Header Word Bit Definitions (Cont'd)

Bit	Name	Significance
11-08	Command Mode Field	This field acts as an extension of the Command Code and allows additional specification of device commands.
07-05	Packet Format Field	This field defines the header type and interrupt enable. The only valid configurations are: Field Definition 000 Interrupts disabled 100 Interrupts enabled
04-00	Command Code Field	Defines the command category; used together with the Command Mode Field to specify the command.

4.3.2 COMMAND SET

Table 4-10 summarizes the QT12 command set. Some of these commands have sub-commands called **command modes.**

Table 4-10. Command Code and Command Mode Field Definitions

Command Code	Command Name	Command Mode	Mode Name
00001	READ	0000	Read Next (Forward)
		0001	Read Previous (Space Reverse, Read Forward, Space Reverse)*
		0010	Reread Previous (Space Reverse, Read Forward)*
		0011	Reread Next (Read Forward, Space Reverse)*
00100	WRITE CHARACTERISTICS	0000	Load Message Buffer address and Set Device Characteristics
00101	WRITE	0000	Write Data (Next)
		0010	Write Data Retry*

(Continued on next page)

Table 4-10. Command Code and Command Mode Field Definitions (Continued)

Command Code	Command Name	Command Mode	Mode Name
00110	WRITE SUBSYSTEM MEMORY	0000	*
01000	POSITION	0000	Space Records Forward
		0001	Space Records Reverse**
		0010	Skip Tape Marks Forward
		0011	Skip Tape Marks Reverse**
		0100	Rewind
01001	FORMAT	0000	Write Tape Mark
		0001	Erase (Illegal Function Reject)
		0010	Write Tape Mark Retry (Illegal Function Reject)
01010	CONTROL	0000	Message Buffer Release (ignored)
		0001	Rewind and Unload
		0010	NO-OP (Retension Tape)
		0100	Rewind With Immediate Interrupt
01011	INITIALIZE	0000	Controller/Drive Initialize
01111	GET STATUS	0000	Get Status (Output Extended Status Message)

* These commands are rejected by the QT12.

** These commands are supported, but with limitations as to the number of tape marks skipped or records reversed. When reading, the maximum number of tape marks skipped or records reversed is nine contiguous data blocks from a tape mark. When writing, the maximum backspace is 31 data blocks.

4.3.2.1 Read Command

As shown in Table 4-10, the Read command has four modes, three of which are not currently supported by the QT12. This command requires a four-word packet (Fig. 4-2):

- **Header word.** The OPP and SWB bits are ignored.
- **Low-order Buffer Address.**
- **High-order Buffer Address.** This word differs according to the status of the Extended Features option:

- Extended Features disabled: If any bit in the range <15:02> is set to 1, the function is not executed, but instead terminates with an ILA error (Table 4-4). If bits <15:02> are zero, then bits <01:00> specify address bits <A17:A16>, and together with the 16 bits in the second word of the command packet define an 18-bit address.

- Extended Features enabled: If any bit in the range <15:06> is set to 1, the function is not executed but terminates with an ILA error. If bits <15:06> are zero, bits <05:00> specify address bits <A21:A16>, and together the the 16 bits in the second word of the command packet define an 18-bit address.

- **Buffer Extent (Byte Count).** The Read command assumes a record of known length, so the byte count must be correct; see Table 4-4 for error conditions that result from an incorrect byte count. A byte count of 0 indicates that 65,536 bytes are expected.

A Read operation that encounters a tape mark transfers no data and gives a Tape Status Alert termination.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl	Device Dep.			Mode				Format 1			Command				
ACK	CVC	OPP	SWB	0	m	m	m	IE	0	0	0	0	0	0	1
A15	Low-order Buffer Address														A00
0	High-order Buffer Address							0	A21				A18	A17	A16
Buffer Extent (Byte Count) (16-bit Positive Integer)															

Figure 4-3. Read Command Packet

4.3.2.2 Write Characteristics Command

The Write Characteristics command (Fig. 4-4) tells the QT12 the location and size of the message buffer, and what action to take on certain conditions. It must be the first command issued to the QT12 after an initialization.

The first word of the command packet is the header word, as usual. The second and third words specify the location of the associated characteristics data buffer, which must have an even address in CPU memory space. The command is terminated with a Function Reject if any of the following bits are set to 1:

- Bit 0 of the second command packet word
- Bits <15:02> of the third packet word, Extended Features disabled
- Bits <15:06> of the third packet word, Extended Features enabled

The fourth word specifies the length in bytes of the characteristic data buffer. The minimum length is 6 bytes, and the maximum is 10 bytes when Extended Features is enabled.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl	Device Dep.			Mode				Format 1			Command				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
Characteristic Data Address (Low-order)															
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	0
Characteristic Data Address (High-order)															
0	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16
Buffer Extent (Byte Count) (16-bit Positive Integer)															

COMMAND PACKET

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Message Buffer Address (Low-order)															
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	0
Message Buffer Address (High-order)															
0	0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16
Length of Message Buffer (Minimum 14 Bytes) (16-bit Positive Integer)															
0							0	ESS	ENB	EAI	ERI	0	0	0	0
XIRG Retry Limit				No-XIRG Retry Limit				RTY		HSP	Buffer Control		Unit Select		

CHARACTERISTICS DATA

Figure 4-3. Write Characteristics Command Packet and Characteristics Data

In the characteristics data buffer, the first two words specify the address of the message buffer. The third word specifies the message buffer length in bytes; the minimum length is 14 bytes, and the maximum is 16 bytes when Extended Features is enabled. The fourth word is the Characteristics Mode word, which causes specific actions in response to certain conditions. Table 4-11 defines bits in this word.

Table 4-11. Characteristics Mode Word Bit Definitions

Bit	Name	Significance
15-08	Not defined	Always zeros.
07	Enable Skip Tape Marks Stop (ESS)	When set, this bit instructs the controller to stop and set the Logical End of Tape (LET) status bit when it detects a double tape mark during a Skip Tape Marks command. Otherwise, Skip Tape Marks terminates only if it encounters BOT or EOT or if the tape mark count is exhausted. When set, ESS also enables ENB (bit 06).
06	Enable Tape Mark Stop Off BOT (ENB)	This bit is meaningful only if ESS (bit 07) is set. If ENB and ESS are set, then if a Skip Tape Marks Forward command is issued and the first record seen is a tape mark, the QT12 stops the operation and sets LET in TXSTO. If ENB is clear under these same conditions, QT12 counts the tape mark and continues.
05	Enable Attention Interrupts (EAI)	Not used by the QT12; should be zero.
04	Enable Message Buffer Release Interrupts (ERI)	If this bit is zero, interrupts are not generated upon completion of a Message Buffer Release command; only SSR is re-asserted. If ERI is set to 1, an interrupt is generated, but without a message packet.
03-00	Not defined	Always zeros.

The fifth Characteristics Data word, the Extended Characteristics word (Figure 4-3), can be specified only when Extended Features is enabled. Most options that it defines do not apply to the QT12, so bits <15:06> and <04:03> are always zero. Bit 05 selects transport speed: 0 = low speed, 1 = high speed. Bits <02:00> are used to select transport number, but at present the QT12 supports only a single transport, so initializing sets these bits to zero.

4.3.2.3 Write Command

The QT12 supports only the Write Data command. Table 4-10 defines the two acceptable modes: Write Data and Write Data Retry. The Write command packet (Fig. 4-4) contains four words:

- **Header Word.** The QT12 does not support byte swapping, so SWB is ignored.
- **Low-order Bus Address.** Specifies bits <15:00> of the starting address of the data buffer.
- **High-order Bus Address.** When Extended Features is enabled, bits <05:00> of this word represent address bits <A21:A16>. When Extended Features is disabled, only <A17:A16> may be set to 1. These bits, together with the 16 bits specified by word 2, comprise the 18- or 22-bit starting address of the data buffer. If any other bits of word 3 are set, the function is not performed but terminates with ILA error status (Table 4-4).
- **Buffer Extent (Byte Count).** This word specifies the number of bytes available in the data buffer and the number of bytes to be written onto tape. A byte count of 0 specifies that 65,536 (64K) bytes are to be written.

If a Write command is executed at or beyond the logical or physical end of tape, the data are written but a TSA termination occurs (Table 4-2). EOT remains set until passed in the reverse direction.

The QT12 does not support bus parity communication with the drive interface, but streaming drives incorporate a sophisticated write verify mechanism. See also subsection 2.4.4, Extended Features.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl	Device Dep.			Mode				Format 1			Command				
ACK	CVC	0	SWB	0	m	m	m	IE	0	0	0	0	1	0	1
Bus Address (Low-order)															
A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	0
Bus Address (High-order)															
0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16
Buffer Extent (Byte Count) (16-bit Positive Integer)															

Figure 4-4. Write Command Packet

4.3.2.4 Position Command

Positioning functions are implemented to the extent that they allow proper operation of DEC operating systems and utilities. The five acceptable modes, as listed in Table 4-10, are Space Records Forward and Reverse, Skip Tape Marks Forward and Reverse, and Rewind. The command packet (Figure 4-5) contains two words, the header word and a tape mark/record count word.

- A Space Records operation skips over the number of records specified in word 2, but terminates when a tape mark is encountered (Table 4-4). The RLS bit in TXSTO is set if the record count is not decremented to 0.
- A Skip Tape Marks operation skips over the number of tape marks specified in word 2. It terminates when two consecutive tape marks are encountered and ESS is set; see also Table 4-11, ESS and ENB bits. RLS is set if the tape mark count is not decremented to 0.
- A Rewind command rewinds to BOT. The interrupt, if enabled, does not occur until the tape reaches BOT and stops. The second word of the command packet is ignored.

If BOT is encountered during a reverse position operation, the RIB bit in TXST3 is set and causes a Tape Status Alert termination. If a reverse position command is issued while the tape is already at BOT, the NEF bit in TXSTO is set and causes a Function Reject termination; in this case, the tape will not move.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl ACK	Device Dep.			Mode				Format 1			Command				
	CVC	0	0	0	m	m	m	IE	0	0	0	1	0	0	0
Tape Mark/Record Count (16-bit Positive Integer)															

Figure 4-5. Position Command Packet

4.3.2.5 Format Command

The only valid format command is Write Tape Mark (Table 4-10). Other format commands terminate with Function Reject and set ILC error bit. The command packet (Fig. 4-6) consists of two words: the header and a second word that is read but ignored.

If this command is executed beyond the logical or physical EOT market, a Tape Status Alert termination occurs. The EOT bit remains set until EOT is passed in the reverse direction.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl ACK	Device Dep.			Mode				Format 1			Command				
	CVC	0	0	0	m	m	m	IE	0	0	0	1	0	0	1
(Not Used)															

Figure 4-6. Format Command Packet

4.3.2.6 Control Command

Table 4-10 defines the four modes of the Control command. The command packet (Fig. 4-7) contains two words: the header, and a second word that is read but ignored.

- The QT12 ignores the Message Buffer Release command.
- The Rewind and Unload command rewinds the tape to BOT. It causes an immediate interrupt and termination; the drive goes offline and remains offline until the tape reaches BOT and the cartridge is replaced.
- The NO-OP command causes a tape retension pass.

- The Rewind With Immediate Interrupt command applies to multi-drive systems; however, the QT12 supports only a single tape drive. The command differs from the normal Rewind command (subsection 4.3.2.5) in that termination occurs at the start of rewind. The MOT bit in TXSTO is set if a Get Status command is performed (subsection 4.3.2.9).

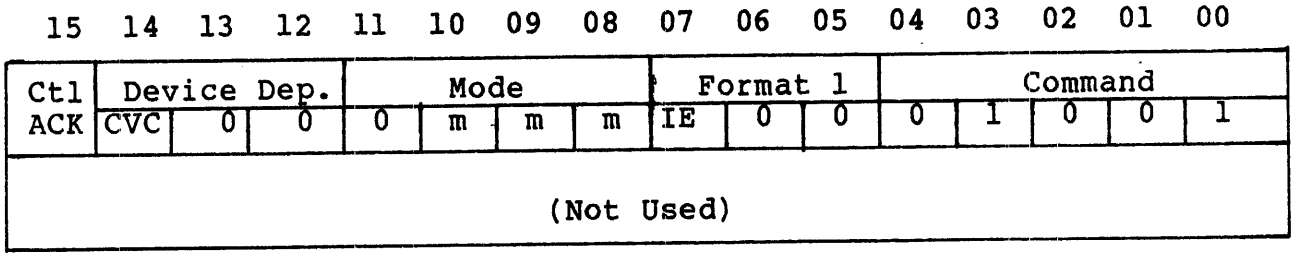


Figure 4-7. Control Command Packet

4.3.2.7 Initialize Command

This command performs a NO-OP. Normal termination occurs, but no action is performed. Figure 4-8 illustrates the command packet.

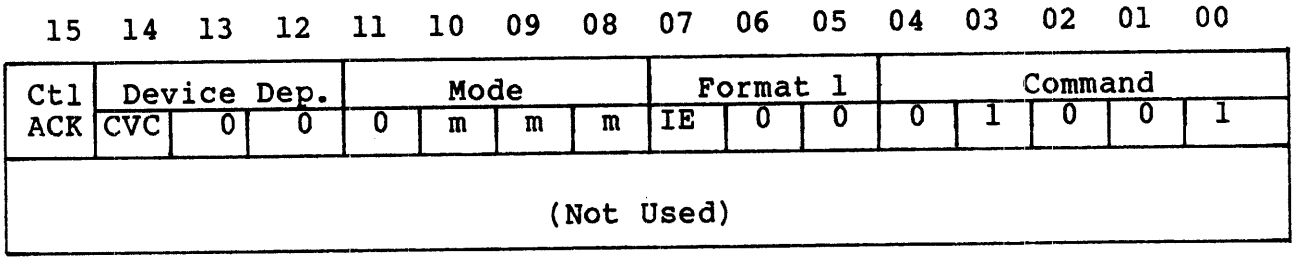


Figure 4-8. Initialize Command Packet

4.3.2.8 Get Status Command

The Get Status command (Fig. 4-9) causes a message packet to be deposited in the message buffer area and thereby updates the Extended Status registers. These registers normally are updated after every command, except Message Buffer Release, so the Get Status command is needed only under one of the following circumstances:

- The QT12 has been idle for an extended period of time.
- An extended status register update is required without performing a tape motion command.
- The unit number of the tape transport is required.

The error bits in the Extended Status registers are cleared by any command, so Get Status does not return the error bits generated by a previous tape operation.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Ctl	Device Dep.			Mode				Format 1			Command				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	1	1	1
Not Used															

Figure 4-9. Get Status Command Packet

4.3.3 BUFFER OWNERSHIP AND CONTROL

Buffer ownership prevents the QT12 from updating the message buffer while the CPU is reading it, or the CPU from updating the command buffer while the QT12 is reading it.

Each buffer can be owned by the QT12 or by the CPU, but not by both. Ownership of a buffer can be transferred only by the current owner. Because there are two buffers and two possible owners, there are four types of transfer:

- **Command Buffer, from CPU to QT12.** The CPU writes the address of the command buffer into the TSDB register, thus clearing the SSR bit in TSSR.
- **Command Buffer, from QT12 to CPU.** The QT12 deposits a message packet that has the ACK bit set in the message header word (see Figure 4-10), thus setting the SSR bit in TSSR.
- **Message Buffer, from CPU to QT12.** The CPU sets the ACK bit in the command buffer and then passes the command buffer to the controller, using the TSDBX/TSDB registers. The QT12 responds by setting SSR and performing an interrupt (if the IE bit is set).
- **Message Buffer, from QT12 to CPU.** The QT12 writes the message buffer and sets the SSR bit.

4.3.4 MESSAGE PACKET FORMAT

A message packet consists of a **header word**, a **data field length word**, the residual byte/record/tape mark count word, and the extended status registers. Figure 4-10 illustrates the format of a message packet.

The residual byte/record/tape mark count word and the extended status registers are described in subsections 4.2.5 through 4.2.10. The paragraphs that follow describe the message packet header word and data field length word.

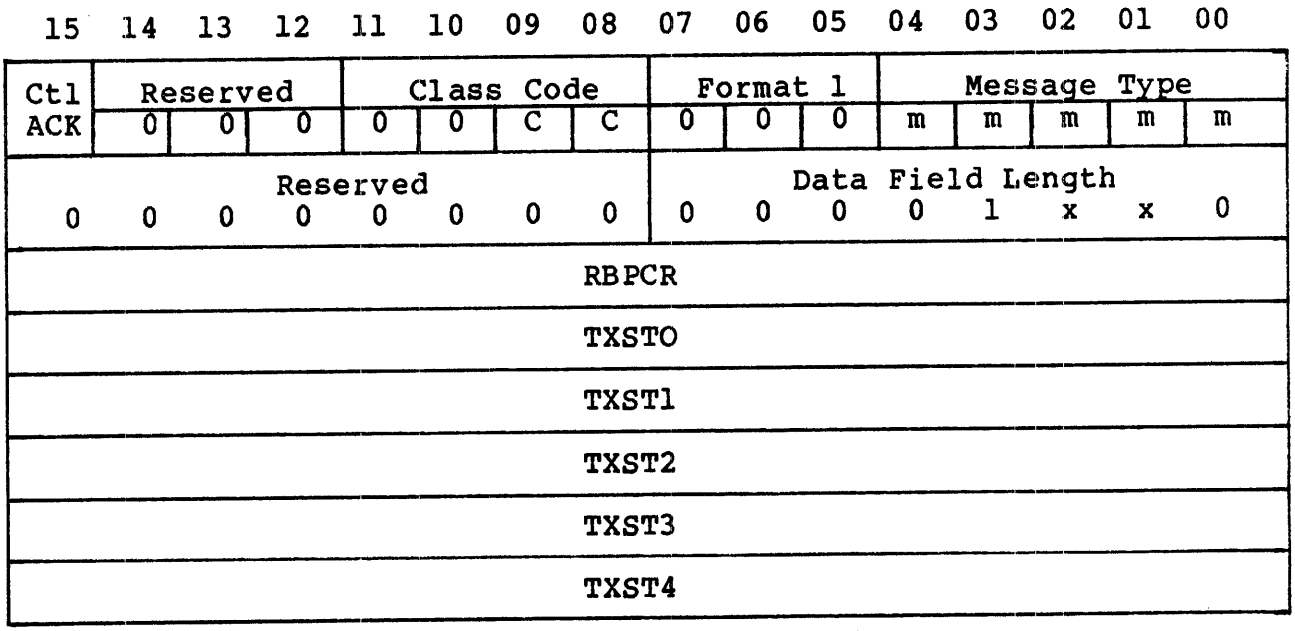


Figure 4-10. Message Packet

4.3.4.1 Message Packet Header Word

The header word is available in the first word of the message packet. Table 4-12 defines the bits in this word.

Table 4-12. Message Packet Header Word Bit Definitions

Bit	Name	Significance
15	Acknowledge (ACK)	Set by the QT12 to inform the CPU that the command buffer is available for command packets.
14-12	Reserved	Always zero.
11-08	Class Codes (CC11 - CC08)	These bits define the class of failure when the Message Type Code field (bits <04:00>) indicates other than a normal End. Possible binary codes are:

(Continued on next page)

Table 4-12. Message Packet Header Word Bit Definitions (Continued)

Bit	Name	Significance
		Message Type / Class Code / Definition ATTN / 0000 / Online or offline ATTN / 0001 / Not used FAIL / 0000 / Not used FAIL / 0001 / Illegal Command (ILC), Illegal Address (ILA), or Need Buffer Address (NBA) on a tape motion command
07-05	Packet Format field (PF07-PF05)	Written as all zeroes, specifies a one-word message header.
04-00	Message Type code (MC04-MC00)	Binary form 10xxx, which indicates that the message code contains a header word, a data length word, and xxx data/status words: TC Code / Message / Definition 0,2 / 10000 / End 3 / 10001 / Fail 4,5,6,7 / 10010 / Error 1,7 / 10011 / Attention

4.3.4.2 Data Field Length Word

The data length field word is available in the second word of the message packet. Table 4-13 defines the bits in this word.

Table 4-13. Data Field Length Word Bit Definitions

Bit	Name	Significance
15-08	Reserved	Always zeroes.
07-00	Data Field Length (DL07-DL00)	This field specifies how many bytes of information the following message contains. If Extended Features is disabled, the value of this field is 12_8, which indicates that the rest of the message consists of the RBPCR and four Extended Status Registers. If Extended Features is enabled, the value is 14_8, which indicates the presence of TXST4.

5.1 OVERVIEW

This section discusses QT12 software compatibility. The following table outlines the contents of this section.

Subsection	Title
5.1	Overview
5.2	Limitations
5.3	DEC Diagnostics
5.4	Emulex Diagnostics
5.5	RT-11
5.6	RSX-11M
5.7	RSTS
5.8	MicroVMS

5.2 LIMITATIONS

The QIC-24 recording format does not allow destructive writes.

The QIC-02 intelligent controller on the drive will attempt to re-read blocks of data when an error is encountered. While this recovery is in progress, some operating systems may timeout. Use of certified tapes will minimize this possibility.

The QT12 is not well suited to perform backup in timesharing environments. System loading causes many repositions of the tape cartridge. The tape becomes too tight, resulting in I/O errors and subsystem position errors.

5.3 DEC DIAGNOSTICS

The QT12 emulation is not compatible with DEC XXDP+ diagnostic test functions, but it is compatible with UPD2 utilities.

5.4 EMULEX DIAGNOSTICS

Several Emulex diagnostic programs are available which exercise and report the operational status of the QT12 Tape Controller. These programs are listed and described in Table 1-2. A comprehensive user's guide is supplied with each diagnostic program.

5.5 RT-11

The QT12 supports a comprehensive set of file- and device-oriented backup utilities for the DEC RT-11 operating system. Subsections 5.4.1 through 5.4.5 outline optimal use of the QT12 with each of these utilities.

NOTE

The QT12 is a fast and reliable device for performing backup. However, when used with certain utilities that were not designed to provide data at a high rate, the QT12 and its drive may not stream continuously.

5.5.1 BACKUP UTILITY PROGRAM (BUP)

BUP is a specialized file transfer program used for backing up and restoring large files or volumes. Its design makes effective use of the QT12 streaming mode, and it can back up an RL02 or equivalent disk in less than 3 minutes. No special operating instructions are necessary when using the QT12 as a single backup device; refer to the DEC RT-11 System Utilities Manual, referenced in Appendix A-1 of this document.

5.5.2 DEVICE UTILITY PROGRAM (DUP)

DUP is a device maintenance program used to initialize and create files. It does not buffer its input/output data sufficiently to allow the QT12 to maintain streaming operation, but it provides several alternate backup methods. Again, consult the RT-11 System Utilities Manual for details.

5.5.3 PERIPHERAL INTERCHANGE PROGRAM (PIP)

PIP is a file transfer and file maintenance utility program. Like DUP, it does not allow the QT12 to maintain streaming. The QT12 supports all PIP functions except the VERIFY function or /V switch option. SRCCOM and BINCOM (subsection 5.4.4) can be used to provide the verify function. Consult the RT-11 System Utilities Manual

5.5.4 SOURCE AND BINARY COMPARE UTILITIES (SRCCOM and BINCOM)

SRCCOM and BINCOM compare two ASCII or binary files and list the differences between them. These utilities can be substituted for the VERIFY function of PIP, which the QT12 does not support.

5.5.5 MAKING A BOOTABLE RT-11 TAPE

When the QT12 is used as the primary system backup device, bootable tapes are necessary. For example, consider a Winchester disk-based system that uses the QT12 as the load medium. Such a system requires bootable tapes that contain executable programs to allow the user to format the Winchester disk, load the operating system, and/or restore system backups.

The DEC RT-11 System User's Guide, referenced in Appendix A-1, explains how to create a bootable volume. To boot the resulting tape, use a hardware bootstrap or the QT12 boot program presented in Appendix B of this document. Once a tape containing MSBOOT is successfully booted, it displays the following prompt:

```
MSBOOT V05-00
*
```

Any standalone RT-11 structured program can be made bootable by use of the following guidelines:

The MSBOOT program searches the input device to locate the specified file and read it into memory. After successfully loading the program, MSBOOT starts it at the relative start address minus 2, specified in block 0 offset 40 of the program image. Therefore, you must ensure that the bootable program start address is preceded by a valid one-word instruction such as HALT or NOP.

Alternatively, you may modify location 40 of the program. In the following sample dialog, user input appears in **bold** type. The symbol **<return>** represents the carriage return key, and **^Y** represents the key combination CONTROL-Y. (For a description of the SIPP utility, see the RT-11 System Utilities manual.)

```
.R SIPP<return>
*Program.SAV<return>
Base? <return>
Offset?  40<return>
Base          Offset        Old       New?
 000000        000040    xxxxxx       xxxxxx+2
 000000        000042    xxxxxx       ^Y
```

The program's location must be restored before you run it under an RT-11 monitor.

5.6 RSX-11M

Most utilities supported by RSX-11M enhance the operation of the QT12 Tape Controller. PIP is not supported, however, because some of its functions require backspacing (see also Table 4-10).

5.6.1 BACKUP AND RESTORE UTILITY (BRU)

The online and stand-alone versions of BRU (BRUSYS.SYS and BRU64K.SYS respectively) can be used with the QT12 cartridge tape unit, but at present a volume cannot extend over multiple tapes. The APPEND/VER switch combination is not supported. For information regarding backup and restore commands, see the DEC RSX-11M Utilities Manual, which is referenced in Appendix A-1 of this document.

5.6.1.1 Creating a Bootable BRU Tape

The following example assumes that BRU64K.SYS and BRU64K.STB, its symbol table file, are located in UIC [1,51]:

```
>VMR [1,51]BRU64K<return>          ! Build image of stand-!
                                   alone program
VMR>SAVE MS:BRU64K<return>         ! Write bootable image
```

5.6.1.2 Restoring a Bootable BRU Tape

If the hardware bootstrap is not available, the program listed in Appendix B can be used. Enter it into memory starting at address 7776 octal.

Once the code has been entered and verified, start the processor at location 10000_8 with the line clock disabled. When the program displays a message indicating completion of the bootstrap operation, enable the line clock. Refer to the RSX-11M Utilities Manual for more information.

The default vector address established for the MS device is incorrect, so you must enter the following command when using the QT12 as one of the BRU devices:

```
MS:/VEC=224<return>
```

5.6.2 DISK SAVE AND COMPRESS UTILITY (DSC)

DSC and its stand-alone versions (DSCSYS.SYS and DSC64K.SYS) can be used with the QT12 to save and restore disk volumes, but at present a volume cannot extend over multiple tapes. See the RSX-11M Utilities Manual for instructions.

5.7 RSTS/E

5.7.1 SAVE AND RESTORE UTILITY (SAV/RES)

The QT12 supports all tape options of the SAV/RES function. The only restriction is the limit of one volume per cartridge. For instructions, see the DEC RSTS/E Utilities Reference Manual, which is referenced in Appendix A-1 of this document.

5.7.2 BACKUP UTILITY (BACKUP)

The QT12 supports basic BACKUP operations and has no restrictions on number of entries. Prior to the most current version of RSTS 9.0, BACKUP reported a false error message if the index file exceeded 160 entries. This was due to the limitations of the QIC-02 interface.

5.7.3 PERIPHERAL INTERCHANGE PROGRAM PIP

The QT12 supports RSTS/E PIP operations. See the RSTS/E Utilities Reference Manual for instructions. Early termination (CTRL-C) of the first file transferred to a new tape causes subsequent accesses to return device errors. The tape must be re-initialized.

5.8 MicroVMS

MicroVMS will support TS11 devices provided that a TS11 driver is installed. Refer to Emulex MicroVMS TS11 Software Installation Guide listed in Appendix A-1.

5.8.1 COPY UTILITY (COPY)

There are no copy limitations.

5.8.2 STANDALONE BACKUP UTILITY

There are no limitations if the standalone backup kit is built with TS11 support. See Emulex MicroVMS TS11 Software Driver (TSDRIVER) Installation Guide listed in Appendix A.

5.8.3 BACKUP UTILITY (BACKUP)

Due to the limitations of the QIC-02 interface, BACKUP operations can not use /VER switch for append operations, except when the first save-set per tape is written. To accomplish BACKUP/VER with APPEND (/NOREWIND) use the following procedure:

```
BACKUP/NOREWIND  SYS$MANAGER:*.* MSAO:APPEND.BCK/SAVE

BACKUP/COMPARE/REWIND  MSAO:APPEND.BCK/SAVE SYS$MANAGER:*.*
```

The first command appends a save-set onto the tape. The second command rewinds the tape and compares the new save-set to the disk files.

5.8.4 EXCHANGE UTILITY

Attempting to copy a zero block file inhibits copying of that file and all subsequent files. In order to write onto the tape in the future, the tape must be re-initialized.

6.1 OVERVIEW

This section contains a technical description of the QT12 Tape Controller's architecture and interfaces. The following table outlines the contents of this section.

Subsection	Title
6.1	Overview
6.2	QT12 Block Diagram
6.3	Tape Format

6.2 QT12 BLOCK DIAGRAM

Figure 6-1 shows the block diagram of the QT12 Tape Controller. It comprises three major sections, as described in subsections 6.2.1 through 6.2.3: microengine, LSI-11 bus interface, and tape transport interface.

6.2.1 MICROENGINE

The microengine does not handle data directly; instead, it directs data at a block level. It performs the following functions:

- Supervises all operations within the controller
- Recognizes commands from the LSI-11 bus and returns status information
- Sends necessary commands to the tape drive and processes drive status
- Keeps track of the ring buffer, determines when there are free blocks to be filled or full blocks to be emptied, and calculates block addresses, which it passes to the DMA controllers

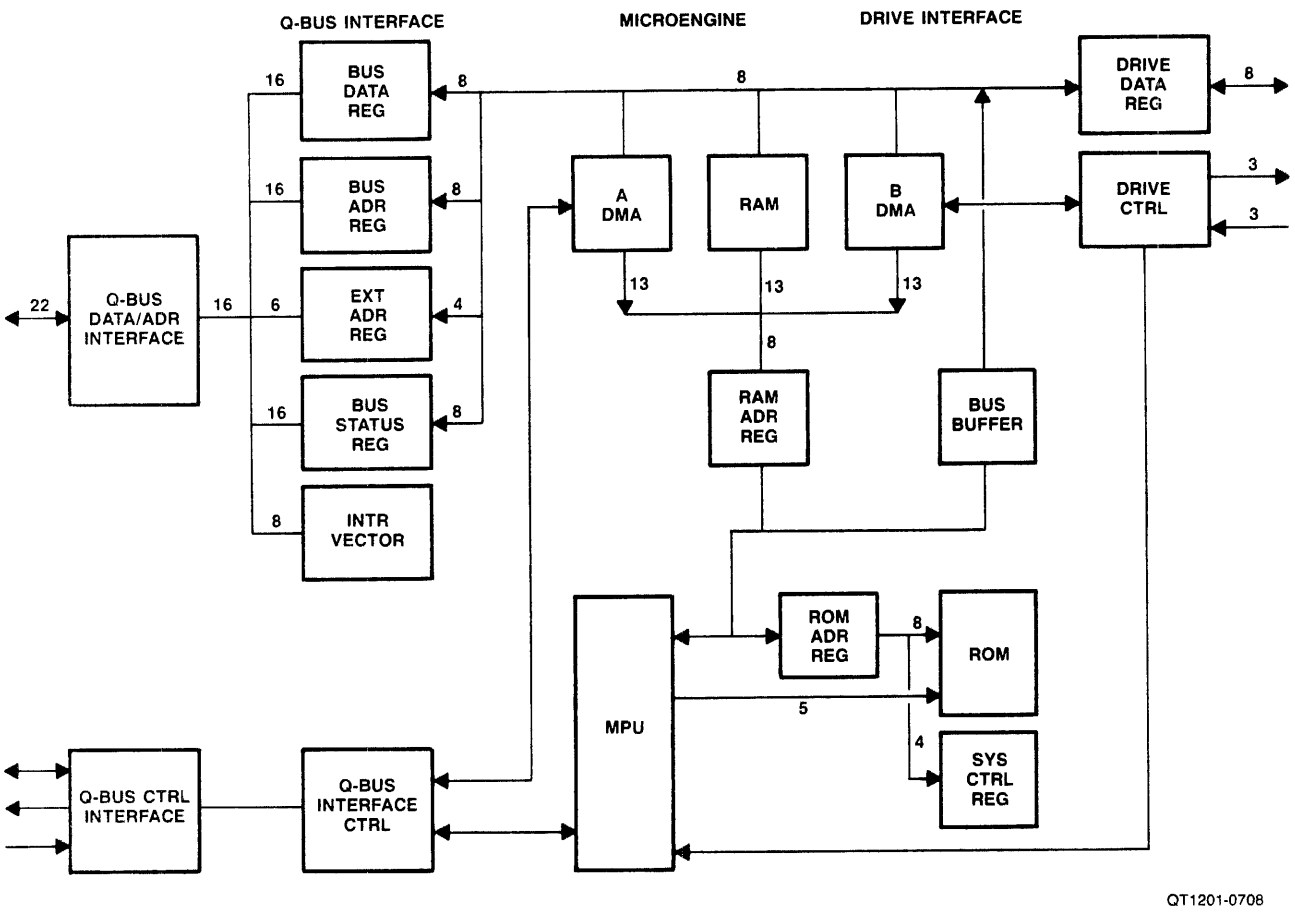


Figure 6-1. QT12 Tape Controller Block Diagram

The microengine has seven principal components:

- **MPU (Microprocessor Unit).** Fetches and executes instructions and performs calculations necessary to its control functions. It has access to one page of the RAM buffer, which it uses for writing and reading control headers and for handling command and message packets.
- **ROM Address Register.** Holds the lower eight bits of the ROM address during the data portion of the instruction fetch.
- **ROM (Read-only Memory).** Holds all the instructions for the MPU.
- **System Control Register.** Contains 16 control lines selected by four bits of the ROM address. When enabled by an MPU port bit, these signals are used to enable internal bus sources, clock data into bus destinations. and perform various control functions.
- **Bus Buffer.** Isolates the microengine from the internal data bus, so that the MPU can fetch and execute instructions while the DMA controllers are performing DMA operations.
- **RAM (Random Access Memory) Address Register.** Holds the RAM address during the data portion of a RAM read or write cycle by the MPU. Addresses 8 through 14 are pulled high for this function.
- **RAM.** To avoid the long repositioning delay associated with streaming drives, the QT12 buffers records in an on-board 16K byte buffer containing 32 pages of 512 bytes each. Because the MPU is not in the data path, all data going into or out of the QT12 must pass through the RAM.

6.2.2 LSI-11 BUS INTERFACE

The LSI-11 bus interface communicates data, commands, and status to the LSI-11 bus. It includes the following components:

- **LSI-11 Bus Data/Address Interface.** Buffers data, address, command, and status information.
- **Bus Data Register.** Passes bidirectional DMA data to the LSI-11 bus, and receives command packet addresses from the LSI-11 bus.

- **Bus Address Register.** Generates the 16 lower address bits for DMA operations. It is incremented by 1 for byte transfers and by 2 for word transfers. A carry is forwarded to the Extended Address Register. The MPU loads the Bus Address Register with the starting address at the start of each transfer.

- **Extended Address Register.** Handles address bits <A21:16>. It is loaded from the LSI-11 bus for command packet pointers, or from the MPU at the start of DMA transfers. During DMAs, it is incremented on a carry from the address register.

- **Interrupt Vector.** Output to the LSI-11 bus during an interrupt.

- **LSI-11 Bus Control Interface.** Buffers the LSI-11 bus control lines.

- **LSI-11 Bus Interface Control.** Handles all handshaking with the LSI-11 bus. It acquires the bus for DMA and interrupt operations and controls the bus registers and interface. It passes control and status between the interface and the MPU and A-DMA controller.

- **A-DMA.** Addresses internal RAM for the data communicated on the LSI-11 bus. It also keeps the byte count and interrupts the MPU when the transfer is complete.

The QT12 PCBA is designed to interface with connector rows A and B on the LSI-11 CPU backplane. The 18 pins in each connector row are reference designated A through V, except that letters G, I, O, and Q (from right to left) are not used. In designations of pin/signal assignments, the component side of the PCBA is side 1 and the solder side is side 2.

NOTE

In this manual, directions for locating components on the PCBA assume that the QT12 is being viewed from the component side with edge connectors A and B at the bottom.

Table 6-1 lists and describes LSI-11 bus interface pin assignments. These signal lines communicate data, commands, and status information between the CPU and the QT12. See also subsection 1.8 for LSI-11 bus interface specifications.

Table 6-1. LSI-11 Bus Interface Pin Assignments

Connector A Signal			Connector B Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
BIRQ5 L	A	+5	BDCOK H	A	+5
BIRQ6 L	B	-12	BPOK H	B	-12
BDAL16 L	C	GND	BDAL18 L	C	GND
BDAL17 L	D	+12	BDAL19 L	D	+12
SSPARE1	E	BDOUT L	BDAL20 L	E	BDAL2 L
SSPARE2	F	BRPLY L	BDAL21 L	F	BDAL3 L
SSPARE3	H	BDIN L	SSPARE	H	BDAL4 L
GND	J	BSYNC L	GND	J	BDAL5 L
MSPAREA	K	BWTBT L	MSPAREB	K	BDAL6 L
MSPAREB	L	BIRQ4 L	MSPAREB	L	BDAL7 L
GND	M	BIAKI L	GND	M	BDAL8 L
BDMRL	N	BIAKO L	BSACK L	N	BDAL9 L
BHALT	P	BBS7 L	BIRQ7 L	P	BDAL10 L
BREF L	R	BDMGI L	BEVNT L	R	BDAL11 L
+5B or +12B	S	BDMGO L	+12B	S	BDAL12 L
GND	T	BINIT L	GND	T	BDAL13 L
PSPARE1	U	BDAL0 L	PSPARE2	U	BDAL14 L
+5B	V	BDAL1 L	+5	V	BDAL15 L

6.2.3 TAPE TRANSPORT INTERFACE

The tape transport interface passes data, control, and status between the controller and the tape transport. It includes the following components:

- **B-DMA.** Addresses RAM for data to or from the tape drive. It keeps track of the byte count and informs the microengine of the block completion.
- **Drive Data Register.** Transmits and receives data over the drive data lines.
- **Drive Control.** Performs the handshaking with the tape drive interface. It controls the drive data register and communicates with the B-DMA controller for byte transfer timing.

Table 6-2 defines input/output pin assignments; all odd pins are grounded at both host and drive. Cables are described in subsection 2.7, Cabling. See also subsection 1.8 for tape transport interface specifications.

Table 6-2. Input/Output Pin Assignments

Pin	Name	Description
12	HB7	Host bus bit 7: MSB of eight-bit bidirectional data bus.
14	HB6	Host bus bit 6.
16	HB5	Host bus bit 5.
18	HB4	Host bus bit 4.
20	HB3	Host bus bit 3.
22	HB2	Host bus bit 2.
24	HB1	Host bus bit 1.
26	HB0	Host bus bit 0: LSB of eight-bit bidirectional data bus.
28	ONL	Online: This signal is grounded by the host. Always online.
30	REQ	Request: Host-generated signal that indicates command data have been placed on the data bus, or status data have been accepted from the data bus.
32	RST	Reset: Host-generated signal to cause drive reset (same as power-up reset).
34	XFR	Transfer: Host-generated signal to indicate that write data have been placed on data bus, or read data have been taken from the data bus.
36	ACK	Acknowledge: Drive-generated signal that indicates the drive has taken write data from the data bus or placed read data on the data bus.
38	RDY	Ready: Drive-generated signal that indicates the following conditions: • Command data have been taken from the bus. • Status data have been placed on the bus.

(Continued)

Table 6-2. Input/Output Pin Assignments (Continued)

Pin	Name	Description
		• Rewind, Retension, or Erase command has completed. • A buffer is ready to be filled, or a Write File Mark command may be issued in write mode. • A Write File Mark function has completed. • A buffer is ready to be emptied in read mode. • The drive is ready to receive a new command.
40	EXC	Exception: Drive-generated signal that indicates an exception condition within the drive.
42	DIR	Direction: Drive-generated signal that controls the direction of the bidirectional data bus. False (high) indicates host to drive; true (low) indicates drive to host.

6.3 TAPE FORMAT

The QT12 is compatible with both QIC-24 and QIC-11 format and recording standards. The method of recording is NRZI (non-return to zero inverted), where 1 is represented by a flux reversal in the bit cell and 0 is represented by the absence of a flux reversal. Figure 6-2 illustrates the tape data format for the QIC-24 standard.

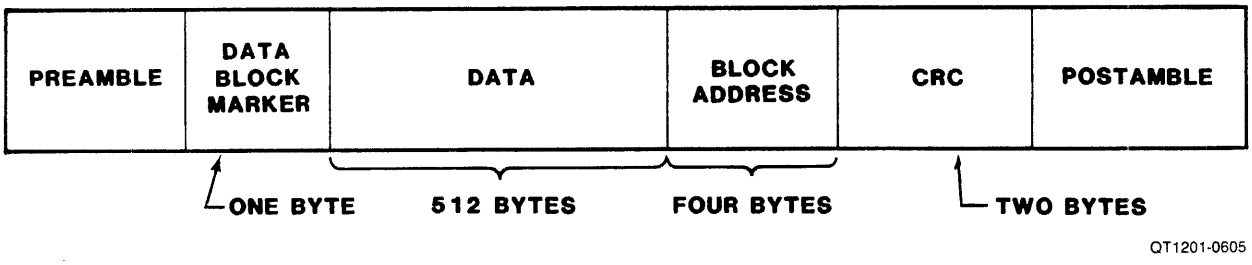


Figure 6-2. QT12 Tape Controller QIC-24 Tape Format

The following paragraphs define each of the fields in Figure 6-2 and note the differences between the QIC-24 and QIC-11 formats.

- **Preamble:** Used to synchronize the phase locked loop (PLL) in the read electronics to the data frequency; normally contains 120 to 300 flux reversals.
- **Data Block Marker:** A one-byte code that identifies the start of data.
- **Data:** Contains 512 bytes of either data or file marks.
- **Block Address:** In the QIC-24 format, a four-byte field that identifies a block recorded on tape. In the QIC-11 format, the block address consists of one byte.
- **CRC:** Cyclical redundancy check, consisting of two bytes calculated from the data and block address.
- **Postamble:** Used as a guard band; normally consists of five to 20 flux reversals.

Appendix A
RELATED DOCUMENTATION

The DEC manuals listed in this appendix may be ordered from the following address:

Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

Title:	RT-11 System Utilities Manual
Publication Number:	AA-M239B-TC
Title:	RT-11 System User's Guide
Publication Number:	AA-5279C-TC
Title:	RSX-11M/M-PLUS Utilities Manual
Publication Number:	AA-L681A-TC
Title:	RSTS/E Utilities Reference Manual
Publication Number:	AA-EZ11A-TC

The Emulex manuals listed in this appendix may be ordered from the following address:

Emulex Corporation
3545 Harbor Blvd.
Costa Mesa, CA 92626
(714) 662-5600 TWX 910-595-2521

Title:	QT12 Installation Diagnostics (T1QX1A/T1QX2A) User's Guide
Publication Number:	PX9950909
Title:	QT12 Logic and Data Reliability Diagnostic (T1QX3A) User's Guide
Publication Number:	PX9950910
Title:	QT12/TC03 MicroVAX TS11 Emulation Installation Diagnostic (IQT12) User's Guide
Publication Number:	VX9950906
Title:	Emulex MicroVMS TS11 Software Driver (TSDRIVER) Installation Guide
Publication Number:	VD9950902
Title:	Emulex QT12 Tape Controller Board Level Cabling Kit Instruction Sheet
Publication Number:	QT1252401

BLANK

The following code is provided for your use in bootstrapping a QT12 tape. This program can be entered into memory from ODT and executed, or assembled and run from an existing system device. The program starts at 10000. This code can **not** be used on the MicroVAX.

```
 1                                      .TITLE    MS BOOTSTRAP MODULE
 2    000000                            .ASECT
 3                 007776               . = 7776
 4    007776       046523               .WORD     "SM"              ;Device ID
                                                                    ;reversed
 5    010000       012701    START:     MOV       #172522,R1        ;R1=TSSR
      010002       172522
 6    010004       010102               MOV       R1,R2             ;R2=TSSR
 7    010006       005000               CLR       R0                ;Clear R0
 8    010010       105711    1$:        TSTB      @R1               ;Wait for
                                                                    ;SSR
 9    010012       100376               BPL       1$
10    010014       010704               MOV       PC,R4             ;R4=PC of
                                                                    ;"SM"+20
11    010016       112737               MOVB      #200,@#172523     ;Write
                                                                    ;byte bit
                                                                    ;15
      010020       000200
      010022       172523
12    010024       005242               INC       -(R2)             ;Write
                                                                    into TSDB
13    010026       105711    2$:        TSTB      @R1               ;Wait for
                                                                    ;SSR
14    010030       100376               BPL       2$
15    010032       005711               TST       @R1               ;? Error?
16    010034       100761               BMI       START             ;If SC=1
                                                                    ;retry,
                                                                    ;else
17    010036       005007               CLR       PC                ;jump to
                                                                    ;zero
18                 010000               .END      START
```

BLANK

Appendix C
GLOSSARY

C.1 OVERVIEW

This subsection contains definitions of technical terms that are used in this manual. Some of these definitions may differ from standard usage. For definitions of other terms, you may wish to consult The DEC Dictionary, which can be ordered from the following address:

Digital Press
30 North Ave.
Burlington, MA 01803

C.2 DEFINITIONS

Access Time: The time between issuance of a tape read, write, or space command (by the controller) and the reading or writing of the first character in the target tape record.

BOT: Beginning of tape marker, which marks the physical beginning of the tape.

Command Packet (I/O Request): A set of control words issued from the CPU (i.e., from the operating system, I/O driver, or diagnostic program) to the QT12 to initiate and control operation.

Command Buffer: An area of contiguous 16-bit words in the host CPU's memory space. The I/O Request Packets are built there and are retrieved by the QT12.

Command Delay: The elapsed time between the indication from the controller signifying the completion of an operation (e.g., Read or Write) and the issuance of the next command to the controller by the operating software.

Command Pointer: The high (most significant) 16 bits of an 18-bit modulo-4 address which points to a command packet located in the CPU's memory space. In extended operation, the term command pointer refers to the high 20 bits of a 22-bit modulo-4 address which points to a command packet located in the CPU's memory space.

Configuration: The physical and logical arrangement of a system; the manner in which the parts of the system relate to one another.

EOT: End of tape marker, which marks the physical end of the tape.

Extended Features: Mode of operation of the QT12 which extends the functionality of the subsystem beyond that allowed by DEC's TS11/TS04 compatibility. Includes 22-bit memory addressing and additional status and functions. Requires use of special software, which is not supplied with the QT12 and which may not presently exist.

Header Word: The first word of a command packet or message packet (q.v.).

Message Buffer: An area of contiguous words in the CPU's memory space. The message packets are stored there by the QT12.

Message Packet: A group of status words issued from the QT12 to the CPU to indicate status of the magnetic tape subsystem and/or operation completed.

Modulo-4 Address: An address within the CPU's memory space which is evenly divisible by 4 (that is, octal 0, 4, 10, 14, 20, and so on).

TSBA: QT12 Bus Address Register--a read-only hardware register in the I/O address space.

TSDB: QT12 Data Buffer Register--a write-only hardware register in the I/O address space.

TSSR: QT12 Status Register--a read/write register in the I/O address space.

TXSTn: Extended Status Register n, one of five status registers deposited into the Message Buffer area.

Packet: A contiguous sequence of words.

Packet Protocol: A method of communication between CPU software and the QT12 via areas in CPU memory space, following the rules dictated by DEC's TSV05 compatibility requirements. The QT12 accesses a command packet (q.v.), located in a command buffer area in CPU memory space, to provide status information to the software. This technique allows large amounts of information to be passed while allowing the device to occupy only two hardware I/O addresses.

Q-22: LSI-11 system bus containing 22-bit memory addressing capability.

Record Buffering: Capability of the QT12 to store an entire tape record, up to 15872 bytes in length, during Read or Write command sequences to allow overlapping of tape repositioning with transfer of data to and from the CPU.

Reinstruct Time: The period of time following reading or writing the last character of a record allowed by a tape transport for a controller to issue the next command in order to avoid slowing or stopping the tape.

Repositioning: A characteristic of a streaming tape drive whereby tape motion is halted and the tape is readied for the next operation by decelerating the tape current direction and bringing it to a stop, then accelerating and decelerating the tape in the opposite direction and bringing it to a stop. The tape is not stopped in the gap, as with conventional tape drives.

Streaming Technology: Operation of a magnetic tape transport without stopping in the inter-record gap. Requires that, for maximum efficiency, commands of similar type, speed, and direction be supplied by the controller within a relatively short reinstruct period (q.v.). The 0.25-inch streaming QIC-02 cartridge drives operate in this fashion.

Start/Stop Technology: (Formatted, Conventional) Operating characteristic of a magnetic tape drive that can rapidly accelerate and decelerate tape motion to allow the tape to come to rest with the read/write head positioned in the inter-record gap.

Zero Block File: A file that contains no data.

EMULEX

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publication.

Manual Part Number _____ **Rev.** _____

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

What features are most useful? _____

What faults or errors have you found in the manual? _____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

☐ Please send me the current copy of the *Controller Handbook*, which contains the information on the remainder of EMULEX's controller products.

Name _____ Street _____

Title _____ City _____

Company _____ State/Country _____

Department _____ Zip _____

Additional copies of this document are available from:

Emulex Corporation
3545 Harbor Boulevard
P.O. Box 6725
Costa Mesa, CA 92626
Attention: Customer Services

Fold Here and Staple

Do Not Tear — Fold Here

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 202 COSTA MESA. CA

POSTAGE WILL BE PAID BY ADDRESSEE

EMULEX CORPORATION
3545 HARBOR BOULEVARD
P.O. BOX 6725
COSTA MESA, CALIFORNIA 92626
ATTN: TECHNICAL PUBLICATIONS