APPENDIX G

4-BIT COLOUR GRAPHICS OUTPUT CARD

G1 General Description

The 4-bit Colour Graphics Output Card accepts a 4-bit monochrome signal (produced by 4 memory planes) and produces a 16 colour output. Each colour has a possible 2^4(16) level output, thus the 16 colours can be chosen from any of 16^3(4096) possible colours. This is achieved by programming a look-up table with the required data.

The output of the card will directly drive a colour TV monitor. Mixed synchronisation signal is output on green.

The card will accept the outputs of up to 28 1-bit memory planes. By the use of a 4-way selector different memory planes can be selected thus changing the picture.

The output of one memory plane can be connected to provide for a cursor. The colour of the cursor is chosen from one of the 16 available colours. The colour is programmed via wire links on the PCB. Alternatively, the colour can be software controlled with the addition of extra memory planes.

A VDU input (balanced line) allows for an asynchronous signal to produce a white output superimposes on the graphics display. (e.g. alphanumerics).

G2 Detailed Description

G2.1 Board Address

More than 1 graphics output card can be incorporated. The maximum number plus their memory planes must not exceed 32. e.g. if each output card has 4 memory planes and 1 cursor plane the maximum = 5 (5 x 4 memory planes + 5 x 1 cursor plane + 5x1 O/P cards = 30).

Each card requires 2 addresses:

a. LS address - Selects address register
b. HS address - Selects data register.

The board address is achieved using a link field on the PCB. Table G2.1 shows the addresses and the required links to be fitted.

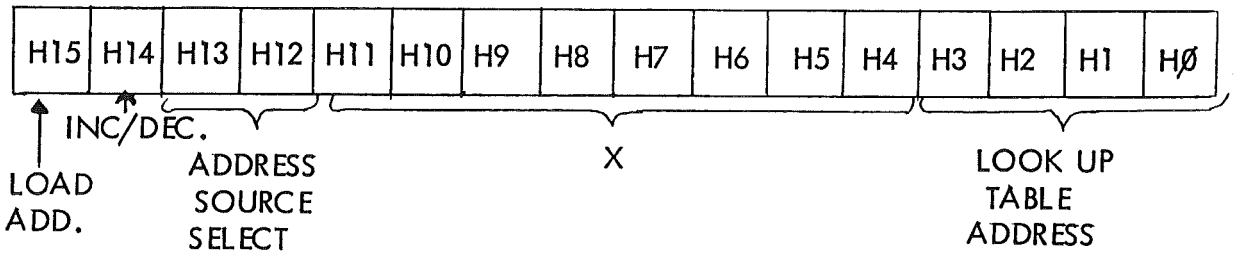
PDP/11-LSI/11 Address (Octal)	Links				Function
	1	2	3	4	
170100 - 170102	0	0	0	0	O/P Card Ø
170104 - 170106	1	0	0	0	O/P Card 1
170110 - 170112	0	1	0	0	O/P Card 2
170114 - 170116	1	1	0	0	O/P Card 3

0 - Link to 0V
1 - Link to 5V

TABLE G2.1 - Board Address Linking

G2.2 Programming of Look-Up Table

G2.2.1 Address Register



G2.3 Circuit Description

G2.3.1 Loading Look Up Table

Fig. G2.3.1 shows the timing diagram for loading data into the look-up table (RAM).

The address, A1 - A5 is fed into a magnitude computer (C6) for board addressing. AØ selects data register or address register.

The RAM address is fed onto H0-H3 which is clocked into an up/down counter B1, by WRITE via C13. H14 selects whether B1 is to be incremented or decremented. H15 is set to enable B4 such that the address is loaded onto the internal 4-bit address bus. H15 also blanks the video output while the look up table is being loaded. ELCLK clocks the address through C4 and C5 onto the RAMs.

Bit AØ is then set to enable writing of Data. Data is fed from H0-H11 (12 bits) onto the internal data bus to the RAMs. "WRITE" clocks the data in (via C13).

The trailing edge of WRITE increments (or decrements if H14 = 0) the up/down counter. ELCLK clocks this next address through C4 and C5 onto the RAMs. The data loading is then repeated until all RAM is loaded.

G2.3.2 Outputting Data from Memory Planes

The balanced lines of the memory planes are fed to line receivers (A7 - A13). Only those used are fitted onto the PCB. These are patched to flip-flops (B10 - B13). Again only those flip-flops used are fitted. ELCLK clocks the data through onto the 4-bit internal address bus.

It is then clocked through flip-flops C4 & C5 by the next positive edge of ELCLK. It is then clocked into the RAMs by a third ELCLK pulse. This clocking by ELCLK delays the video output to the memory plane output by 3 pixel cycles but ensures that the RGB video outputs are in synchronism with each other.

G2.3.3 Video O/P

The RAMs output the data from the addressed location. There are 4 bits per colour. Each 4 bits are fed to a D-A converter then to a co-axial output enabling it to drive a video monitor directly.

G2.3.4 Blanking

Blanking is achieved by turning on the Nand gates (D1 - D3). Blanking can be initiated by a number of sources.

a. When loading the look up table, (via D8 pin 15).
b. LUNBNK - line unblank
c. FUNBNK - Frame unblank
d. Ext. Blnk. - External blank

LUNBNK is delayed by D1. It has a different delay for going active and inactive.

The VDU input overrides blanking.

G2.3.5 VDU Input

Colour VDU's may be overlayed as follows :

On the customisation wiring connect CD1, CC1, CE1/2 CH1/2 as follows:

BV1 Red VDU+	CD1 Green VDU+	CE2 Blue VDU+
BV2 Red VDU-	CC2 Green VDU-	CE1 Blue VDU-

Remove the 'necked' track between patch pins R-G, B-G, remove necked track to 'C'.

Patch as follows V patched to R
D27 patched to G
D26 patched to B.

G2.3.6 Mixed Synchronisation

The mixed sync signal is fed out on the green video output. Because of delays of the video signal, mixed sync is also delayed via C10 and D11, both being clocked by ELCLK.

G2.3.7 Cursor

A memory plane is fed to the cursor input (C10). This disables B11 - B13 and enables B10. The 4 bits input to IC28 determine the colour of the cursor. The colour can either be hard-wired via the patch panel or be software controlled by feeding in 4 memory planes to B10. The colour of the cursor will be one of the 16 colours selected.

G3 Applications of the 4-Bit Graphics O/P Card

This section describes some of the ways the 4 bit graphics output card can be used.

G3.1 16 Colour

This is perhaps the simplest application where each of the 16 codes represents a different colour. Table G3.1 shows the codes to be programmed in the look up table for an 8 colour system. In this case each code would be loaded into 2 locations so as to fill the look up table completely. The order in which they are arranged will depend upon the application to give the best contrast or the most meaningful picture.

G3.2 8 Colour Graphics + Overlay

Fig. G3.1 shows the 16 positions of the look up table. The overlay (O/L) is provided by the MSB of the 4 bits. Thus the top 8 bits of the look up table provides O/L. It can be seen, therefore, that the O/L can be just 1 colour (All 8 O/L positions programmed with the same value) or up to 8 colours. Obviously, O/L with more than one colour becomes dependant upon the background colour. This can be an advantage as this means a contrast can always be given between the O/L colour and the background colour.

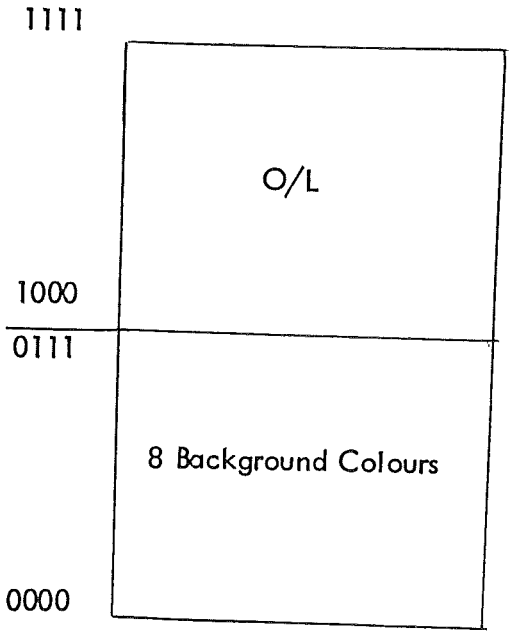


FIG. G3.1

Example : 8 background colours + 2 O/L colours

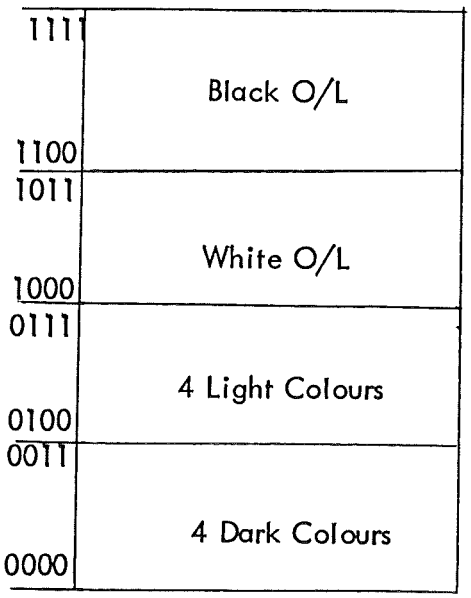


FIG. G3.2

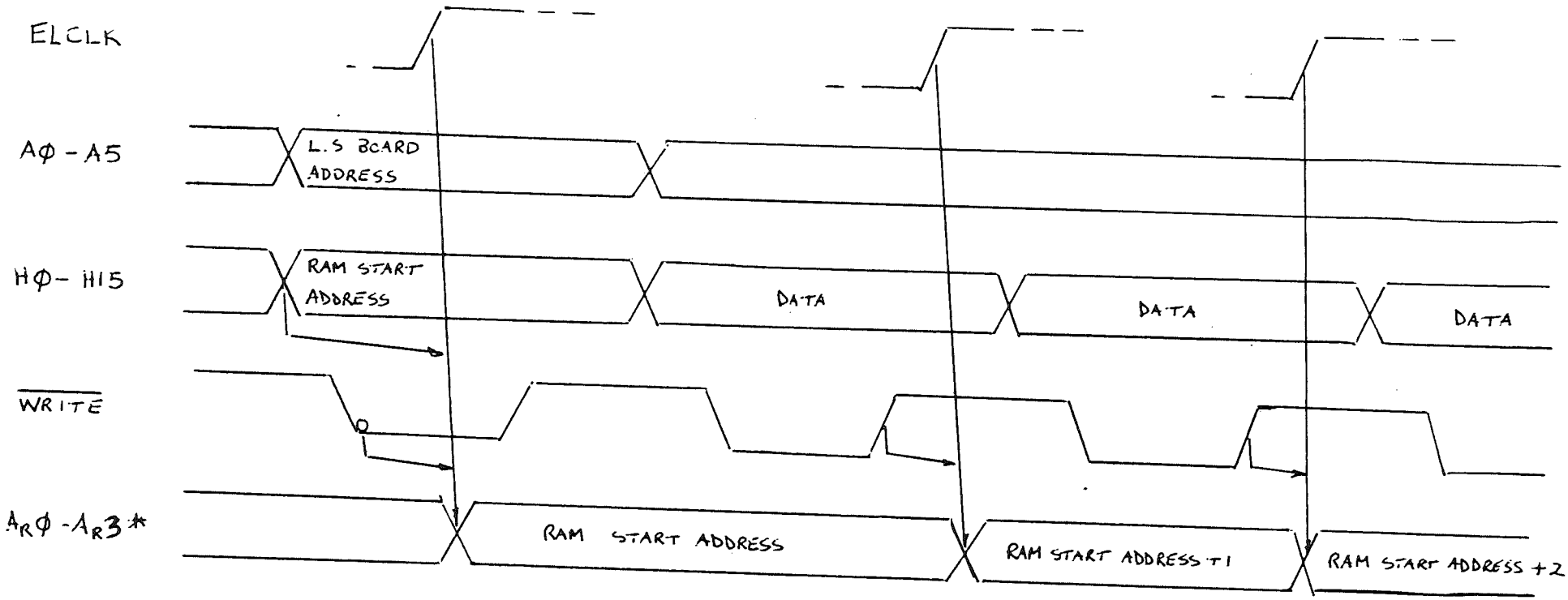
Fig. G3.2 shows how the look up table is configured. The table is arranged such that the white O/L will be selected when the background is a dark colour and black when the background is a light colour thus giving maximum contrast.

This principle can be extended by using 2 bits for O/L and 2 bits for background.

COLOUR	VIDEO O/P			OCTAL COLOUR
	RED	GREEN	BLUE	
RED	1111	0000	0000	0017
GREEN	0000	1111	0000	0360
BLUE	0000	0000	1111	7400
WHITE	1111	1111	1111	7777
BLACK	0000	0000	0000	0000
YELLOW	1111	1111	0000	0377
CYAN	0000	1111	1111	7760
MAGENTA	1111	0000	1111	7417

TABLE G3.1

LOOK UP TABLE CODES FOR 8 COLOUR SYSTEM



* LEVELS AFTER IC's C4 & C5

FIG G.2.3.1

TIMING DIAGRAM SHOWING LOADING OF LOOK UP TABLE

APPENDIX H

8-BIT PSEUDO-COLOUR O/P CARD

H1 General Description

The pseudo-colour output card accepts an 8-bit monochrome signal (produced by 8 memory planes) and produces a 256 colour output. Each colour has a possible 2^4 (16) level output, thus the 256 colours can be chosen from any of 16^3 (4 096) possible colours. This is achieved by programming a look up table with the required data.

The output of the card will directly drive a colour TV monitor. Mixed synchronisation signal is output on green.

The card will accept the output of up to 28 1-bit memory planes. By the use of a 4-way selector different memory planes can be selected thus changing the picture.

The output of 1 memory plane can be connected to provide a cursor. The colour of the cursor is chosen from one of the 256 available colours. The colour is programmed via wire links on the PCB. Alternatively, the colour can be software controlled with the addition of extra memory planes.

A VDU input (balanced line) allows for an asynchronous signal to produce a white output superimposed on the graphic display (e.g. for alphanumerics.)

H2 Detailed Description

Figure H2.1 shows a block diagram of how an 8 bit Pseudo-Colour O/P Card is connected into a 214 system.

Data in can take 2 forms, synchronous and asynchronous. Synchronous data is synchronised to the 214 clock and is directed through the LUT. Asynchronous data is not synchronised to the 214 clock and is not directed through the LUT. Asynchronous data will always give a peak white O/P (e.g alpha-numerics can be O/P asynchronously).

Syncrhonised data is fed to the LUT. The LUT sees the 8-bit data as an address. The contents of this address is the data value that is O/P to the monitor.

The value of the data stored in the LUT is programmable. For method of programming the LUT see detailed description (H2.2.).

H2.1 Board Address

More than one pseudo-colour O/P card can be incorporated. The maximum number plus their memory planes must not exceed 32. If each output card has 8 memory planes and 1 cursor plane the maximum = 3 (3 x 8 memory planes + 3 x 1 cursor planes + 3 x 1 O/P card = 30).

Each card requires 2 addresses:

a. LS address - selects address register
b. MS address - selects data register.

The board address is achieved using a link field on the PCB. Table H2.1 shows the addresses and the required links to be fitted.

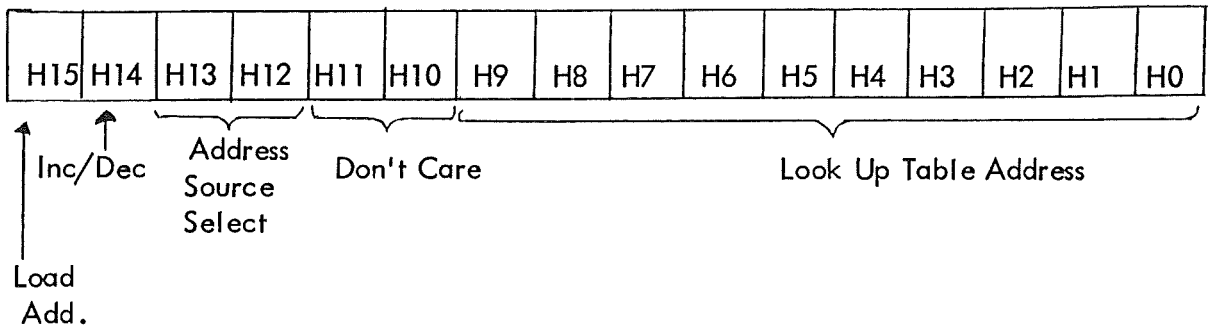
PDP11 - LSI11 Address (octal)	Links				Function
	1	2	3	4	
170100 - 170102	0	0	0	0	O/P Card Ø
170104 - 170106	1	0	0	0	O/P Card 1
170110 - 170112	0	1	0	0	O/P Card 2
170114 - 170116	1	1	0	0	O/P Card 3

0 - Link to 0V
1 - Link to 5V

TABLE H2.1 - Board Address Linking

H2.2 Programming of Look-Up Table

H2.2.1 Address Register

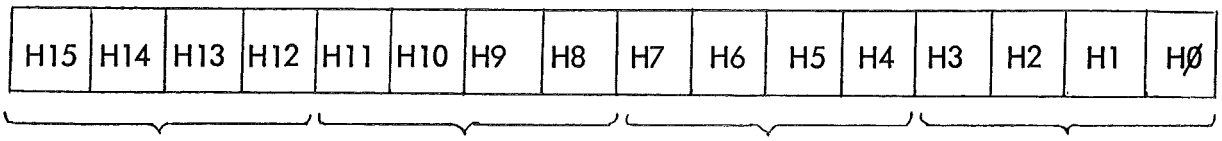


HØ - H9 - LOOK UP TABLE ADDRESS (0 - 1Ø23)

H12 - H13 - ADDRESS SOURCE SELECT - Selects 1 of 4 groups of memory planes. This is the mechanism to display different pictures from different memory planes. (Ø - 3).

H14 - INC/DEC - Allows for automatic increment or decrement of the RAM address when writing data to RAM. This facility does not occur when reading data from RAM. 1 = INC, Ø = DEC.

H15 - LOAD ADDRESS - Should be set to enable access to the address register for loading the look up table. When set the display will be blanked.



The data register is 12 bits, 4 bits for each colour.

It can be seen from the above that the procedure for loading the look up table is:

a. Select Address Register
b. Write look up table start address
   Set H14 as required
   Set H15
c. Select Data Register
   Write data to every location (the address is automatically incremented/decremented each data write cycle).
d. Select Address Register
   Set H12 and H13 as required
   Reset H15.

The output card will now output video data.

H2.3 Circuit Description

Figure H2.3 shows a block diagram of the Pseudo-Colour Card.

H2.3.1 Loading Look-Up Table

Fig. H2.3.1 shows the timing diagram for loading data into the look-up table (RAM).

The address A1 - A5 is fed into the magnitude comparitor D3 for board addressing. AØ selects data register or address register. The RAM address is fed onto HØ - H9 (10 bits) which is clocked into an up/down counter (B1 - B3) by write via D2.

The up/down counter consists of 3 binary counters cascaded to produce a 10 bit internal address bus. H14 (INC/DEC) either enables the address to count up or count down. H15 is set to enable B5 and B6 loading the address onto the internal address bus. H15 also blanks the video output while the look-up table is being loaded. ELCLK clocks the address through D9 and D10 onto the RAMs.

Bit AØ is then set to enable writing of Data. Data is fed from HØ-H11 (n-bits) onto the internal data bus to the RAMs. 'Write' clocks the data into the RAMs. The trailing edge of write increments (or decrements if H14 = 0) the up/down counter. ELCLK clocks this next address through D9 and D10 onto the RAMs. The data loading is then repeated until all RAM is loaded.

H2.3.2 Reply

Reply to the computer is generated by monostables 4ca and 4cb. In the absence of a Read or Write 4cb is held reset by 7B2. When a Read or Write is received, the reset on 4cb is released and 4Ca is triggered provided that it is enabled at pin 4Ca2 by the device address. 4C1 13 goes high which triggers 4Cb. The Q output of 4Ca is "anded" with the Q output of 4Cb at 4B6 to generate Reply, and the Write pulse is "ANDED" with the Q output of 4Ca at 9B8 to generate the registers write pulse. This circuit arrangement ensures that when writing to the registers, Reply is sent after the Write Registers pulse has expired. This is a particular requirement of the address register (1C, 2C, 3C) because it has a latch type load input.

H2.3.3 Outputting Data from Memory Planes

The balanced lines of the memory planes are fed to line receivers (A8 - A14). Only those used are fitted onto the PCB. These are patched to flip-flops (B10, B11, B13, B14) Again, only those flip-flops used are fitted. ELCLK, clocks the data through onto the 8 bit internal address bus. It is then clocked through flip-flops D9 and D10 by the next positive edge of ELCLK. The RAM data is output to ICs D14, C14 and C13 which is clocked by a 3rd ELCLK pulse. This clocking by ELCLK delays the video output to the memory plane output by 3 pixel cycles, but ensure that the RGB video outputs are in synchronism with each other.

H2.3.4 Video O/P

The RAMs output the data from the addressed location. There are 4 bits per colour. Each 4 bits are fed to a D-A converter then to a co-axial output enabling it to drive a video monitor directly.

H2.3.5 Blanking

Blanking is achieved by turning on the Nand gates (D11-D13). Blanking can be initiated by a number of sources.

a. When loading the look-up table. (via D4 Q4).
b. LUNBNK - line unblank
c. FUNBNK - Frame unblank
d. Ext Blank - External Blank.

LUNBNK is delayed by D7. It has a different delay for going active and inactive.

The VDU input overrides blanking.

H2.3.6 VDU Input

The VDU input is fed in on a balanced line to ICs D11, D12 and D13 via ICD8. This sets all the 12 O/P bits thus giving a white video signal. This signal overrides the RAM O/P.

H2.3.7 Mixed Synchronisation

The mixed sync signal is fed out on the green video output. Because of delays of the video signal, mixed sync is also delayed via ICD1 and ICD7 both being clocked by ELCLK.

H2.3.8 Cursor Input

A memory plane is fed to the cursor input (D1). This disables ICB11-ICB14 and enables ICB10. The 8 bits input to ICB10 determine the colour of the cursor. The colour can either be hard wired via the patch panel or be software controlled by feeding in extra memory planes to ICB10.

H3 Applications of the 8 Bit Pseudo-Colour O/P Card

This section describes some of the ways the pseudo-colour O/P card can be used.

H3.1 Simple Pseudo-Colour

A range of colours is selected and loaded into the look up table accordingly. Up to 256 different colours can be selected. If less colours are required the colour information is loaded into more than 1 address. e.g. if 128 colours are required each colour is loaded into 2 addresses of the look up table.

H3.2 Pseudo-Colour O/P + Overlay (8 bits only)

Fig. H3.1 shows the 256 positions of the look up table. The overlay (O/L) is provided by the MSB of the 8 bit RAM address. Thus the top 128 bits of the look up table provides O/L. It can be seen, therefore, that the O/L can be just 1 colour (all 128 O/L positions programmed with the same value) or up to 128 colours. Obviously, O/L with more than one colour becomes dependant upon the background colour. This can be an advantage as this means that a contrast can always be given between the O/L colour and the background colour.

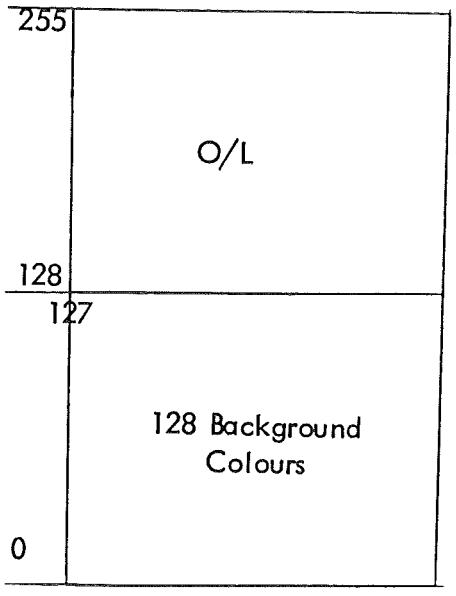


Fig. H3.1

This principle can be extended by using more than 1 bit for O/L.

H3.3 Cursor

A cursor can be implemented in 2 different ways:

a. The Cursor Input

The cursor plane is fed through one of the balanced line receivers and via the patch panel, is connected to the cursor pin. When the cursor goes active selector 3 is enabled and the other 3 selectors disabled. The 8 patch pins to selector 3 must be hard wired to give a LUT address. The colour required for the cursor must be the corresponding data value stored at this address. e.g. If a white cursor is required and the 8 patch pins are all pulled high, an LUT address 255 (1111 1111 binary) the data value stored in 255 must = 7777.

b. Cursor as an Overlay

The cursor can be fed into the LUT as an overlay. In the example shown in H3.2 in all locations 128 - 255 the colour value of the cursor is programmed.

H3.4 1024 Colours

The pseudo colour card can be extended to 10 bits giving a facility of 1024 colours. Other options can also be implemented. The following are a few examples.

a. 8 bit colour + overlay – cursor

b. 9 bit colour + overlay.

Note : Bits A8 and A9 are not channel selectable, but are common to all channels.

H3.5 Colour Values

Table H3.5 shows a table of octal values corresponding to various colours. The table is included as a guide to the programmer when selecting his colours. Slight variations of these values will correspond to different shades of the colours stated, thus some experimentation is required when selecting the final colours required.

The colours are programmed as a 12 bit word organised as follows :

BITS 0 - 11		
11 10 9 8	7 6 5 4	3 2 1 0
4 bits of Blue	4 Bits of Green	4 Bits of Red

H3.6 Patching Details

Figs. H3.6.2 and H3.6.3 give example patching details for a pseudo colour card. The system has 8 memory planes for 8 bit image, an overlay and a cursor. The cursor uses the cursor input.

Fig. H3.6.2 shows the actual patching required. Fig. H3.6.3 is used for software as a function indicator.

Channel 0 is used for the 8 bit image.

Channel 3 is used for the cursor.

A8 is used for the overlay.

Location 255 is the cursor location thus if white address 255 must be programmed accordingly. Fig. H3.6.1 shows how the LUT is programmed. The O/L is to be all Red.

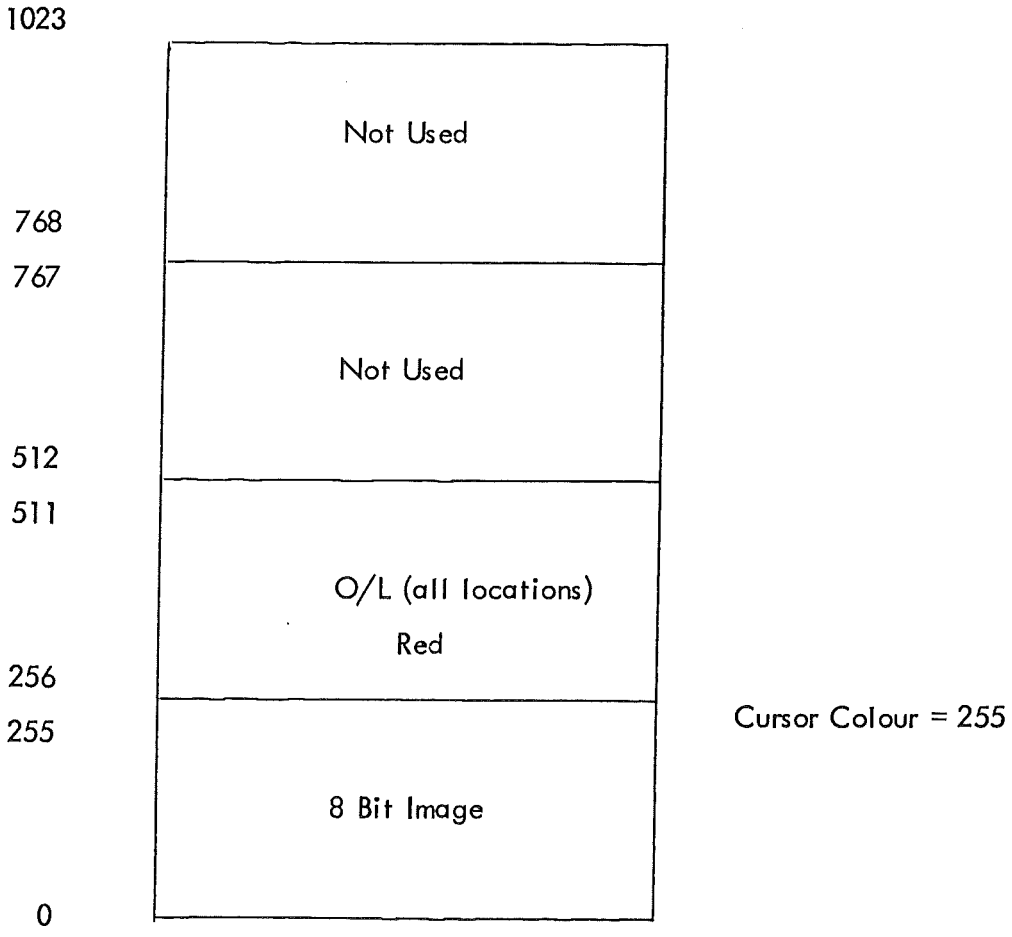


Fig. H3.6.2.1

Example of LUT Programme

H3.6.1 Unused Inputs

Some of the inputs on the patching field need to be tied to 0v when not used. These are :

a. A8

b. A9

c. Cursor

d. If a channel is partially utilised, the rest of the input on that channel.

If a whole channel is not used the inputs can be left open circuit.

H3.6.2 VDU Colour Overlay

Colour VDU's may be overlayed as follows :

On the customisation wiring connect CD1, CC1, CE1/2, CH1/2 as follows :

BV1	Red	VDU+	CD1	Green	VDU+	CE2	Blue	VDU+
BV2	Red	VDU-	CC2	Green	VDU-	CE1	Blue	VDU-

Remove the 'necked' track between patch pins R-G, B-G, remove necked track to 'C'.

Patch as follows V patched to R
D27 patched to G
D26 patched to B.

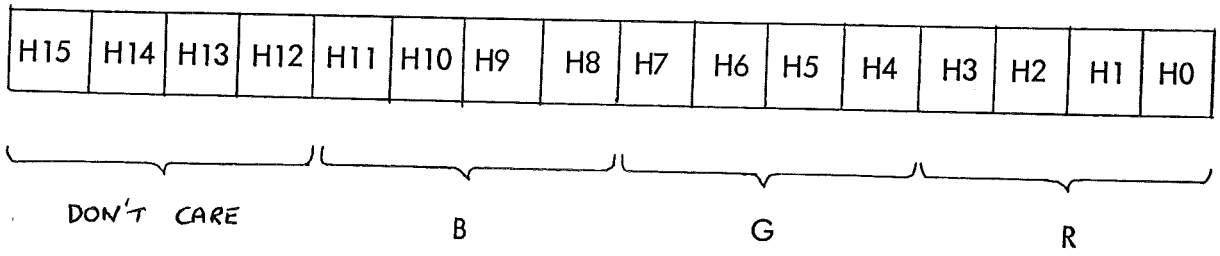
HØ - H3 - LOOK UP TABLE ADDRESS

H12 - H13 - ADDRESS SOURCE SELECT - selects 1 of 4 groups of memory planes. This is the mechanism to display different pictures from different memory planes.

H14 - INC/DEC - allows for automatic increment or decrement of the RAM address when writing data to RAM. This facility does not occur when reading data from RAM.

H15 - LOAD ADDRESS - is set when loading look up table (RAM). Also blanks display while RAM is being loaded.

G2.2.2 Data Register



The data register is 12 bits , 4 bits for each colour.

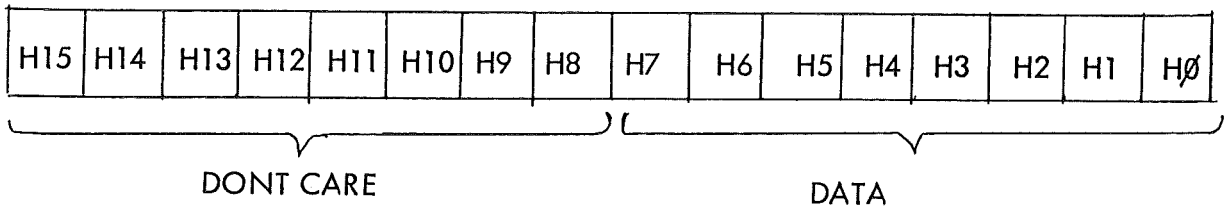
It can be seen from the above that the procedure for loading the look up table is:

a. Select Address Register
b. Write look up table start address
   Set H14 as required
   Set H15
c. Select Data Register
   Write data to every location (the address is automatically incremented/decremented each data write cycle)
d. Select Address Register
   Set H12 and H13 as required
   Reset H15.

The output card will now output video data.

HØ - H11	-	LOOK - UP TABLE ADDRESS
H12 - H13	-	ADDRESS SOURCE SELECT - Selects 1-of-4 groups of memory planes. This is the mechanism to display different pictures from different memory planes.
H14	-	INC/DEC - Allows for automatic increment or decrement of the RAM address when writing data to RAM. This facility does not occur when reading data from RAM.
H15	-	LOAD ADDRESS - Is set when loading look-up table (RAM). Also blanks display while RAM is being loaded.

F2.2.2 Data Register



The data register is 8 bits.

It can be seen from the above that the procedure for loading the look-up table is:

a. Select Address Register
b. Write look-up table start address
   Set H14 as required
   Set H15 as required
c. Select Data Register
   Write data to every location (The address is automatically incremented/decremented each data write cycle).
d. Select Address Register
   Set H12 and H13 as required
   Reset H15.

The output card will now output video data.

F2.3 Circuit Description

F2.3.1 Loading Look-Up Table

Fig. F2.3.1 shows the timing diagram for loading data into the look-up table (RAM).

FIG. H.2.1

SYSTEM O/P CONFIGURATION

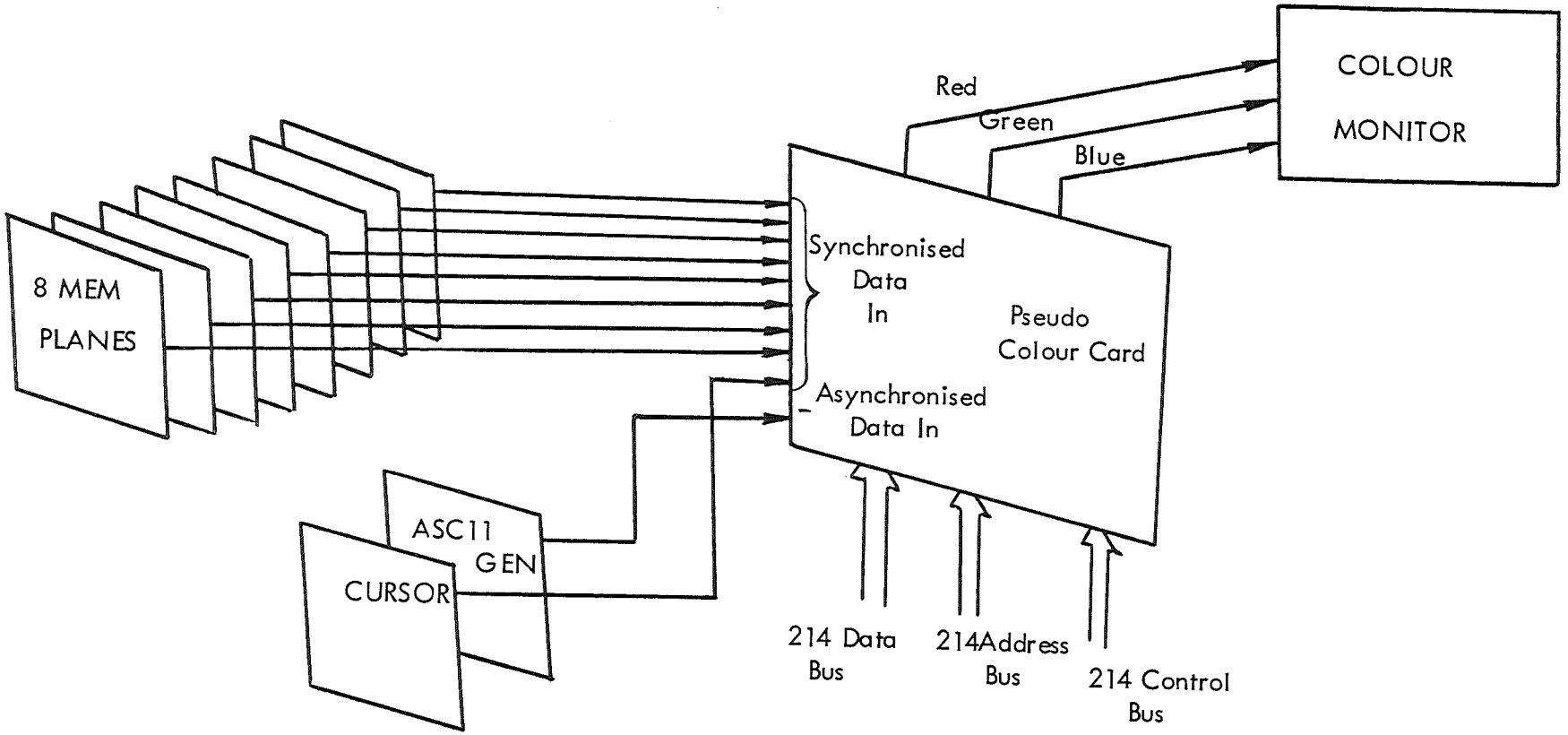
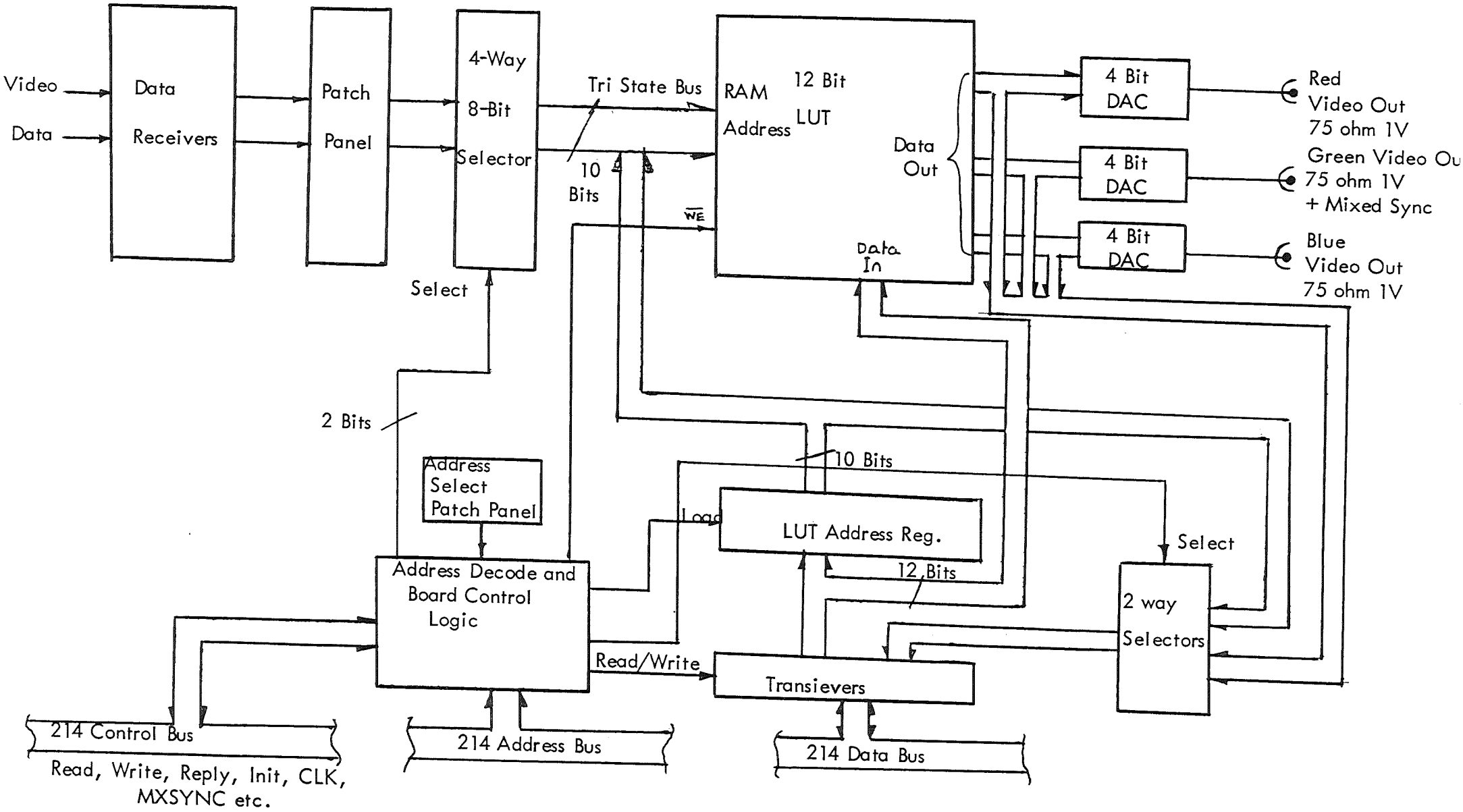
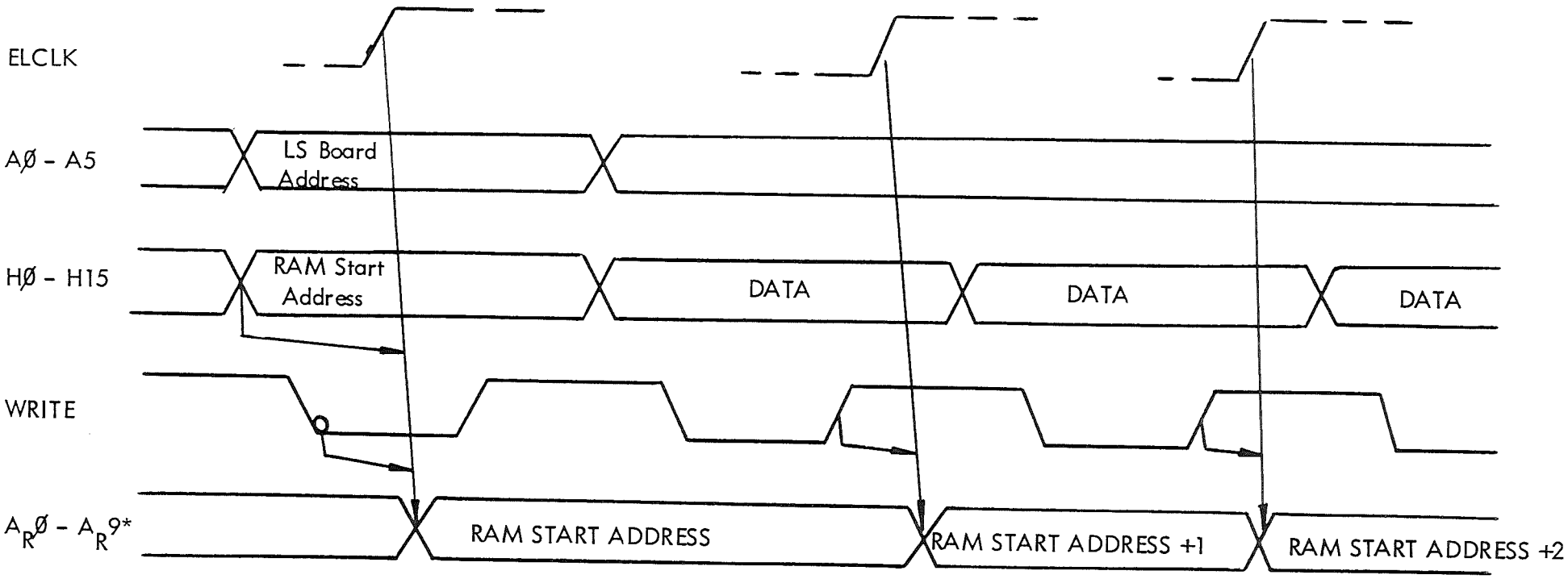


FIG. H2.3

Block Diagram of 8 bit Pseudo-Colour Card





* THE CODE AFTER D9 & D10

FIG. H2.3.1

TIMING DIAGRAM SHOWING LOADING OF LOOK UP TABLE

FIG. H3.6.2

SUPERVISOR	8 - BIT PSEUDO COLOUR O/P CARD PATCHING TABLE	
CUSTOMER	EXAMPLE PATCHING	
UNIT NO.	214-0-3-3-XXX	DATE

Data Bit(D)	Patch Panel Linking	
D0	1A	Channel Select = 00
D1	1B	
D2	1C	
D3	1D	
D4	1E	
D5	1F	
D6	1G	
D7	1H	
	2A	Channel Select = 01
	2B	
	2C	
	2D	
	2E	
	2F	
	2G	
	2H	
	3A	Channel Select = 10
	3B	
	3C	
	3D	
	3E	
	3F	
	3G	
	3H	
+5V	4A	Channel Select = 11
+5V	4B	
+5V	4C	
+5V	4D	
+5V	4E	
+5V	4F	
+5V	4G	
+5V	4H	
D8	A8	Common I/P's to all Channels
0V	A9	
D9	Cursor	

	L.U.T. Device Address		
Board Pos'n	Address	Pin No.	Destination
1	170100	1	0V
		2	0V
		3	0V
		4	0V
2	170104	1	+5V
		2	0V
		3	0V
		4	0V
3	170110	1	0V
		2	+5V
		3	0V
		4	0V
4	170114	1	+5V
		2	+5V
		3	0V
		4	0V

013-378

FIG. H3.6.3

8 - Bit Pseudo-Colour O/P Card

Memory Plane Assignment and Output Selection	Memory Card		Pseudo-Colour Look-Up Table Address Bit
	No.	Function	
O/P Channel 0	D0	8 bit image	0
	D1		1
	D2		2
	D3		3
	D4		4
	D5		5
	D6		6
	D7		7
O/P Channel 1			0
			1
			2
			3
			4
			5
			6
			7
O/P Channel 2			0
			1
			2
			3
			4
			5
			6
			7
O/P Channel 3			0
			1
			2
		Cursor Address = 255	3
			4
			5
			6
			7
All Channels		Overlay (Red)	8
			9

Org. No. 013-377 Customer :

OCTAL	COLOUR
1 - 17	15 levels of Red (17 = peak Red)
20, 40, 60, 100 etc. - 360	15 levels of Green (360 = peak Green).
400, 1000, 1400, 2000 etc. - 7400	15 levels of Blue (7400 = peak Blue)
7777	WHITE
0	BLACK

FIG. H3.5