datamate
general purpose computers

DATAMATE 70
COMPUTER REFERENCE MANUAL
PRELIMINARY EDITION
DCS - 70951

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P.O. BOX 310 BIG SPRING, TEXAS 79720 (915) 267-6353

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CHAPTER 1

FEATURES OF THE DATAMATE 70 COMPUTER

The Datamate-developed, Datamate-written assembler makes maximum utilization of the advanced hardware design, the powerful instruction repertoire, and is tailored to the users of this class of computer. A Symbolic Editor, relocating loader, I/O drivers, diagnostics, and a debug package are included.

Addressing may be accomplished in six modes, including direct, indexed, relative, and indirect. A large 512 word floating page makes programming fast and simple.

Proper attention has been given to the overall design of the I/O, including hardware design, instruction format, standard DMA, and single-word I/O functions, all to achieve maximum I/O flexibility and efficiency.

The basic Datamate 70 is housed in a cabinet 19" X 20" X 1 3/4" high, and may include the CPU, full power, and up to 1,024 words of ROM, 256 words of scratch-pad memory, plus space for I/O device controllers. For applications requiring extended memory, a 5 1/4" high package can house all of the above, plus 16K of core memory. An additional expansion unit allows use of the full 32K core capability.

1.1 General

The Datamate 70 is a general purpose, parallel 16-bit digital computer of advanced architecture, designed for on-line data acquisition, control and monitor functions, automatic test and instrumentation, communications data concentrators and educational applications. Extensive use of MSI devices and the latest memory technology allows computational power far surpassing its small size and low price.

The Datamate 70 has eleven powerful registers, four of which are 16-bit arithmetic accumulators, with two of those being available as index registers.

A wide range of optional memories may be chosen to tailor the DM-70 for specific use requirements. These include lithium core memories operating at 1.0 us full cycle time plus semiconductor memories of the read-only, and the read-write type, which operate at much higher rates.

Direct Memory Access is built-in as an integral machine function, providing 16-bit I/O transfer at one million words per second.

An efficient, user-oriented instruction set includes over 144 instructions in five classes, in a powerful micro-programmed format. Particular care has been given in the design of the instruction set to facilitate the writing of re-entrant code.

Register to Register 16-bit Add/Subtract time is 1.0 us.

Processor options include a hardware bootstrap loader implemented in the form of a semiconductor ROM, hardware multiply and divide and expanded program interrupts.

1.2 Software System

Flexible, expandable, modular software available on the DM-70 includes an Assembler, Loaders, I/O Drivers, a Debug Package, Symbolic Editor and Diagnostics.

1.21 Assembler

SASS, the DM-70 Symbolic Assembly System is a flexible assembly system designed to combine powerful assembly capability and I/O support with simplicity of use. SASS supports all standard peripherals and equipment configurations and includes the following standard features:

- Free format source statements
- Local Symbolic References
- Conditional Code Generation
- Symbolic addressing in all machine addressing modes
- Absolute, Relocatable or mixed object code
- Highly compact binary object tapes
- Extensive error checking and error documentation
- Powerful data generation capability
- Cross-reference listing of program symbols
- Two pass operation
- Minimum configuration for the operation of SASS is a Datamate 70 CPU with 4K memory and ASR 33 Teletype

1.22 Loaders

Initial loading of the DM-70 computer utilizes the standard bootstrap (MINI-LOAD) for the loading of absolute binary data. MINI-LOAD format provides two words of control data providing the beginning and end addresses of the program being loaded. A hardware semiconductor read-only memory (ROM) that contains a copy of MINI-LOAD is available as a standard option.

Loading of programs not requiring linkage to library routines and programmer defined external subroutines may be accomplished utilizing MIDI-LOAD. Relocation and checksum evaluation is provided by MIDI-LOAD.

MAXI-LOAD is the DM-70 full system loader providing for relocation and linkage of separately assembled programs. Additionally MAXI-LOAD features library search/load and the printing of a memory map indicating run-time core utilization. MAXI-LOAD communicates with any appropriate I/O devices.

1.23 I/O Drivers

I/O Drivers are available for all standard DM-70 peripherals. These drivers provide the programmer a means of easily performing required I/O operations.

1.24 Debug Package

The DM-70 on-line debug package is designed to provide virtually "hands-off" program debug facilities. Commands processed by the program include, examine and change register, examine and change memory, search memory, fill memory, list memory, dump memory in MINI-LOAD format, load MINI-LOAD format programs, set/clear breakpoint, and transfer control to a specified location.

1.25 Symbolic Editor

The DM-70 Symbolic Editor Program produces a new symbolic file from an old file in accordance with an update file. The update file, prepared either off- or on- line specifies the insertion, deletion, or replacement of records.

1.26 Instruction Diagnostics

The DM-70 Instruction Diagnostic Package, consists of modularly constructed routines providing for comprehensive testing of the DM-70 instruction set, memory and input/output devices. Readily identifying hardware malfunctions, these routines simplify and speed the job of maintenance personnel.

CHAPTER 2

SYSTEM ARCHITECTURE

DM-70 SYSTEM ARCHITECTURE

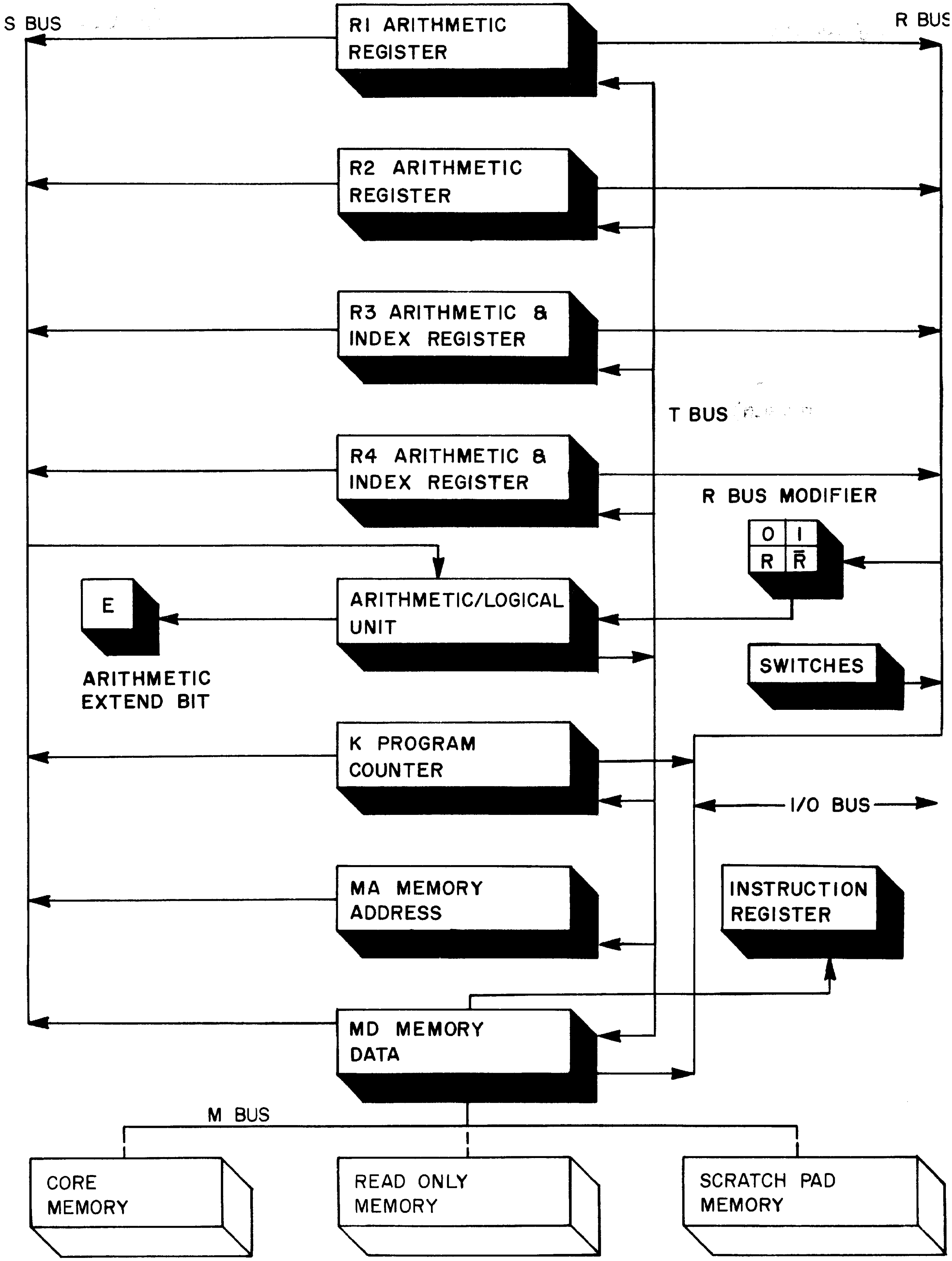


Fig. 2.1

2.1 Registers

Eleven registers are included ın the DM-70 system architecture which are described in the following sections.

2.11 Multi-Accumulator Registers

The DM-70 has four sixteen-bit general-purpose registers, Rl, R2, R3 and R4. All four can be used as accumulators in arithmetic and logical operations. Data may be transferred directly to and from memory using any of these four registers. All four registers have the capability of communicating with peripheral devices so that one register can be used for input/output data transfers without disturbing others currently being used for computations.

2.12 Index Registers

Two of the general purpose registers, R3 and R4, may be utilized as index registers for address arithmetic. Indexed addressing does not add any additional time in referencing memory. Register R3 may also be utilized for indexing input/output device addresses.

2.13 E Register

The E Register is a single bit extension register which serves as a link between the general-purpose registers for multiple precision arithmetic, or to indicate an arithmetic overflow on an add, subtract, increment or decrement instruction which references a register. The E register may be set, cleared or tested under program control. An arithmetic overflow occurs when the absolute value of the result is ≥32768. If there is no arithmetic overflow the E bit is not affected by the arithmetic operation.

2.14 I Register

The Instruction Register is a four-bit register which holds the current instruction being executed.

2.15 K Register

The Program Instruction Counter is a fifteen-bit register which holds the address of the next instruction to be fetched from memory. The K Register is normally automatically incremented by one after the execution of each instruction. The K Register will be augmented by the value of the variable length skip field plus one when a skip instruction is effected. A jump instruction will set the contents of the K Register to any memory address.

2.16 MA

The Memory Address Register is a fifteen-bit register which holds the address of the memory location being accessed.

2.17 MD

The Memory Data Register is a sixteen-bit register which holds the data transferred into or out of memory during the preceding memory cycle.

2.18 Switch Register

The console Switch register is a sixteen-bit register which may be transferred to the processor under manual control, and merged or transferred under program control

2.19 I/O Device Address Register

The I/O Device Address Register is a six bit register which holds the address of the I/O device being communicated with. Any of 62 external devices may be addressed.

2.2 Bus System

The bus system by which data is routed within the computer may be seen in Fig. 2.1. There are five major buses in the DM-70. Although the buses are represented by a single line in this figure, each bus is composed of 16 individual lines, one for each register bit. The DM-70 arithmetic/logical unit uses an "R-S-T" bus configuration, designating a three bus system which applies the two input buses, R and S, to the Arithmetic/Logical unit with output on the third or T bus. The use of two input buses permits arithmetic operations combining the contents of any two registers. The R bus is connected to the ALU through a 16-bit bus modifier which permits the data presented to the R bus to be forced to zero, one, or presented in either true or complement form. The I/O (Input/Output) bus is bi-directional 16-bit bus providing a means for data to be transferred in and out of the computer. The M (Memory Bus) provides ease of interfacing with various optional memories including ferrite core, and semiconductor scratchpad and read-only types.

2.3 Arithmetic/Logical Unit

The Arithmetic/Logical Unit can perform a number of functions as data is presented to it from the R and S buses. The basic arithmetic and logical operations such as addition, subtraction, comparison, logical instructions, register change, and a portion of the shift/rotate instructions are generated in this unit. The E register (2.13) is closely associated with the Arithmetic/Logical unit and may be altered by results generated within it.

2.4 Memory

The standard memory is a wide range, lithium core type consisting of 4,096 sixteen-bit words expandable in 4,096 word plug-in modules to 32,768 words, with a full cycle time of 1.0 us. Optional memories include smaller word capacity semiconductor read-write and read only memories.

2.5 Input/Output

The input/output (I/O) facilities of the Datamate 70 are organized for a direct-to-memory transfer of data. In addition,to facilitate the utilization of I/O devices which do not normally require block transfer of data (e.g., ASR-33 Teleprinter), programmed I/O (PIO) channels are provided. The I/O bus contains all the necessary signal lines for either PIO or DMA channel operation.

The Direct Memory Access (DMA) I/O channels are used for I/O devices which require high data transfer rate or which are inherently block transfer devices (e.g., magnetic tape and drum or disc). The DMA I/O bus is an integral part of the Datamate 70 basic configuration and no options are required to configure the DMA bus.

CHAPTER 3

INSTRUCTION REPERTOIRE

3.1 Memory Reference Instructions (MR Class)

Memory reference instructions are utilized to load and store the general purpose registers Rl through R4 and to modify the contents of memory locations. All memory reference instructions follow the format of Figure 3.1.

o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

OP	R	I	X	Displacement

Figure 3.1, Memory Reference Instructions

In all memory reference instructions, bits 0-8 specify a displacement address. The displacement address may be modified by the value of X (bits 9-10) or I (bit 11), or both, to form a fifteen bit effective address.

3.2 Effective Address Generation

The effective address is the fifteen-bit address that is the source or destination of a Memory Reference Instruction operand. Addressing, i.e., effective address generation can be accomplished in one of six modes: direct, indexed, relative (forward or backward), indirect, indexed-indirect and relative-indirect. If indexing is combined with indirection, the indexing occurs pre-indirection. Indexing requires no additional time. Indirect addressing may be multi-level with each level of indirection requiring an additional memory cycle.

3.21 Page Zero Addressing

If X is 00, the effective address E is simply that specified by the displacement address (bits 0-8) an address in the octal range of 00000 to 00777. This group of 512 locations is referred to as page zero.

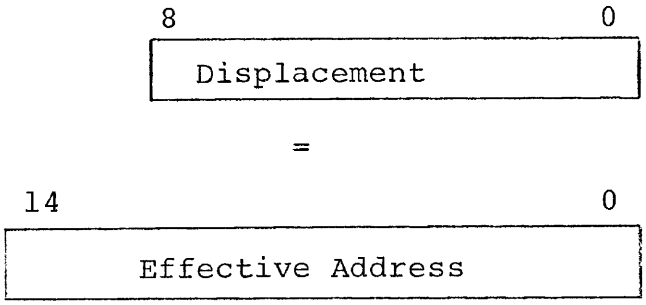


Figure 3.2 Page Zero Addressing

3.22 Indexed Addressing

Register R3 or R4 may be used as index registers. If X = 10, R3 is selected; if X = 11, R4 is selected. The effective address is formed by adding the contents of the selected register to the displacement address. (The displacement is interpreted as an unsigned nine bit number in the range $0 \leq d \leq 511$).

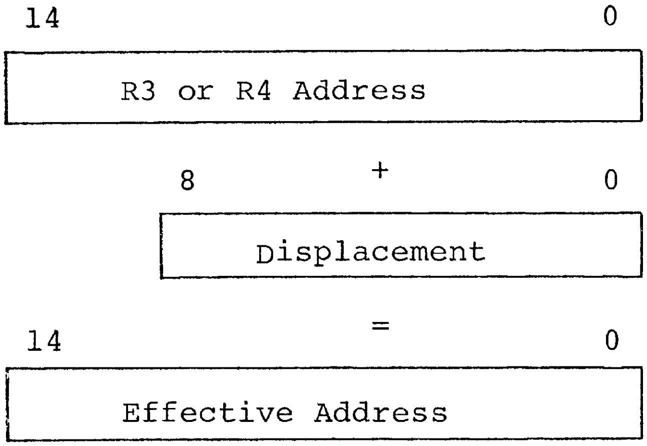


Figure 3.3, Indexed Addressing

3.23 Relative Addressing

If X = 01, the effective address is determined by adding to the address specified in the K register (instruction counter) the displacement specified in the instruction word. The displacement is interpreted as a twos complement binary integer in the range $-256 \leq d \leq 255$.

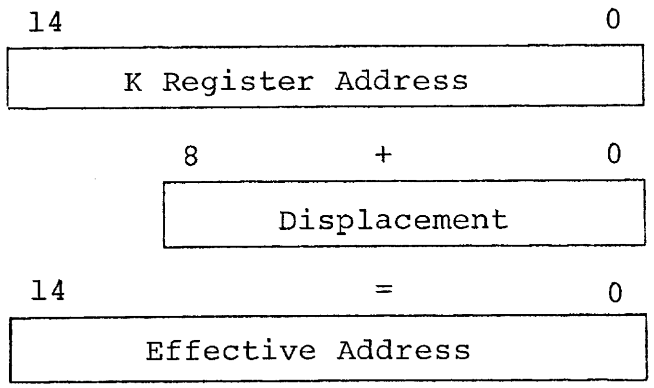


Figure 3.4, Relative Addressing

3.24 Indirect Addressing

If bit 11 is a 0, the addressing is direct and the effective address is found as in Sections 3.21 through 3.22. If bit 11 is a 1, addressing is indirect. Indirect addressing utilizes the effective address to access another word in memory which is taken as the new memory address for the same instruction. This new address word contains sixteen bits. The first fifteen bits specify the new address. If the leftmost bit (bit 15) is a one, indirect addressing occurs again and still another address is obtained. This multiple-step indirect addressing may be carried out to any number of levels.

3.3 Load and Store Instructions

o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

OP	R	I	X	Displacement

The R portion of the load or store instruction specifies the register:

00 = Rl

01 = R2

10 = R3

11 = R4

3.31 LDR R: OP = 01

Load the contents of the addressed location into Register R, replacing the previous contents of R. The contents of the memory cell are not altered.

Inst.	Octal Code
LDR Rl	04
LDR R2	05
LDR R3	06
LDR R4	07

3.32 STR R: OP = 11

Store the contents of Register R into the addressed location replacing the previous contents of the addressed location. The contents of Register R are not altered.

Inst.	Octal Code
STR R1	14
STR R2	15
STR R3	16
STR R4	17

3.4 Jump and Memory Modification Instructions

15 12	11	10 9	8 0
OP	I	X	Displacement

3.41 JMP Jump OP = 1000 Octal Code = 10

This instruction allows the programmer to alter the normal sequence of instructions by directing the computer to take its next instruction from the addressed location. The contents of K and MA is set according to the memory address portion of the instruction word.

3.42 JSB Jump to Subroutine OP = 1001 Octal Code = 11

This instruction stores the contents of the K register plus one in Register R4 and the next instruction to be executed will be that contained in the addressed location.

3.43 ISZ Increment and Skip if Zero OP = 1010 Octal Code = 12

Add one to the contents of the addressed memory location and place the result back in the location. If the result of the addition is zero, skip the next instruction. The extend register is not affected by the instruction.

3.44 DSZ Decrement and Skip if Zero OP = 1011 Octal Code = 13

Subtract one from the contents of the addressed memory location and place the result back in the location. If the result of the instruction is zero, skip the next instruction. The extend register is not affected by the instruction.

3.5 Register to Register Instructions (RR Class)

Register to Register instructions are defined by bits 14, 15 and 8 = 0, and an octal digit of 1 through 5 in the OP code field (bits 9-11) as in Fig. 3.41.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	RD		Op Code			0	RS		S			L		

Figure 3.51 Register to Register Instructions

3.51 Specifying Source and Destination Registers RS and RD

Bits 12 and 13 designate the destination register in all Register to Register (RR) instructions and bits 6 and 7 designate the source register. The following binary pattern defines the source or destination register:

Bits 12 - 13 or 6 - 7

00 = R1

01 = R2

10 = R3

11 = R4

3.52 ADD Add Octal Op Code 1

Add the contents of the source and destination registers and place the result in the destination register. The result may set the E bit to one (Sec. 2.13). Carry out may occur (Sec. 3.57, note).

$$RS + RD \rightarrow RD$$

3.53 SUB Subtract Octal Op Code 2

Subtract the contents of the destination register from the contents of the source register and place the result in the destination register. The result of the operation may set the E bit to one (Sec. 2.13). Carry out may occur (Sec. 3.57, note).

$$RS - RD \rightarrow RD$$

3.54 AND And Octal Op Code 3

Perform the logical And operation on the contents of the source and destination registers and place the result in the destination register.

$$RS \wedge RD \rightarrow RD$$

3.55 IOR Inclusive OR Octal Op Code 4

Perform the logical Inclusive Or operation on the contents of the source and destination registers and place the result in the destination register.

$$RS \vee RD \rightarrow RD$$

3.56 CPR Compare Octal Op Code 5

Compare the contents of the source and destination registers by subtracting the destination register from the source register. The contents of neither the source nor destination registers is altered, but the result of the comparison may be tested for an appropriate skip condition defined in Section 3.57. The E register is not affected. Carry out may occur as a result of the comparison. See the note in Section 3.57.

3.57 Variable Length Conditional Skip Micro Codes

The S & L Fields (bits 0-5 Fig. 3.5) define a variable length conditional skip micro code which may be combined with any of the Register to Register (RR) instructions described in this section or with any of the register change instructions (RC) or Shift Rotate instructions described in Sections 3.7 or 3.8 respectively. The S field defines one of eight possible skip conditions, and the L field defines a forward skip of L program steps where $7 \geq L \geq 0$, providing a skip of zero to seven program steps.

The S field is defined as follows:

Octal	Digit	(bits 3 - 5)
SK	0	Unconditional Skip
LT	1	Skip if $RD < 0$
GT	2	Skip if $RD > 0$
EQ	3	Skip if $RD = 0$
LE	4	Skip if $RD \leq 0$
GE	5	Skip if $RD \geq 0$
CS	6	Skip if carry
ES	7	Skip if E Set and Reset E

NOTE: Carry out of bit 15 may occur as the result of any instruction utilizing addition or subtraction. The carry out condition is not saved as is overflow, consequently if knowledge of a carry is required the CS test must be combined with the instruction in question.

3.6 Immediate Instructions (IM Class)

The Immediate Class of instructions contains all the instruction types found in the Register to Register (RR) class. With this type of instruction the contents of the right half of the instruction word (bits 0 - 7) is utilized as an eight bit unsigned second operand rather than the contents of the source register. The operation codes are represented by the same octal digits as for the RR class. The two classes are distinguished by a one in bit 8 for the immediate group.

15 14	13 12	11 10 9	8	7 0
0 0	RD	Op Code	1	M (Operand)

3.61 ADI Add Immediate Octal Op Code 1

Add the contents of operand field M to the contents of the destination register and place the result in the destination register. The result of the operation may set the E register (Sec. 2.13). Carry out may occur (Sec. 3.57, note).

$$RD + M \rightarrow RD$$

3.62 SBI Subtract Immediate Octal Op Code 2

Subtract the contents of the operand field M from the contents of the destination register. The result of the operation may set the E register (Sec. 2.13). Carry out may occur (Sec. 3.57, note).

$$RD - M \rightarrow RD$$

3.63 ANI And Immediate Octal Op Code 3

Perform the logical And operation on the contents of the operand field M and the right 8 bits of the destination register and place the result in the destination register. The left 8 bits of the destination register are set to zero.

$$RD \wedge M \rightarrow RD$$

3.64 ORI Or Immediate Octal Op Code 4

Perform the logical Inclusive Or operation on the contents of the M field and the right 8 bits of the destination register and place the result in the destination register. The contents of the left 8 bits of the destination register are unchanged.

$$RD \vee M \rightarrow RD$$

3.65 CPI Compare Immediate Octal Op Code 5

Compare the contents of the M field with the contents of the 16 bit destination register. The contents of neither is altered. If the result of the comparison is not equal to zero, the next instruction is skipped. Carry out may occur (Sec. 3.57, note.)

3.7 Register Change Instructions (RC Class)

Register Change Instructions are defined by a zero in bits 14 and 15 and an operation code of 6 in bits 9-11. The nature of the register change is defined by the C field, bits 6-8. The variable length skip field, bits 0-5, are described in Sec. 3.57. The skip is associated with the destination register RD. The test for a specified skip condition is made after execution of the operation specified in bits 6-8.

15 14		11 9	8 6	5 3	2 0
0 0	R D	1 1 0	C	S	L

Fig. 3.71 Register Change Instructions

3.71 ICR Increment Register C Field = Octal Code 0

Add one to the contents of the destination register and place the result in the destination register. The E register may be set as a result of this instruction. Carry out may occur (Sec. 3.57, note).

$$RD + 1 \rightarrow RD$$

3.72 DCR Decrement Register C Field = Octal Code 1

Subtract one from the contents of the destination register and place the result in the destination register. The E bit may be set as a result of this instruction. Carry out may occur (Sec. 3.57, note).

$$RD - 1 \rightarrow RD$$

3.73 CML Complement Register C Field = Octal Code 2

Form the ones complement of the contents of the destination register and place the result in the destination register.

$$\overline{RD} \rightarrow RD$$

3.74 NEG Negate Register C Field = Octal Code 3

Form the twos complement of the destination register and place the result in the destination register. Carry out may occur (Sec. 3.57, note).

3.75 STE Set E C Field = Octal Code 4

The E Register is set to 1

E = 1

3.76 CLR Clear R C Field = Octal Code 5

The Destination Register is set to 0

RD = 0

3.77 EXB Exchange Bytes C Field = Octal Code 6

The left and right hand bytes of the selected destination register RD are exchanged

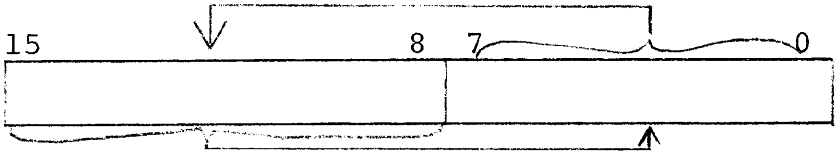


Fig. 3.72 Exchange Bytes

3.78 Multiply/Divide C Field = Octal Code 7 (Processor Option)

3.8 Shift/Rotate Instructions (SR Class)

Shift/Rotate Instructions are defined by a zero in bits 14 and 15 and an octal operation code of 7 in bits 9-11. The result of a Shift/Rotate instruction may be tested for any of the conditional skip instructions described in Section 3.57.

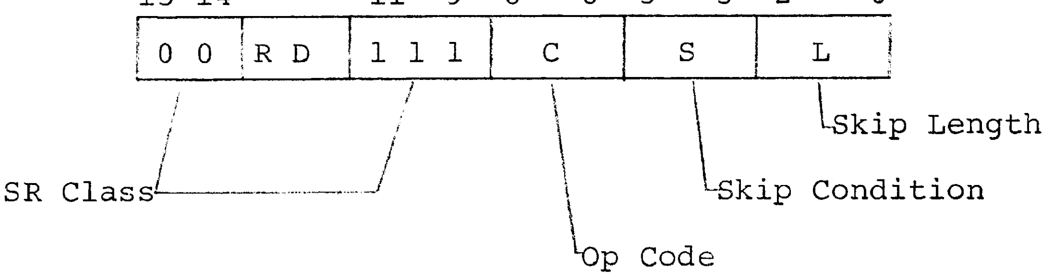


Fig. 3.81 Shift Rotate Instructions

3.81 ASR Arithmetic Shift Right Octal Op Code = 0

The contents of the destination register RD are shifted one place to the right. The bit shifted out of the low order position of RD is lost. Bit 15 is unchanged and is copied one place to the right.

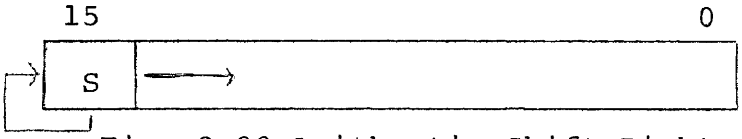


Fig. 3.82 Arithmetic Shift Right

3.82 ASL Arithmetic Shift Left Octal Op Code = 1

The contents of the destination register RD are shifted one place to the left. Bit 15 is unchanged and zero is shifted into the low order position of RD. The bit shifted out of position 14 is lost. The E bit is set if as a result of the shift, bit 15 differs from bit 14.

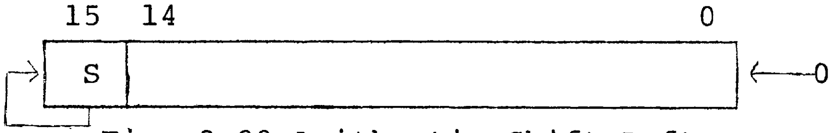


Fig. 3.83 Arithmetic Shift Left

3.83 LSR Logical Shift Right Octal Op Code = 2

The contents of the destination register RD are shifted one place to the right. Zero is shifted into the high order position of RD. The E register retains the bit shifted out of bit position 0 of RD.

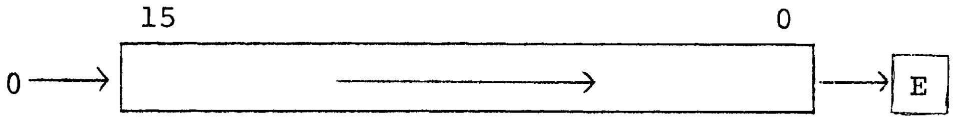


Fig. 3.84 Logical Shift Right

3.84 LSL Logical Shift Left Octal Op Code = 3

The contents of the destination register RD are shifted one place to the left. Zero is shifted into the low order positions of RD. The E register retains the bit shifted out of bit position 15 of RD.

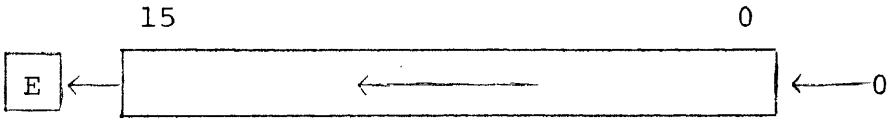


Fig. 3.85 Logical Shift Left

3.85 LRR Logical Rotate Right Octal Op Code = 4

The contents of destination register RD are rotated one place to the right. Bit position 0 is rotated into position 15. The E register is not affected.

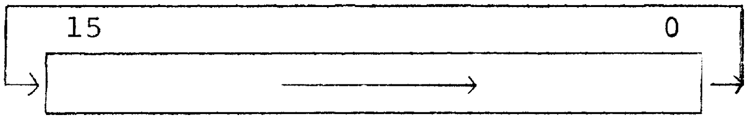


Fig. 3.86 Logical Rotate Right

3.86 LRL Logical Rotate Left Octal Op Code = 5

The contents of the destination register RD are rotated one position to the left. Bit position 15 is rotated into position 0. The E Register is not affected.

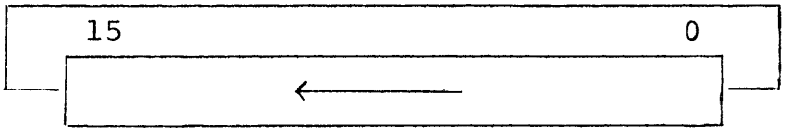
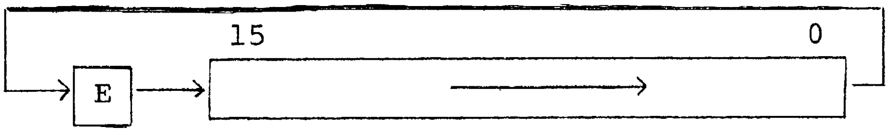


Fig. 3.87 Logical Rotate Left

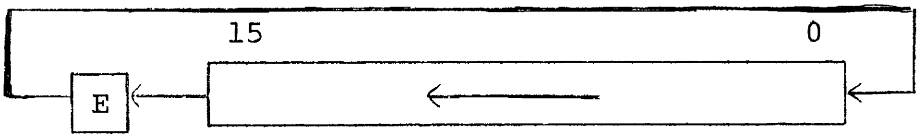
3.87 ERR Extended Rotate Right Octal Op Code = 6



The contents of the destination register are rotated right one place with the E register.

Fig. 3.88

3.88 ERL Extended Rotate Left Octal Op Code = 7



The contents of the destination register are rotated left one place with the E register.

Fig. 3.89

3.9 Input/Output and Interrupt Instructions (I/O Class)

The instructions in this class reference the I/O and interrupt systems. Several processor control instructions are also included in this class. They are divided by function into four groups: I/O Transfer Instructions (3.92) I/O Control Instructions (3.97) Interrupt Processing Instructions (3.98) and Processor Control Instructions (3.99). Bits 14 and 15 and octal op codes bits 9 - 11 = 0 define the I/O class of instructions.

3.91 I/O Device Addressing

I/O Device addresses are specified as follows: The D field, bits 0-4 of the instruction word, Fig. 3.91, specifies a displacement device address in the range $0 \leq D \leq 31$. If the Index bit 5 is zero this represents the actual device address. This address is placed in the device address register and is retained for subsequent transfer or control instructions. If the index bit is one the effective device address is formed by adding the contents of Register R3 to the displacement address and the result is placed in the device address register. The effective address A must be in the range $1 \leq A \leq 63$ in the standard DM-70 configuration but this range may be expanded to meet special I/O requirements. Device address one is reserved for the console switch register. If a device address of zero is issued the current address contained in the device address register remains unchanged.

3.92 I/O Transfer Instructions

Instructions in this group effect a transfer of data between any of the four general purpose registers R1, R2, R3, or R4 and any of the 64 I/O devices or device controllers designated by the effective device address. The console switch register is assigned the device address one.

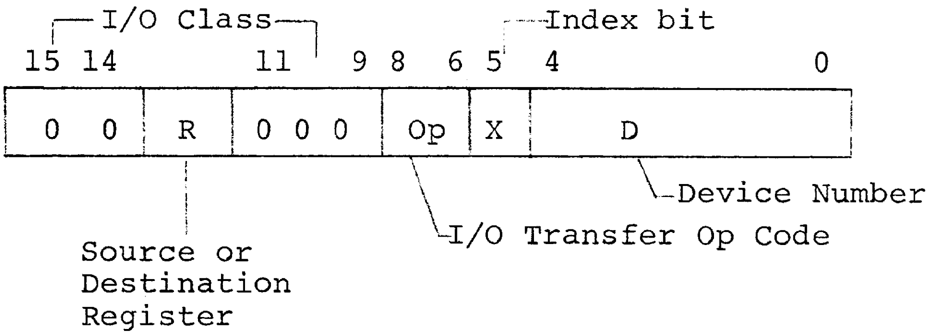


Fig. 3.91 I/O Transfer Instructions

3.93 Merge Device to Register MDR Octal Op Code = 02

If the I/O device is ready, the contents of the device buffer is merged (logical Inclusive Or Operation) with the contents of the specified destination register RD, and the next instruction is skipped. If the device is busy no merging of data takes place and the next instruction is executed. If the device buffer is less than 16 bits, the unused bits assume the default condition 0.

3.94 Transfer Device to Register TDR Octal Op Code = 03

If the device is ready, the contents of the specified I/O device buffer is transferred to the selected R register and the next instruction is skipped. If the device is busy, no transfer takes place and the next instruction is executed. Unused bits are treated as in Section 3.92.

3.95 Transfer Register to Device TRD Octal Op Code = 04

If the device is ready, the contents of the register specified by the R field is transferred to the device buffer specified by the device address and the next instruction is skipped. If the device is busy, no transfer takes place and the next instruction is executed. The contents of the specified register are not altered.

3.96 Transfer Status to Register TSR Octal Op Code = 05

The contents of the status register of the specified I/O device are transferred to the specified R register.

3.97 I/O Control Instructions Octal Op Codes 6 and 7

These control instructions transmit a control code to the specified I/O device for interpretation by the device controller. The instruction following a device control instruction is normally skipped if the device control instruction is accepted. The stop control instruction is always accepted by the device controller and does not cause the next instruction to be skipped. An octal code of 6 or 7 in bits 6 - 8 together with bits 12 and 13 (C field of Figure 3.92) provide for the transmission of eight control codes to the device controller.

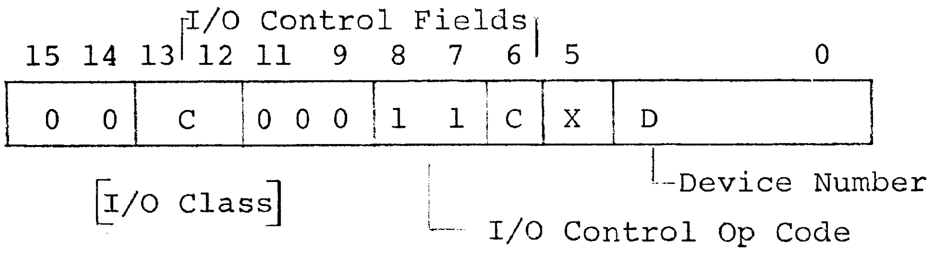


Fig. 3.92 I/O Control Instructions

3.98 Interrupt Processing Instructions

Interrupt processing instructions are used to arm, disarm, enable, or disable the interrupts or return from an interrupt servicing program.

Each interrupt may be ARMED or DISARMED individually. If the interrupt is ARMED, a device can cause the interrupt to advance to a WAITING state. The interrupts may be ENABLED or DISABLED in groups of eight or sixteen with a single instruction capability of enabling or disabling the entire interrupt system. If an interrupt is ARMED and ENABLED, it may pass from the WAITING state to the ACTIVE state. If the interrupt is ARMED and DISABLED, it may pass to the WAITING state, but will not go to the ACTIVE state until it is enabled. The interrupt processing instruction format is shown in Figure 3.93.

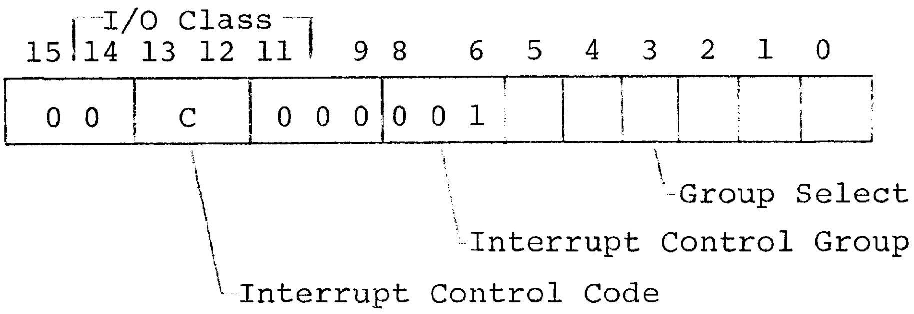


Fig. 3.93 Interrupt Enable and Disable

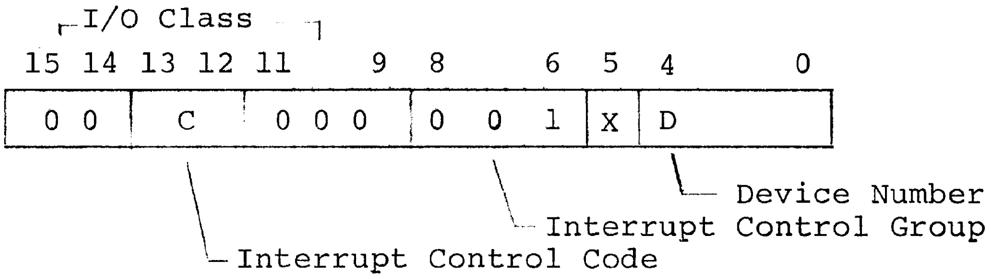


Fig. 3.94 Interrupt Arm and Disarm

ARM Arm Interrupt C = 00 Arm the specified interrupt

DSA Disarm Interrupt C = 01 Disarm the specified interrupt

ENI Enable Interrupt C = 10 Enable the groups of interrupts specified by bits 0 - 5. Bits 0 - 3 reference groups of eight interrupts and bits 4 - 5 reference group of sixteen interrupts.

DSI Disable Interrupt C = 11 Disable the groups of interrupt, specified by bits 0 - 5. Group references are the same as for the enable interrupts.

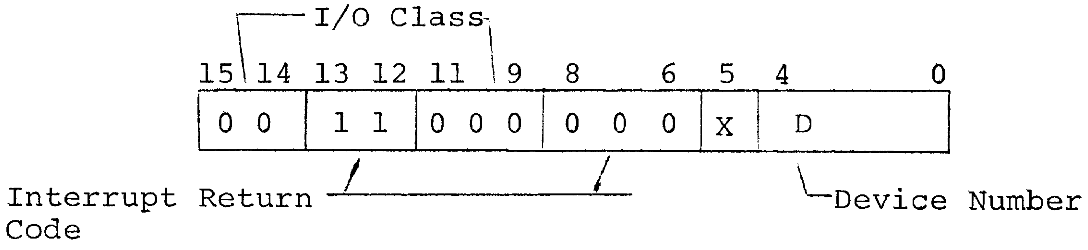


Fig. 3.95 Interrupt Return

RTJ Interrupt Return Restore the contents of the K Register and E bit from the first location of the pair of dedicated memory locations assigned to that interrupt and reset the interrupt.

15	0	
E	K	L
JUMP ADDRESS		L + 1

$$L = 2M + 0010_8$$

Fig. 3.96 Interrupt Locations for Device "M"

Interrupt locations are situated on page zero. (Sec. 3.21) The pair of memory locations L and L + 1 associated with device interrupt "M" are shown in Figure 3.96. When the interrupt for device "M" advances to the active state, processing is interrupted and the K register (program counter) and extend bit are stored in the first location of the pair of locations associated with that interrupt. The address in the next location is then accessed and used as a direct jump to the required program. The first instruction of the interrupt response program is then accessed and processing proceeds in a normal fashion. The program may be interrupted by a higher priority interrupt at any time after the first instruction is executed. At the end of interrupt processing subroutine when it is desired to return to the program which was running at the time the interrupt occurred, an interrupt return instruction is issued (See Fig. 3.95). This instruction accomplishes an indirect jump through the first location of the interrupt location pair and restores the K register and extend bit.

3.99 Processor Control Instructions

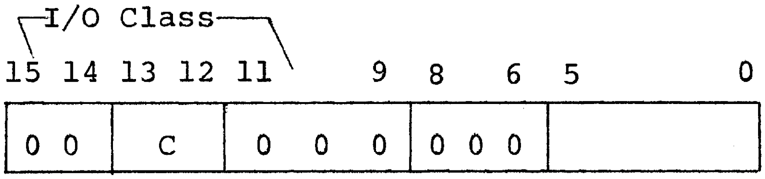


Fig. 3.97 Processor Control Instructions

HLT	HALT	C = 00	Instruction Processing is halted. The processor is not interruptable.
WAT	WAIT	C = 01	The computer enters a quiescent state and may be interrupted.
RST	RESET	C = 10	All I/O devices and interrupts are reset.

CHAPTER 4

CONSOLE OPERATION AND DISPLAY

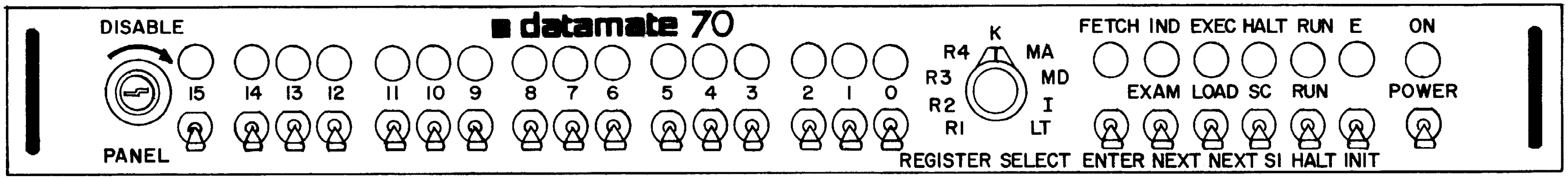


Fig. 4.1 Datamate 70 Console

4.1 Introduction

The Datamate 70 Console (Fig. 4.1) provides for program test and maintenance operations. Processor registers can be selectively displayed and loaded. Memory data may be examined or loaded. Single Instruction and Single Cycle operation is provided. The panel controls may be disabled by means of a key lock switch for critical applications to prevent accidental alteration of the operation of the program. A lamp test is provided. Each of the indicators and controls appearing on the front panel of the DM-70 is described below.

4.11 Console Displays

A sixteen bit lighted display provides for selective display under control of the register select switch of the four sixteen bit general purpose registers Rl, R2, R3, and R4, the K, MA, MD register and the four bit instruction register. Single lamps display the state of the E register, the next machine cycle (FETCH, INDIRECT, or EXECUTE) to be entered, the RUN or HALT state of the processor, and power.

4.12 Console Controls

REGISTER SELECT

This nine position switch selects which of the eight registers Rl, R2, R3, R4, K, MA, MD or I are displayed on the sixteen bit lighted display. The position of the Register Select Switch may be changed while the program is running. The ninth position (LT) causes all indicators on the control panel to be lighted for test purposes.

ENTER

Actuating the momentary ENTER switch enters the contents of the sixteen bit switch register into the register selected by the REGISTER SELECT switch. Exceptions are MD and the I registers which cannot be loaded from the SWITCH REGISTER. The switch is inactive in the RUN mode.

EXAM/NEXT

Raising the EXAM/NEXT Switch to the momentary EXAM position causes the contents of the memory location specified in the K Register to be displayed as MEMORY DATA for examination purposes. Depressing the switch to the momentary NEXT position provides the EXAM function and in addition causes the K Register to be incremented by one, thus providing for rapid examination of the contents of consecutive memory locations. The switch is inactive in the RUN mode.

LOAD/NEXT

Raising the LOAD Switch to the momentary LOAD position transfers Switch Register Data to the memory location specified by the K Register. Upon completion of the load, the data is displayed as MEMORY DATA. Depressing the switch to the momentary NEXT position provides the LOAD function and in addition causes the K Register to be incremented by one, thus providing for storage of data in consecutive memory locations. The switch is inactive in the RUN mode.

SI/SC (Single Instruction - Single Cycle)

Downward actuation (Single Instruction) of the momentary SI/SC Switch causes execution of the instruction located in the memory location specified by the K register. Upon completion of the instruction, the K register will be incremented by one and the processor will halt. The SI position is normally used while debugging a program. Upward actuation (Single Cycle) of the momentary switch causes execution of one and only one cycle (FETCH, INDIRECT, or EXECUTE) relative to execution of an instruction. The instruction being executed on a cycle-to-cycle basis is located in the memory location specified by the K register. Upon completion of the FETCH cycle, the K register is incremented by one. This switch is normally used as a maintenance aid, but can also be useful as a program debugging aid. The switch is inactive in the RUN mode.

RUN/HALT

Upward actuation of the momentary RUN/HALT switch places the processor in the RUN mode. Downward actuation of the switch places the processor in the HALT mode upon completion of the instruction currently being executed.

INIT

Actuating the momentary INIT (Initialize) Switch resets all I/O and interrupts, the E register and sets the mode to FETCH. INIT is inactive when the processor is in the RUN mode.

POWER

The power switch applies or removes power from the computer.

PANEL DISABLE

The key lock switch disables ENTER, EXAM/NEXT, LOAD/NEXT, SC/SI, RUN/HALT and INIT switches.

CHAPTER 5

APPENDICES

APPENDIX A

DM-70 INSTRUCTION REPERTOIRE

CLASS	MENMONIC	TIME (usec)	DESCRIPTION
Memory Reference	LDR	2.0	Load Register from Memory
	STR	2.0	Store Register in Memory
	JMP	1.0	Unconditional Jump
	JSB	3.0	Jump to Subroutine
	ISZ	3.0	Increment Memory,Skip if Zero
	DSZ	3.0	Increment Memory,Skip if Zero
Register-to Register	ADD	1.0	Add Source Reg.to Dest.Reg.
	SUB	1.0	Subtract Dest.Reg.from Source Reg.
	AND	1.0	'AND' Source Reg.to Dest.Reg.
	IOR	1.0	'IOR' Source Reg.to Dest.Reg.
	CPR	1.0	Compare Source Reg.to Dest.Reg.
	TST	1.0	Test Reg. according to Skip Micro
	TSE	1.0	Test the E Bit, and Clear
	NOP	1.0	No Operation
Immediates	ADI	1.0	Add Immediate
	SBI	1.0	Subtract Immediate
	ANI	1.0	'AND' Immediate
	ORI	1.0	'IOR' Immediate
	CPI	1.0	Compare Immediate
Register Change	ICR	1.0	Increment Register
	DCR	1.0	Decrement Register
	CML	1.0	Ones Complement Register
	NEG	1.0	Negate Register
	STE	1.0	Set E Bit
	CLR	1.0	Clear Register
	EXB	1.0	Exchange Register Bytes
	MPY	-	(Processor Option)
	DIV	-	(Processor Option)

DM-70 INSTRUCTION REPERTOIRE (CONTINUED)

CLASS	MNEMONIC	TIME (usec)	DESCRIPTION
Shift/Rotate	ASR	1.0	Arithmetic Shift Right Register
	ASL	1.0	Arithmetic Shift Left Register
	LSR	1.0	Logical Shift Right Register
	LSL	1.0	Logical Shift Left Register
	LRR	1.0	Logical Rotate Right Register
	LRL	1.0	Logical Rotate Left Register
	ERR	1.0	Extended Rotate Right Register
	ERL	1.0	Extended Rotate Left Register
Skip Micros	SK	*	Unconditional Skip
	LT	*	Skip if Dest. Reg. < 0
	GT	*	Skip if Dest. Reg > 0
	EQ	*	Skip of Dest. Reg. =0
	LE	*	Skip if Dest. Reg. ≤ 0
	GE	*	Skip if Dest. Reg. ≥ 0
	CS	*	Skip if Carry Set
	ES	*	Skip if E Set and Reset
I/O	MDR	2 .0	Merge Device with Register
	TDR	2.0	Transfer Device to Register
	TRD	2.0	Transfer Register to Device
	TSR	2.0	Transfer Device Status to Reg.
	DCO	2.0	Device Control
I/O Interrupt	ARM	1.0	Arm Interrupt(s)
	DSA	1.0	Disarm Interrupt(s)
	ENI	1.0	Enable Interrupt group(s)
	DSI	1.0	Disable Interrupt group(s)
	RTJ	2.0	Interrupt Return Jump
Processor Control	HLT	1.0	Halt (not interruptable)
	WAT	1.0	Wait (may be interrupted)
	RST	1.0	System Reset

* No additional execution time is required when combined with Register to Register, Register Change or Shift/Rotate Class instructions.

APPENDIX B

DM-70 INSTRUCTION REPERTOIRE
Binary and Octal Codes

MEMORY REFERENCE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LDR	0	1	R		I	X		Displacement								
STR	1	1														

OCTAL	
0 – – D D D	LDR
0 – – D D D	STR

JUMP/MEMORY MODIFICATION

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JMP	1	0	0	0	I	X		Displacement								
JSB	1	0	0	1												
ISZ	1	0	1	0												
DSZ	1	0	1	1												

OCTAL	
1 0– D D D	JMP
1 1– D D D	JSB
1 2– D D D	ISZ
1 3– D D D	DSZ

REGISTER-TO-REGISTER

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD	0	0	R	D	0	0	1	0	R	S		S			L	
SUB					0	1	0									
AND					0	1	1									
IOR					1	0	0									
CPR					1	0	1									
TST	0	0	R		1	0	0	0	R			S			L	
TSE	0	0	0	0	1	0	0	0	0	0	1	1	1		L	
NOP	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

OCTAL	
0 R 1 R S L	ADD
0 R 2 R S L	SUB
0 R 3 R S L	AND
0 R 4 R S L	IOR
0 R 5 R S L	CPR
0 R 4 R S L	TST
0 0 4 0 7 L	TSE
0 0 4 0 0 0	NOP

IMMEDIATE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADI	0	0	R	D	0	0	1	1	Operand							
SBI					0	1	0									
ANI					0	1	1									
ORI					1	0	0									
CPI					1	0	1									

OCTAL	
0 R 1 4 X X	ADI
0 R 2 4 X X	SBI
0 R 3 4 X X	ANI
0 R 4 4 X X	ORI
0 R 5 4 X X	CPI

DM-70 INSTRUCTION REPERTOIRE
Binary and Octal Codes (Continued)

REGISTER CHANGE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICR	0	0	R	D	1	1	0	0	0	0		S			L	
DCR								0	0	1						
CML								0	1	0						
NEG								0	1	1						
STE								1	0	0						
CLR								1	0	1						
EXB								1	1	0						
MPY	Processor Option							1	1	1			-			
DIV	Processor Option							1	1	1			-			

OCTAL						
0	R	6	0	S	L	ICR
0	R	6	1	S	L	DCR
0	R	6	2	S	L	CML
0	R	6	3	S	L	NEG
0	R	6	4	S	L	STE
0	R	6	5	S	L	CLR
0	R	6	6	S	L	EXB

SHIFT/ROTATE

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ASR	0	0	R	D	1	1	1	0	0	0	S				L	
ASL								0	0	1						
LSR								0	1	0						
LSL								0	1	1						
LRR								1	0	0						
LRL								1	0	1						
ERR								1	1	0						
ERL								1	1	1						

OCTAL						
0	R	7	0	S	L	ASR
0	R	7	1	S	L	ASL
0	R	7	2	S	L	LSR
0	R	7	3	S	L	LSL
0	R	7	4	S	L	LRR
0	R	7	5	S	L	LRL
0	R	7	6	S	L	ERR
0	R	7	7	S	L	ERL

SKIP FIELD

	5	4	3	OCTAL
SK	0	0	0	0
LT	0	0	1	1
GT	0	1	0	2
EQ	0	1	1	3
LE	1	0	0	4
GE	1	0	1	5
CS	1	1	0	6
ES	1	1	1	7

DM-70 INSTRUCTION REPERTOIRE
Binary and Octal Codes (Continued)

INPUT/OUTPUT

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MDR	0	0	R		0	0	0	0	1	0	X	Device				
TDR								0	1	1						
TRD								1	0	0						
TSR								1	0	1						
DCO			C					1	1	C	X	Device				

OCTAL						
0	R	0	2	D	D	MDR
0	R	0	3	D	D	TDR
0	R	0	4	D	D	TRD
0	R	0	5	D	D	TSR
0	C	0	C	D	D	DCO

I/O INTERRUPT

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARM	0	0	0	0	0	0	0	0	0	1	X	Device				
DSA			0	1												
ENI			1	0							G	G	G	G	G	G
DSI			1	1												
RTJ			1	1				0	0	0	X	Device				

OCTAL						
0	0	0	1	D	D	ARM
0	1	0	1	D	D	DSA
0	2	0	1	G	G	ENI
0	3	0	1	G	G	DSI
0	3	0	0	D	D	RTJ

PROCESSOR CONTROL

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HLT	0	0	0	0	0	0	0	0	0	0	Ignored					
WAT			0	1												
RST			1	0												

OCTAL						
0	0	0	0	-	-	HLT
0	1	0	0	-	-	WAT
0	2	0	0	-	-	RST

APPENDIX C

ASCII TELETYPE CODES

Teletype Character	Octal Code
SPECIAL CHARACTERS	
space or blank	240
!	241
"	242
#	243
$	244
%	245
&	246
'	247
(	250
)	251
*	252
+	253
,	254
-	255
.	256
/	257
NUMERIC CHARACTERS	
0	260
1	261
2	262
3	263
4	264
5	265
6	266
7	267
8	270
9	271
SPECIAL CHARACTERS	
:	272
;	273
<	274
=	275
>	276
?	277
@	300

Teletype Character	Octal Code
ALPHABETIC CHARACTERS	
A	301
B	302
C	303
D	304
E	305
F	306
G	307
H	310
I	311
J	312
K	313
L	314
M	315
N	316
O	317
P	320
Q	321
R	322
S	323
T	324
U	325
V	326
W	327
X	330
Y	331
Z	332
SPECIAL CHARACTERS	
[	333
\	334
]	335
↑	336
←	337
Rubout	377

ASCII TELETYPE CODES (Continued)

Teletype Character	Octal Code	Teletype Character	Octal Code
SPECIAL CHARACTERS		SPECIAL CHARACTERS	
NUL	200	X-ON	221
SOM	201	TAPE AUX ON	222
EOA	202		
EOM	203	X-OFF	223
EOT	204	TAPE AUX OFF	224
WRU	205		
RU	206	ERROR	225
BEL	207	SYNC	226
FE	210	LEM	227
H TAB	211	S0	230
LINE FEED	212	S1	231
V TAB	213	S2	232
FORM	214	S3	233
RETURN	215	S4	234
S0	216	S5	235
SI	217	S6	236
DCO	220	S7	237

APPENDIX D

OCTAL-DECIMAL INTEGER CONVERSION TABLE

0000 to 0777 (Octal)	0000 to 0511 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
0000	0000	0001	0002	0003	0004	0005	0006	0007
0010	0008	0009	0010	0011	0012	0013	0014	0015
0020	0016	0017	0018	0019	0020	0021	0022	0023
0030	0024	0025	0026	0027	0028	0029	0030	0031
0040	0032	0033	0034	0035	0036	0037	0038	0039
0050	0040	0041	0042	0043	0044	0045	0046	0047
0060	0048	0049	0050	0051	0052	0053	0054	0055
0070	0056	0057	0058	0059	0060	0061	0062	0063
0100	0064	0065	0066	0067	0068	0069	0070	0071
0110	0072	0073	0074	0075	0076	0077	0078	0079
0120	0080	0081	0082	0083	0084	0085	0086	0087
0130	0088	0089	0090	0091	0092	0093	0094	0095
0140	0096	0097	0098	0099	0100	0101	0102	0103
0150	0104	0105	0106	0107	0108	0109	0110	0111
0160	0112	0113	0114	0115	0116	0117	0118	0119
0170	0120	0121	0122	0123	0124	0125	0126	0127
0200	0128	0129	0130	0131	0132	0133	0134	0135
0210	0136	0137	0138	0139	0140	0141	0142	0143
0220	0144	0145	0146	0147	0148	0149	0150	0151
0230	0152	0153	0154	0155	0156	0157	0158	0159
0240	0160	0161	0162	0163	0164	0165	0166	0167
0250	0168	0169	0170	0171	0172	0173	0174	0175
0260	0176	0177	0178	0179	0180	0181	0182	0183
0270	0184	0185	0186	0187	0188	0189	0190	0191
0300	0192	0193	0194	0195	0196	0197	0198	0199
0310	0200	0201	0202	0203	0204	0205	0206	0207
0320	0208	0209	0210	0211	0212	0213	0214	0215
0330	0216	0217	0218	0219	0220	0221	0222	0223
0340	0224	0225	0226	0227	0228	0229	0230	0231
0350	0232	0233	0234	0235	0236	0237	0238	0239
0360	0240	0241	0242	0243	0244	0245	0246	0247
0370	0248	0249	0250	0251	0252	0253	0254	0255

	0	1	2	3	4	5	6	7
0400	0256	0257	0258	0259	0260	0261	0262	0263
0410	0264	0265	0266	0267	0268	0269	0270	0271
0420	0272	0273	0274	0275	0276	0277	0278	0279
0430	0280	0281	0282	0283	0284	0285	0286	0287
0440	0288	0289	0290	0291	0292	0293	0294	0295
0450	0296	0297	0298	0299	0300	0301	0302	0303
0460	0304	0305	0306	0307	0308	0309	0310	0311
0470	0312	0313	0314	0315	0316	0317	0318	0319
0500	0320	0321	0322	0323	0324	0325	0326	0327
0510	0328	0329	0330	0331	0332	0333	0334	0335
0520	0336	0337	0338	0339	0340	0341	0342	0343
0530	0344	0345	0346	0347	0348	0349	0350	0351
0540	0352	0353	0354	0355	0356	0357	0358	0359
0550	0360	0361	0362	0363	0364	0365	0366	0367
0560	0368	0369	0370	0371	0372	0373	0374	0375
0570	0376	0377	0378	0379	0380	0381	0382	0383
0600	0384	0385	0386	0387	0388	0389	0390	0391
0610	0392	0393	0394	0395	0396	0397	0398	0399
0620	0400	0401	0402	0403	0404	0405	0406	0407
0630	0408	0409	0410	0411	0412	0413	0414	0415
0640	0416	0417	0418	0419	0420	0421	0422	0423
0650	0424	0425	0426	0427	0428	0429	0430	0431
0660	0432	0433	0434	0435	0436	0437	0438	0439
0670	0440	0441	0442	0443	0444	0445	0446	0447
0700	0448	0449	0450	0451	0452	0453	0454	0455
0710	0456	0457	0458	0459	0460	0461	0462	0463
0720	0464	0465	0466	0467	0468	0469	0470	0471
0730	0472	0473	0474	0475	0476	0477	0478	0479
0740	0480	0481	0482	0483	0484	0485	0486	0487
0750	0488	0489	0490	0491	0492	0493	0494	0495
0760	0496	0497	0498	0499	0500	0501	0502	0503
0770	0504	0505	0506	0507	0508	0509	0510	0511

1000 to 1777 (Octal)	0512 to 1023 (Decimal)

	0	1	2	3	4	5	6	7
1000	0512	0513	0514	0515	0516	0517	0518	0519
1010	0520	0521	0522	0523	0524	0525	0526	0527
1020	0528	0529	0530	0531	0532	0533	0534	0535
1030	0536	0537	0538	0539	0540	0541	0542	0543
1040	0544	0545	0546	0547	0548	0549	0550	0551
1050	0552	0553	0554	0555	0556	0557	0558	0559
1060	0560	0561	0562	0563	0564	0565	0566	0567
1070	0568	0569	0570	0571	0572	0573	0574	0575
1100	0576	0577	0578	0579	0580	0581	0582	0583
1110	0584	0585	0586	0587	0588	0589	0590	0591
1120	0592	0593	0594	0595	0596	0597	0598	0599
1130	0600	0601	0602	0603	0604	0605	0606	0607
1140	0608	0609	0610	0611	0612	0613	0614	0615
1150	0616	0617	0618	0619	0620	0621	0622	0623
1160	0624	0625	0626	0627	0628	0629	0630	0631
1170	0632	0633	0634	0635	0636	0637	0638	0639
1200	0640	0641	0642	0643	0644	0645	0646	0647
1210	0648	0649	0650	0651	0652	0653	0654	0655
1220	0656	0657	0658	0659	0660	0661	0662	0663
1230	0664	0665	0666	0667	0668	0669	0670	0671
1240	0672	0673	0674	0675	0676	0677	0678	0679
1250	0680	0681	0682	0683	0684	0685	0686	0687
1260	0688	0689	0690	0691	0692	0693	0694	0695
1270	0696	0697	0698	0699	0700	0701	0702	0703
1300	0704	0705	0706	0707	0708	0709	0710	0711
1310	0712	0713	0714	0715	0716	0717	0718	0719
1320	0720	0721	0722	0723	0724	0725	0726	0727
1330	0728	0729	0730	0731	0732	0733	0734	0735
1340	0736	0737	0738	0739	0740	0741	0742	0743
1350	0744	0745	0746	0747	0748	0749	0750	0751
1360	0752	0753	0754	0755	0756	0757	0758	0759
1370	0760	0761	0762	0763	0764	0765	0766	0767

	0	1	2	3	4	5	6	7
1400	0768	0769	0770	0771	0772	0773	0774	0775
1410	0776	0777	0778	0779	0780	0781	0782	0783
1420	0784	0785	0786	0787	0788	0789	0790	0791
1430	0792	0793	0794	0795	0796	0797	0798	0799
1440	0800	0801	0802	0803	0804	0805	0806	0807
1450	0808	0809	0810	0811	0812	0813	0814	0815
1460	0816	0817	0818	0819	0820	0821	0822	0823
1470	0824	0825	0826	0827	0828	0829	0830	0831
1500	0832	0833	0834	0835	0836	0837	0838	0839
1510	0840	0841	0842	0843	0844	0845	0846	0847
1520	0848	0849	0850	0851	0852	0853	0854	0855
1530	0856	0857	0858	0859	0860	0861	0862	0863
1540	0864	0865	0866	0867	0868	0869	0870	0871
1550	0872	0873	0874	0875	0876	0877	0878	0879
1560	0880	0881	0882	0883	0884	0885	0886	0887
1570	0888	0889	0890	0891	0892	0893	0894	0895
1600	0896	0897	0898	0899	0900	0901	0902	0903
1610	0904	0905	0906	0907	0908	0909	0910	0911
1620	0912	0913	0914	0915	0916	0917	0918	0919
1630	0920	0921	0922	0923	0924	0925	0926	0927
1640	0928	0929	0930	0931	0932	0933	0934	0935
1650	0936	0937	0938	0939	0940	0941	0942	0943
1660	0944	0945	0946	0947	0948	0949	0950	0951
1670	0952	0953	0954	0955	0956	0957	0958	0959
1700	0960	0961	0962	0963	0964	0965	0966	0967
1710	0968	0969	0970	0971	0972	0973	0974	0975
1720	0976	0977	0978	0979	0980	0981	0982	0983
1730	0984	0985	0986	0987	0988	0989	0990	0991
1740	0992	0993	0994	0995	0996	0997	0998	0999
1750	1000	1001	1002	1003	1004	1005	1006	1007
1760	1008	1009	1010	1011	1012	1013	1014	1015
1770	1016	1017	1018	1019	1020	1021	1022	1023

OCTAL-DECIMAL INTEGER CONVERSION TABLE (Continued)

2000 to 2777 (Octal)	1024 to 1535 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
2000	1024	1025	1026	1027	1028	1029	1030	1031
2010	1032	1033	1034	1035	1036	1037	1038	1039
2020	1040	1041	1042	1043	1044	1045	1046	1047
2030	1048	1049	1050	1051	1052	1053	1054	1055
2040	1056	1057	1058	1059	1060	1061	1062	1063
2050	1064	1065	1066	1067	1068	1069	1070	1071
2060	1072	1073	1074	1075	1076	1077	1078	1079
2070	1080	1081	1082	1083	1084	1085	1086	1087
2100	1088	1089	1090	1091	1092	1093	1094	1095
2110	1096	1097	1098	1099	1100	1101	1102	1103
2120	1104	1105	1106	1107	1108	1109	1110	1111
2130	1112	1113	1114	1115	1116	1117	1118	1119
2140	1120	1121	1122	1123	1124	1125	1126	1127
2150	1128	1129	1130	1131	1132	1133	1134	1135
2160	1136	1137	1138	1139	1140	1141	1142	1143
2170	1144	1145	1146	1147	1148	1149	1150	1151
2200	1152	1153	1154	1155	1156	1157	1158	1159
2210	1160	1161	1162	1163	1164	1165	1166	1167
2220	1168	1169	1170	1171	1172	1173	1174	1175
2230	1176	1177	1178	1179	1180	1181	1182	1183
2240	1184	1185	1186	1187	1188	1189	1190	1191
2250	1192	1193	1194	1195	1196	1197	1198	1199
2260	1200	1201	1202	1203	1204	1205	1206	1207
2270	1208	1209	1210	1211	1212	1213	1214	1215
2300	1216	1217	1218	1219	1220	1221	1222	1223
2310	1224	1225	1226	1227	1228	1229	1230	1231
2320	1232	1233	1234	1235	1236	1237	1238	1239
2330	1240	1241	1242	1243	1244	1245	1246	1247
2340	1248	1249	1250	1251	1252	1253	1254	1255
2350	1256	1257	1258	1259	1260	1261	1262	1263
2360	1264	1265	1266	1267	1268	1269	1270	1271
2370	1272	1273	1274	1275	1276	1277	1278	1279

	0	1	2	3	4	5	6	7
2400	1280	1281	1282	1283	1284	1285	1286	1287
2410	1288	1289	1290	1291	1292	1293	1294	1295
2420	1296	1297	1298	1299	1300	1301	1302	1303
2430	1304	1305	1306	1307	1308	1309	1310	1311
2440	1312	1313	1314	1315	1316	1317	1318	1319
2450	1320	1321	1322	1323	1324	1325	1326	1327
2460	1328	1329	1330	1331	1332	1333	1334	1335
2470	1336	1337	1338	1339	1340	1341	1342	1343
2500	1344	1345	1346	1347	1348	1349	1350	1351
2510	1352	1353	1354	1355	1356	1357	1358	1359
2520	1360	1361	1362	1363	1364	1365	1366	1367
2530	1368	1369	1370	1371	1372	1373	1374	1375
2540	1376	1377	1378	1379	1380	1381	1382	1383
2550	1384	1385	1386	1387	1388	1389	1390	1391
2560	1392	1393	1394	1395	1396	1397	1398	1399
2570	1400	1401	1402	1403	1404	1405	1406	1407
2600	1408	1409	1410	1411	1412	1413	1414	1415
2610	1416	1417	1418	1419	1420	1421	1422	1423
2620	1424	1425	1426	1427	1428	1429	1430	1431
2630	1432	1433	1434	1435	1436	1437	1438	1439
2640	1440	1441	1442	1443	1444	1445	1446	1447
2650	1448	1449	1450	1451	1452	1453	1454	1455
2660	1456	1457	1458	1459	1460	1461	1462	1463
2670	1464	1465	1466	1467	1468	1469	1470	1471
2700	1472	1473	1474	1475	1476	1477	1478	1479
2710	1480	1481	1482	1483	1484	1485	1486	1487
2720	1488	1489	1490	1491	1492	1493	1494	1495
2730	1496	1497	1498	1499	1500	1501	1502	1503
2740	1504	1505	1506	1507	1508	1509	1510	1511
2750	1512	1513	1514	1515	1516	1517	1518	1519
2760	1520	1521	1522	1523	1524	1525	1526	1527
2770	1528	1529	1530	1531	1532	1533	1534	1535

3000 to 3777 (Octal)	1536 to 2047 (Decimal)

	0	1	2	3	4	5	6	7
3000	1536	1537	1538	1539	1540	1541	1542	1543
3010	1544	1545	1546	1547	1548	1549	1550	1551
3020	1552	1553	1554	1555	1556	1557	1558	1559
3030	1560	1561	1562	1563	1564	1565	1566	1567
3040	1568	1569	1570	1571	1572	1573	1574	1575
3050	1576	1577	1578	1579	1580	1581	1582	1583
3060	1584	1585	1586	1587	1588	1589	1590	1591
3070	1592	1593	1594	1595	1596	1597	1598	1599
3100	1600	1601	1602	1603	1604	1605	1606	1607
3110	1608	1609	1610	1611	1612	1613	1614	1615
3120	1616	1617	1618	1619	1620	1621	1622	1623
3130	1624	1625	1626	1627	1628	1629	1630	1631
3140	1632	1633	1634	1635	1636	1637	1638	1639
3150	1640	1641	1642	1643	1644	1645	1646	1647
3160	1648	1649	1650	1651	1652	1653	1654	1655
3170	1656	1657	1658	1659	1660	1661	1662	1663
3200	1664	1665	1666	1667	1668	1669	1670	1671
3210	1672	1673	1674	1675	1676	1677	1678	1679
3220	1680	1681	1682	1683	1684	1685	1686	1687
3230	1688	1689	1690	1691	1692	1693	1694	1695
3240	1696	1697	1698	1699	1700	1701	1702	1703
3250	1704	1705	1706	1707	1708	1709	1710	1711
3260	1712	1713	1714	1715	1716	1717	1718	1719
3270	1720	1721	1722	1723	1724	1725	1726	1727
3300	1728	1729	1730	1731	1732	1733	1734	1735
3310	1736	1737	1738	1739	1740	1741	1742	1743
3320	1744	1745	1746	1747	1748	1749	1750	1751
3330	1752	1753	1754	1755	1756	1757	1758	1759
3340	1760	1761	1762	1763	1764	1765	1766	1767
3350	1768	1769	1770	1771	1772	1773	1774	1775
3360	1776	1777	1778	1779	1780	1781	1782	1783
3370	1784	1785	1786	1787	1788	1789	1790	1791

	0	1	2	3	4	5	6	7
3400	1792	1793	1794	1795	1796	1797	1798	1799
3410	1800	1801	1802	1803	1804	1805	1806	1807
3420	1808	1809	1810	1811	1812	1813	1814	1815
3430	1816	1817	1818	1819	1820	1821	1822	1823
3440	1824	1825	1826	1827	1828	1829	1830	1831
3450	1832	1833	1834	1835	1836	1837	1838	1839
3460	1840	1841	1842	1843	1844	1845	1846	1847
3470	1848	1849	1850	1851	1852	1853	1854	1855
3500	1856	1857	1858	1859	1860	1861	1862	1863
3510	1864	1865	1866	1867	1868	1869	1870	1871
3520	1872	1873	1874	1875	1876	1877	1878	1879
3530	1880	1881	1882	1883	1884	1885	1886	1887
3540	1888	1889	1890	1891	1892	1893	1894	1895
3550	1896	1897	1898	1899	1900	1901	1902	1903
3560	1904	1905	1906	1907	1908	1909	1910	1911
3570	1912	1913	1914	1915	1916	1917	1918	1919
3600	1920	1921	1922	1923	1924	1925	1926	1927
3610	1928	1929	1930	1931	1932	1933	1934	1935
3620	1936	1937	1938	1939	1940	1941	1942	1943
3630	1944	1945	1946	1947	1948	1949	1950	1951
3640	1952	1953	1954	1955	1956	1957	1958	1959
3650	1960	1961	1962	1963	1964	1965	1966	1967
3660	1968	1969	1970	1971	1972	1973	1974	1975
3670	1976	1977	1978	1979	1980	1981	1982	1983
3700	1984	1985	1986	1987	1988	1989	1990	1991
3710	1992	1993	1994	1995	1996	1997	1998	1999
3720	2000	2001	2002	2003	2004	2005	2006	2007
3730	2008	2009	2010	2011	2012	2013	2014	2015
3740	2016	2017	2018	2019	2020	2021	2022	2023
3750	2024	2025	2026	2027	2028	2029	2030	2031
3760	2032	2033	2034	2035	2036	2037	2038	2039
3770	2040	2041	2042	2043	2044	2045	2046	2047

OCTAL-DECIMAL INTEGER CONVERSION TABLE (Continued)

4000 to 4777 (Octal)	2048 to 2559 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
4000	2048	2049	2050	2051	2052	2053	2054	2055
4010	2056	2057	2058	2059	2060	2061	2062	2063
4020	2064	2065	2066	2067	2068	2069	2070	2071
4030	2072	2073	2074	2075	2076	2077	2078	2079
4040	2080	2081	2082	2083	2084	2085	2086	2087
4050	2088	2089	2090	2091	2092	2093	2094	2095
4060	2096	2097	2098	2099	2100	2101	2102	2103
4070	2104	2105	2106	2107	2108	2109	2110	2111
4100	2112	2113	2114	2115	2116	2117	2118	2119
4110	2120	2121	2122	2123	2124	2125	2126	2127
4120	2128	2129	2130	2131	2132	2133	2134	2135
4130	2136	2137	2138	2139	2140	2141	2142	2143
4140	2144	2145	2146	2147	2148	2149	2150	2151
4150	2152	2153	2154	2155	2156	2157	2158	2159
4160	2160	2161	2162	2163	2164	2165	2166	2167
4170	2168	2169	2170	2171	2172	2173	2174	2175
4200	2176	2177	2178	2179	2180	2181	2182	2183
4210	2184	2185	2186	2187	2188	2189	2190	2191
4220	2192	2193	2194	2195	2196	2197	2198	2199
4230	2200	2201	2202	2203	2204	2205	2206	2207
4240	2208	2209	2210	2211	2212	2213	2214	2215
4250	2216	2217	2218	2219	2220	2221	2222	2223
4260	2224	2225	2226	2227	2228	2229	2230	2231
4270	2232	2233	2234	2235	2236	2237	2238	2239
4300	2240	2241	2242	2243	2244	2245	2246	2247
4310	2248	2249	2250	2251	2252	2253	2254	2255
4320	2256	2257	2258	2259	2260	2261	2262	2263
4330	2264	2265	2266	2267	2268	2269	2270	2271
4340	2272	2273	2274	2275	2276	2277	2278	2279
4350	2280	2281	2282	2283	2284	2285	2286	2287
4360	2288	2289	2290	2291	2292	2293	2294	2295
4370	2296	2297	2298	2299	2300	2301	2302	2303

	0	1	2	3	4	5	6	7
4400	2304	2305	2306	2307	2308	2309	2310	2311
4410	2312	2313	2314	2315	2316	2317	2318	2319
4420	2320	2321	2322	2323	2324	2325	2326	2327
4430	2328	2329	2330	2331	2332	2333	2334	2335
4440	2336	2337	2338	2339	2340	2341	2342	2343
4450	2344	2345	2346	2347	2348	2349	2350	2351
4460	2352	2353	2354	2355	2356	2357	2358	2359
4470	2360	2361	2362	2363	2364	2365	2366	2367
4500	2368	2369	2370	2371	2372	2373	2374	2375
4510	2376	2377	2378	2379	2380	2381	2382	2383
4520	2384	2385	2386	2387	2388	2389	2390	2391
4530	2392	2393	2394	2395	2396	2397	2398	2399
4540	2400	2401	2402	2403	2404	2405	2406	2407
4550	2408	2409	2410	2411	2412	2413	2414	2415
4560	2416	2417	2418	2419	2420	2421	2422	2423
4570	2424	2425	2426	2427	2428	2429	2430	2431
4600	2432	2433	2434	2435	2436	2437	2438	2439
4610	2440	2441	2442	2443	2444	2445	2446	2447
4620	2448	2449	2450	2451	2452	2453	2454	2455
4630	2456	2457	2458	2459	2460	2461	2462	2463
4640	2464	2465	2466	2467	2468	2469	2470	2471
4650	2472	2473	2474	2475	2476	2477	2478	2479
4660	2480	2481	2482	2483	2484	2485	2486	2487
4670	2488	2489	2490	2491	2492	2493	2494	2495
4700	2496	2497	2498	2499	2500	2501	2502	2503
4710	2504	2505	2506	2507	2508	2509	2510	2511
4720	2512	2513	2514	2515	2516	2517	2518	2519
4730	2520	2521	2522	2523	2524	2525	2526	2527
4740	2528	2529	2530	2531	2532	2533	2534	2535
4750	2536	2537	2538	2539	2540	2541	2542	2543
4760	2544	2545	2546	2547	2548	2549	2550	2551
4770	2552	2553	2554	2555	2556	2557	2558	2559

5000 to 5777 (Octal)	2560 to 3071 (Decimal)

	0	1	2	3	4	5	6	7
5000	2560	2561	2562	2563	2564	2565	2566	2567
5010	2568	2569	2570	2571	2572	2573	2574	2575
5020	2576	2577	2578	2579	2580	2581	2582	2583
5030	2584	2585	2586	2587	2588	2589	2590	2591
5040	2592	2593	2594	2595	2596	2597	2598	2599
5050	2600	2601	2602	2603	2604	2605	2606	2607
5060	2608	2609	2610	2611	2612	2613	2614	2615
5070	2616	2617	2618	2619	2620	2621	2622	2623
5100	2624	2625	2626	2627	2628	2629	2630	2631
5110	2632	2633	2634	2635	2636	2637	2638	2639
5120	2640	2641	2642	2643	2644	2645	2646	2647
5130	2648	2649	2650	2651	2652	2653	2654	2655
5140	2656	2657	2658	2659	2660	2661	2662	2663
5150	2664	2665	2666	2667	2668	2669	2670	2671
5160	2672	2673	2674	2675	2676	2677	2678	2679
5170	2680	2681	2682	2683	2684	2685	2686	2687
5200	2688	2689	2690	2691	2692	2693	2694	2695
5210	2696	2697	2698	2699	2700	2701	2702	2703
5220	2704	2705	2706	2707	2708	2709	2710	2711
5230	2712	2713	2714	2715	2716	2717	2718	2719
5240	2720	2721	2722	2723	2724	2725	2726	2727
5250	2728	2729	2730	2731	2732	2733	2734	2735
5260	2736	2737	2738	2739	2740	2741	2742	2743
5270	2744	2745	2746	2747	2748	2749	2750	2751
5300	2752	2753	2754	2755	2756	2757	2758	2759
5310	2760	2761	2762	2763	2764	2765	2766	2767
5320	2768	2769	2770	2771	2772	2773	2774	2775
5330	2776	2777	2778	2779	2780	2781	2782	2783
5340	2784	2785	2786	2787	2788	2789	2790	2791
5350	2792	2793	2794	2795	2796	2797	2798	2799
5360	2800	2801	2802	2803	2804	2805	2806	2807
5370	2808	2809	2810	2811	2812	2813	2814	2815

	0	1	2	3	4	5	6	7
5400	2816	2817	2818	2819	2820	2821	2822	2823
5410	2824	2825	2826	2827	2828	2829	2830	2831
5420	2832	2833	2834	2835	2836	2837	2838	2839
5430	2840	2841	2842	2843	2844	2845	2846	2847
5440	2848	2849	2850	2851	2852	2853	2854	2855
5450	2856	2857	2858	2859	2860	2861	2862	2863
5460	2864	2865	2866	2867	2868	2869	2870	2871
5470	2872	2873	2874	2875	2876	2877	2878	2879
5500	2880	2881	2882	2883	2884	2885	2886	2887
5510	2888	2889	2890	2891	2892	2893	2894	2895
5520	2896	2897	2898	2899	2900	2901	2902	2903
5530	2904	2905	2906	2907	2908	2909	2910	2911
5540	2912	2913	2914	2915	2916	2917	2918	2919
5550	2920	2921	2922	2923	2924	2925	2926	2927
5560	2928	2929	2930	2931	2932	2933	2934	2935
5570	2936	2937	2938	2939	2940	2941	2942	2943
5600	2944	2945	2946	2947	2948	2949	2950	2951
5610	2952	2953	2954	2955	2956	2957	2958	2959
5620	2960	2961	2962	2963	2964	2965	2966	2967
5630	2968	2969	2970	2971	2972	2973	2974	2975
5640	2976	2977	2978	2979	2980	2981	2982	2983
5650	2984	2985	2986	2987	2988	2989	2990	2991
5660	2992	2993	2994	2995	2996	2997	2998	2999
5670	3000	3001	3002	3003	3004	3005	3006	3007
5700	3008	3009	3010	3011	3012	3013	3014	3015
5710	3016	3017	3018	3019	3020	3021	3022	3023
5720	3024	3025	3026	3027	3028	3029	3030	3031
5730	3032	3033	3034	3035	3036	3037	3038	3039
5740	3040	3041	3042	3043	3044	3045	3046	3047
5750	3048	3049	3050	3051	3052	3053	3054	3055
5760	3056	3057	3058	3059	3060	3061	3062	3063
5770	3064	3065	3066	3067	3068	3069	3070	3071

OCTAL-DECIMAL INTEGER CONVERSION TABLE (Continued)

6000 to 6777 (Octal)	3072 to 3583 (Decimal)

Octal	Decimal
10000 -	4096
20000 -	8192
30000 -	12288
40000 -	16384
50000 -	20480
60000 -	24576
70000 -	28672

	0	1	2	3	4	5	6	7
6000	3072	3073	3074	3075	3076	3077	3078	3079
6010	3080	3081	3082	3083	3084	3085	3086	3087
6020	3088	3089	3090	3091	3092	3093	3094	3095
6030	3096	3097	3098	3099	3100	3101	3102	3103
6040	3104	3105	3106	3107	3108	3109	3110	3111
6050	3112	3113	3114	3115	3116	3117	3118	3119
6060	3120	3121	3122	3123	3124	3125	3126	3127
6070	3128	3129	3130	3131	3132	3133	3134	3135
6100	3136	3137	3138	3139	3140	3141	3142	3143
6110	3144	3145	3146	3147	3148	3149	3150	3151
6120	3152	3153	3154	3155	3156	3157	3158	3159
6130	3160	3161	3162	3163	3164	3165	3166	3167
6140	3168	3169	3170	3171	3172	3173	3174	3175
6150	3176	3177	3178	3179	3180	3181	3182	3183
6160	3184	3185	3186	3187	3188	3189	3190	3191
6170	3192	3193	3194	3195	3196	3197	3198	3199
6200	3200	3201	3202	3203	3204	3205	3206	3207
6210	3208	3209	3210	3211	3212	3213	3214	3215
6220	3216	3217	3218	3219	3220	3221	3222	3223
6230	3224	3225	3226	3227	3228	3229	3230	3231
6240	3232	3233	3234	3235	3236	3237	3238	3239
6250	3240	3241	3242	3243	3244	3245	3246	3247
6260	3248	3249	3250	3251	3252	3253	3254	3255
6270	3256	3257	3258	3259	3260	3261	3262	3263
6300	3264	3265	3266	3267	3268	3269	3270	3271
6310	3272	3273	3274	3275	3276	3277	3278	3279
6320	3280	3281	3282	3283	3284	3285	3286	3287
6330	3288	3289	3290	3291	3292	3293	3294	3295
6340	3296	3297	3298	3299	3300	3301	3302	3303
6350	3304	3305	3306	3307	3308	3309	3310	3311
6360	3312	3313	3314	3315	3316	3317	3318	3319
6370	3320	3321	3322	3323	3324	3325	3326	3327

	0	1	2	3	4	5	6	7
6400	3328	3329	3330	3331	3332	3333	3334	3335
6410	3336	3337	3338	3339	3340	3341	3342	3343
6420	3344	3345	3346	3347	3348	3349	3350	3351
6430	3352	3353	3354	3355	3356	3357	3358	3359
6440	3360	3361	3362	3363	3364	3365	3366	3367
6450	3368	3369	3370	3371	3372	3373	3374	3375
6460	3376	3377	3378	3379	3380	3381	3382	3383
6470	3384	3385	3386	3387	3388	3389	3390	3391
6500	3392	3393	3394	3395	3396	3397	3398	3399
6510	3400	3401	3402	3403	3404	3405	3406	3407
6520	3408	3409	3410	3411	3412	3413	3414	3415
6530	3416	3417	3418	3419	3420	3421	3422	3423
6540	3424	3425	3426	3427	3428	3429	3430	3431
6550	3432	3433	3434	3435	3436	3437	3438	3439
6560	3440	3441	3442	3443	3444	3445	3446	3447
6570	3448	3449	3450	3451	3452	3453	3454	3455
6600	3456	3457	3458	3459	3460	3461	3462	3463
6610	3464	3465	3466	3467	3468	3469	3470	3471
6620	3472	3473	3474	3475	3476	3477	3478	3479
6630	3480	3481	3482	3483	3484	3485	3486	3487
6640	3488	3489	3490	3491	3492	3493	3494	3495
6650	3496	3497	3498	3499	3500	3501	3502	3503
6660	3504	3505	3506	3507	3508	3509	3510	3511
6670	3512	3513	3514	3515	3516	3517	3518	3519
6700	3520	3521	3522	3523	3524	3525	3526	3527
6710	3528	3529	3530	3531	3532	3533	3534	3535
6720	3536	3537	3538	3539	3540	3541	3542	3543
6730	3544	3545	3546	3547	3548	3549	3550	3551
6740	3552	3553	3554	3555	3556	3557	3558	3559
6750	3560	3561	3562	3563	3564	3565	3566	3567
6760	3568	3569	3570	3571	3572	3573	3574	3575
6770	3576	3577	3578	3579	3580	3581	3582	3583

7000 to 7777 (Octal)	3584 to 4095 (Decimal)

	0	1	2	3	4	5	6	7
7000	3584	3585	3586	3587	3588	3589	3590	3591
7010	3592	3593	3594	3595	3596	3597	3598	3599
7020	3600	3601	3602	3603	3604	3605	3606	3607
7030	3608	3609	3610	3611	3612	3613	3614	3615
7040	3616	3617	3618	3619	3620	3621	3622	3623
7050	3624	3625	3626	3627	3628	3629	3630	3631
7060	3632	3633	3634	3635	3636	3637	3638	3639
7070	3640	3641	3642	3643	3644	3645	3646	3647
7100	3648	3649	3650	3651	3652	3653	3654	3655
7110	3656	3657	3658	3659	3660	3661	3662	3663
7120	3664	3665	3666	3667	3668	3669	3670	3671
7130	3672	3673	3674	3675	3676	3677	3678	3679
7140	3680	3681	3682	3683	3684	3685	3686	3687
7150	3688	3689	3690	3691	3692	3693	3694	3695
7160	3696	3697	3698	3699	3700	3701	3702	3703
7170	3704	3705	3706	3707	3708	3709	3710	3711
7200	3712	3713	3714	3715	3716	3717	3718	3719
7210	3720	3721	3722	3723	3724	3725	3726	3727
7220	3728	3729	3730	3731	3732	3733	3734	3735
7230	3736	3737	3738	3739	3740	3741	3742	3743
7240	3744	3745	3746	3747	3748	3749	3750	3751
7250	3752	3753	3754	3755	3756	3757	3758	3759
7260	3760	3761	3762	3763	3764	3765	3766	3767
7270	3768	3769	3770	3771	3772	3773	3774	3775
7300	3776	3777	3778	3779	3780	3781	3782	3783
7310	3784	3785	3786	3787	3788	3789	3790	3791
7320	3792	3793	3794	3795	3796	3797	3798	3799
7330	3800	3801	3802	3803	3804	3805	3806	3807
7340	3808	3809	3810	3811	3812	3813	3814	3815
7350	3816	3817	3818	3819	3820	3821	3822	3823
7360	3824	3825	3826	3827	3828	3829	3830	3831
7370	3832	3833	3834	3835	3836	3837	3838	3839

	0	1	2	3	4	5	6	7
7400	3840	3841	3842	3843	3844	3845	3846	3847
7410	3848	3849	3850	3851	3852	3853	3854	3855
7420	3856	3857	3858	3859	3860	3861	3862	3863
7430	3864	3865	3866	3867	3868	3869	3870	3871
7440	3872	3873	3874	3875	3876	3877	3878	3879
7450	3880	3881	3882	3883	3884	3885	3886	3887
7460	3888	3889	3890	3891	3892	3893	3894	3895
7470	3896	3897	3898	3899	3900	3901	3902	3903
7500	3904	3905	3906	3907	3908	3909	3910	3911
7510	3912	3913	3914	3915	3916	3917	3918	3919
7520	3920	3921	3922	3923	3924	3925	3926	3927
7530	3928	3929	3930	3931	3932	3933	3934	3935
7540	3936	3937	3938	3939	3940	3941	3942	3943
7550	3944	3945	3946	3947	3948	3949	3950	3951
7560	3952	3953	3954	3955	3956	3957	3958	3959
7570	3960	3961	3962	3963	3964	3965	3966	3967
7600	3968	3969	3970	3971	3972	3973	3974	3975
7610	3976	3977	3978	3979	3980	3981	3982	3983
7620	3984	3985	3986	3987	3988	3989	3990	3991
7630	3992	3993	3994	3995	3996	3997	3998	3999
7640	4000	4001	4002	4003	4004	4005	4006	4007
7650	4008	4009	4010	4011	4012	4013	4014	4015
7660	4016	4017	4018	4019	4020	4021	4022	4023
7670	4024	4025	4026	4027	4028	4029	4030	4031
7700	4032	4033	4034	4035	4036	4037	4038	4039
7710	4040	4041	4042	4043	4044	4045	4046	4047
7720	4048	4049	4050	4051	4052	4053	4054	4055
7730	4056	4057	4058	4059	4060	4061	4062	4063
7740	4064	4065	4066	4067	4068	4069	4070	4071
7750	4072	4073	4074	4075	4076	4077	4078	4079
7760	4080	4081	4082	4083	4084	4085	4086	4087
7770	4088	4089	4090	4091	4092	4093	4094	4095

APPENDIX E

OCTAL-DECIMAL FRACTION CONVERSION TABLE

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000	.000000	.100	.125000	.200	.250000	.300	.375000
.001	.001953	.101	.126953	.201	.251953	.301	.376953
.002	.003906	.102	.128906	.202	.253906	.302	.378906
.003	.005859	.103	.130859	.203	.255859	.303	.380859
.004	.007812	.104	.132812	.204	.257812	.304	.382812
.005	.009765	.105	.134765	.205	.259765	.305	.384765
.006	.011718	.106	.136718	.206	.261718	.306	.386718
.007	.013671	.107	.138671	.207	.263671	.307	.388671
.010	.015625	.110	.140625	.210	.265625	.310	.390625
.011	.017578	.111	.142578	.211	.267578	.311	.392578
.012	.019531	.112	.144531	.212	.269531	.312	.394531
.013	.021484	.113	.146484	.213	.271484	.313	.396484
.014	.023437	.114	.148437	.214	.273437	.314	.398437
.015	.025390	.115	.150390	.215	.275390	.315	.400390
.016	.027343	.116	.152343	.216	.277343	.316	.402343
.017	.029296	.117	.154296	.217	.279296	.317	.404296
.020	.031250	.120	.156250	.220	.281250	.320	.406250
.021	.033203	.121	.158203	.221	.283203	.321	.408203
.022	.035156	.122	.160156	.222	.285156	.322	.410156
.023	.037109	.123	.162109	.223	.287109	.323	.412109
.024	.039062	.124	.164062	.224	.289062	.324	.414062
.025	.041015	.125	.166015	.225	.291015	.325	.416015
.026	.042968	.126	.167968	.226	.292968	.326	.417968
.027	.044921	.127	.169921	.227	.294921	.327	.419921
.030	.046875	.130	.171875	.230	.296875	.330	.421875
.031	.048828	.131	.173828	.231	.298828	.331	.423828
.032	.050781	.132	.175781	.232	.300781	.332	.425781
.033	.052734	.133	.177734	.233	.302734	.333	.427734
.034	.054687	.134	.179687	.234	.304687	.334	.429687
.035	.056640	.135	.181640	.235	.306640	.335	.431640
.036	.058593	.136	.183593	.236	.308593	.336	.433593
.037	.060546	.137	.185546	.237	.310546	.337	.435546
.040	.062500	.140	.187500	.240	.312500	.340	.437500
.041	.064453	.141	.189453	.241	.314453	.341	.439453
.042	.066406	.142	.191406	.242	.316406	.342	.441406
.043	.068359	.143	.193359	.243	.318359	.343	.443359
.044	.070312	.144	.195312	.244	.320312	.344	.445312
.045	.072265	.145	.197265	.245	.322265	.345	.447265
.046	.074218	.146	.199218	.246	.324218	.346	.449218
.047	.076171	.147	.201171	.247	.326171	.347	.451171
.050	.078125	.150	.203125	.250	.328125	.350	.453125
.051	.080078	.151	.205078	.251	.330078	.351	.455078
.052	.082031	.152	.207031	.252	.332031	.352	.457031
.053	.083984	.153	.208984	.253	.333984	.353	.458984
.054	.085937	.154	.210937	.254	.335937	.354	.460937
.055	.087890	.155	.212890	.255	.337890	.355	.462890
.056	.089843	.156	.214843	.256	.339843	.356	.464843
.057	.091796	.157	.216796	.257	.341796	.357	.466796
.060	.093750	.160	.218750	.260	.343750	.360	.468750
.061	.095703	.161	.220703	.261	.345703	.361	.470703
.062	.097656	.162	.222656	.262	.347656	.362	.472656
.063	.099609	.163	.224609	.263	.349609	.363	.474609
.064	.101562	.164	.226562	.264	.351562	.364	.476562
.065	.103515	.165	.228515	.265	.353515	.365	.478515
.066	.105468	.166	.230468	.266	.355468	.366	.480468
.067	.107421	.167	.232421	.267	.357421	.367	.482421
.070	.109375	.170	.234375	.270	.359375	.370	.484375
.071	.111328	.171	.236328	.271	.361328	.371	.486328
.072	.113281	.172	.238281	.272	.363281	.372	.488281
.073	.115234	.173	.240234	.273	.365234	.373	.490234
.074	.117187	.174	.242187	.274	.367187	.374	.492187
.075	.119140	.175	.244140	.275	.369140	.375	.494140
.076	.121093	.176	.246093	.276	.371093	.376	.496093
.077	.123046	.177	.248046	.277	.373046	.377	.498046

OCTAL-DECIMAL FRACTION CONVERSION TABLE (Continued)

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000000	.000000	.000100	.000244	.000200	.000488	.000300	.000732
.000001	.000003	.000101	.000247	.000201	.000492	.000301	.000736
.000002	.000007	.000102	.000251	.000202	.000495	.000302	.000740
.000003	.000011	.000103	.000255	.000203	.000499	.000303	.000743
.000004	.000015	.000104	.000259	.000204	.000503	.000304	.000747
.000005	.000019	.000105	.000263	.000205	.000507	.000305	.000751
.000006	.000022	.000106	.000267	.000206	.000511	.000306	.000755
.000007	.000026	.000107	.000270	.000207	.000514	.000307	.000759
.000010	.000030	.000110	.000274	.000210	.000518	.000310	.000762
.000011	.000034	.000111	.000278	.000211	.000522	.000311	.000766
.000012	.000038	.000112	.000282	.000212	.000526	.000312	.000770
.000013	.000041	.000113	.000286	.000213	.000530	.000313	.000774
.000014	.000045	.000114	.000289	.000214	.000534	.000314	.000778
.000015	.000049	.000115	.000293	.000215	.000537	.000315	.000782
.000016	.000053	.000116	.000297	.000216	.000541	.000316	.000785
.000017	.000057	.000117	.000301	.000217	.000545	.000317	.000789
.000020	.000061	.000120	.000305	.000220	.000549	.000320	.000793
.000021	.000064	.000121	.000308	.000221	.000553	.000321	.000797
.000022	.000068	.000122	.000312	.000222	.000556	.000322	.000801
.000023	.000072	.000123	.000316	.000223	.000560	.000323	.000805
.000024	.000076	.000124	.000320	.000224	.000564	.000324	.000808
.000025	.000080	.000125	.000324	.000225	.000568	.000325	.000812
.000026	.000083	.000126	.000328	.000226	.000572	.000326	.000816
.000027	.000087	.000127	.000331	.000227	.000576	.000327	.000820
.000030	.000091	.000130	.000335	.000230	.000579	.000330	.000823
.000031	.000095	.000131	.000339	.000231	.000583	.000331	.000827
.000032	.000099	.000132	.000343	.000232	.000587	.000332	.000831
.000033	.000102	.000133	.000347	.000233	.000591	.000333	.000835
.000034	.000106	.000134	.000350	.000234	.000595	.000334	.000839
.000035	.000110	.000135	.000354	.000235	.000598	.000335	.000843
.000036	.000114	.000136	.000358	.000236	.000602	.000336	.000846
.000037	.000118	.000137	.000362	.000237	.000606	.000337	.000850
.000040	.000122	.000140	.000366	.000240	.000610	.000340	.000854
.000041	.000125	.000141	.000370	.000241	.000614	.000341	.000858
.000042	.000129	.000142	.000373	.000242	.000617	.000342	.000862
.000043	.000133	.000143	.000377	.000243	.000621	.000343	.000865
.000044	.000137	.000144	.000381	.000244	.000625	.000344	.000869
.000045	.000141	.000145	.000385	.000245	.000629	.000345	.000873
.000046	.000144	.000146	.000389	.000246	.000633	.000346	.000877
.000047	.000148	.000147	.000392	.000247	.000637	.000347	.000881
.000050	.000152	.000150	.000396	.000250	.000640	.000350	.000885
.000051	.000156	.000151	.000400	.000251	.000644	.000351	.000888
.000052	.000160	.000152	.000404	.000252	.000648	.000352	.000892
.000053	.000164	.000153	.000408	.000253	.000652	.000353	.000896
.000054	.000167	.000154	.000411	.000254	.000656	.000354	.000900
.000055	.000171	.000155	.000415	.000255	.000659	.000355	.000904
.000056	.000175	.000156	.000419	.000256	.000663	.000356	.000907
.000057	.000179	.000157	.000423	.000257	.000667	.000357	.000911
.000060	.000183	.000160	.000427	.000260	.000671	.000360	.000915
.000061	.000186	.000161	.000431	.000261	.000675	.000361	.000919
.000062	.000190	.000162	.000434	.000262	.000679	.000362	.000923
.000063	.000194	.000163	.000438	.000263	.000682	.000363	.000926
.000064	.000198	.000164	.000442	.000264	.000686	.000364	.000930
.000065	.000202	.000165	.000446	.000265	.000690	.000365	.000934
.000066	.000205	.000166	.000450	.000266	.000694	.000366	.000938
.000067	.000209	.000167	.000453	.000267	.000698	.000367	.000942
.000070	.000213	.000170	.000457	.000270	.000701	.000370	.000946
.000071	.000217	.000171	.000461	.000271	.000705	.000371	.000949
.000072	.000221	.000172	.000465	.000272	.000709	.000372	.000953
.000073	.000225	.000173	.000469	.000273	.000713	.000373	.000957
.000074	.000228	.000174	.000473	.000274	.000717	.000374	.000961
.000075	.000232	.000175	.000476	.000275	.000720	.000375	.000965
.000076	.000236	.000176	.000480	.000276	.000724	.000376	.000968
.000077	.000240	.000177	.000484	.000277	.000728	.000377	.000972

OCTAL-DECIMAL FRACTION CONVERSION TABLE (Continued)

OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.	OCTAL	DEC.
.000400	.000976	.000500	.001220	.000600	.001464	.000700	.001708
.000401	.000980	.000501	.001224	.000601	.001468	.000701	.001712
.000402	.000984	.000502	.001228	.000602	.001472	.000702	.001716
.000403	.000988	.000503	.001232	.000603	.001476	.000703	.001720
.000404	.000991	.000504	.001235	.000604	.001480	.000704	.001724
.000405	.000995	.000505	.001239	.000605	.001483	.000705	.001728
.000406	.000999	.000506	.001243	.000606	.001487	.000706	.001731
.000407	.001003	.000507	.001247	.000607	.001491	.000707	.001735
.000410	.001007	.000510	.001251	.000610	.001495	.000710	.001739
.000411	.001010	.000511	.001255	.000611	.001499	.000711	.001743
.000412	.001014	.000512	.001258	.000612	.001502	.000712	.001747
.000413	.001018	.000513	.001262	.000613	.001506	.000713	.001750
.000414	.001022	.000514	.001266	.000614	.001510	.000714	.001754
.000415	.001026	.000515	.001270	.000615	.001514	.000715	.001758
.000416	.001029	.000516	.001274	.000616	.001518	.000716	.001762
.000417	.001033	.000517	.001277	.000617	.001522	.000717	.001766
.000420	.001037	.000520	.001281	.000620	.001525	.000720	.001770
.000421	.001041	.000521	.001285	.000621	.001529	.000721	.001773
.000422	.001045	.000522	.001289	.000622	.001533	.000722	.001777
.000423	.001049	.000523	.001293	.000623	.001537	.000723	.001781
.000424	.001052	.000524	.001296	.000624	.001541	.000724	.001785
.000425	.001056	.000525	.001300	.000625	.001544	.000725	.001789
.000426	.001060	.000526	.001304	.000626	.001548	.000726	.001792
.000427	.001064	.000527	.001308	.000627	.001552	.000727	.001796
.000430	.001068	.000530	.001312	.000630	.001556	.000730	.001800
.000431	.001071	.000531	.001316	.000631	.001560	.000731	.001804
.000432	.001075	.000532	.001319	.000632	.001564	.000732	.001808
.000433	.001079	.000533	.001323	.000633	.001567	.000733	.001811
.000434	.001083	.000534	.001327	.000634	.001571	.000734	.001815
.000435	.001087	.000535	.001331	.000635	.001575	.000735	.001819
.000436	.001091	.000536	.001335	.000636	.001579	.000736	.001823
.000437	.001094	.000537	.001338	.000637	.001583	.000737	.001827
.000440	.001098	.000540	.001342	.000640	.001586	.000740	.001831
.000441	.001102	.000541	.001346	.000641	.001590	.000741	.001834
.000442	.001106	.000542	.001350	.000642	.001594	.000742	.001838
.000443	.001110	.000543	.001354	.000643	.001598	.000743	.001842
.000444	.001113	.000544	.001358	.000644	.001602	.000744	.001846
.000445	.001117	.000545	.001361	.000645	.001605	.000745	.001850
.000446	.001121	.000546	.001365	.000646	.001609	.000746	.001853
.000447	.001125	.000547	.001369	.000647	.001613	.000747	.001857
.000450	.001129	.000550	.001373	.000650	.001617	.000750	.001861
.000451	.001132	.000551	.001377	.000651	.001621	.000751	.001865
.000452	.001136	.000552	.001380	.000652	.001625	.000752	.001869
.000453	.001140	.000553	.001384	.000653	.001628	.000753	.001873
.000454	.001144	.000554	.001388	.000654	.001632	.000754	.001876
.000455	.001148	.000555	.001392	.000655	.001636	.000755	.001880
.000456	.001152	.000556	.001396	.000656	.001640	.000756	.001884
.000457	.001155	.000557	.001399	.000657	.001644	.000757	.001888
.000460	.001159	.000560	.001403	.000660	.001647	.000760	.001892
.000461	.001163	.000561	.001407	.000661	.001651	.000761	.001895
.000462	.001167	.000562	.001411	.000662	.001655	.000762	.001899
.000463	.001171	.000563	.001415	.000663	.001659	.000763	.001903
.000464	.001174	.000564	.001419	.000664	.001663	.000764	.001907
.000465	.001178	.000565	.001422	.000665	.001667	.000765	.001911
.000466	.001182	.000566	.001426	.000666	.001670	.000766	.001914
.000467	.001186	.000567	.001430	.000667	.001674	.000767	.001918
.000470	.001190	.000570	.001434	.000670	.001678	.000770	.001922
.000471	.001194	.000571	.001438	.000671	.001682	.000771	.001926
.000472	.001197	.000572	.001441	.000672	.001686	.000772	.001930
.000473	.001201	.000573	.001445	.000673	.001689	.000773	.001934
.000474	.001205	.000574	.001449	.000674	.001693	.000774	.001937
.000475	.001209	.000575	.001453	.000675	.001697	.000775	.001941
.000476	.001213	.000576	.001457	.000676	.001701	.000776	.001945
.000477	.001216	.000577	.001461	.000677	.001705	.000777	.001949

APPENDIX F

POWERS OF TWO

2^n	n	2^{-n}
1	0	1 0
2	1	0 5
4	2	0 25
8	3	0 125
16	4	0 062 5
32	5	0 031 25
64	6	0 015 625
128	7	0 007 812 5
256	8	0 003 906 25
512	9	0 001 953 125
1 024	10	0 000 976 562 5
2 048	11	0 000 488 281 25
4 096	12	0 000 244 140 625
8 192	13	0 000 122 070 312 5
16 384	14	0 000 061 035 156 25
32 768	15	0 000 030 517 578 125
65 536	16	0 000 015 258 789 062 5
131 072	17	0 000 007 629 394 531 25
262 144	18	0 000 003 814 697 265 625
524 288	19	0 000 001 907 348 632 812 5
1 048 576	20	0 000 000 953 674 316 406 25
2 097 152	21	0 000 000 476 837 158 203 125
4 194 304	22	0 000 000 238 418 579 101 562 5
8 388 608	23	0 000 000 119 209 289 550 781 25
16 777 216	24	0 000 000 059 604 644 775 390 625
33 554 432	25	0 000 000 029 802 322 387 695 312 5
67 108 864	26	0 000 000 014 901 161 193 847 656 25
134 217 728	27	0 000 000 007 450 580 596 923 828 125
268 435 456	28	0 000 000 003 725 290 298 461 914 062 5
536 870 912	29	0 000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0 000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0 000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0 000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0 000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0 000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0 000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0 000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0 000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0 000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0 000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0 000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0 000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0 000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0 000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0 000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0 000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0 000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0 000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0 000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0 000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0 000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0 000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0 000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0 000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0 000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0 000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5

APPENDIX G

OCTAL REPRESENTATION FOR COMMON CONSTANTS

Miscellaneous Constants	Decimal	Octal
$\sqrt{2}$	1. 414 213 562 4	1. 324 047 463 201
$\sqrt{3}$	1. 732 050 807 6	1. 566 636 564 132
$\sqrt{5}$	2. 236 067 977 5	2. 170 673 633 460
$\sqrt{6}$	2. 449 489 742 8	2. 346 107 024 023
$\sqrt{7}$	2. 645 751 311 1	2. 512 477 651 650
$\sqrt{8}$	2. 828 427 124 8	2. 650 117 146 402
$\sqrt{10}$	3. 162 277 660 2	3. 123 054 072 667
π	3. 141 592 653 6	3. 110 375 524 211
2π	6. 283 185 307 1	6. 220 773 250 413
$1/\pi$	. 318 309 886 2	. 242 763 015 564
$1/2\pi$	. 159 154 943 1	. 121 371 406 672
$1^o=1/360$ of a circle	. 002 777 777 8	. 001 330 133 015
e	2. 718 281 828 5	2. 557 605 213 053
$1/e$	. 367 879 441 2	. 274 265 306 615
$\log_{10}e$	. 434 294 481 9	. 336 267 542 512
$\log_e 10$	2. 302 585 093 0	2. 232 730 673 533
$\log_e 2$	. 693 147 180 6	. 542 710 277 600
$\log_{10}\pi$	. 497 149 872 7	. 376 424 666 307
$\log_e \pi$	1. 144 729 885 8	1. 112 064 044 344