TO: DISTRIBUTION

FROM: P. MICHIENZI

DATE: JANUARY 23, 1986

SUBJ: **SPECIFICATION FOR 1/4" TAPE DRIVE CONTROLLER**

Attached is a preliminary 1/4" tape drive controller specification. Please review and return any comments to me by February 6, 1986.

Thanks,

Pete

DISTRIBUTION:
Fred Hayes
Phil Goldman
Ric Plummer
Jenny Ryan
John Cameron
Jim Stair
Phil Schreibman
Bob Angelini
Lary Gravett
Kim Cabot
Mike Feldstein
Don Carson
Bob Houde

REVISIONS			
REV	ECO	APP.BY	DATE

DRAWN
P. MICHIENZI

CHECKED
J. RYAN

ENGINEER
P. MICHIENZI

FIRST USED ON

APOLLO COMPUTER INC.

TITLE

CONTROLLER - QIC-36, 1/4" TAPE

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

TABLE OF CONTENTS

1.0 INTRODUCTION

This document specifies the functional, electrical, physical, reliability and certification requirements for a 1/4" tape controller which interfaces a QIC-36, 1/4" cartridge tape drive (basic interface) to an IBM PC -XT/AT, QIC-02 I/O structured compatible system. The tape controller will be used in Apollo's Domain Series DN3000 System.

The Apollo part number for the DN3000 1/4" Tape controller is 008845-001.

This document is both a purchase specification which the vendor must adhere to and a product or functional specification used as a reference for systems integrators and programming engineers. Sections 11.0 through 13.0 of this document designate the theory of operation, programming and systems software information which are to be used for reference and general knowledge only.

2.0 REFERENCE DOCUMENTS

2.1 Industry Standards and Vendor Documents

2.1.1 "1/4 - Inch Cartridge Tape Drive Basic Interface" Quarter -Inch Compatibility Committee, QIC-36 revision C, 9/14/84.

2.1.2 "Proposed Standard for Data Interchange on the Streaming 1/4" Magnetic Tape Cartridge using Group Code Recording at 10,000 FRCI". QIC-24, Revision D, April 22, 1983.

2.1.3 Specification - Archive Corp. SC-499 Tape controller information guide. (Preliminary)

2.1.4 "Specification - 1/4" Cartridge Tape Drive Interface Standard," QIC-02, Rev. D, Sept. 23, 1982.

2.1.5 Theory of Operation - Intelligent 1/4" Tape Drive, Archive Corp. #20100-001, Rev. C, August 16, 1982.

2.2 Apollo Documents

2.2.1 Specification - 1/4" Cartridge Tape Drive with QIC-36 (basic) Interface APN 008850.

2.2.2 Specification - Apollo DN3000 System I/O Bus. (Preliminary) Sept. 13, 1985.

3.0 ENVIRONMENTAL SPECIFICATIONS

3.1 Operational Environment

The 1/4" Tape controller shall be capable of operating under any combination of the following conditions without failure to meet all of the requirements of this document.

Ambient Temperature:	5 Degrees C. to 60 Degrees C. (41 Degrees F. to 140 Degrees F.)
Relative Humidity:	0% to 99% (Non-Condensing)
Wet Bulb Temperature:	26 Degrees C. Maximum (78.8 Degrees F. Max.)
Temperature Gradient:	1 Degree C. Per minute maximum (33.8 Degree F. per minute Max.) 20 Degrees C. per hour Max. without condensation (68 Degrees F. per hour Max.)
Altitude:	-1000 to 15,000 feet above sea level
Vibration: (Apollo DN3000 system mounting configuration)	0 - 63 Hz, 0.0005 inches max. Peak to Peak displacement. 63 - 500Hz, 1.0G Peak Maximum Acceleration.
Shock: (Apollo DN3000 system mounting configuration)	2.5G Peak Max. (1/2 Sine Wave, 11 msec duration on any axis)

3.2 Non-Operating (Unpackaged) Environment

The 1/4" Tape controller shall be capable of withstanding any combination of the following conditions in a powered off state without damage or degradation of life expectancy.

Ambient Temperature:	-30 Degrees C. to 60 Degrees C) (-22 Degrees F to 140 Degrees F)
Relative Humidity:	0% to 99% (Non-Condensing)
Wet Bulb Temperature:	26 Degrees C. Maximum (78.8 Degrees F. Max.)
Temperature Gradient:	30 Degrees C. Per hour max. without condensation (86 Degrees F. Per hour max.)
Altitude:	-1000 to 15,000 feet above sea level 1 hour min. exposure unpackaged.
Vibration: (Apollo DN3000 system mounting configuration)	0 - 17 Hz. 0.1 inches max. Peak to Peak displacement. 17 - 500 Hz, 1.5G Peak Max. Acceleration
Shock: (Apollo DN3000 system mounting configuration)	2.5G Peak Max. (1/2 Sine Wave, 11 msec duration on any axis)

3.3 PACKAGING

3.3.1 Electro-Static Protection (ESP)

The controller shall be packaged in anti-static material to prevent damage from electrostatic discharge.

3.3.2 Physical Stability

If the packaged controllers are shipped in a stacked configuration, the stack must be stable so as to permit safe transportation or movement of the packaged controllers by sliding in the intended direction of travel. The controllers in their shipping packages, will not be subject to tipping over when placed with any of the four base edges downward on a surface inclined at a 20 Degree angle. This applies to controllers packaged on a skid or pallet.

3.3.3 Mechanical Shock

The 1/4" Tape controller packaged as shipped in its cushioned shipping container must be able to resist damage resulting from random shock or impact for non-operating conditions.

This packaged controller shall be designed to withstand impacts resulting from flat drop free fall onto a concrete or equivalent floor as follows:

FREE FALL FLAT DROP TESTS

TOTAL PACKAGE WEIGHT	DROP HEIGHT
20 lbs or less (single controller)	36 inches
21 lbs to 40 lbs	30 inches
41 lbs to 80 lbs	24 inches

Each of the six package surfaces must withstand a minimum of one such impact, and the surface judged most vulnerable to shock input will experience three (3) impacts.

4.0 POWER SPECIFICATIONS

The voltages and currents required to operate the controller board, along with the applicable pin numbers of the J1 I/O connector are shown in Table 1.0.

J1 I/O PIN NUMBER	VOLTAGE	CURRENT	MAXIMUM RIPPLE
B03, B29	+5VDC +/-5% including ripple	1.0A Typical 1.25A Maximum	100 mv
B01, B10, B31	+5VDC/+12VDC Return		
B09	+12VDC +/-5% including ripple	.065A Typical .125A Maximum	500 mv to 10 KHz 200 mv beyond 10 KHz

Table 1.0

5.0 MECHANICAL SPECIFICATIONS

5.1 Dimensions

Width: 13.5 in (34.29CM)

Height: 4.2 in (10.67CM)

Weight: 0.6 lbs

5.2 I/O Bus Slot Location

The 1/4" Tape controller, consisting of a single printed circuit board, plugs directly into any I/O expansion slot of an Apollo DN3000 system. See Figure 1.0 for Controller I/O connector J1 location.

5.3 Controller Jumper Configurations

To avoid bus contention between the 1/4" tape controller and any other controller utilizing the I/O backplane in the DN3000 system. The tape controller must be configured as follows:

5.3.1 Device Address (Base Address) -0200 (HEX)

5.3.2 DMA Channel - 1

5.3.3 Interrupt Request Level - 5

Table 2.0 describes all jumper options and their functions along with the Apollo configurations designated by an asterik (*) and the configuration received from the vendor designated by a dot (•).

See Figure 1.0 for jumper locations.

TABLE 2.0 CONTROLLER JUMPER CONFIGURATION

DESCRIPTION	JUMPER LOCATION	OPTION
TAPE FORMAT	CC	IN = QIC-24 * ● OUT = QIC-11
TAPE SPEED	DD	OUT (90IPS) * ● FOR VENDOR USE ONLY
NUMBER OF TRACKS	Y	IN = 9 TRACKS * ● OUT = 4 TRACKS
POWER-ON CONFIDENCE TEST	KK	IN = TEST AT POWER-ON* ● OR RESET OUT = TEST DISABLED
I/O REGISTER BASE ADDRESS	A3 THRU A9 A3 THRU A8 = OUT* ● A9 = IN* ●	IN = ADDRESS BIT TRUE OUT = ADDRESS BIT FALSE NOTE: BASE ADDRESS IS SELECTABLE FROM 0 TO 3F8 HEX ON 8-BYTE BOUNDARIES.
DMA PRIORITY LEVEL (SELECT ONE PAIR)	DRQ1, DACK1 DRQ2, DACK2 DRQ3, DACK3	BOTH IN = PRIORITY LEVEL 1* ● BOTH IN = PRIORITY LEVEL 2 BOTH IN = PRIORITY LEVEL 3
INTERRUPT PRIORITY	IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7	IN = PRIORITY LEVEL 2 ● IN = PRIORITY LEVEL 3 IN = PRIORITY LEVEL 4 IN = PRIORITY LEVEL 5* IN = PRIORITY LEVEL 6 IN = PRIORITY LEVEL 7
LOOP ON ERROR MAINTENANCE	FF C	OUT* ● (FOR VENDOR USE ONLY) OUT* ● (FOR VENDOR USE ONLY)
TEST CONFIGURATION	HH	OUT* ● (FOR VENDOR USE ONLY)
NO DESCRIPTION	NN	OUT* ● (FOR VENDOR USE ONLY)
READY INTERRUPT DISABLE " " "	RR RR	OUT ● READY ENA IN* READY DISABLED - NOT ON INT. - OR - READY ENA - WHEN DONE INT DISABLED

● As-Shipped Configuration from vendor

* Apollo Configuration

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

6.0 FUNCTIONAL SPECIFICATIONS

6.1 General

6.1.1 The appropriate manufacturer's specifications contain information which must be used in conjunction with the specifications covered in this document. In case of conflict, Apollo specifications shall be in force.

6.1.2 The 1/4" Tape controller shall meet all of the requirements of this document while utilizing 1/4" tape drives which comply with the specifications for Apollo part number 008850, and will electrically interface to a QIC-02 command set compatible Apollo DN3000 system I/O bus.

6.2 Command Set

The controller shall utilize the QIC-02 standard command set as follows:

Select, Soft Lock Off	H'01'
Select, Soft Lock On	H'11'
BOT	H'21'
Erase	H'22'
Retension	H'24'
Select Q11 Format	H'26'
Select Q24 Format	H'27'
Write	H'40'
Write File Mark (WFM)	H'60
Read	H'80'
Read File Mark (RFM)	H'A0'
Read Status	H'C0'

6.3 Performance

Tape drives controlled	1
Transfer rate	90KB/sec
Recording tracks	9 track serpentine
Recording Code	(0,2) Run length limited, GCR
Data Buffering	3 x 512 Byte blocks minimum
Write/Read re-tries	16 maximum
Error detection	CRC (standard)

6.4 Diagnostics/Led's

6.4.1 Power-On Confidence test (POC)

The controller level diagnostics are located physically on the board in PROM. They are activated when power is applied or when a reset command is issued from the host.

A POC test or controller initialization occurs automatically when power is applied or when a reset command is issued. This test includes sub-tests of the following:

*Microprocessor Internal Ram and Basic Instructions

*LSI controller operation

*16K Ram Ic

*Data Separator Logic (discrete)

Successful completion of the above tests are reported to the host by the assertion of EXC-(from status register) within five secs. If EXC-is not asserted within this time a failure is indicated.

Each logic group except the microprocessor has an associated Led diagnostic indicator as follows:

*DS1-LS1 Controller chip

*DS2-16K Ram bufffer logic

*DS3-Data Separator logic

*DS4,DS5 - Not Used

Successful completion of all tests is indicated by a single blink of all five Led's following the off period during which the tests are performed. Each time a test fails the associated Led blinks and the test is repeated; hence, a blinking indicator is a visual indication of the area of failure. If the microprocessor fails the results are unpredictable.

7.0 HOST INTERFACE SPECIFICATIONS

The 1/4" tape controller will be electrically and mechanically compatible with the IBM PC XT/AT I/O structured DN3000 system, use DMA for data transfer and respond to the standard QIC-02 command set.

In general the controller will meet all of the requirements of the specifications referenced in Sections - 2.1.4 and 2.1.5 of this document.

7.1 Host Interface Signal Level

All signals to the host are standard tri-state TTL levels as follows:

False = High = 2.4 to 5.25 VDC

True = Low = 0 to 0.8 VDC

Off = High Impedance State

Voltages shall be measured at the controller connector - J1

7.2 Signal Loading

Signal from the host to the controller are loaded by not more than 2.0MA. Command, address, DMA and Interrupt request lines drive into not more than PAL1628A or equivalent inputs. The data lines drive into a single low power schottky (LS) input.

7.3 I/O Connector

The controller interfaces to the DN3000 system via card edge connector J1. The connector has 62-pins and mates to the 62-pins host system I/O bus connector with 100-MIL card tab spacing.

7.4 I/O Pin Assignments

Table 3.0 summarizes Pin Assignments for the I/O bus connector – J1.

TABLE 3.0 – I/O CONNECTOR J1 SIGNAL DESCRIPTIONS

PIN	NAME	DESCRIPTION
A02	DB7	DATA BUS BIT 7
A03	DB6	DATA BUS BIT 6
A04	DB5	DATA BUS BIT5
A05	DB4	DATA BUS BIT 4
A06	DB3	DATA BUS BIT 3
A07	DB2	DATA BUS BIT 2
A08	DB1	DATA BUS BIT 1
A09	DB0	DATA BUS BIT 0
A11	AEN	ADDRESS ENABLE
A12 THRU A31	A19 THRU A00	SYSTEM ADDRESS BUS
B02	RESET DRV	RESET DRIVE
B18	DRQ1	DMA REQUEST PRIORITY LEVEL 1
B06	DRQ2	DMA REQUEST PRIORITY LEVEL 2
B16	DRQ3	DMA REQUEST PRIORITY LEVEL 3
B17	/DACK1	DMA ACKNOWLEDGE PRIORITY LEVEL 1
B26	/DACK2	DMA ACKNOWLEDGE PRIORITY LEVEL 2
B15	/DACK3	DMA ACKNOWLEDGE PRIORITY LEVEL 3
B13	/IOW	I/O WRITE
B14	/IOR	I/O READ
B04	IRQ2	INTERRUPT REQUEST PRIORITY LEVEL 2
B25	IRQ3	INTERRUPT REQUEST PRIORITY LEVEL 3
B24	IRQ4	INTERRUPT REQUEST PRIORITY LEVEL 4
B23	IRQ5	INTERRUPT REQUEST PRIORITY LEVEL 5
B22	IRQ6	INTERRUPT REQUEST PRIORITY LEVEL 6
B21	IRQ7	INTERRUPT REQUEST PRIORITY LEVEL 7
B27	T/C	TERMINAL COUNT
B30	OSC	OSCILLATOR (14.31818 MHZ CLOCK)

NOTE: Refer to Section 11.0 for I/O Signal Descriptions

8.0 TAPE DRIVE INTERFACE SPECIFICATIONS

8.1 General

The 1/4" Tape controller must allow interfacing to a QIC-36 (basic interface) compatible 1/4" cartridge tape drive which is internally mounted with the controller in the DN3000 system.

Interconnections from drive to controller are made via a card-edge connector on the drive.

The drive to controller interface cable is a 3M-3365, 50-wire flat cable with CA-50, IDS socket.

Maximum interface cable length is 10 ft. See figure 1.0 for location of drive interface connector J2.

The 1/4" tape drive which interfaces to the 1/4" tape controller must meet the requirements of specifications referenced in Sections 2.1.1 and 2.2.1 of this document to operate correctly in the Apollo DN3000 system.

8.2 Interface Signal Levels

All Interface signals between the basic tape drive and the controller are TTL logic levels as defined below:

Signal True = Logic 1 (Low) 0.00 to 0.55 VDC

Signal False = Logic 0 (High) 2.40 to 5.25 VDC

8.3 Signal Loading

All Signals from the tape drive to the controller are capable of driving one standard TTL load in addition (1.6mA) in addition to the 23mA required by the tape drive interface terminations. Refer to the specifications in sections 2.1.1 and 2.1.5 of this document.

8.4 Signal Terminations

All Signals between the controller and the tape drive must be terminated with 330 ohms +/-5% to ground and 220 ohms +/-5% to 5VDC.

Signal inputs to the controller must be terminated at the controller. Signal outputs from the controller are terminated in the tape drive. Figure 2.0 shows the signal termination scheme.

8.5 Pin Assignments

Table 4.0 identifies the tape drive/controller interface signals. This signal interface is pin and plug compatible with the QIC-36 interface standard (See Section 2.1.1) except as noted.

CONNECTOR J3 PIN ASSIGNMENTS/SIGNAL DESCRIPTIONS

TABLE 4.0

PIN	NAME	TO*	DESCRIPTION
02	GO-	D	GO. MOTION CONTROL FOR CAPSTAN SERVO.
04	REV-	D	REVERSE. DIRECTION CONTROL FOR CAPSTAN SERVO
06	TR3-	D	TRACK SELECT BIT 3 (MSB).
08	TR2-	D	TRACK SELECT BIT 2
10	TR1-	D	TRACK SELECT BIT 1.
12	TR0-	D	TRACK SELECT BIT 0 (LSB).
14	RST-	D	RESET. CAUSE DRIVE TO PERFORM INITIALIZATION AND HEAD RECALIBRATION
22	DS0-	D	DRIVE SELECT.
24	■HC-	D	HIGH CURRENT. ENABLES OPERATION WITH ALTERNATE TAPE TYPE. (DC600A).
26	RDP-	C	READ DATA PULSE. READ DATA IS PRESENT AT THE DRIVE INTERFACE.
28	UTH-	C	UPPER TAPE HOLE.
30	LTH-	C	LOWER TAPE HOLE.
32	• SLD-	C	RESPONSE FROM DRIVE WHEN SELECTED.
34	CIN-	C	CARTRIDGE IN. TAPE CARTRIDGE IN PLACE.
36	USF-	C	UNSAFE. SAFE PLUG ON CARTRIDGE IS IN THE UNSAFE POSITION, I.E. WRITING IS ENABLED.
38	TCH-	C	TACHOMETER. CAPSTAN TACHOMETER PULSES.
40	WDA-	D	WRITE DATA.
42	WDA+	D	INVERSE OF WRITE DATA SIGNAL.
44	•THD-	D	THRESHOLD - INVOKES A PERCENTAGE QUALIFYING AMPLITUDE FOR THE READ SIGNAL OFF TAPE.
46	HSD-	D	HIGH SPEED DRIVE. TAPE SPEED = 90 IPS.
48	WEN-	D	WRITE ENABLE.
50	EEN-	D	ERASE ENABLE.

*C = CONTROLLER
D = DRIVE

■ The controller shall discriminate between DC300XL and DC600A cartridges by measurement of BOT to load distance and shall select the appropriate basic drive write current.

• These signals are not present on the controller drive interface connector J3.

9.0 AGENCY COMPLIANCE

The 1/4" tape controller shall conform to the following certification requirements.

9.1 Safety

U.L. - recognized by U.L. and meet 94 V-0 flammability rating.

CSA - certified by Canadian Standards Association (CSA) as a component.

9.2 Emissions

FCC - Tested for compliance with FCC Class B, Part 15, Subchapter J and VDE Standard 0871 for radio frequency emissions, when installed in an Apollo system.

10.0 RELIABILITY AND LIFE

10.1 MTBF

The calculated MTBF for the 1/4" Tape controller shall be a minimum of 400,000 power on hours, using accepted calculation methods for a benign environment.

10.2 Life

The minimum life expectancy of the controller shall be 5-years.

10.3 Error Rates

The controller is expected to have a read data reliability rate: When connected to Apollo 1/4" Tape drive #008850 and utilizing Apollo 1/4" tape cartridge 004634 as follows:

Recoverable (Soft) error rate - No more than 1 in 10E8 bits

Non-Recoverable (Hard) error rate - No more than 1 in 10E10 bits.

11.0 THEORY OF OPERATIONS

This section is for reference only. It describes the major functions of the controller including a block diagram, I/O signal descriptions, I/O port assignments, control/status registers, DMA channel, interrupt priority level and resets.

For more information describing the controller and QIC-02 based I/O registers refer to the specifications listed in sections 2.1.4 and 2.1.5 of this document.

11.1 Block Diagram Descriptions

The microprocessor based 1/4" tape controller performs the function of an intelligent streaming tape controller. In the write mode, it accepts data from the host, formats it into blocks, appends CRC, GCR encodes the data and writes it to tape. The controller performs a read after write data check using the appended CRC to insure data integrity. In the read mode, the controller reads data from tape, GCR decodes the data, checks the CRC and sends the data to the host.

See Figure 3.0 for block diagram of the controller circuitry.

Following is a functional description of the controller:

(To be supplied)

11.1.1 Register Base Address Decoder

11.1.2 Register Select

11.1.3 DMA Control

11.1.4 Interrupt Control

11.1.5 Control Status

11.1.6 Data Register

11.1.7 Microprocessor

11.1.8 Host Data Sequencer

11.1.9 Buffer Memory Control

11.1.10 Data Buffers

11.1.11 Write Data Sequencer

11.1.12 Read Data Sequencer

11.1.13 PLL

11.2 I/O Signal Descriptions

Following is a description of the I/O channel signals present on the controller I/O bus connector – J1.

SIGNAL	I/O	DESCRIPTION
OSC	O	Oscillator: High-Speed clock with a 70-NS period (14.31818 MHz). It has a 50% duty cycle.
Reset Drv	O	This line is used to reset or initialize system logic upon power-up or during a low line voltage outage. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. A0 is the least significant bit (LSB) and A19 is the most significant bit (MSB). These lines are generated by either the processor or DMA controller. They are active high.
D0-D7	O	Data bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory and I/O devices. D0 is the least significant bit (MSB). These lines are active high.
IRQ2-IRQ7	I	Interrupt request 2 to 7: These lines are used to signal the processor that an I/O device requires attention. They are prioritized with IRQ2 as the highest priority and IRQ7 as the lowest. An interrupt request is generated by raising an IRQ line (low to high) and holding it high until it is acknowledged by the processor. (Interrupt service routine).

IOR	O	-I/O read command: This command line instructs an I/O device to drive its data onto the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
IOW	O	-I/O write command: This command line instructs an I/O device to read the data on the data bus. It may be driven by the processor or the DMA controller. This signal is active low.
DRQ1-DRQ3	I	DMA request 1 to 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. They are prioritized with DRQ3 being the lowest and DRQ1 being the highest. A request is generated by bringing a DRQ line to an active level (High). A DRQ line must be held high until the corresponding dack line goes active.
DACK0 - DACK3	O	-DMA acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3) and to refresh system dynamic memory (DACK0). They are active low.
AEN	O	Address Enable: This line is used to De-gate the processor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active (high), the DMA controller has control of the address bus, data bus, read command lines (memory and I/O), and the write command lines (memory and I/O).
T/C	O	Terminal Count: This line provides a pulse when the terminal count for any DMA channel is reached. This signal is active high.

11.3 I/O Port Assignments (Base Address)

The I/O Registers occupy eight adjacent locations in the systems I/O address map. Only four of the address locations are used by the 1/4" tape controller.

Note: The jumper-selectable base address is factory-set at 200 HEX.

See Table 2.0 for details

11.3.1 Data/Command Register: Base Address +0
(Read or Write)

11.3.2 Control Register (Write Only): Base Address +1
Status Register (Read Only).

11.3.3 Start DMA (DMAGO): Base Address +2. Any Write to this Register will cause DMAGO to be active.

11.3.4 Reset DMA (RSTDMA): Base Address +3. Any Write to this Register will cause RSTDMA to be active.

11.4 Control/Status Register Descriptions

11.4.1 Control Register (Write)

Bit 7	1 = RSTSAC	Reset Controller Microprocessor
Bit 6	1 = REQ	Request to LSI Chip
Bit 5	1 = IEN	Enables interrupts IEN = 0, Masks Interrupts
Bit 4	1 = DNIEN	Enables Done Interrupt DNIEN = 0, Masks done interrupt.

(Bits 0–3 Not Used)

11.4.2 Status Register (Read)

Bit 7	0 = IRQF	Interrupt request flag, ORING of RDY and EXC, and done if DNIEN is set.
Bit 6	0 = RDY	Ready, From LSI Chip.
Bit 5	0 = EXC	Exception, from LSI Chip
Bit 4	1 = DONE	Done, From DMA logic
Bit 3	1 = DIRC	Direction, indicates direction of bus is from controller to I/O bus.

(Bits 0–2 Not Used)

11.5 DMA Channel

The tape controller uses the systems I/O bus DMA controller to transfer data to and from the system main memory. The DMA channel is also jumper-selectable (See Table 2.0).

The tape-controller DMA logic can be initialized by writing to address location base +3 (RSTDMA). RSTDMA initializes the DMA sequencer, clears all control register bits to 0, and sets done to 1 (Power-on reset from the system performs the same functions). The following sequence may be used to start DMA transfer:

1. Issue a transfer command to the tape controller.
2. Set up the DMA controller's register (But leave the mast bit set).
3. Write (any value) to the tape controller register at base address +2 (DMAGO)
4. Clear the mask bit in the 8237 DMA controller.
5. Repeat above from Step 2 for each subsequent block.

11.6 Interrupt Priority Level

The controller interrupt priority level is jumper-selectable (See Table 2.0) each interrupt source bit, RDY, EXC, and DONE (See Status Register - Section 11.4.2), can be read through the status register regardless of the state of the interrupt masks: IEN = 0, DNIEN = 0, (See Control Register - Section 11.4.1). The IRQ line is tri-stated when IEN is cleared. This allows other systems I/O bus options the use of that interrupt line when the tape controller is not using it. Therefore, the systems I/O bus interrupt controller should be programmed to respond to the tape controller's IRQF only after IRQ has been enabled by setting IEN.

Interrupts to the host will be caused for the following reasons:

1. After completion of any command when status is valid and ready to be checked.
2. A soft reset has been issued.
3. An exception condition occurs such as illegal command or an erroneous condition occurs during the operation of the tape drive while doing a command.

11.7 Resets

Four reset signals (Two DMA resets, and two microprocessor/tape drive resets) are available on the controller.

11.7.1 DMA Resets:

* RSTDMA. (RSTDMA is discussed in Section 11.5)
* Reset DRV. This is the power-on reset from the systems power supply, and performs the same functions as RSTDMA.

11.7.2 Microprocessor and Tape Drive Resets:

* Microprocessor reset. Reset the controller microprocessor when any of the following conditions occur:

  A. The +5V Supply drops below 4.6V.

  B. The +12V Supply drops below 9V.

  C. RSTSAC is set.

Note: Microprocessor reset will also cause a tape drive reset.

*RSTSAC. Activated by writing a 1 to control register bit 7. RSTSAC must be set, held for more than 25 usec, then cleared by either writing a 0 to control register bit 7 or by a RSTDMA.

12.0 PROGRAMMING INFORMATION

This section is for reference only. It describes the QIC-02 command set, programming flow charts, and maximum command timings. Refer to specifications listed in sections 2.1.4 and 2.1.5 of this document for additional information on command sequencing, status register sense bytes, QIC-24 tape format and command timing diagram descriptions.

12.1 Command Set Descriptions

12.1.1 Select, Soft Lock Off (0000 0001)

The select command selects the tape drive. The drive shall remain until changed by another select command or reset.

12.1.2 Select, Soft Lock On* (0001 0001)

This command is identical in function to the select, soft lock off command and additionally provides a soft lock on the cartridge. Execution of the select command or reset unlocks the cartridge.

12.1.3 Bot Command (0010 0001)

The BOT command positions the tape in the cartridge in the selected device to BOT (beginning of tape).

12.1.4 Retension Command (0010 0100)

The retension command shall be used in accordance with cartridge tape manufacturer's instructions. The retension command moves the tape in the device to BOT, then to EOT and then back to BOT.

12.1.5 Erase Command (0010 0010)

The erase command completely erases the tape in the selected drive. The erase command moves the tape in the device to BOT, activates the erase head and moves to EOT, deactivates the erase head and moves the tape back to BOT. The erase command also fulfills the requirements of initialization.

*Note: Softlock "On" enables the "Selected" LED of the tape drive and issues an exception status if the cartridge is removed during next command issued.

12.1.6 Write Command (0100 0000)

When the write command is issued the device requests and transfers data. The Ready line is activated when the device is ready for a data block transfer. When the ready line is active, the host terminates transfer of write data by issuing a write-file-mark command. Note: A write command following cartridge insertion or reset shall commence recording at BOT. Otherwise recording shall commence at the current tape position. NOTE: If the host starts transfer between blocks before ready is asserted, ready may not be asserted when the early warning hole of the last track is detected by the device, thus the device ceases to transfer additional data blocks from the host. The device terminates the write command and reports end of media by means of an exception and read status.

12.1.7 Read Command (1000 0000)

When the read command is issued the device transfer data. The ready line is activated when the device is ready for a data block transfer. The read command shall be terminated by the device if a file mark is detected. The host is informed by means of an exception and a read status sequence. When ready is true, the host may alternatively terminate the read command by issuing a read-file-mark command. If a read command is issued, the command is accepted and the drive continues reading. Note: A read command following cartridge insertion or reset shall commence at BOT, otherwise the read command commences from the current tape position. Note: If the host starts transfer between blocks before ready is asserted, ready may not be

12.1.8 Write-File-Mark Command (0110 0000)

The Write-File-Mark (WFM) command causes a file mark to be written on the tape in the selected drive. Note: A WFM command following cartridge insertion or reset shall commence recording at BOT, otherwise recording shall commence at the current tape position.

12.1.9 Read-File-Mark Command (1010 0000)

The Read-File-Mark (RFM) command causes the tape in the selected drive to be moved to the next file mark. Note: A RFM command following cartridge insertion or reset shall commence reading at the BOT, otherwise, reading shall commence at the current tape position.

12.1.10 Read Status Command (1100 0000)

The Read Status command provides the host with information about the selected device. The host issues the read status command. The device transfers the standard six bytes to the host.

12.1.11 Select Q11 Format Command (0010 0110)

The Select Q11 format command selects the QIC-11 format as the current format.

12.1.12 Select Q24 Format Command (0010 0111)

The Select Q24 format command selects the QIC-24 format as the current format.

12.2 Command Flow Charts

The Diagrams in Appendix A specify the flow of the command structures.

These flow charts are helpful for any software engineer who is designing a software driver. The flow charts in Appendix A are listed as follows:

	DESCRIPTION	FIGURE
12.2.1	Read File Flow Diagram	4.0
12.2.2	Write File Flow Diagram	5.0
12.2.3	Read File Mark Flow Diagram	6.0
12.2.4	Write File Mark Flow Diagram	7.0
12.2.5	Erase Command Flow Diagram	8.0
12.2.6	Initialize Cartraidge Command Flow Diagram	9.0
12.2.7	BOT Command Flow Diagram	10.0
12.2.8	Select Softlock Command Flow Diagram	11.0
12.2.9	Select Format Command Flow Diagram	12.0
12.2.10	Reset Flow Diagram	13.0
12.2.11	Done Flow Diagram	14.0
12.2.12	Read Status Flow Diagram	15.0
12.2.13	Send Command Flow Diagram	16.0

12.3 QIC-02 Command Maximum Timings

The maximum QIC-02 Command Set Timings before time-out conditions are generated are as follows:

12.3.1 Retension Command

450ft tape - 180 seconds

600ft tape - 241 seconds (Worst Case)

12.3.2 BOT Command

600ft tape - 1 min 20 sec.

12.3.3 Reset Command

5 Sec

12.3.4 Erase Command

4 Min

13.0 SYSTEMS SOFTWARE INFORMATION

This section is for referenced only. It describes the minimum revision levels for diagnostic tests and operating systems software support.

13.1 Diagnostic Level Test

The systems or device level diagnostic test is called CTAPE.DEX and is located in the SAU8 Directory on the DN3000 system disk. The minimum diagnostic revision level required is 1.0. The minimum required O.S. Level of AEGIS containing SAU8 Directory is SR9.2.1.

13.2 Operating Systems Software (AEGIS)

The 1/4" Cartridge tape controller will operate only in an Apollo DN3000 system backplane which utilizes QIC-02 command compatible I/O bus.

The DN3000 operating systems software which supports the 1/4" Tape controller functionality is located in the SAU8 directory on the systems disk. The minimum O.S. Revision level required is SR9.2.1.

Appendix A

– Command Flow Charts –

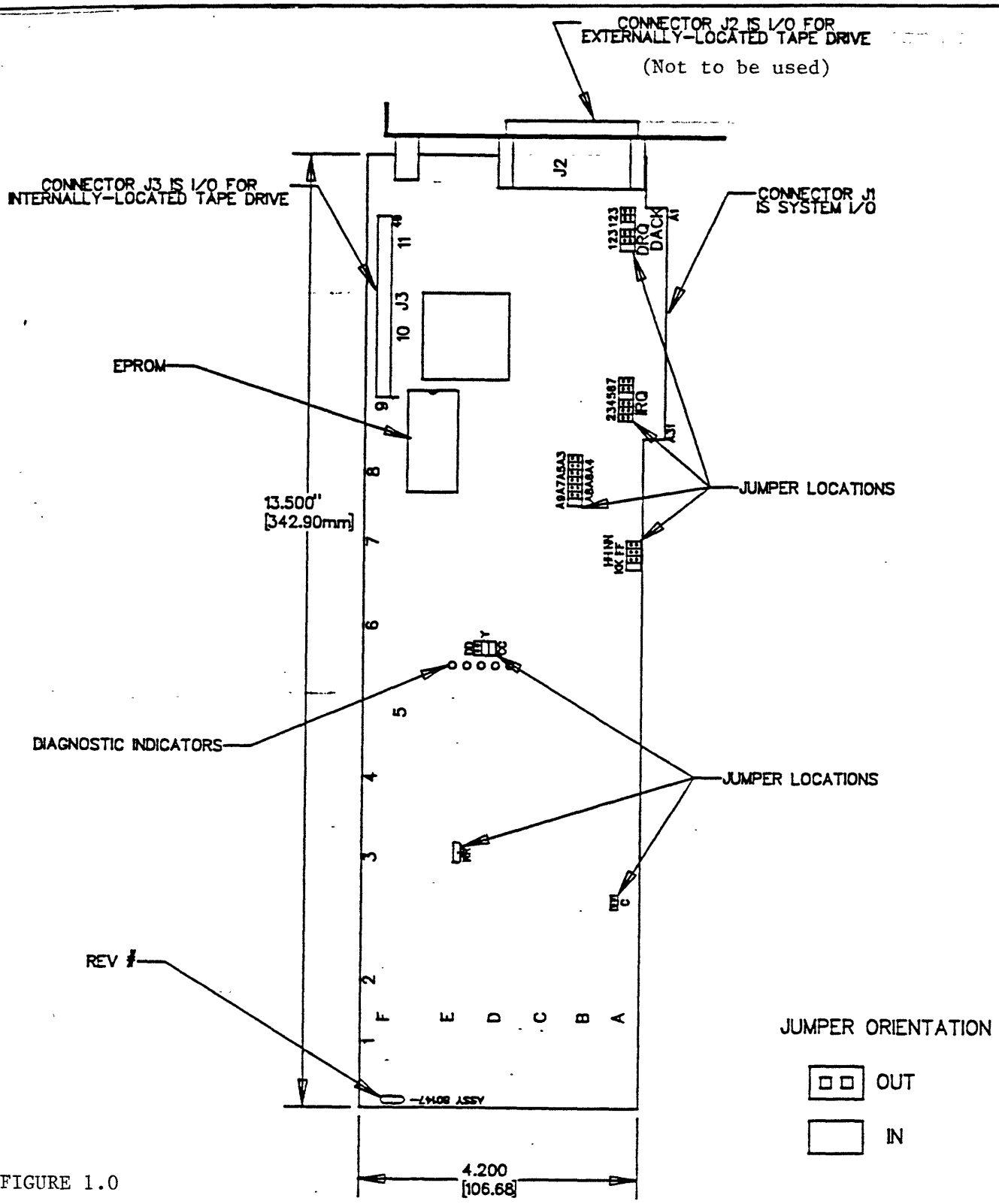


FIGURE 1.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

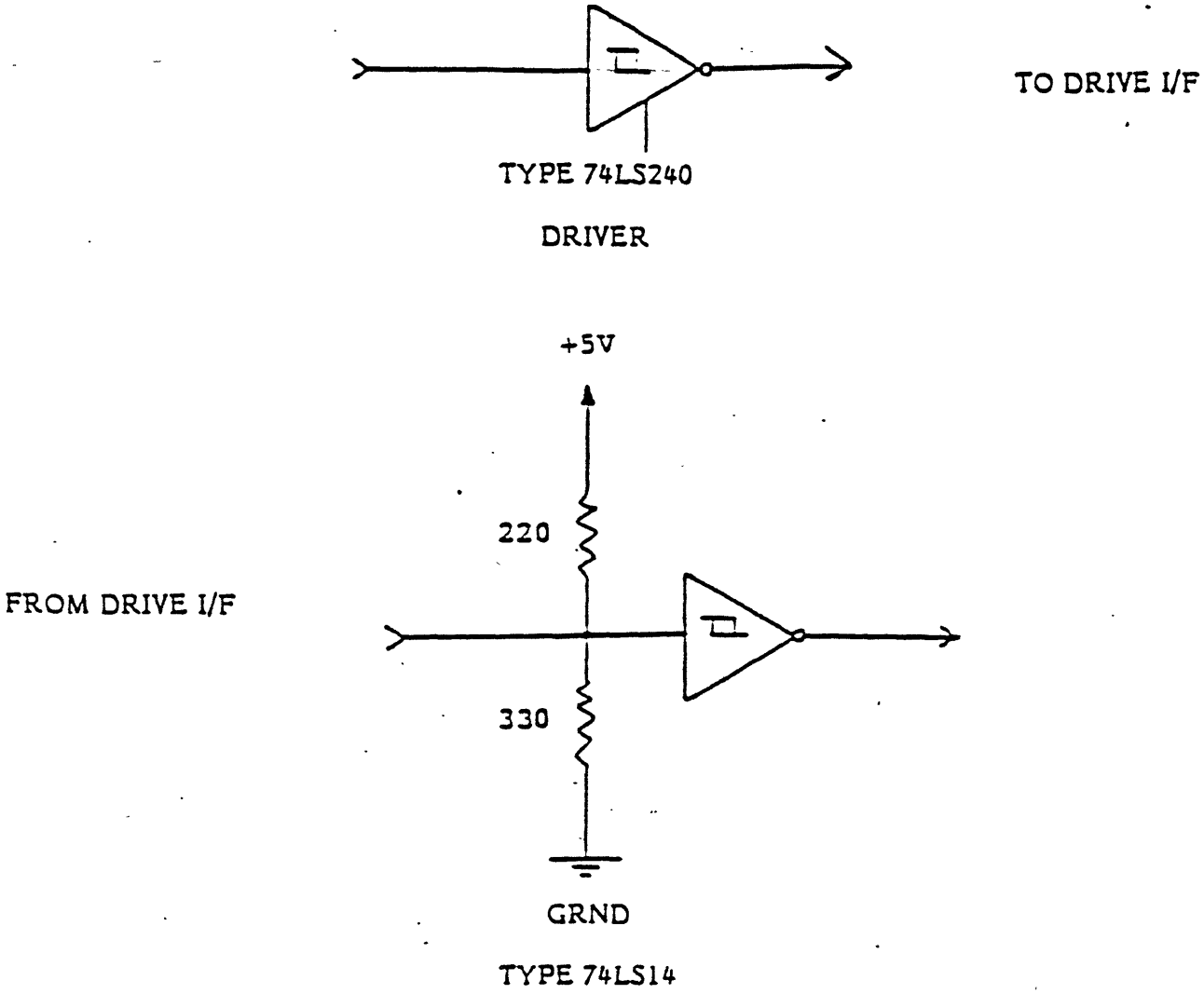
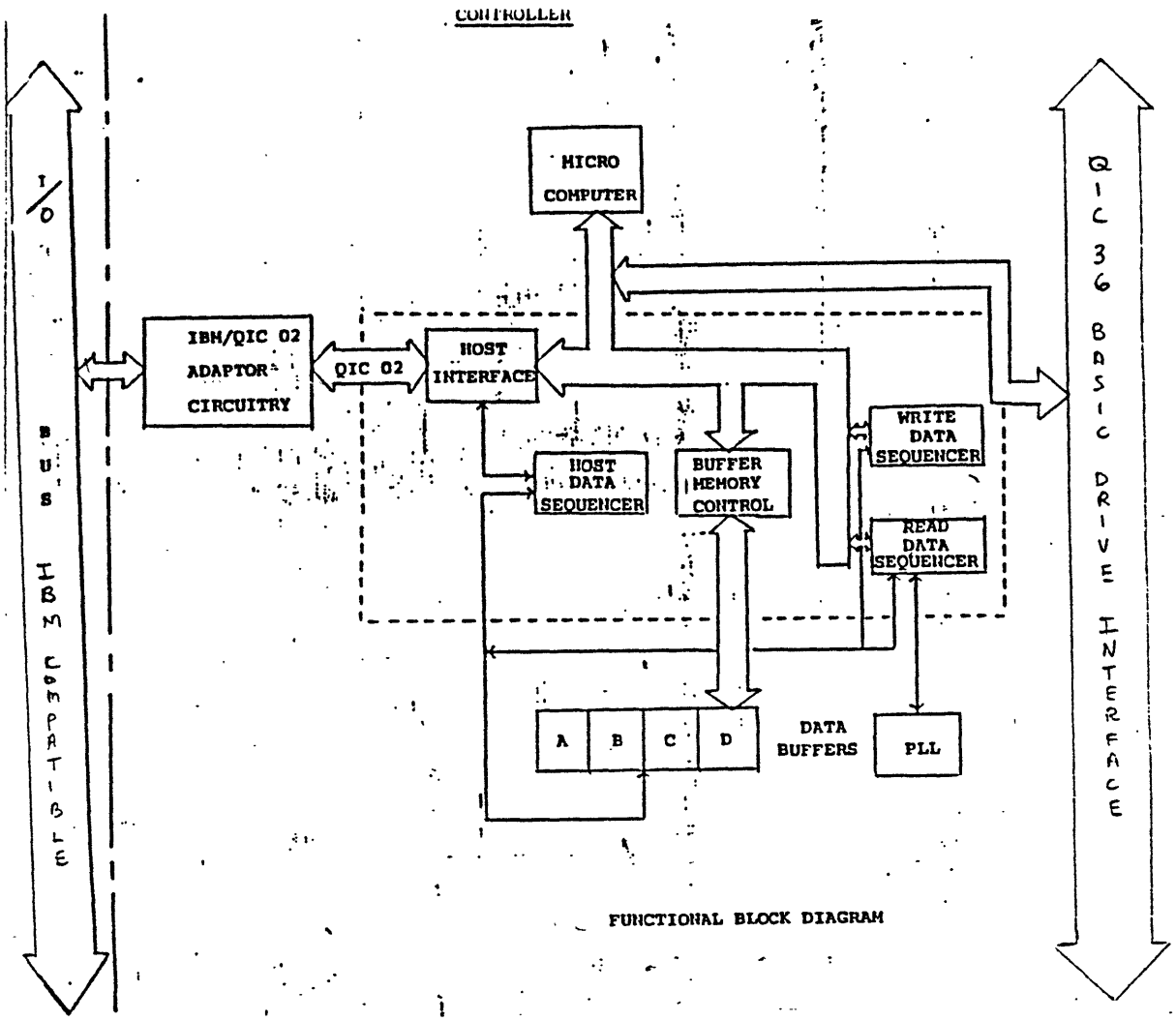


Figure 2.0 Interface Signal Termination

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0



FUNCTIONAL BLOCK DIAGRAM

FIGURE 3.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

READ FILE FLOW DIAGRAM

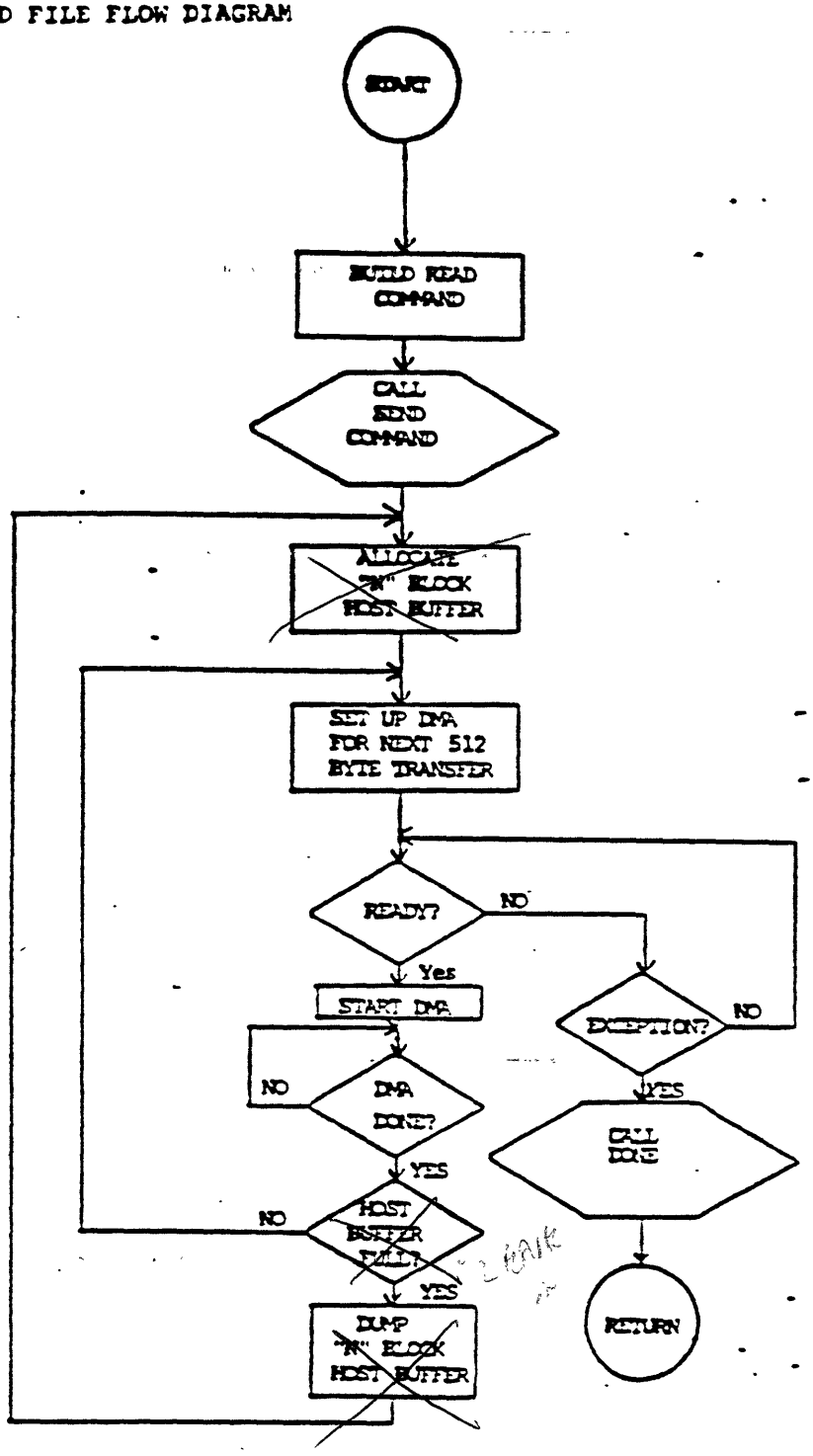


Figure 4.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

WRITE FILE FLOW DIAGRAM

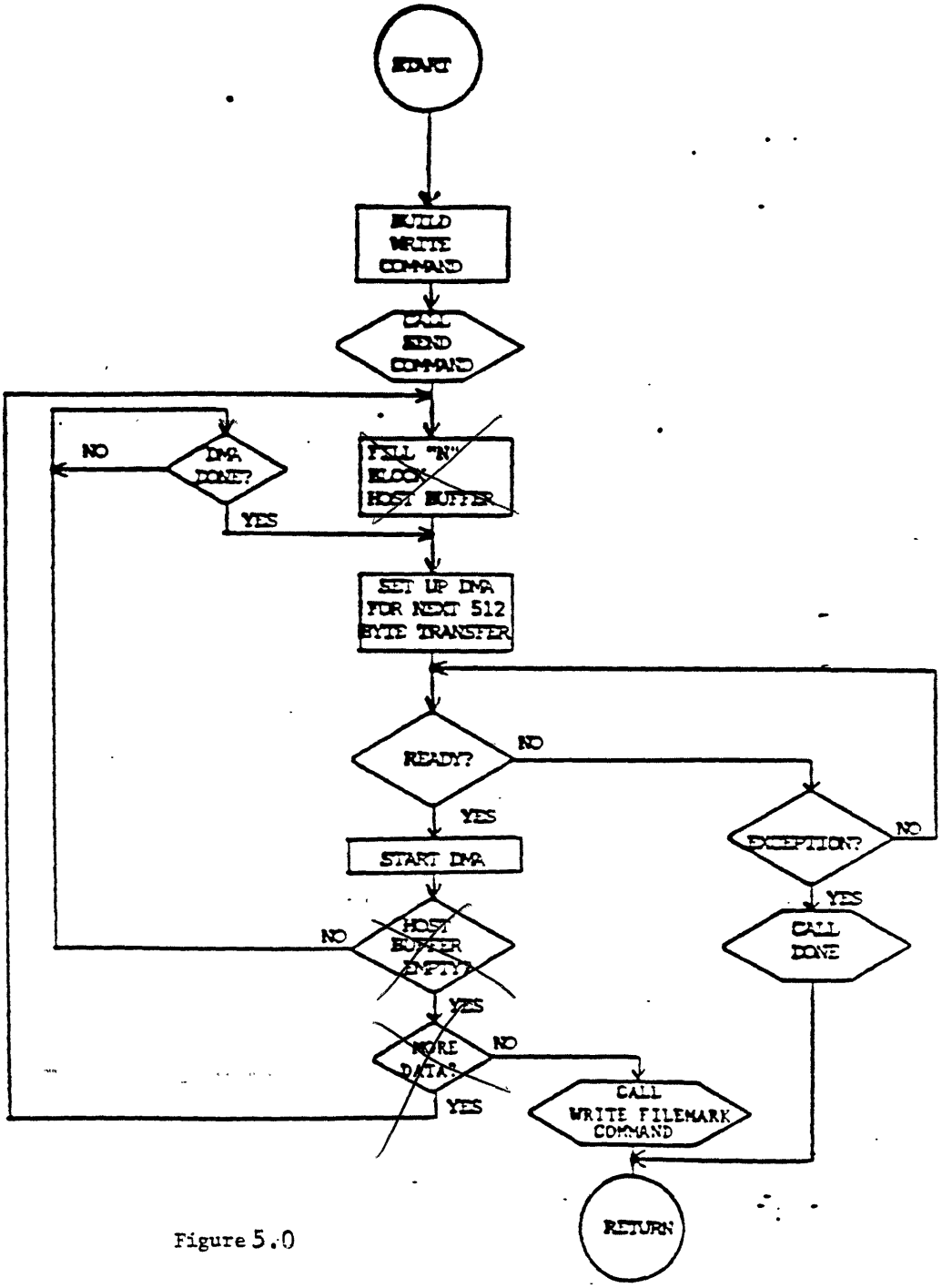


Figure 5.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

READ FILE MARK FLOW DIAGRAM

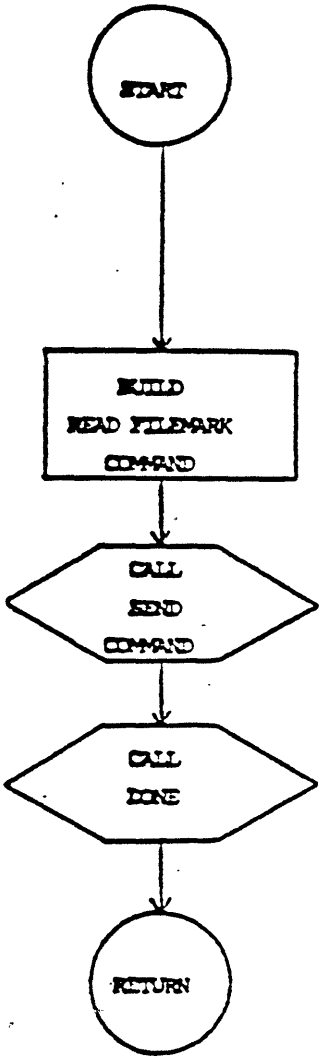


Figure 6.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

WRITE FILE MARK FLOW DIAGRAM

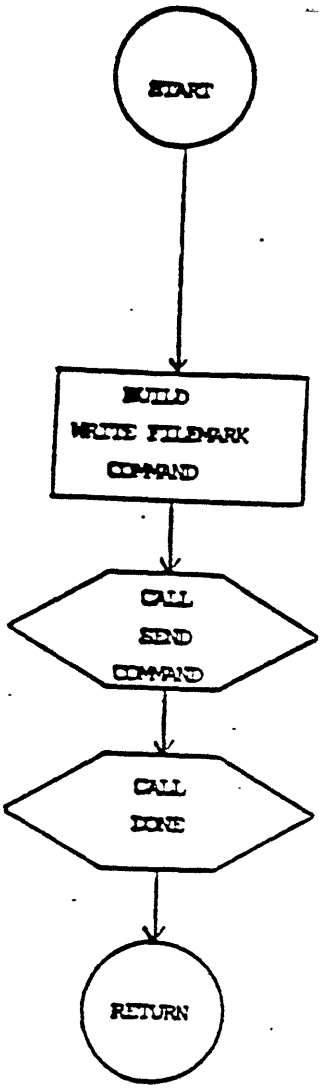


Figure 7.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

ERASE COMMAND FLOW DIAGRAM

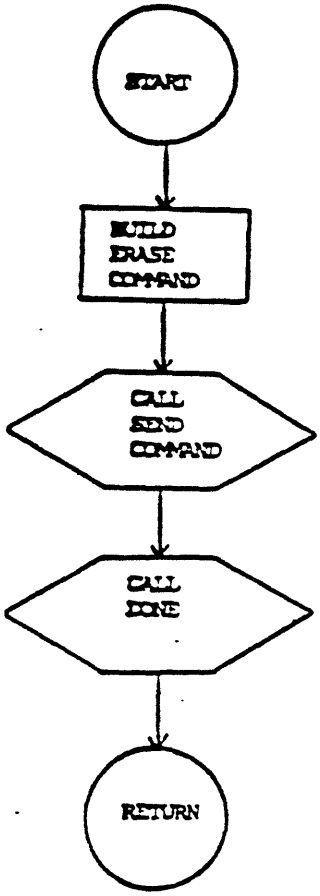


Figure 8.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

INITIALIZE CARTRIDGE COMMAND FLOW DIAGRAM

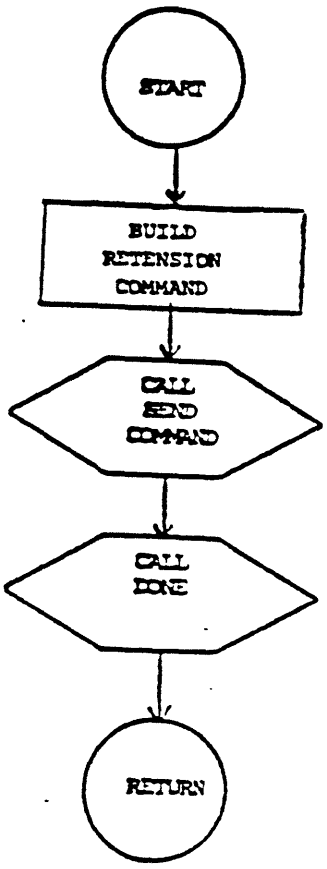


Figure 9.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

BOT COMMAND FLOW DIAGRAM

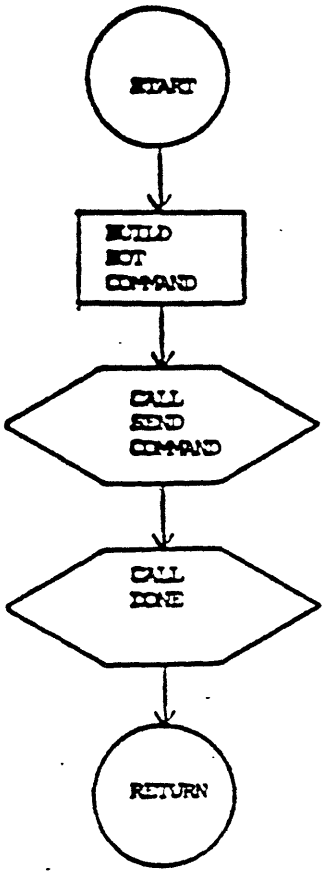


Figure 10.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

SELECT, SOFT LOCK COMMAND FLOW DIAGRAM

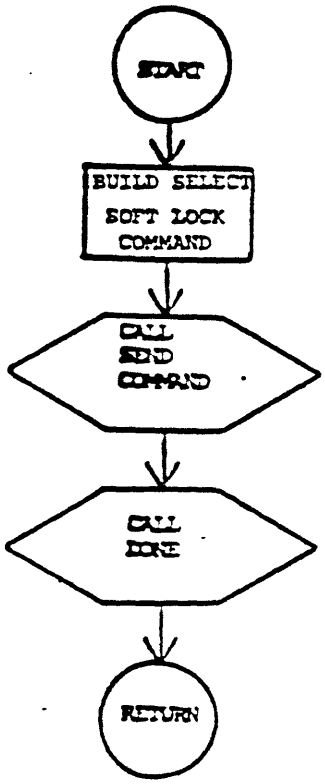


Figure 11.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

SELECT FORMAT COMMAND FLOW DIAGRAM

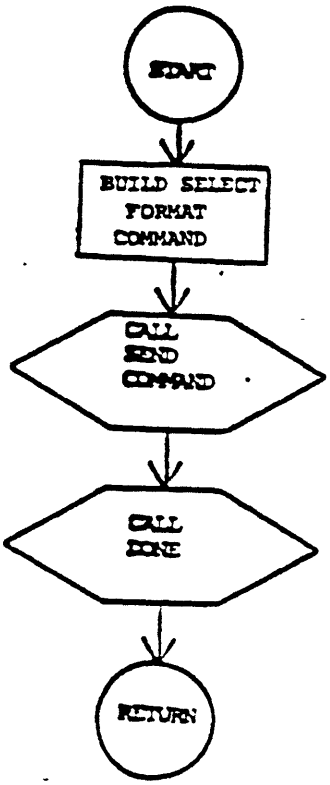


Figure 12.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

RESET FLOW DIAGRAM

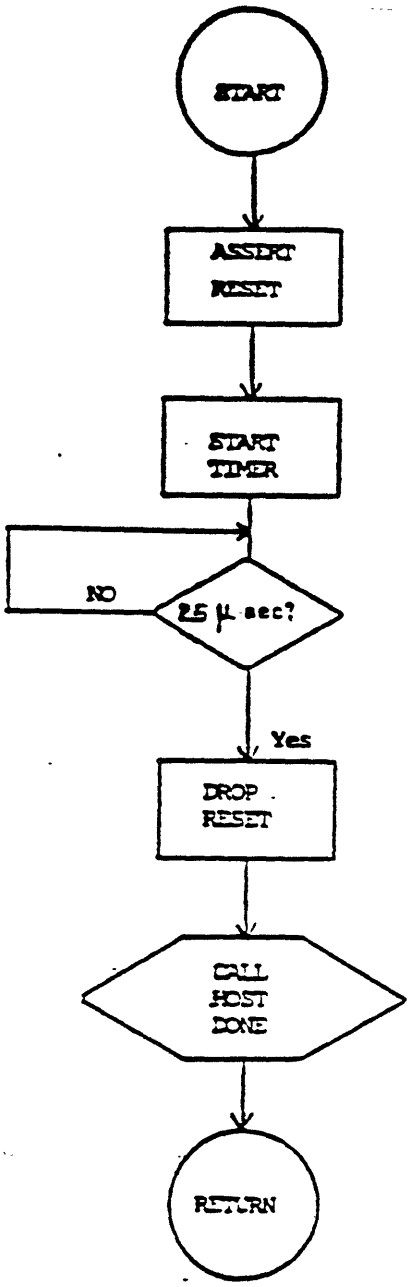


Figure 13.0

DONE FLOW DIAGRAM

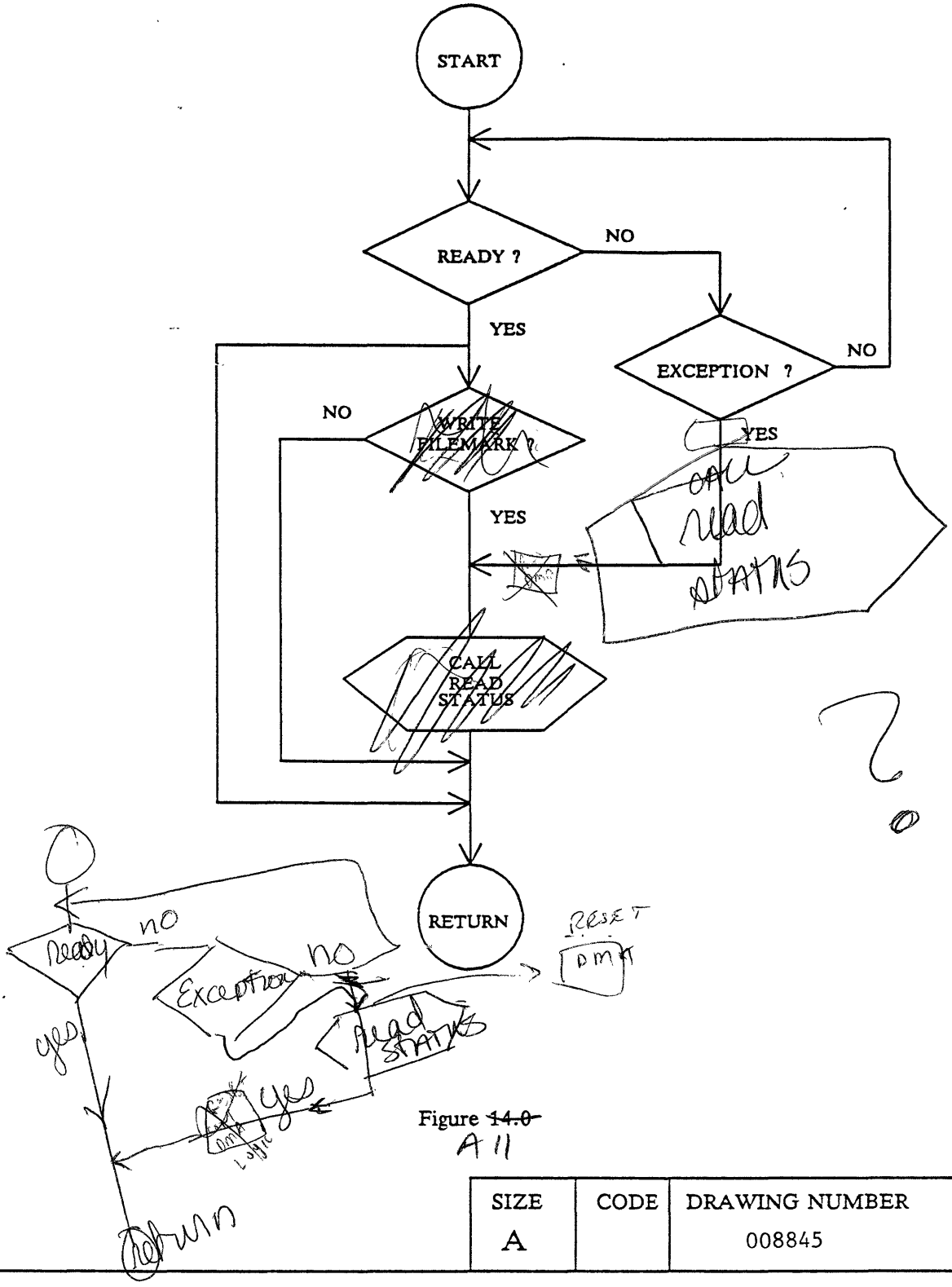


Figure ~~14.0~~
A11

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0

READ STATUS FLOW DIAGRAM

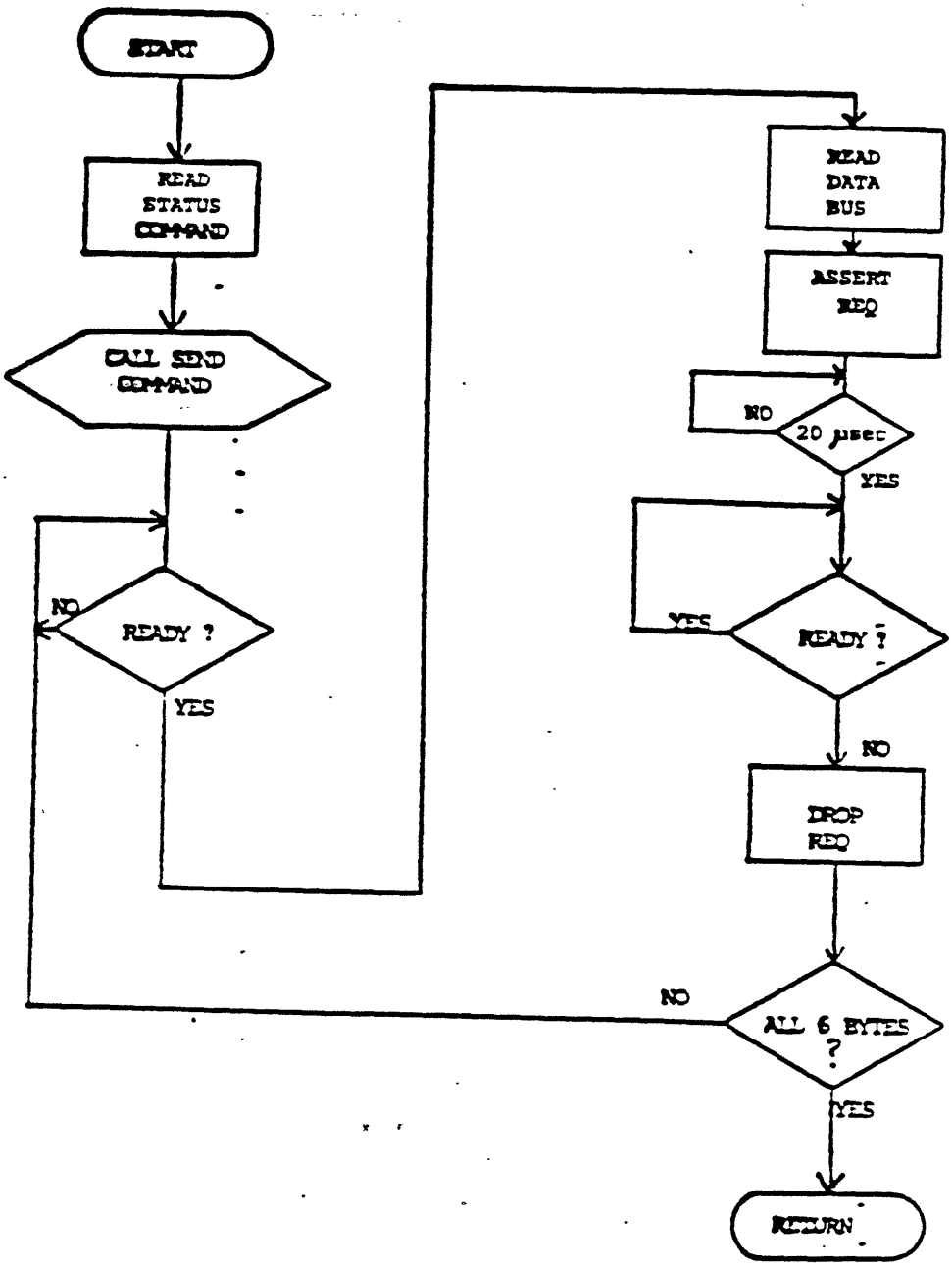


Figure 15.0

SIZE	CODE	DRAWING NUMBER	REV.
A		008845	E0