



**Am95/6110
Single Density
Floppy Disk Controller**

User's Manual

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PREFACE

This manual provides general information, an installation and interface guide, and programming information for the Advanced Micro Computer, Am95/6110 Flexible Disk Controller board. Additional information can be obtained from the following documents.

Western Digital Corporation
FD1771 A/B-01 Data Sheet

Advanced Micro Devices
Am9517 Data Sheet
Am9517 Application Note
Am9085 Data Sheet

This manual is intended for use by systems engineering and programming personnel. A minimum of tutorial information is included. Standard abbreviations and acronyms are used in the text.

Both active-high (positive true) and active-low (negative true) signals are discussed. To eliminate confusion and simplify the notation, the following signal convention is used. Whenever a signal is active-low, its mnemonic is followed by an asterisk (*). For example, MEMR* denotes an active-low signal. Active-high signals are denoted without the asterisk.

The information in this manual is believed to be accurate and complete at the time it was printed. However, AMC reserves the right to change specifications without notice. No responsibility is assumed for errors that might appear in this manual. No part of this manual may be copied or reproduced in any form without prior written permission from AMC.

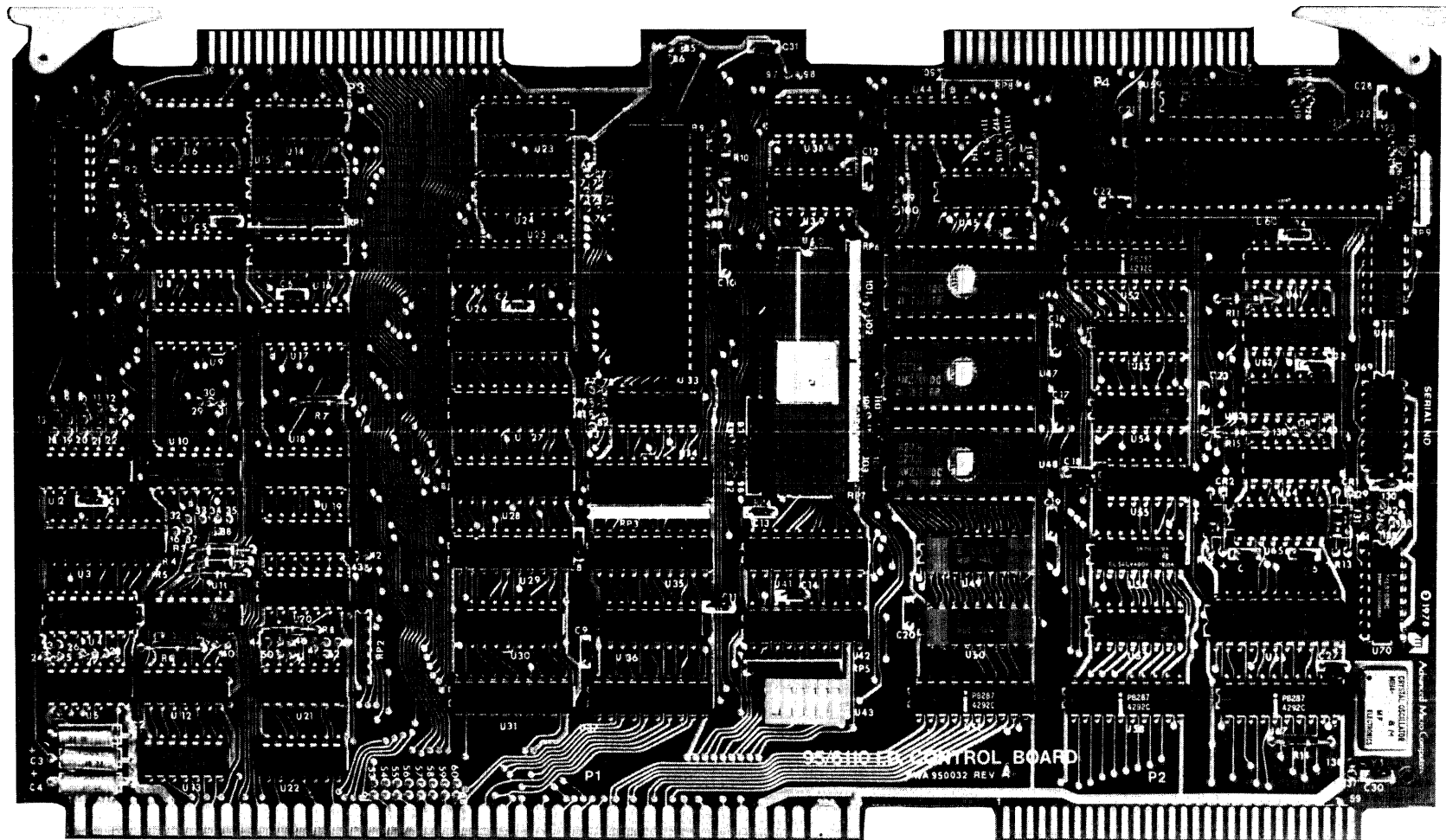
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CONTROL BOARD
WA 950032 REV A

SERIAL NO.

O 1977

PHILIP SCHAFFNER
WA 950032
REV A

CHAPTER 1

GENERAL INFORMATION

1-1. INTRODUCTION

The Am95/6110 is a single density floppy disk controller for up to four selectable single or double sided floppy disk drives, using an Am9085 microprocessor based design which provides reliable and flexible functions. Features include: a 20-bit DMA address capability allowing it to address up to 1 megabyte of main memory, drive write protection, automatic CRC generation and check, full IBM 3740 compatible soft sector formatting, automatic track seek verify, and head unloading after two idle disk rotations to assure long diskette life. An automatic bootstrap load from track 00, sector 01 (jumper selectable) is done at system initialization without system processor intervention.

The Am95/6110 is fully TTL compatible. It is provided with an adaptable interface to microprocessor systems comprising an 8-bit parallel bus, 20-bit address bus, and appropriate control lines. An on-board DMA interface transfers data directly to or from external memory and the disk controller.

1-2. PHYSICAL DESCRIPTION

The Am95/6110 Floppy Disk Controller board is a two layer printed circuit board. An 86-pin and 60-pin connector provide bus compatibility with AMC's System 8/8 and the Intel Multibus[†] in either a Multi-master or Single-master bus configuration. Physical characteristics of the Am 95/6110 are:

[†] Multibus is a trademark of Intel Corporation

Board Dimensions

Width	30.48 cm (12 inches)
Depth	17.15 cm (6.75 inches)
Thickness	1.50 cm (0.60 inches)

Interface Connectors

P1	- 86 pin, .156 in pin spacing edge connector
P2	- 60 pin, .10 in pin spacing edge connector
P3	- 50 pin, .10 in pin spacing edge connector
P4	- 50 pin, .10 in pin spacing edge connector

Power Requirements

V _{CC}	+ 5 V, \pm 5%
V _{DD}	+12 V, \pm 5%
V _{BB}	- 5 V, \pm 5%
I _{CC}	3 AMP
I _{DD}	300 mA
I _{BB}	150 mA

Environmental Requirements

Operating Temperature	0°C to 55°C
Relative Humidity	up to 90% without condensation
Storage Temperature	-40°C to +75°C

1-3. FUNCTIONAL DESCRIPTION

The Am95/6110 Floppy Disk Controller (FDC) is an intelligent disk controller that accepts commands from a host computer via the system bus, and permits the host CPU/operating system to access data stored on a floppy diskette. Data is stored in random-access form. Data can be read from or new data written onto a selected location on the disk-

ette. Communication between the host CPU and the FDC is conducted over a standard Intel Multibus compatible system bus.

The FDC and host CPU exchange information through the mailbox registers (R0-R4), associated with I/O ports (R0-R3.) Bits 2 through 7 of the address from the system bus are decoded and compared with the board address to determine if the command is intended for the FDC board. Bits 0 and 1 are used to specify a particular mailbox register. The data for reading or writing on the floppy diskette is transferred under Direct Memory Access (DMA) control.

When the host computer sends a command to the FDC, execution and control of the resulting operations are performed by the on-board Am9085 microprocessor, utilizing the DMA controller (Am9517) and the floppy disk controller (FD1771).

The command set is used to invoke firmware residing in 2K of on-board PROM. Each command invokes a portion of the firmware. When executed, the various firmware routines perform the floppy

disk controller functions. The FD1771 floppy disk controller chip, controlled by the Am9085, selects a particular disk drive, accesses a predetermined location on that diskette, and either reads data from or writes data onto that diskette. Data read is separated, put into 8-bit bytes, and is either transferred into the buffer memory or sent byte-by-byte to a main memory whose location is designated by the DMA. Data transferred to the buffer memory can be sent to main memory by the DMA after the sector is completely read. Data can be read and transferred in sector or block (continuous sector) form. Data written onto the diskette goes to the FD1771 byte-by-byte in the same manner described for the read mode. The FD1771 serializes, formats, and sends the data to the specific location on the diskette to be written.

Status, address, data, and control signals for the internal operations of the FDC are routed on the internal address and data bus lines. The FDC board status register contents are loaded into R4 which can be examined by the host CPU.

CHAPTER 2

INSTALLATION AND INTERFACE

2-1. INTRODUCTION

This chapter provides instructions for unpacking and preparing the Am95/6110 Board for connection to a microcomputer system. System Bus signal characteristics, connector pin assignments and timing information necessary to interface the FDC board to a CPU and the FDC board to a Floppy Disk Drive are also included in this chapter.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection. Shipping damages should be immediately reported to the carrier.

NOTE

Do not attempt to service the board yourself as this will void the warranty.

It is suggested that salvageable shipping cartons and packing materials be saved in case the product must be shipped in the future.

2-3. PRE-INSTALLATION OPTION SELECTION

Before connecting the FDC board to the microcomputer system, switches and jumpers must be set to the desired positions to select the features that are required to customize the board for

its intended use. The following paragraphs provide information on switch and jumper selection.

2-4. DATA BUS

The FDC board can be interfaced to the host CPU through either an 8-bit or a 16-bit system data bus. Jumpers and switches provided on the board must be placed in the proper position to configure the board for the data bus with which it is to be used. Jumper installation for 8 or 16 bit data control is shown in table 2-1. When the jumper is installed between pins 34-38, the FDC is configured to operate with an 8-bit data bus. When the jumper is installed between pins 33-34, the FDC is configured for a 16-bit data bus, with DMA $\emptyset = 0$ addressing in the Low Order Byte. When the jumper is installed between 34-35, the FDC is configured for a 16-bit data bus, with DMA $\emptyset = 0$ addressing in the High Order Byte.

2-5. BOARD SELECT SWITCHES

Six two-position DIP switches (SW1 through SW6) are used to select the addresses to which the FDC board will respond. As shown in table 2-2, address bits 2 through 7 must correspond to switches SW1-SW6, respectively. A logical 1 on the port address bus corresponds to the on position of the board select switches. Address bus bits \emptyset and 1 are decoded for the external addresses of registers R \emptyset through R4.

2-6. MEMORY CONTROL SELECTION

To customize the FDC board for the specific size of the E-PROMs being used, it is necessary to apply to the chip sockets the voltages and control sig-

TABLE 2-1. DATA BUS SELECTION.

Data Bus	Jumper Selection	
	From	To
8-bit	34-----	38
16-bit	33	34 - DMA $\emptyset=\emptyset$, Enable Low Byte
16-bit	34	35 - DMA $\emptyset=\emptyset$, Enable High Byte
----- Jumper configuration for factory installed firmware		

TABLE 2-2. BOARD SELECT SWITCH SETTINGS.

SWITCH NUMBER	ADDRESS BIT	I/OWC				I/ORC
SW6	7					
SW5	6					
SW4	5					
SW3	4					
SW2	3					
SW1	2					
Not Used	1	\emptyset	\emptyset	1	1	1
Not Used	\emptyset	\emptyset	1	\emptyset	1	1
Register Selection		R \emptyset	R1	R2	R3	R4

nals required by the chosen devices. The jumpers used to select these voltages and control signals are shown in table 2-3. The E-PROM devices can be either Am9708 (1K) or Am9716 (2K). No jumpers are required to access off-board private memory. Off-board memory, in this context, is specifically private to the floppy disk controller and is not directly addressable by other bus masters in the system.

2-7. INTERRUPT SELECTION

The FDC board is capable of generating a system interrupt on one of eight interrupt lines to be utilized as the system designer wishes. The interrupt is brought off-board through connector P1. The jumper options available for

TABLE 2-3. MEMORY CONFIGURATION.

Memory Device	Jumper Selection	
	From	To
Am9708	81-----	82
	80-----	79
	77-----	78
1K x 8	111----	112
	30-----	31
	115----	116
Am9716	81	83
	80	82
	77	79
2K x 8	111	114
	29	30
	113	115
----- Jumper configuration for factory installed firmware		

connecting the interrupt lines to the edge connector (P1) are shown in table 2-4.

The FDC, Am9085 CPU interrupt jumper options are also shown in table 2-4. For normal system bus operation with the standard OEM firmware installed, jumpers are configured as shown.

2-9. Am9085 CPU, SID JUMPER

The Am9085 serial input data (SID) line is tested by the resident firmware and the results determine if an auto boot will be implemented. When a jumper is installed between SID (86) and Ground (84), SID = \emptyset , the auto boot feature is selected. When this jumper is not installed, at reset the firmware

TABLE 2-4. INTERRUPT JUMPERS.

Interrupt Sources	Jumpers		System Bus Interrupt	J1 Pin	Am9085PU Interrupt
	Source	Interrupt			
Am9085*	59	67	INT \emptyset	41	---
	60	68	INT1	42	---
	57	65	INT2	39	---
	58-----66		INT3	40	---
	55	63	INT4	37	---
	56	64	INT5	38	---
	53	61	INT6	35	---
	54	62	INT7	36	---
INTREQ	88-----87		---	---	RST 7.5
EOPINT	75	76	---	---	RST 6.5
URINT	73	74	---	---	RST 5.5
COMIN	71	72	---	---	TRAP
GROUND	69-----70		---	---	TRAP
GROUND	97-----98		---	---	INTR
----- normal jumper configuration for factory installed firmware					
*FDC Board interrupt to host computer.					

2-8. CPU CLOCK FREQUENCY SELECT

The input clock frequency to the Am9085 is jumper selectable for either 4MHz or 8MHz (for 2MHz or 4MHz boards respectively). Jumper installation selection is shown in table 2-5. If the 8MHz option is used, some of the chips on the FDC must be replaced with devices that operate at the higher frequency. The standard OEM FDC board (2MHz Am9085) is shipped with the 4MHz clock jumper option installed.

TABLE 2-5. CPU CLOCK FREQUENCY SELECTION.

Frequency	Jumper Selection	
	From	To
8MHz	41	42
4MHz	43-----42	
----- normal jumper configuration for factory installed firmware		

performs a status request operation on unit zero and makes the results available to the host system boot program. On OEM boards, this jumper is not installed. The SID/SOD lines are not brought out to connector pins and therefore are not customer usable.

2-10. DMA REQUEST SOURCE (DREQ0-DREQ3)

The direct memory access (DMA) (Am9517) request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. Table 2-6 shows the jumper options used for DMA channel selection. Also shown is the jumper configuration for an OEM board with the standard firmware installed.

2-11. DMA ACKNOWLEDGE (DACK0-DACK3)

DMA Acknowledge is used to notify an individual peripheral that it has been granted a DMA cycle. Table 2-7 shows the jumper configuration to utilize these lines.

2-12. READY/DMA SPEED SELECTION

The ready input is used to extend memory read and write pulses from the Am9517 to synchronize the DMA with slow memory. A jumper must be installed between pins 4 and 3 to enable the Ready Control. Table 2-8 shows the jumper selections for FDC data transfers. When the Ready signal is activated by an external memory (via the system

TABLE 2-6. DMA REQUEST.

Request Source	Jumper Selection From To	Data Channel
TXINT	89 / 93	DREQ3
RXINT	90 / 94	DREQ2
FDDRQ	91 / 94	DREQ1
FDDRQ	92 / 94	DREQ0
----- normal jumper configuration for factory installed firmware		

TABLE 2-7. DMA ACKNOWLEDGE.

Source	Jumper Selection From To	Acknowledge
DACK3	105 / 109	IDACK3
DACK2	106 / 110	IDACK2
DACK1	103 / 107	IDACK1
DACK0	104 / 108	IDACK0
----- normal jumper configuration for factory installed firmware		

TABLE 2-8. DMA SPEED SELECTION.

Control	Jumper Selection	
	From	To
Enable Ready Control	4-----	3
EXT Ready Control	12-----	17
Bypass Delay (INT)	22	17
Delay (Ready Pulse Width)		
1.0 μ sec (.511ms/128 byte)	8	13
1.0 μ sec (.511ms/128 byte)	9	14
1.0 μ sec (.511ms/128 byte)	10	15
1.5 μ sec (.575ms/128 byte)	11	16
1.5 μ sec (.575ms/128 byte)	21	16
1.5 μ sec (.575ms/128 byte)	20	15
1.5 μ sec (.575ms/128 byte)	19	14
1.5 μ sec (.575ms/128 byte)	18	13
----- normal jumper configuration for factory installed firmware		

bus), a jumper is placed between pins 12 and 17 (IACK) to circumvent all of the delay logic. When a delay is not required, a jumper is installed between pins 22 and 17.

2-13. END-OF-PROCESS FLIP/FLOP

The End-of-Process flip/flop is normally set by the EOP output from the DMA controller; however, when a jumper is installed between pins 101 and 102, the EOP flip/flop can be set as a result of the INTREQ (FD1771). When this jumper is installed, either EOP (Am9517) or INTREQ (FD1771) sets the flip/flop. The OEM version of the FDC board is shipped without this jumper installed.

2-14. POWER-ON HOLD

The power-on hold selection is provided to permit the host CPU to be placed in a "hold" state until the FDC releases

it to begin execution. The firmware supplied with the FDC provides the ability for track-0, sector-0 to be automatically read into location zero (0) of host memory to provide an "auto-boot" capability. When the auto boot is desired, a jumper is installed between pins 5 and 6. When power-on hold is not required, with no auto boot, the jumper is installed between pins 6 and 7. On OEM boards (with the standard firmware) the jumper is installed between pins 6 and 7.

2-15. HOLD REQUEST/BUS PRIORITY IN

The FDC board is configured such that the Hold Request signal out for a single master system bus can be either active high or active low. The jumper can be moved for operation using a multi-master system bus, as shown in table 2-9, which is the standard configuration.

TABLE 2-9. BUS PRIORITY IN/HOLD.

Master	Hold Request	Jumper Selection	
		From	To
Single	Active High	48	49
	Active Low	48	52
Multi	Active Low	48-----47	
----- normal jumper configuration for factory installed firmware			

2-16. DATA SEPARATOR CLOCK SELECT

The external data separator has a jumper-selectable clock frequency of 4MHz. When using the external data separator, install a jumper between pins 129 and 131 for a 4MHz clock. An 8MHz test point is available at Pin 134. The OEM configuration is jumpered to operate with an external data separator and a 4MHz clock.

2-17. FD1771 FLOPPY DISK CONTROLLER CLOCK

The FD1771 Floppy Disk Controller has two jumper-selectable clock frequencies: 2MHz and 1MHz. Jumper selections for each frequency are defined in table 2-10. The standard OEM board is shipped with the 2MHz option installed, for a standard 8 inch floppy disk drive.

2-18. DISK INITIALIZATION (DINT)

This input is sampled whenever a write command is executed. If DINT = 0, the operation is terminated and the Write Protect Status bit is set. For the OEM configuration, this input on the FDC board is jumpered to logic high by connecting pins 127 and 128.

2-19. HEAD LOAD TIMING (HLT)

The HLT input of the FD1771 is sampled 10ms after activating the head load output. When a logic high is sampled

TABLE 2-10. FD1771 CLOCK FREQUENCY.

Frequency	Jumper Selection	
	From	To
2MHz	130-----132	
1MHz	133	132
----- normal jumper configuration for factory installed firmware		

on the HLT input, the head is assumed to be engaged. Table 2-11 shows the different jumper options available to activate this input. On the OEM configuration of the FDC the HLT input is jumpered to the HLD signal, which provides a 35ms delay to allow the head load to be accomplished.

TABLE 2-11. HEAD LOAD TIMING.

Time Delay	Jumper Selection	
	From	To
HLD 10ms	123	124
HLD Seek Complete	126	124
HLD 35ms	125-----124	
----- normal jumper configuration for factory installed firmware		

2-20. AUTO RESET

The FDC board is configured with logic and jumpers such that the INIT system Reset line to the system bus can be

activated either by the on-board Am9085 (at power up or manual reset), or under software control. Table 2-12 shows the jumper selections for these options. The OEM board is configured such that, with activation of the OEØ1 line, the system reset line goes low (active) for eight clock periods.

2-21. BUS CLOCK

Availability of a 4MHz or 8MHz external clock is provided for the system bus by installation of jumpers. For the 4MHz bus clock, install a jumper between pins 36 and 37. For the 8MHz bus clock, install a jumper between pins 32 and 37. The OEM version of the FDC is shipped without any jumper installed. No jumpers are required when the bus clock is from another bus master.

2-22. BUS MASTER CONTROL/HOLD ACKNOWLEDGE

The FDC board is jumper-selectable to operate in a multi-master or single master system bus environment. When operating in a single master environment the HACK signal can be selected for either an active high or active low state. Jumper selections for this op-

tion are defined in table 2-13. The OEM board is jumpered for multi-master operation.

2-23. HEAD LOAD CONTROL

Jumpers are provided such that a head load can be implemented by the on-board firmware or by the FD 1771 chip. When a jumper is installed between pins 139 and 140, drive select may be enabled either with the 1771 HEAD LOAD signal or be enabled under firmware control. When a jumper is installed between pins 138 and 139, firmware controls the drive select. The OEM version of the board has a jumper installed between pins 139 and 140.

2-24. BUS PRIORITY OUT (BPRO) DAISY CHAIN

This system-bus signal is used with a serial priority resolution scheme, and is used to pass the bus priority chain to the lower priority bus master. When more than one board capable of being a master is on the system bus, this jumper is installed between pins 39 and 40. The OEM board has this jumper installed.

TABLE 2-12. RESET CONTROL.

Reset Control	Set	Reset	Jumper From	Installation To
Software	OEØ1	8 clock pulses	24-----25 27-----26	
Software	OEØ1	IEØ1	24 27	25 28
Am9085	RST/ØE1	8 clock pulses	23 27	25 26
----- normal jumper configuration for factory installed firmware				

TABLE 2-13. BUS MASTER CONTROL.

System Bus	Jumper From	Installation To	Hold Acknowledge
Multi-Master	45-----50 46-----51		N/A N/A
Single-Master	44 51	45 45	Active Low Active High
----- normal jumper configuration for factory installed firmware			

2-25. INSTALLATION

After using the on-board switches and jumpers to tailor the FDC board for its intended use, insert the board into the system backplane and apply power. If the board fails to operate, notify the Advanced Micro Computers' service manager.

NOTE

Do not return the board to AMC under any circumstances without an approved return material authorization number (RMA), which will be provided by the service manager.

2-26. INTERFACE SIGNAL DESCRIPTION

This section describes the signals that interface the FDC board to the host central processing unit and its peripheral devices. Signals shown with an asterisk (*) following the signal name are active low signals. Active high signals appear without an asterisk suffix.

2-27. CPU/SYSTEM BUS INTERFACE

Connector P1 is an 86-pin double-sided edge connector that interfaces the FDC

board to other system components. Normally, connector P1 plugs into a backplane wiring configuration called a system bus. Pin assignments for Connector P1 are listed in table 2-14.

2-28. Address (ADR0* through ADR13*)

The 20-bit address from the system bus is used by the on-board DMA to access up to 1 megabyte of memory. ADR0* is the least significant bit and ADR13* is the most significant address bit. Address bits 2 through 7 (ADR2*-ADR7*) are compared with the board address select switches; only an address that matches the select switch settings is recognized by the FDC board. Address bits 0 and 1 are used to access various on-board register locations for externally-generated I/O read/write operations.

2-29. Data (DAT0* through DATF*)

Sixteen bidirectional data lines are used to transmit or receive information between the FDC and an external (host) system. These lines are driven by the master on write operations and by the addressed slave (memory or I/O) on read operations. The system bus can handle both 8 or 16 bit data transfers. Only bits DAT0* through DAT7* are used when executing eight-bit transfers (DAT0* is the least significant bit).

TABLE 2-14. SYSTEM BUS CONNECTOR P1 PIN ASSIGNMENTS.

	(Component Side)		(Circuit Side)			
	Pin	Mnemonic	Description	Pin	Mnemonic	Description
Power Supplies	1	GND	Signal GND	2	GND	Signal GND
	3	+5	+5 VDC	4	+5	+5 VDC
	5	+5	+5 VDC	6	+5	+5 VDC
	7	+12	+12 VDC	8	+12	+12 VDC
	9	-5	-5 VDC	10	-5	-5 VDC
	11	GND	Signal GND	12	GND	Signal GND
Bus Controls	13	BCLK*	Bus Clock	14	INIT*	Initialize
	15	BPRN*	Bus Priority In	16	BPRO*	Bus Priority Out
	17	BUSY*	Bus Busy	18	BREQ*	Bus Request
	19	MRDC*	Mem Read Command	20	MWTC*	Mem Write Command
	21	IORC*	I/O Read Command	22	IOWC*	I/O Write Command
	23	XACK*	XFER Acknowledge	24	INH1*	Inhibit 1 (RAM)
	25	AACK*	Not Used	26	INH2*	Inhibit 2 (ROM)
	27	BHEN*	Byte High Enable	28	ADR10*	Address Bus
	29	CBRQ*	Common BUS Request	30	ADR11*	
	31	CCLK*	Constant Clock	32	ADR12*	
	33	INTA*	Interrupt Acknowledge	34	ADR13*	
Interrupts	35	INT6*	Parallel Interrupt Requests	36	INT7*	Parallel Interrupt Requests
	37	INT4*		38	INT5*	
	39	INT2*		40	INT3*	
	41	INT0*		42	INT1*	
Addresses	43	ADRE*	Address Bus	44	ADRF*	Address Bus
	45	ADRC*		46	ADRD*	
	47	ADRA*		48	ADRB*	
	49	ADR8*		50	ADR9*	
	51	ADR6*		52	ADR7*	
	53	ADR4*		54	ADR5*	
	55	ADR2*		56	ADR3*	
	57	ADRO*		58	ADR1*	
Data	59	DATE*	Data Bus	60	DATF*	Data Bus
	61	DATC*		62	DATD*	
	63	DATA*		64	DATB*	
	65	DAT8*		66	DAT9*	
	67	DAT6*		68	DAT7*	
	69	DAT4*		70	DAT5*	
	71	DAT2*		72	DAT3*	
	73	DATO*		74	DAT1*	
Power Supplies	75	GND	Signal GND	76	GND	Signal GND
	77	--	---	78	--	---
	79	-12	-12 VDC	80	-12	-12 VDC
	81	+5	+5 VDC	82	+5	+5 VDC
	83	+5	+5 VDC	84	+5	+5 VDC
	85	GND	Signal GND	86	GND	Signal GND

2-30. Interrupt Request Lines (INT0* through INT7*)

These eight lines are used to connect jumper-selectable interrupts to the data bus. The on-board Am9085-generated interrupt can be connected to any of the eight interrupt request inputs. INT0* is the highest priority interrupt and INT7* is the lowest priority.

2-31. Initialization

This signal from the system bus resets the board to a known internal state.

2-32. Input/Output Read Command (IORC*)

The IORC* signal is used for I/O input control. The I/O port address is on the system address bus. IORC*, along with a port address recognized by the FDC, is a request to read data from the addressed FDC register.

2-33. Input/Output Write Command (IOWC*)

The IOWC* signal indicates that an I/O port address is on the system bus address lines. The address and data must be stable on the system bus 50ns prior to activation of the write command.

2-34. Memory Read Command (MRDC*)

The MRDC* signal performs in the same manner as the IORC* signal except that a memory address is on the address bus instead of an I/O port address. MRDC* is generated by the FDC to read data from main (host) memory.

2-35. Memory Write Command (MWTC*)

The MWTC* signal performs in the same manner as the IOWC* signal except that a memory address is on the address bus instead of an I/O port address. MWTC*

is generated by the FDC to write data into the main (host) memory.

2-36. Transfer Acknowledge (XACK*)

This signal is sent to the FDC from the system bus indicating that the specified read or write operation has been completed and that data has been placed onto, or accepted from, the system bus data lines.

2-37. FLOPPY DISK DRIVE INTERFACE

Connector P4 is a 50-pin double-sided edge connector that interfaces the FDC board to the floppy disk drives. The floppy disks are connected together through a 50-pin flat cable to P4 of the FDC board and additional disk drives are connected in daisy chain fashion, drive-to-drive. Pin assignments for Connector P4 are listed in table 2-15. The last drive connected to the string must have a terminator installed.

2-38. Track Greater Than 43 (TG43*)

TG43* active indicates to the disk drive that the read/write head of the selected drive is positioned between tracks 44 and 76. Activation of the signal occurs only during a read or write command.

2-39. Write Protect (WRPT*)

When a write command is issued by the FDC, the write protect signal is sampled by the FD1771. A logic low terminates the command and sets the write protect status bit.

2-40. Track 00 (TR00*)

At a logic low, the TR00* signal from the disk drive indicates the read/write head is positioned at track 00.

TABLE 2-15. P4 CONNECTOR PIN ASSIGNMENT.

Component Side			Circuit Side		
Pin	Mnemonic	Description	Pin	Mnemonic	Description
2	GND	Signal Ground	1	GND	Signal Ground
4	GND	Signal Ground	3		
6	TG43	Track Greater than 43	5		
8			7		
10	* 2 SIDED	2 Sided	9		
12	* DISK CHANGE		11		
14	* SIDE SELECT		13		
16	* IN USE		15		
18	* HEAD LOAD		17		
20	INDEX	Index Pulse	19		
22	* READY	Ready	21		
24	* Sector	Sector (851 Only)	23		
26	DS01	Drive 1 Select	25		
28	DS02	Drive 2 Select	27		
30	DS03	Drive 3 Select	29		
32	DS04	Drive 4 Select	31		
34	DIR	Direction	33		
36	STEP	Step	35		
38	WD	Write Data	37		
40	WG	Write Gate	39		
42	TR00	Track00	41		
44	WPRT	Write Protect	43		
46	RD	Read Data	45		
48	SEP DATA	Separated Data	47		
50	SEP CLK	Separated Clock	49	GND	Signal Ground

*These signals are defined in more detail in the Shugart SA800/801 OEM Manual.

2-41. Index Pulse (IP*)

The index pulse is a 10usec logic low pulse which indicates to the FDC that the selected disk drive read/write head has sensed the index notch on the diskette.

2-42. Ready

This signal from the selected floppy disk drive indicates its ready status and is examined prior to initiating a read or write command by the FD1771. A logic-low at P4 (READY*) indicates that the drive is ready. If the ready signal is high, no read or write operation is performed and an interrupt is gener-

ated. A seek operation can be performed regardless of the ready signal condition.

2-43. Write Gate (WG)

The write gate signal from the FDC board (P4, WRITE GATE*) is activated (logic-low) to the selected drive when a write operation is performed.

2-44. Write Data (WD)

The write data stream is a serial train of data and clock pulses, each pulse being 500ns in duration.

2-45. Direction (DIRC)

The direction signal is either a logic high or low that indicates to the disk drive the direction the heads must move when the step signal activates. A logic-high at P4 (DIR) causes the head to move out (toward track 00); and a logic low causes the head to move in (toward track 76).

2-46. Step (PH1/STEP)

The step signal is a positive pulse of 4usec duration that causes the disk drive heads to move one track in or out (depending on the state of the DIRC signal).

2-47. 2 Sided

This logic-high signal indicates that a double-sided drive is in use.

NOTE

This same pin would be used to indicate seek COMPLETE when used with persi drive.

2-48. Read Data

Raw data (clock and data together) from the diskette come to the FDC board via the READ DATA line and are processed by the on-board data separator where the clock data pulses are separated and gated to the FD1771.

2-49. Drive Select (DS01*-DS04*)

Four drive select lines (DS01*-DS04*) go from the FDC board to the disk drives to select a specific drive. Only one of these lines is active (low) at a time. Each drive is address programmed and is set to a location 1 through 4.

CHAPTER 3 OPERATION AND PROGRAMMING

3-1. INTRODUCTION

The floppy disk controller board operates under command of the host CPU. The host CPU can interrogate the FDC by reading the status byte in the on-board status register. The host CPU can also set-up operating parameters by writing the data into three mail-box registers in the FDC and initiating one of eleven operations by writing a command code into a fourth mail-box register (referred to as the command register). Once a command is initiated, the on-board CPU (under control of the firmware) continues without host CPU intervention until the operation is complete.

Each FDC board may be uniquely configured through the placement of jumpers on the board. The I/O port address to which the FDC board responds may be selected by on-board switches. Placement of jumpers is discussed in chapter 2.

The FDC provides two interfaces, one to the host CPU, and the other to the floppy disk unit. The host CPU/FDC board interface consists of an INTEL MULTIBUS through which commands and data are passed from the host CPU to the FDC. Status, disk data, and 20-bit DMA addresses are passed back to the host CPU. The floppy disk interface consists of head positioning control signals, write gate control signals, and data transfer lines. Each function is hard-wired to the appropriate disk drive.

3-2. BOARD SELECTION

The port address of the FDC board is set-up by six two-position DIP switches. When set, these switches (SW1 through SW6) select the address to

which the FDC board will respond. These switches correspond to address bits 2 through 7, respectively. Address bits 0 and 1 select the I/O port through which parameters are passed.

3-3. FUNCTIONAL CONFIGURATION

Jumpers may be required on the FDC board in positions other than those installed at the factory. The placement, definition, and uses of the jumper selectable features are included in chapter 2. The manner in which they are installed, to accommodate factory installed firmware, is also included. The jumper positions described in chapter 2 should be verified before the board is put into service.

3-4. FIRMWARE DESCRIPTION

The Am95/6110 Floppy Disk Controller firmware (PN-02050068) resides in the Am95/6110 controller E-PROMs. A description of the factory installed firmware is shown as a listing in table 3-1.

The firmware consists of program routines for the on-board Am9085A CPU. These routines interrogate the mail-box registers, set up operating parameters, determine which of the eleven commands is requested, implement the command, exercise the FD1771 Floppy Disk Formatter/Controller, and the Am9517 Multi-mode DMA Controller to produce floppy disk operating signals, and perform other FDC board operations.

Briefly, the firmware and Am9085 CPU function as follows. Writing a command into the command register (R3) sets the Command Bit flip-flop on the FDC board. This causes the on-board CPU to process

TABLE 3-1.

```

AMC MACRO ASSEM 1.0 #001 AMC 95/6110 SINGLE DENSITY FDC V1.3
17DE = TYPE EQU 6110 ;SET TO 6110 OR 6120
      IF TYPE EQ 6120
        TITLE 'AMC 95/6120 SINGLE/DOUBLE DENSITY FDC V1.0'
        ELSE
        TITLE 'AMC 95/6110 SINGLE DENSITY FDC V1.3'
        ENDF
        PAGE 43
      ;
      §-MACRO
      ;
      SIM MACRO VALUE
        MVI A,VALUE
        DB 30H
        ENIM
      RIM MACRO
        DB 20H
        ENIM
      ;
      ; HOST REGISTERS
      ;
0030 = R0 EQU 30H ;UNIT/PAGE
0031 = R1 EQU 31H ;TRACK/MSB ADDRESS
0032 = R2 EQU 32H ;SECTOR/LSB ADDRESS
0033 = R3 EQU 33H ;COMMAND/STATUS
      ;
      ; 1771 REGISTERS
      ;
0000 = FICST EQU 0 ;COMMAND/STATUS
0001 = FDTRK EQU 1 ;TRACK
0002 = FDSEC EQU 2 ;SECTOR
0003 = FDATA EQU 3 ;DATA-TRACK FOR SEEK
      ;
      ; FDC REGISTERS
      ;
0048 = CMDSTA EQU 48H ;COMMAND/STATUS
0049 = RESET EQU 49H ;SYSTEM 29 RESET
004A = SEGMT EQU 4AH ;ADDRESS PAGE
004B = CMDRES EQU 4BH ;COMMAND RESET
004D = IRSEL EQU 4DH ;UNIT SELECT
004E = RELSE EQU 4EH ;SYSTEM 29 RELEASE
      ;
      ; 1771 COMMANDS
      ;

```


TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #002 AMC 95/6110 SINGLE DENSITY FDC V1.3

00D0 = FRCIN EQU 0D0H ;FORCE STATUS I
000A = RESTR EQU 0AH ;RESTORE
001E = SEEK EQU 1EH ;SEEK TRACK
0088 = READ EQU 88H ;READ SECTOR
00A8 = WRITE EQU 0A8H ;WRITE SECTOR
00F4 = WRTRK EQU 0F4H ;WRITE TRACK
005A = STEP EQU 5AH ;STEP IN
0016 = LDHED EQU 16H ;LOAD HEAD
0010 = UNLOD EQU 10H ;UNLOAD HEAD
;
; DMA PORTS
;
0010 = DM0AD EQU 10H ;CHANNEL 0 ADDRESS
0011 = DM0WC EQU 11H ;CHANNEL 0 WORD COUNT
0012 = DM1AD EQU 12H ;CHANNEL 1 ADDRESS
0013 = DM1WC EQU 13H ;CHANNEL 1 WORD COUNT
0014 = DM2AD EQU 14H ;CHANNEL 2 ADDRESS
0015 = DM2WC EQU 15H ;CHANNEL 2 WORD COUNT
0016 = IM3AD EQU 16H ;CHANNEL 3 ADDRESS
0017 = IM3WC EQU 17H ;CHANNEL 3 WORD COUNT
0018 = DMCST EQU 18H ;COMMAND/STATUS
0019 = IMREQ EQU 19H ;REQUEST
001E = IMMDE EQU 1EH ;MODE
001C = DMBFF EQU 1CH ;BYTE FLIP-FLOP
001D = DMCLR EQU 1DH ;RESET
001F = DMMSK EQU 1FH ;MASK
;
; ERROR MASKS
;
009C = RDMSK EQU 9CH ;READ ERROR
00FC = WRMSK EQU 0FCH ;WRITE ERROR
;
; REQUEST FORMATS
;
; HOME
; R0=UNIT
; R3=REQUEST FUNCTION 0
;
; SETPAR
; R0=UNIT
; R1=TRACK
; R2=SECTOR(2-7TH BIT SET TO FORCE SIDE COMPARE - 6120 ONLY)
;
; R3=REQUEST FUNCTION 1

```


TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #004 AMC 95/6110 SINGLE DENSITY FDC V1.3
;
; BITS 0-1 AND 2-4 ARE MUTUALLY EXCLUSIVE THUS:
; BITS 0 AND 2=ILLEGAL REQUEST FUNCTION
; 1 AND 2=TIME-OUT ON DEVICE BUSY OR LOST INTERRUPT
;
; UNIT FORMAT:
; BIT 0-1=UNIT 0-3
; 2=SIDE 0=0, 1=1
; 3=DENSITY 0=SINGLE, 1=DOUBLE
; 4=RETRY 0=NONE, 1=9 FOR READ/WRITE, 5 FOR SEEK/HOME
; 5=BUFFERING 0=DISK TO HOST, 1=DISK TO BUFFER TO HOST
; 6=INTERRUPT REQUEST 0=NONE, 1=INTERRUPT HOST
; 7=INTERLACE, 0=1/1, 1=2/1
;
0000 = PORG EQU 0 ;PROGRAM ORIGIN
0000 = RAMAD EQU 0000H ;DATA ORIGIN
;
0000 ORG PORG
;
; IPL RAM TEST - UP/DOWN FF-00 PATTERN-(B KEEPS ERROR CODE THROUGHOUT)
;
0000 3ED0 MVI A,FRCIN
0002 1300 OUT FDCST ;TERMINATE 1771 ACTIVITY
0004 01FF0F LXI B,0FFFH
0007 79 MOV A,B
0008 1333 CUT R3 ;INITIALLY SET ALL ERRORS
000A 110004 LXI D,1024
000D 210010 LXI H,RAMAD+1024
0010 2B FILL DCX H ;INITIALLY FILL ALL RAM WITH FF
0011 71 MOV M,C
0012 1B DCX D
0013 7A MOV A,D
0014 B3 ORA E
0015 C21000 JNZ FILL
0018 1604 MVI D,4
001A 7E UPF MOV A,M ;CHECK FOR FF AND SET 00 UP
001B 91 SUB C
001C C26900 JNZ PROM
001F 77 MOV M,A
0020 23 INX H
0021 1B DCX I
0022 7B MOV A,E
0023 B2 ORA D
0024 C21A00 JNZ UPF

```

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#005	AMC 95/6110 SINGLE DENSITY FDC V1.3
0027 21000C		LXI H,RAMAD
002A 1604		MVI D,4
002C 7E	UPZ	MOV A,M ;CHECK FOR 00 AND SET FF UP
002D B7		ORA A
002E C26900		JNZ PROM
0031 71		MOV M,C
0032 23		INX E
0033 1B		DCX D
0034 7A		MOV A,D
0035 B3		ORA E
0036 C34000		JMP DNI
0039		ORG 39H
0039 C37001	RFTURN	JMP CMLLP ;FOR USER PROGRAM RETURN
	;	
	;	INTERRUPT 7.5
	;	
003C D1		POP D ;CLEAR RST RETURN
003D 1B00		IN FDCST
003F C9		RET
0040 C22C00	DNI	JNZ UPZ
0043 1604		MVI D,4
0045 2B	DNF	DCX E ;CHECK FOR FF AND SET 00 DOWN
0046 7F		MOV A,M
0047 91		SUB C
0048 C26900		JNZ PROM
004B 77		MOV M,A
004C 1B		DCX D
004D 7A		MOV A,D
004E B3		ORA E
004F C24500		JNZ DNF
0052 210010		LXI H,RAMAD+1024
0055 1604		MVI D,4
0057 2B	DNZ	DCX H ;CHECK FOR 00 AND SET FF DOWN
0058 7E		MOV A,M
0059 B7		ORA A
005A C26900		JNZ PROM
005D 71		MOV M,C
005E 1B		DCX D
005F 7A		MOV A,D
0060 B3		ORA E
0061 C25700		JNZ DNZ
0064 060E		MVI B,0EH
0066 78		MOV A,B

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #006 AMC 95/6110 SINGLE DENSITY FDC V1.3
0067 D333 ; OUT R3 ;SET NO RAM ERROR
;
; IPL PROM TEST - UP/DOWN CHECKSUM AND COMPARE
;
0069 110A01 PROM LXI D,ENTST
006C 210004 LXI H,1024
006F 4D MOV C,L
0070 1A UPC LDAX D ;CHECKSUM UPWARDS
0071 13 INX D
0072 81 ADD C
0073 4F MOV C,A
0074 2B DCX H
0075 7C MOV A,H
0076 B5 ORA I
0077 C27000 JNZ UPC
007A FE XCHG
007B 1604 MVI D,4
007D 91 SUB C ;COMPLEMENT CHECKSUM
007F 4F MOV C,A
007F 2B DNC DCX H
0080 7E MOV A,M ;CHECKSUM DOWNWARDS
0081 81 ADD C
0082 4F MOV C,A
0083 1B DCX D
0084 7A MOV A,D
0085 B3 ORA E
0086 C27F00 JNZ INC
0089 B1 ORA C
008A C29300 JNZ DMA
008D 78 MOV A,B
008E E60D ANI 0DE
0090 47 MOV E,A
0091 F333 OUT R3 ;SET NO PROM ERROR
;
; IPL DMA TEST - MEMORY/MEMORY TRANSFER
;
0093 D31D DMA OUT DMCLR ;RESET IMA
0095 0EFF MVI C,0FFF
0097 110A01 LXI I,ENTST
009A 21000C LXI E,RAMAD
009D 79 MOV A,C
009E D311 OUT IM0WC ;SOURCE WORD COUNT
00A0 AF XRA A

```


TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#008	AMC 95/6110 SINGLE DENSITY FDC V1.3
00E7 1F	RAR	
00E8 FA0A01	JC	ENTST ;BUSY
00FB 79	MOV	A,C
00EC 1301	OUT	FDTRK ;SET TRACK REGISTER
00EE 7A	MOV	A,D
00EF D302	OUT	FDSFC ;SET SECTOR REGISTER
00F1 7B	MOV	A,E
00F2 D303	OUT	FDATA ;SET DATA REGISTER
00F4 DB01	IN	FDTRK
00F6 91	SUB	C
00F7 4F	MOV	C,A ;CHECK TRACK REGISTER
00F8 DB02	IN	FDSEC
00FA 92	SUB	D
00FB B1	ORA	C ;CHECK SECTOR REGISTER
00FC 4F	MOV	C,A
00FD DB03	IN	FDATA
00FF 93	SUB	E
0100 B1	ORA	C ;CHECK DATA REGISTER
0101 C20A01	JNZ	ENTST
0104 79	MOV	A,B
0105 E607	ANI	7
0107 47	MOV	B,A
0108 D333	OUT	R3 ;SET NO FDC ERROR
	:	
	;	INITIALIZE WORKING STORAGE
	:	
010A 31200C	ENTST LXI	SP,STACK
010D AF	XRA	A
010E D301	OUT	FDTRK ;SET TRACK 0
0110 D34B	OUT	CMDRES ;CLEAR COMMAND FF
0112 21FFFF	LXI	H,-1
0115 22010C	SHLD	POSN ;CLEAR UNIT POSITIONS
0118 22030C	SHLD	POSN+2
011B 23	INX	H
011C 2C	INR	L
011D 22050C	SHLD	SECTOR ;SECTOR 1, TRACK 0
0120 32130C	STA	INTFLG ;NO INTERRUPT REQUEST
0123 3C	INR	A
0124 32140C	STA	SECINC ;1/1 INTERLACE
0127 3E08	MVI	A,8
0129 32080C	STA	RECNT ;RETRY COUNT-1
012C 07	RLC	
012D 4F	MOV	C,A

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #009 AMC 95/6110 SINGLE DENSITY FDC V1.3

012E 32070C STA UNIT ;UNIT 0 WITH RETRY
IF TYPE EQ 6120
MVI A,READ
STA IOCODE ;SET NO SIDE COMPARE FOR READ/WRITE
MVI A,0CH
ELSE
0131 3E04 MVI A,4
ENDIF
0133 D34D OUT DRSEL ;UNIT ZERO, SINGLE DENSITY, SIDE 0
0135 3E7F MVI A,127
0137 32000C STA SECLEN ;SECTOR LENGTH-1
013A 21E102 LXI H,FUNTN
013D 220B0C SHLD JPTAB ;MISCELLANEOUS FUNCTION JUMP
0140 211F05 LXI F,NPRED
0143 220D0C SHLD JPTAB+2 ;NON-BUFFERED READ JUMP
0146 21C505 LXI H,NBRIT
0149 220F0C SHLD JPTAB+4 ;NON-BUFFERED WRITE JUMP
014C 213406 LXI H,PGMRD
014F 22110C SHLD JPTAB+6 ;USER PROGRAM READ JUMP
0152 78 MOV A,B
0153 B7 ORA A
0154 C26701 RNZ SETCOM ;GO SET COMPLETE ON IPL ERROR
0157 RIM
0158 B7 ORA A
0159 F26906 JP BOOT ;GO BOOT SYSTEM 29
;
; STATUS REQUEST C=UNIT
;
015C C19201 STREQ CALL SELUN ;SET UNIT STUFF
015F 79 MOV A,C
0160 C16202 CALL READY
0163 0F SIDSTA RRC
0164 31200C ILLCOM LXI SP,STACK
0167 F680 SETCOM ORI 80H ;SET COMPLETE
0169 D333 OUT R3 ;TELL USER
016P 3A130C LDA INTFLG
016E D348 OUT CMDSTA ;SET/CLEAR INTERRUPT
0170 DE48 CMDLP IN CMDSTA ;CHECK FOR USER COMMAND
0172 B7 ORA A
0173 F27001 JP CMDIP
0176 D34B OUT CMDRES ;CLEAR COMMAND FF
0178 DB33 IN R3 ;FETCH REQUEST
017A 5F MOV E,A

```


TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#010	AMC 95/6110 SINGLE DENSITY FDC V1.3
017B E63F		ANI 3FH
017D 4F		MOV C,A ;COUNT-1
017E AB		XRA E
017F 07		RLC
0180 07		RLC
0181 07		RLC
0182 5F		MOV E,A
0183 AF		XRA A
0184 57		MOV D,A
0185 131D		OUT DMCLR ;RESET DMA
0187 210F0C		LXI H,JPTAB
018A 19		DAD D
018B 5E		MOV E,M ;FETCH VECTOR JUMP
018C 23		INX H
018D 56		MOV D,M
018E DB30		IN R0 ;PAGE/UNIT
0190 EB		XCHG
0191 E9		PCHL ;GO TO JUMP ADDRESS
	;	
	;	SELECT UNIT AND SET VARIABLES C=UNIT
	;	
0192 79	SELUN	MOV A,C
0193 32070C		STA UNIT
0196 21070C	SETUN	LXI H,UNIT
0199 46		MOV B,M ;SAVE PRIOR DRIVE
019A 71		MOV M,C
019B 79		MOV A,C
019C E608		ANI E
019F 17		RAL
019F 17		RAL
01A0 17		RAL
01A1 17		RAL
01A2 C67F		ADI 127
01A4 32000C		STA SECLN ;SECTOR LENGTH-1
01A7 79		MOV A,C
01A8 E610		ANI 10H
01AA 0F		RRC
01AB 32080C		STA RFCNT ;RETRY COUNT-1
01AE 79		MOV A,C
01AF 07		RLC
01B0 F601		ANI 1
01B2 3C		INR A
01B3 32140C		STA SECINC ;INTERLACE

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#011	AMC 95/6110 SINGLE DENSITY FDC V1.3
01B6 79		MOV A,C
01B7 0F		RRC
01B8 E620		ANI 20H
01BA 32130C		STA INTFLG ;INTERRUPT REQUEST
01BD 79		MOV A,C
01BE 11C505		LXI I,NBRIT
01C1 211F05		LXI H,NBRED
01C4 E620		ANI 20H
01C6 CACF01		JZ SETVEC
01C9 113704		LXI D,BFRIT
01CC 210703		LXI H,BFRED
01CF 220D0C	SETVEC	SHLD JPTAB+2 ;SET JUMP TABLE ADDRESSES
01D2 FB		XCHG
01D3 220F0C		SHLD JPTAB+4
01D6 79		MOV A,C
		IF TYPE EQ 6120
		ANI 0FH
		XRI 0CH
		ELSE
01D7 E607		ANI 7
01D9 EB04		XRI 4
		ENDIF
01DB D34D		OUT DRSEL ;SELECT DRIVE
01DD E603		ANI 3
01DF 5F		MOV E,A
01E0 1600		MVI D,0
01E2 21010C		LXI H,POSN
01E5 19		DAD D
01E6 7E		MOV A,M ;CURRENT UNIT POSITION
01E7 D301		OUT FDIRK ;TELL 1771
01E9 79		MOV A,C
01EA A8		XRA B
01EB E603		ANI 3
01ED C8		RZ ;SAME DRIVE
01EE 7E		MOV A,M
01FF 1610		MVI D,UNLOD
01F1 CD8502		CALL LOADA ;UNLOAD HEAD
01F4 C30004		JMP POSNC ;AND POSITION NEW DRIVE
		;
		;
		HOME REQUEST C=UNIT
01F7 CD1502	HMREQ	CALL HOME
		IF TYPE EQ 6120

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0  #012  AMC 95/6110 SINGLE DENSITY FDC V1.3

                                INR      A
                                ENDIF
01FA E6F9      PUTST1 ANI      0F9H      ;PUT STATUS TYPE I
01FC 57        MOV      D,A
01FD 73        MOV      A,B
01FE 32050C    STA      SECTOR
0201 7A        MOV      A,D
0202 0F        RRC
0203 0F        RRC
0204 E606     ANI      6
0206 B2        ORA      D
0207 E6L6     ANI      0E6H
0209 5F        MOV      F,A
020A 7A        MOV      A,D
020B E601     ANI      1
020D 07        RLC
020E 07        RLC
020F 07        RLC
0210 07        RLC
0211 B3        ORA      E
0212 C36301   JMP      SIDSTA
;
; HOME FUNCTION C=UNIT
;
0215 CD9201   HOME CALL      SELUN
0219 0601     MVI      P,1
021A AF       XRA      A
021B 32060C   STA      TRACK
021E 3A080C   LDA      RECNT
0221 0F       RRC
0222 320A0C   STA      SKTRY
0225 CD3E02   HOMEL CALL     RESTORE
0228 F8       RM        ;NOT READY
0229 F604     ANI      4
022B 7B       MOV      A,E
022C C0       RNZ      ;GOOD HOME
022D 210A0C   LXI      H,SKTRY
0230 35       DCR      M
0231 F22502   JP      HOMEL      ;RETRY
0234 C9       RET
;
; RESET NON-BUFFERED ADDRESS - - FALL INTO RESTORE - -
;

```

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #013 AMC 95/6110 SINGLE DENSITY FDC V1.3

0235 2A002F RSNBA IHLT BUFF
0233 7D MOV A,L
0239 D316 OUT DM3AD
023E 7C MOV A,H
023C D316 OUT FM3AD
;
; EXECUTE RESTORE
;
023E 3A070C RESTORE LDA UNIT
0241 CD6202 CALL READY
0244 FB RM ;NOT READY
0245 3A070C LIA UNIT
0248 F603 ANI 3
024A 5F MOV E,A
024E 1600 MVI D,0
024D 21010C LXI E,POSN
0250 19 DAD D
0251 72 MOV M,D ;SET POSTION ZERO
0252 160A MVI D,RESTR
0254 CD8702 CALL ISSUE
0257 E6DC ANI 0DCH
0259 5F STSID MOV E,A
025A DB49 IN CMDSTA
025C E610 ANI 10H
025F 07 RLC
025F B3 ORA E
0260 5F MOV E,A
0261 C9 RET
;
; CHECK READY FOR TYPE I COMMANDS
;
READY IF TYPE EQ 6120
ANI 0FH
XRI 1CH
ELSE
0262 E607 READY ANI 7
0264 EE0C XRI 0CH
ENDIF
0266 D34D OUT ERSEL
0268 57 MOV D,A
0269 3ED0 MVI A,FRCIN
026B D300 OUT FDCST
026D E5 PUSH H

```

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#014	AMC 95/6110 SINGLE DENSITY FDC V1.3
026F E1	POP	H
026F E5	PUSH	H
0270 E1	POP	H
0271 DB00	IN	FDCST
0273 E6C0	ANI	0C0H
0275 C15902	CALL	STSID
0278 7A	MOV	A,D
	IF	TYPE EQ 6120
	ANI	0FH
	ELSE	
0279 E607	ANI	7
	ENDIF	
027B D34D	OUT	DRSEL
027E 7B	MOV	A,E
027E B7	ORA	A
027F C9	RET	
	;	
	;	LOAD HEAD FOR READ/WRITE
	;	
0280 1616	LOAD MVI	D,LDHED
0282 3A060C	LDA	TRACK
0285 D303	LOADA OUT	FDATA
	;	
	;	ISSUE COMMAND IN D
	;	
0287 1E00	ISSUE MVI	E,0
0289 1D	ISSUEA DCR	E
029A CAA902	JZ	ISSUEC :BUSY
028D DB00	IN	FDCST
028F 1F	RAR	
0290 DA9902	JC	ISSUEA
0293	SIM	1BH ;CLEAR INTERRUPT
0296 7A	MOV	A,D
0297 D300	ISSUEE OUT	FDCST ;ISSUE COMMAND
0299 FB	EI	
029A 11D007	ISSUED LXI	D,2000
029D AF	ISSUEB XRA	A
029E 3D	ISSUEF DCR	A
029F C29E02	JNZ	ISSUEF ;WAIT FOR INTERRUPT
02A2 1B	DCX	D
02A3 7A	MOV	A,D
02A4 E3	ORA	E
02A5 C29D02	JNZ	ISSUEB

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #015 AMC 95/6110 SINGLE DENSITY FDC V1.3

02A8 F3          DI
02A9 7E          ISSUEC MOV    A,B
02AA 32050C      STA    SECTOR
02AD 3E06        MVI    A,6
02AF C36401      JMP    ILLCOM ;NO INTERRUPT
;
;               SET PARAMETER REQUEST C=UNIT, HL=TRACK/SECTOR
;
02B2 DB31        SETPAR IN     R1
02B4 67          MOV    H,A
02B5 DB32        IN     R2
;               IF TYPE EQ 6120
MOV    B,A
ANI    7FH
ENDIF
02B7 6F          MOV    L,A
02B8 22050C      SHLD  SECTOR
;               IF TYPE FQ 6120
MVI    L,80H
MOV    A,B
ANA    L           ;STRIP COMPARE FLAG
RLC
MOV    B,A
MOV    A,C
ANI    4           ;STRIP SIDE FLAG
ORA    B
RLC
ORA    L
STA    IOCODE     ;SET CONDITIONAL READ/WRITE
ENDIF
02BB CD9601      CALL  SETUN     ;SET UNIT STUFF
02BE AF          BRTN  XRA    A
02BF C36701      JMP    SETCOM
;
;               CLEAR INTERRUPT REQUEST
;
02C2 AF          CLRINT XRA    A
02C3 47          NOINT MOV    B,A
02C4 AF          XRA    A
02C5 D343        OUT   CMDSTA ;CLEAR INTERRUPT
02C7 78          MOV    A,B
02C8 F680        ORI    80H
02CA D333        OUT   R3

```

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #016 AMC 95/6110 SINGLE DENSITY FDC V1.3
02CC C37001 JMP CMDLP
;
; RETURN UNIT REQUEST
;
02CF 3A070C INTUNT LDA UNIT
02D2 C3C302 JMP NOINT
;
; RETURN TRACK REQUEST
;
02D5 3A060C INTTRK LDA TRACK
02D8 C3C302 JMP NOINT
;
; RETURN SECTOR REQUEST
;
02DE 3A050C INTSEC LDA SECTOR
02DE C3C302 JMP NOINT
;
; REQUEST CODES 0-63
;
02E1 59 FUNTN MOV E,C
02E2 4F MOV C,A
02E3 7B MOV A,E
02E4 FE06 CPI 8
02E6 3F05 MVI A,5
02E8 D26701 JNC SETCOM ;ILLEGAL FUNCTION
02EB 1600 MVI D,0
02ED 21F702 LXI H,VECTAB
02F0 19 DAD D
02F1 19 DAD D
02F2 5F MOV E,M
02F3 23 INX H
02F4 56 MOV D,M
02F5 FB XCHG
02F6 E9 PCHL
02F7 F701 VECTAB DW HMREQ ;HOME REQUEST
02F9 B202 DW SETPAR ;SET I/O PARAMETERS
02FB 5C01 DW STREQ ;STATUS REQUEST
02FD C202 DW CLRINT ;CLEAR INTERRUPT REQUEST
02FF CE06 DW INIDSK ;INITIALIZE DISK REQUEST
0301 CF02 DW INTUNT ;INTERROGATE UNIT
0303 D502 DW INTTRK ;INTERROGATE TRACK
0305 DB02 DW INTSEC ;INTERROGATE SECTOR
;

```

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #017 AMC 95/6110 SINGLE DENSITY FDC V1.3

;      MULTIPLE SECTOR BUFFERED READ A=PAGE
:
0307 D34A      BFRED  OUT      SEGMT      ;SET PAGE
0309 3F00      MVI      A,BUFF-BUFF/256*256
030B D310      OUT      DM0AD      ;M/M SOURCE ADDRESS
030E 3E0F      MVI      A,BUFF/256
030F D310      OUT      IM0AD
0311 DB32      IN       R2
0313 D312      OUT      IM1AD      ;M/M DESTINATION ADDRESS
0315 DB31      IN       R1
0317 D312      OUT      DM1AD
0319 AF        XRA      A
031A 32000C    STA      RETRY      ;SET READ RETRY
031D 3E00      BFREDR  MVI      A,BUFF-BUFF/256*256
031F D316      OUT      IM3AD      ;INPUT ADDRESS
0321 3E0F      MVI      A,BUFF/256
0323 D316      OUT      IM3AD
0325 3A000C    LDA      SECLEN
0328 6F        MOV      L,A
0329 D311      OUT      DM0WC      ;M/M SOURCE WORD COUNT
032B AF        XRA      A
032C D311      OUT      IM0WC
032E 7D        MOV      A,L
032F D317      OUT      IM3WC      ;INPUT WORD COUNT
0331 AF        XRA      A
0332 D317      OUT      DM3WC
0334 57        MOV      D,A
0335 3F98      MVI      A,98H
0337 D31B      OUT      IMMDE      ;M/M SOURCE MODE
0339 3E85      MVI      A,85H
033F D31F      OUT      IMMDE      ;M/M DESTINATION MODE
033D 3E57      MVI      A,57H
033F D31B      OUT      IMMDE      ;INPUT MODE
0341 3A050C    LDA      SECTOR
0344 47        MOV      B,A
0345 CDEF03    BFREDL  CALL     POSITN  ;READ LOOP B=SECTOR. C=COUNT, (HL)=POSITION
0348 FAFA01    JM      PUTST1
034E AF        BFREDS  XRA      A
034C D348      OUT      CMDSTA  ;INPUT TO LOCAL BUFFER
034F 78        MOV      A,P
034F D302      OUT      FDSEC   ;DESIRED SECTOR
0351 3ED0      MVI      A,FRCIN
0353 D302      OUT      FDCST   ;REQUEST STATUS I

```


TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#018	AMC 95/6110 SINGLE DENSITY FDC V1.3
0355 3E40		MVI A,40H
0357 E318		OUT IMCST ;COMMAND DMA
0359 3E07		MVI A,7
035B D31F		OUT IMMSK ;ENABLE CHANNEL 3
035D		SIM 1BH
0360 DB00		IN FICST ;HEAD LOAD STATUS
0362 E620		ANI 20H
0364 CC8002		CZ LOAD
		IF TYPE FQ 6120
		LDA ICCODE
		ELSE
0367 3F88		MVI A,READ
		ENDIF
0369 CD9702		CALL ISSUEF ;EXECUTE READ
036C E69C		ANI RIMSK
036E CAA203		JZ BFRDGD ;GOOD READ
0371 FA8C03		JM PUTST2 ;NOT READY
0374 57		MOV L,A
0375 3E0F		MVI A,0FH
0377 D31F		OUT IMMSK ;DISABLE CHANNEL 3
0379 21090C		LXI H,RETRY
037C 34		INR M
037E 3A080C		LDA RECNT
0380 BF		CMP M
0381 7A		MOV A,D
0382 FA8C03		JM PUTST2 ;END RETRY
0385 CD3E02		CALL RSTORF
0388 C31D03		JMP BFRDR
038B AF	PUTST3	XRA A
038C 57	PUTST2	MOV I,A ;SAVE SECTOR/SET READ-WRITE STATUS
038D 73		MOV A,B
038E 32050C		STA SECTOR
0391 7A		MOV A,D
0392 E620		ANI 20H
0394 0F		RRC
0395 0F		RRC
0396 0F		RRC
0397 B2		CRA F
0398 E61C		ANI 0DCH
039A 57		MOV D,A
039B E61C		ANI 1CH
039E 82		ADD D
039E 0F		RRC

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#019	AMC 95/6110 SINGLE DENSITY FDC V1.3
039F C36701		JMP SETCOM
03A2 32090C	BFREIG	STA RETRY ;RESET RETRY
03A5 2F		CMA
03A6 D31F		OUT DMMSK ;DISABLE CHANNEL 3
03A8 3A000C		LDA SECLEN
03AB D313		OUT DM1WC ;M/M DESTINATION WORD COUNT
03AD AF		XRA A
03AE D313		OUT IM1WC
03B0 3F41		MVI A,41H
03B2 D318		OUT DMCST ;COMMAND DMA
03B4 3E04		MVI A,4
03B6 D348		OUT CMDSTA ;LOCAL BUFFER TO HOST
03B9 D319		OUT DMREQ ;REQUEST DMA
03BA DB18	BFRETW	IN DMCST ;WAIT DMA TRANSFER
03BC E602		ANI 2
03BE CABA03		JZ BFREDD
03C1 3A140C		LDA SECINC
03C4 90		ADD F ;ADVANCE SECTOR
03C5 47		MOV B,A
03C6 D61E		SUI 27
03C8 DAF103		JC BFREDD ;NOT END TRACK
03CB C2D103		JNZ BFREDA ;END 2/1 INTERLACE TRACK
03CE 3A140C		LDA SECINC
03D1 47	BFRETA	MOV F,A
03D2 3E		DCR A
03D3 C2E103		JNZ BFREDD ;END 2/1 INTERLACE HALF TRACK
03D6 21060C		LXI H,TRACK
03D9 7E		MOV A,M
03DA 3C		INR A ;ADVANCE TRACK
03DB FE4D		CPI 77
03DD CA8B03		JZ PUTST3 ;DISK OVERFLOW
03E0 77		MOV M,A
03E1 0E	BFREDD	DCR C ;CHECK SECTOR COUNT
03E2 FA8B03		JM PUTST3 ;END REQUEST
03E5 3E01		MVI A,1
03E7 90		SUB E
03E8 C24B03		JNZ BFREDS ;SAME TRACK
03EB 57		MOV D,A
03EC C34503		JMP BFREDD ;DIFFERENT TRACK
	:	
	;	RE-POSITION TRACK
	;	
03EF 3A070C	POSITN	LDA UNIT

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#020	AMC 95/6110 SINGLE DENSITY FDC V1.3
03F2 E603		ANI 3
03F4 5F		MOV E,A
03F5 1600		MVI D,0
03F7 21010C		LXI H,POSN
03FA 19		DAD D
03FB 3A060C		LDA TRACK
03FE BE		CMP M
03FF C8		RZ
0400 3A080C	POSNC	LDA RFCNT
0403 0F		RRC
0404 320A0C		STA SKTRY ;RETRY COUNT
0407 7E	POSNA	MOV A,M
0408 B7		ORA A
0409 FA2C04		JM POSND ;INITIAL REFERENCE - RESTORE FOR SYNC
040C 3A070C		LDA UNIT
040F CD6202		CALL READY
0412 F8		RM
0413 3A060C		LDA TRACK
0416 D303		OUT FDATA
0418 77		MOV M,A ;UPDATE POSITION
0419 161E		MVI D,SEEK
041B CD8702		CALL ISSUE
041E E698		ANI 9EH
0420 C8		RZ ;GOOD SEEK
0421 F3		RM ;NOT READY
0422 5F		MOV E,A
0423 3A0A0C	POSNB	LDA SKTRY
0426 3D		DCR A
0427 320A0C		STA SKTRY
042A 7E		MOV A,E
042B F3		RM ;END RETRY
042C CD3E02	POSND	CALL RESTORE
042F E604		ANI 4
0431 C20704		JNZ POSNA
0434 C32304		JMP POSNB
	;	
	;	MULTIPLE SFCTOR BUFFERED WRITE A=PAGE
	;	
0437 D34A	BFRIT	OUT SEGMT ;SET PAGE
0439 3E00		MVI A,BUFF-BUFF/256*256
043E D312		OUT DM1AD ;M/M DESTINATION ADDRESS
043D 3E0F		MVI A,BUFF/256
043F D312		OUT DM1AD

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#021	AMC 95/6110 SINGLE DENSITY FDC V1.3
0441	DB32	IN R2
0443	D310	OUT IM0AL ;M/M SOURCE ADDRESS
0445	DB31	IN R1
0447	D310	OUT IM0AD
0449	3E00	MVI A,BUFF-BUFF/256*256
044B	D316	OUT IM3AD ;OUTPUT ADDRESS
044D	3E0F	MVI A,BUFF/256
044F	D316	OUT IM3AD
0451	3A000C	LTA SECLEN
0454	6F	MOV L,A
0455	D313	OUT IM1WC ;M/M DESTINATION WORD COUNT
0457	AF	XRA A
0459	D313	OUT DM1WC
045A	7D	MOV A,L
045B	D317	OUT IM3WC ;OUTPUT WORD COUNT
045D	AF	XRA A
045E	D317	OUT IM3WC
0460	57	MOV D,A
0461	3E98	MVI A,98H
0463	D31B	OUT IMMDE ;M/M SOURCE MODE
0465	3E95	MVI A,95H
0467	D31B	OUT IMMDE ;M/M DESTINATION MODE
0469	3E5B	MVI A,5BH
046B	D31B	OUT IMMDE ;OUTPUT MODE
046D	3A050C	LDA SECTOR
0470	47	MOV F,A
0471	CDEF03	BFRITL CALL POSITN ;WRITE LOOP B=SECTOR, C=COUNT, (HI)=POSITION
0474	Fafa01	JM PUTST1
0477	3A000C	BFRITS LDA SECLEN
047A	D311	OUT IM0WC ;M/M SOURCE WORD COUNT
047C	AF	XRA A
047D	32090C	STA RETRY ;SET RETRY COUNT
0480	D311	OUT IM0WC
0482	3E41	MVI A,41H
0484	D318	OUT IMCST ;COMMAND DMA
0486	3E06	MVI A,6
0488	D349	OUT CMDSTA ;HOST TO LOCAL BUFFER
048A	3E04	MVI A,4
048C	D319	OUT IMREQ ;REQUEST DMA
048E	DE18	BFRITW IN IMCST ;WAIT DMA TRANSFER
0490	E602	ANI 2
0492	CA8E04	JZ BFRITW
0495	AF	BFRITR XRA A

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#022	AMC 95/6110 SINGLE DENSITY FDC V1.3
0496 D34B	OUT	CMDSTA ;OUTPUT FROM LOCAL BUFFER
0498 78	MOV	A,B
0499 D302	OUT	FDSEFC ;DESIREFT SECTOR
049B 3ED0	MVI	A,FRCIN
049E D300	OUT	FDCST ;REQUEST STATUS I
049F 3E40	MVI	A,40H
04A1 D318	OUT	DMCST ;COMMAND DMA
04A3 3E07	MVI	A,7
04A5 D31F	OUT	DMMSK ;ENAELE CHANNEL 3
04A7	SIM	1BH
04AA DB00	IN	FDCST ;HEAD LOAD STATUS
04AC E620	ANI	20H
04AE CC8002	CZ	LOAD
	IF TYPE	EQ 6120
	LDA	IOCODE
	ORI	20H
	ELSE	
04P1 3EAB	MVI	A,WRITE
	ENDIF	
04B3 C19702	CALL	ISSUEE ;EXECUTE WRITE
04B6 F6FC	ANI	WRMSK
04B8 CAEE04	JZ	BFRITG ;GOOD WRITE
04BB 57	MOV	D,A
04BC E6C0	ANI	0C0H
04BE 7A	MOV	A,D
04BF C28C03	JNZ	PUTST2 ;NOT READY OR WRITE PROTECT
04C2 3F0F	MVI	A,0FH
04C4 D31F	OUT	DMMSK ;DISABLE CHANNEL 3
04C6 21090C	LXI	H,RETRY
04C9 34	INR	M
04CA 3A080C	LDA	RECNT
04CD BE	CMP	M
04CE 7A	MOV	A,D
04CF FA8C03	JM	PUTST2 ;END RETRY
04D2 C13E02	CALL	RESTORE
04D5 C1EF03	CALL	POSITN
04D8 FAFA01	JM	PUTST1
04EB 3E00	MVI	A,BUFF-BUFF/256*256
04ED D316	OUT	DM3AD ;RESET OUTPUT ADDRESS
04EF 3E0F	MVI	A,BUFF/256
04F1 D316	OUT	DM3AD
04F3 3A000C	LDA	SECLEN
04E6 D317	OUT	DM3WC ;RESET OUTPUT WORD COUNT

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #023 AMC 95/6110 SINGLE DENSITY FDC V1.3

04E8 AF XRA A
04E9 D317 OUT DM3WC
04FB C39504 JMP BFRITR
04EE 2F BFRITG CMA
04EF D31F OUT DMMSK ;DISABLE CHANNEL 3
04F1 3A140C LDA SECINC
04F4 80 ADD B ;ADVANCE SECTOR
04F5 47 MOV B,A
04F6 D61B SUI 27
04F9 DA1105 JC BFRITD ;NOT END TRACK
04FB C20105 JNZ BFRITA ;END 2/1 INTERLACE TRACK
04FE 3A140C LIA SECINC
0501 47 BFRITA MOV B,A
0502 3D DCR A
0503 C21105 JNZ BFRITD ;END 2/1 INTERLACE HALF TRACK
0506 21060C LXI H,TRACK
0509 7E MOV A,M
050A 3C INR A ;ADVANCE TRACK
050B FE4D CPI 77
050D CA8B03 JZ PUTST3 ;DISK OVERFLOW
0510 77 MOV M,A
0511 0D BFRITD DCR C ;CHECK SECTOR COUNT
0512 FA8B03 JM PUTST3 ;END REQUEST
0515 3E01 MVI A,1
0517 90 SUB B
0518 C27704 JNZ BFRITS ;SAME TRACK
051B 57 MOV D,A
051C C37104 JMP BFRITL ;DIFFERENT TRACK
;
; MULTIPLE SECTOR NON-BUFFERED READ A=PAGE
;
051F D34A NBRED OUT SEGMT ;SET PAGE
0521 DB32 IN R2
0523 D316 OUT DM3AD ;INPUT ADDRESS
0525 DB31 IN R1
0527 D316 NBREDB OUT DM3AD
0529 3F47 MVI A,47H
052B D31B OUT DMMDE ;INPUT MODE
052D 3E02 MVI A,2
052F D348 OUT CMDSTA ;INPUT TO HOST
0531 3E40 MVI A,40H
0533 D318 OUT DMCST ;COMMAND DMA
0535 3A050C LDA SECTOR

```

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #024 AMC 95/6110 SINGLE DENSITY FDC V1.3

0538 47          MOV      B,A
0539 AF          XRA      A
053A 320900     STA      RETRY ;SET READ RETRY
053D CDEF03     NBEREDR CALL    POSITN
0540 FAFA01     JM       PUTST1
0543 3A000C     NBREDL  LDA      SFCLEN
0546 D317      OUT      DM3WC ;INPUT WORD COUNT
0548 AF          XRA      A
0549 D317      OUT      DM3WC
054B DB16      IN       DM3AD
054D 6F         MOV      L,A
054E DB16      IN       DM3AD
0550 57         MOV      H,A
0551 22000F     NBRFDS  SHLD    BUFF ;SAVE ADDRESS FOR RETRY
0554 78         MOV      A,B
0555 D302      OUT      FDSEC ;DESIRED SECTOR
0557 3ED0      MVI     A,FRGIN
0559 D300      OUT      FDCST ;REQUEST STATUS 1
055B 3E07      MVI     A,7
055D D31F      OUT      IMMSK ;ENABLE CHANNEL 3
055F           SIM     1FH
0562 DE00      IN       FDCST ;HEAD LOAD STATUS
0564 E620      ANI     20H
0566 CC8202     CZ      LOAI
IF TYPE EQ 6120
LDA      ICCODE
ELSE
0569 3E38      MVI     A,READ
ENDIF
056E CD9702     CALL    ISSUE ;EXECUTE READ
056E E69C      ANI     RDMSK
0570 C81005     JZ      NBEREDG ;GOOD READ
0573 FA8C03     JM      PUTST2 ;NOT READY
0576 57         MOV     D,A
0577 3E2F      MVI     A,0FH
0579 131F      OUT     IMMSK ;DISABLE CHANNEL 3
057B 21090C     LXI    H,RETRY
057E 34         INR    M
057F 3A080C     LDA    HECNT
0582 BE        CMP    M
0583 7A        MOV    A,D
0584 FA8C03     JM      PUTST2 ;END RETRY
0587 CD3502     CALL    RSNBA

```

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#025		AMC 95/6110 SINGLE DENSITY FDC V1.3
058A C33D05		JMP	NBREDR
058D 32090C	NBREDG	STA	RETRY ;RESET RETRY COUNT
0590 2F		CMA	
0591 D31F		OUT	DMMSK ;DISABLE CHANNEL 3
0593 3A140C		LIA	SECINC
0596 80		AID	B ;ADVANCE SECTOR
0597 47		MOV	B,A
0598 D61B		SUI	27
059A DAB305		JC	NBREDD ;NOT END TRACK
059D C2A305		JNZ	NBREDA ;END 2/1 INTERLACE TRACK
05A0 3A140C		LIA	SECINC
05A3 47	NBKEDA	MOV	E,A
05A4 3D		DCR	A
05A5 C2B305		JNZ	NBREDD ;END 2/1 INTERLACE HALF TRACK
05A8 21060C		LXI	F,TRACK
05AB 7E		MOV	A,M
05AC 3C		INR	A ;ADVANCE TRACK
05AD FF4D		CPI	77
05AF CA8E03		JZ	PUTST3 ;DISK OVERFLOW
05B2 77		MOV	M,A
05B3 0D	NBREDT	DCR	C ;CHECK SECTOR COUNT
05B4 79		MOV	A,C
05B5 3C		INR	A
05B6 CA8E03		JZ	PUTST3 ;END REQUEST
05B9 FA7506		JM	FOOTA ;SYSTEM 29 BOOT EXIT
05BC 3E01		MVI	A,1
05BE 90		SUB	E
05BF C25405		JNZ	NBREDS ;SAME TRACK
05C2 C33D05		JMP	NBREDR ;DIFFERENT TRACK
	;		
	;		
	;		
			MULTIPLE SECTOR NON-BUFFERED WRITE A=PAGE
05C5 D34A	NBRIT	OUT	SEGMT ;SET PAGE
05C7 DB32		IN	R2
05C9 D316		OUT	IM3AD ;OUTPUT ADDRESS
05CB LP31		IN	R1
05CD D316		OUT	DM3AD
05CF 3E4F		MVI	A,4BH
05I1 D31B		OUT	IMMDE ;OUTPUT MODE
05D3 3E02		MVI	A,2
05D5 D348		OUT	CMDSTA ;OUTPUT FROM HOST
05D7 3F40		MVI	A,40H
05D9 D31B		OUT	DMCST ;COMMAND DMA

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#026	AMC 95/6110 SINGLE DENSITY FDC V1.3
05DB 3A050C		LDA SECTOR
05DF 47		MOV E,A
05DF AF		XRA A
05E0 32090C		STA RETRY ;SET WRITE RETRY
05E3 CDEF03	NBRITR	CALL POSITN
05E6 FAFA01		JM PUTST1
05E9 3A000C	NBRITL	LDA SECLEN
05EC 1317		OUT DM3WC ;OUTPUT WORD COUNT
05EE AF		XRA A
05EF 1317		OUT DM3WC
05F1 DB16		IN DM3AD
05F3 6F		MOV L,A
05F4 DB16		IN DM3AD
05F6 67		MOV E,A
05F7 22000F		SHLD BUFF ;SAVE ADDRESS FOR RETRY
05FA 78	NBRITS	MOV A,B
05FB D302		OUT FDSEC ;DESIRED SECTOR
05FD 3ED0		MVI A,FRCIN
05FF 1300		OUT FDCST ;REQUEST STATUS 1
0601 3E07		MVI A,7
0603 D31F		OUT DMMSK ;ENABLE CHANNEL 3
0605		SIM 1BH
0608 DB00		IN FDCST ;HEAD LOAD STATUS
060A E620		ANI 20H
060C CC8002		CZ LOAD
		IF TYPE FQ 6120
		LDA IOCODE
		ORI 20H
		FLSE
060F 3EAB		MVI A,WRITE
		ENDIF
0611 CD9702		CALL ISSUEE ;EXECUTE WRITE
0614 E6FC		ANI WMSK
0616 CA3606		JZ NBRITG ;GOOD WRITE
0619 57		MOV I,A
061A E6C0		ANI 0C0H
061C 7A		MOV A,D
061F C28C03		JNZ PUTST2 ;NOT READY OR WRITE PROTECT
0620 3E0F		MVI A,0FH
0622 131F		OUT IMMSK ;DISABLE CHANNEL 3
0624 21090C		LXI H,RETRY
0627 34		INR M
0628 3A080C		LDA RECNT

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#027	AMC 95/6110 SINGLF DENSITY FDC V1.3
062B BE		CMP M
062C 7A		MCV A,D
062I FA8C03		JM PUTST2 ;END RETRY
0630 C13502		CALL RSNBA
0633 C3E305		JMP NBRITR
0636 32090C	NBRITG	STA RETRY ;RESET RETRY
0639 2F		CMA
063A D31F		OUT DMMSK ;DISABLE CHANNEL 3
063C 3A140C		LIA SECINC
063F 90		AID B ;ADVANCE SECTOR
0640 47		MOV B,A
0641 D61B		SUI 27
0643 IA5C06		JC NBRITD ;NOT END TRACK
0646 C24C06		JNZ NBRITA ;END 2/1 INTERLACE TRACK
0649 3A140C		LIA SECINC
064C 47	NBRITA	MOV B,A
064D 3D		DCR A
064E C25C06		JNZ NBRITD ;END 2/1 INTERLACE HALF TRACK
0651 21060C		LXI H,TRACK
0654 7E		MOV A,M
0655 3C		INR A ;ADVANCE TRACK
0656 FE4D		CPI 77
065B CA3E03		JZ PUTST3 ;DISK OVERFLOW
065B 77		MOV M,A
065C 0D	NBRITD	DCR C ;CHECK SECTOR COUNT
065D FA3B03		JM PUTST3 ;END REQUEST
0660 3E01		MVI A,1
0662 90		SUB F
0663 C2FA05		JNZ NBRITS ;SAME TRACK
0666 C3E305		JMP NBRITR ;DIFFERENT TRACK
	;	
	::	
	;	SPECIAL AUTO-BOOT FOR SYSTEM 29
0669 0EFF	BOOT	MVI C,0FFH ;BOOT FLAG
066B AF		XRA A
066C D34A		OUT SEGMT ;SET PAGE
066E I31D		OUT DMCLR ;RESET DMA
0670 D316		OUT DM3AD ;INPUT ADDRESS
0672 C32705		JMP NBREDE ;GO IO IT
0675 78	BOOTA	MOV A,E
0676 32050C		STA SECTOR
0679 D349		OUT RESET ;RETURNS HERE IF BOOT OK
067B D34E		OUT REISE ;RELEASE CPU

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #028 AMC 95/6110 SINGLE DENSITY FDC V1.3

067I 3F20 MVI A,20H
067F D348 OUT CMDSTA ;PULSE INTERRUPT
0681 C3BE02 JMP BRTN

;
;
;
PGMRD USER PROGRAM LOAD AND EXECUTE

0684 D34A PGMRD OUT SEGMENT ;SET PAGE
0686 3E06 MVI A,6
0688 1348 OUT CMDSTA ;HOST TO LOCAL MEMORY
068A D31D OUT DMCLR ;RESET DMA
068C 3E8E MVI A,8EH
068E 131B OUT DMMDF ;SOURCE MODE
0690 1B32 IN R2
0692 D310 OUT IM0AD ;SOURCE ADDRESS
0694 1F31 IN R1
0696 D310 OUT IM0AD
0698 21200C LXI H,PGMAD
069B 7D MOV A,L
069C D312 OUT DMIAD ;DESTINATION ADDRESS
069E 7C MOV A,H
06A1 1312 OUT DMIAD
06A3 131F OUT DMMDE ;DESTINATION MODE
06A5 79 MOV A,C
06A6 3C INR A
06A7 6F MOV L,A
06A8 2600 MVI H,0
06AA 29 DAD H ;VALUE TIMES 64
06AB 29 DAD H
06AC 29 DAD H
06AD 29 DAD H
06AE 29 DAD H
06AF 29 DAD H
06B0 7D MOV A,L
06B1 D311 OUT DM0WC ;SOURCE WORD COUNT
06B3 7C MOV A,H
06B4 D311 OUT DM0WC
06B6 7D MOV A,L
06E7 1313 OUT DMIWC ;DESTINATION WORD COUNT
06B9 7C MOV A,H
06BA D313 OUT DMIWC
06EC 3F41 MVI A,41H
06EE D318 OUT DMCST ;COMMAND LMA

```

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0      #029      AMC 95/6110 SINGLE DENSITY FDC V1.3

06C0 3E04                MVI      A,4
06C2 D319                OUT      DMREQ      ;REQUEST LMA
06C4 DE18                PGMRDW  IN      DMCST      ;WAIT DMA TRANSFER
06C6 E602                ANI      2
06C8 CAC406             JZ      PGMRDW
06CB C3200C             JMP      PGMAD      ;GO TO USER PROGRAM

;
;      INITIALIZE DISK - SINGLE DENSITY
;
06CE CD1502             INIDSK  CALL     HOME
06D1 3A0E0C             LDA     SECTOR
06D4 47                MOV     B,A
06D5 7B                MOV     A,E
06D6 E604                ANI     4
06D8 7B                MOV     A,E
06D9 CAFA01             JZ     PUTST1      ;HOME ERROR
06DC AF                XRA     A
06DD D34B             OUT     CMDSTA      ;DIRECTION
IF     TYPE EQ 6120
MOV     A,C
ANI     0CH
XRI     0CH
JZ     DINADV      ;DOUBLE AND SIDE 2
MOV     A,C
ANI     7
XRI     0CH
OUT     DRSEL      ;FORCE SINGLE DENSITY
ENDIF
06DE 21AC07             INIADV  LXI     H,INITAB
06E2 11200C             LXI     D,PGMAD
06E5 CF9C07             CALL    INIFIL      ;FORM TRACK MASK
06E8 3A060C             LDA     TRACK
06EB 32700C             STA     PGMAD+30
06EE 79                MOV     A,C
06EF E604                ANI     4
06F1 0F                RRC
06F2 0F                RRC
06F3 32710C             STA     PGMAD+81      ;SET SIDE
06F6 F31D             OUT     DMCLR      ;RESET DMA
06F8 21200C             LXI     H,PGMAD
06FB 7D                MOV     A,L
06FC D314             OUT     DM2AD      ;TRACK HEADER ADDRESS
06FE 7C                MOV     A,H

```

TABLE 3-1. (Cont.)

AMC MACRC ASSEM 1.0	#030	AMC 95/6110 SINGLE DENSITY FDC V1.3
06FF D314		OUT DM2AD
0701 3E48		MVI A,72
0703 D315		OUT DM2WC ;TRACK HEADER LENGTH
0705 AF		XRA A
0706 D315		OUT DM2WC
0708 3E4A		MVI A,4AH
070A D31F		OUT LMMDE ;MODE
070C 21690C		LXI H,PGMAD+73
070F 7D		MOV A,L
0710 D316		OUT IM3AD ;SECTOR BODY ADDRESS
0712 7C		MOV A,H
0713 D316		OUT IM3AD
0715 3EB9		MVI A,185
0717 D317		OUT DM3WC ;SECTOR BODY WORD COUNT
0719 AF		XRA A
071A D317		OUT DM3WC
071C 3E5B		MVI A,5BH
071E D31F		OUT IMMDE ;MODE
0720 3F40		MVI A,40E
0722 D319		OUT DMCST ;COMMAND
0724 3E03		MVI A,3
0726 D31F		OUT IMMSK ;MASK 2-3 ON
0728		SIM 1BH
072B 3EF4		MVI A,WRTRK
072D D300		OUT FDCST ;WRITE TRACK
072F 216D07		LXI H,ININT
0732 E5		PUSH H ;INTERRUPT ADDRESS
0733 FB		EI
0734 DB17	WAITC	IN DM3WC ;WAIT TIL PAST SECTOR NUMBER
0736 DE5D		SBI 93
0738 LB17		IN DM3WC ;UPPER ALWAYS ZERO
073A F23407		JP WAITC
073D 21720C		LXI H,PGMAD+82
0740 34		INR M ;ADVANCE SECTOR
0741 7E		MOV A,M
0742 FE1F		CPI 27
0744 CA5107		JZ INITLR
0747 DB13	WAITS	IN DMCST
0749 E608		ANI 8
074F CA4707		JZ WAITS ;WAIT CFANNEL 3 FCP
074E C33407		JMP WAITC ;GO FOR NEXT SECTOR
0751 21CA07	INITLR	LXI H,FILTAB
0754 11690C		LXI D,PGMAD+73

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#031	AMC 95/6110 SINGLE DENSITY FDC V1.3
0757 CD9C07		CALL INIFIL ;FILL TRAILER 1ST HALF
075A DB19	WAITT	IN DMCST
075C E608		ANI 8
075E CA5A07		JZ WAITT ;WAIT CHANNEL 3 EOP
0761 21CA07		LXI H,FILTAB
0764 11C60C		LXI D,PGMAD+166
0767 CD9C07		CALL INIFIL ;FILL TRAILER 2ND HALF
076A C39A02		JMP ISSUED ;WAIT TRACK INTERRUPT
076D 1EFC	ININT	MVI E,WRMSK ;INTERRUPT ON ENT TRACK
076F A3		ANA E
0770 C28C03		JNZ PUTST2 ;TRACK ERROR
0773 3A070C		LDA UNIT
0776 4F		MOV C,A
0777 E603		ANI 3
0779 21010C		LXI H,POSN
077C 35		ADD L
077D 6F		MOV L,A
077E 3E00		MVI A,0
0780 9C		ADC H
0781 67		MOV H,A
0782 3A060C		LDA TRACK
0785 3C		INR A ;ADVANCE TRACK
0786 FE4D		CPI 77
0788 CA8E03		JZ PUTST3 ;END INITIALIZATION
079B 32060C		STA TRACK
078E 77		MOV M,A
078F 165A		MVI I,STEP
0791 CD9702		CALL ISSUE ;STEP IN ONE TRACK
0794 E698		ANI 98H
0796 C2FA01		JNZ PUTST1 ;FAULT
		IF TYPE EQ 6120
		MOV A,C
		ANI 8
		JZ INIADV ;LOOP FOR NEXT TRACK
		MOV A,C
		ANI 0FH
		XRI 0CH
		OUT DRSEL ;RE SELECT DOUBLE DENSITY
INIADV		LXI H,PINTAB
		LXI D,PGMAD
		CALL INIFIL ;FORM DOUBLE TRACK MASK
		LDA TRACK
		STA PGMAD+162

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#032	AMC 95/6110 SINGLE DENSITY FDC V1.3
	MOV	A,C
	ANI	4
	RRC	
	RRC	
	STA	PGMAD+163 ;SIDE
	OUT	IMCLR ;RESET DMA
	LXI	H,PGMAD
	MOV	A,L
	OUT	DM2AD ;TRACK HEADER ADDRESS
	MOV	A,H
	OUT	IM2AD
	MVI	A,145
	OUT	DM2WC ;TRACK HEADER LENGTH
	XRA	A
	OUT	DM2WC
	MVI	A,4AH
	OUT	IMMDE ;MODE
	LXI	E,PGMAD+146
	MOV	A,L
	OUT	DM3AD ;SECTOR BODY ADDRESS
	MOV	A,H
	OUT	DM3AD
	MVI	A,113
	OUT	DM3WC ;SECTOR BODY LENGTH
	MVI	A,1
	OUT	IM3WC
	MVI	A,5BH
	OUT	IMMDE ;MODE
	MVI	A,40H
	OUT	IMCST ;COMMAND
	MVI	A,3
	OUT	IMMSK ;MASK CHANNELS 2-3 ON
	SIM	1EH
	MVI	A,WRTRK
	OUT	FDCST ;WRITE TRACK
	LXI	H,INIINT
	PUSH	H ;INTERRUPT ADDRESS
	EI	
	LXI	D,-185
WAITD	IN	DM3WC ;WAIT TIL PAST SECTOR NUMBER
	MOV	L,A
	IN	DM3WC
	MOV	H,A

TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #033 AMC 95/6110 SINGLE DENSITY FDC V1.3

                                DAD      D
                                JC        WAITD
                                LXI      E,PGMAD+164
                                INR      M      ;ADVANCE SECTOR
                                MOV      A,M
                                CPI      27
                                JZ       DNITLR ;END TRACK
WAITE IN      IMCST
                                ANI      8
                                JZ       WAITE ;WAIT END SECTOR
                                JMP      WAITD
DNITLR LXI    F,DILTAB
                                LXI    D,PGMAD+146
                                CALL   INIFIL ;FILL TRAILER 1ST HALF
WAITF IN      IMCST
                                ANI      8
                                JZ       WAITF ;WAIT END SECTOR
                                LXI    H,DILTAB
                                LXI    D,PGMAD+331
                                CALL   INIFIL ;FILL TRAILER 2ND HALF
                                JMP     ISSUED ;WAIT FOR TRACK INTERRUPT
                                ELSE
0799 C3DF06 JMP     INIADV ;LOOP FOR NEXT TRACK
                                ENDF

                                ;
                                ;      FILL TRACK MASK SUBROUTINE
                                ;
079C 4E      INIFIL MOV     C,M
079D 23      INX     H
079E 7E      MOV     A,M
079F 23      INX     H
07A0 12      INILUP STAX   D
07A1 13      INX     D
07A2 0D      DCR     C
07A3 C2A007 JNZ    INILUP
07A6 7F      MOV     A,M
07A7 B7      ORA     A
07A8 C29C07 JNZ    INIFIL
07AB C9      RFT

                                ;
07AC 28FF    INITAB DB     40,0FFH
07AE 0E00    DB     6,0
07B0 01FC    DB     1,0FCH

```


TABLE 3-1. (Cont.)

```

AMC MACRO ASSEM 1.0 #034 AMC 95/6110 SINGLE DENSITY FDC V1.3
07B2 1AFF DB 26,0FFH
07B4 0600 DB 6,0
07B6 01FF DB 1,0FFH
07B8 0200 DB 2,0
07BA 0101 DB 1,1
07BC 0100 DB 1,0
07BE 01F7 DB 1,0F7H
07C0 0FFF DB 11,0FFH
07C2 0600 DB 6,0
07C4 01FB DB 1,0FBH
07C6 80F5 DB 128,0F5H
07C8 01F7 DB 1,0F7H
07CA 1BFF FILTAB DB 27,0FFH
07CC 42FF DB 66,0FFE
07CE 00 DB 0
IF TYPE EQ 6120
FINTAB DB 90,4EH
DB 12,0
DB 3,0F6H
DB 1,0FCE
DB 50,4EH
DB 12,0
DB 3,0F5H
DB 1,0FEH
DB 2,0
DB 2,1
DB 1,0F7H
DB 22,4EH
DB 12,0
DB 3,0F5H
DB 1,0FBE
DB 128,40H
DB 129,40H
DILTAB DB 1,0F7H
DB 54,4EH
DB 131,4EH
DB 0
ENDIF
;
; WORKING STORAGE
;
0C00 ORG RAMAD
0C00 SECTEN DS 1 :SECTOR LENGTH-1

```

TABLE 3-1. (Cont.)

AMC MACRO ASSEM 1.0	#035	AMC 95/6110 SINGLE DENSITY FDC V1.3
0C01	PCSN DS	4 ;DISK UNIT POSITIONS
0C05	SECTOR DS	1 ;REQUEST SECTOR
0C06	TRACK DS	1 ;REQUEST TRACK
0C07	UNIT DS	1 ;REQUEST UNIT(AMONG OTHER THINGS)
0C08	RECNT DS	1 ;RETRY COUNT-1
0C09	RETRY DS	1 ;READ/WRITE RETRY
0C0A	SKTRY DS	1 ;SEEK/HOME RETRY
0C0B	JPTAB DS	9 ;JUMP TABLE(BITS 6-7 OF REQUEST)
0C13	INTFLG DS	1 ;INTERRUPT FLAG
0C14	SECINC DS	1 ;SECTOR INCREMENT
0C15	IOCODE DS	1 ;READ/WRITE CODE FOR SIDE VERIFY(6120 ONLY)
0C16	DS	RAMAD+32-\$
0C20 =	STACK EQU	\$;PROGRAM STACK
0C20 =	PGMAD EQU	\$;USER PROGRAM AREA
2F00 =	BUFF EQU	RAMAD+3*256 ;I/O BUFFER FOR BUFFERED COMMANDS
0C20	END	

the data (in sequence) from each of the mail-box registers. Multiple, concurrent disk unit operations cannot be performed. Depending on the command, the data from the other mail-box registers are used as operating parameters when the specified sequence of disk unit operations are performed. Each request is terminated by return of a status byte through the status register (R4), signifying completion, and (when errors occur) the error condition. The Command bit flip-flop is reset, waiting for the next command.

3-5. FIRMWARE INVOCATION

The firmware is initiated by a reset. It initially performs a confidence test before accepting commands. The confidence test initially writes a status byte of 0F to the status register R4 and subsequently clears each bit as the respective test completes successfully. The four tests, represented by status bits 0-3 are: RAM, ROM, DMA, and 1771 FDC. At the conclusion of all four tests, one of two procedures occur: If any of the tests failed, the COMPLETE flag is set and the firmware enters the host command wait loop. If no errors occur, the firmware does a STATUS request on drive zero and returns the same result as if requested by the host. If the SID line is low, the firmware automatically reads one sector at single density from side 0, track 0, sector 1 of drive zero, into host memory address 0 and releases the host CPU to execute the content of the sector.

3-6. SYSTEM BUS INTERFACE

The FDC interfaces with the host CPU through edge connector P1. Information is exchanged through the mail-box registers (R0-R4). The FDC board address is selectable and is established through setting switches SW1 through SW6. Five registers are selectable with the remaining two bits. R0 through R3 are available coincident

with a write operation; R4 is available coincident with a read operation.

For example, if the port address is 7CH, the register addresses (coincident with an output instruction) are 7CH through 7FH for registers R0 through R4, respectively. The status register (R4) is addressed by 7FH (coincident with an input instruction). Registers R3 and R4 appear to have the same address. However, because R3 is associated with an output operation and R4 is associated with an input operation, no conflict is introduced.

3-7. MAIL-BOX REGISTERS

Registers R0 through R3 are written by the master CPU and read by the on-board CPU. R4 is written by the on-board CPU and read by the master CPU. Registers R0, R1, and R2 are general purpose registers for parameter input. Register R3 is used as the command register. Register 4 is used as the status register.

Use of the mail-box registers is shown in table 3-2.

3-8. Unit Code

The Unit code is shown in figure 3-1.

Drive Select: specifies the disk drive

Side Select: specifies the side of a double-sided disk

Retries: enables or disables the automatic retry feature.

Data Transfer: specifies the mode in which data is transferred between the host CPU and the disk drive. When in direct mode (0), the DMA must initiate a bus request for each byte. When in buffered mode (1), 128 bytes are transferred from master memory to buffer memory with one DMA bus request,

TABLE 3-2. MAILBOX REGISTER FUNCTIONS.

Command	R0	R1	R2	R3	R4
HOME	UNIT CODE	-	-	0	STATUS
SETPAR	UNIT CODE	TRACK	SECTOR	1	STATUS
STATUS	UNIT CODE	-	-	2	STATUS
CLRINT	-	-	-	3	STATUS
INIDSK	UNIT CODE	-	-	4	STATUS
INTUNT	-	-	-	5	STATUS
INTRK	-	-	-	6	STATUS
INTSEC	-	-	-	7	STATUS
READ	PAGE SEGMENT	MSB (DATA ADDR)	LSB (DATA ADDR)	4X	STATUS
WRITE	PAGE SEGMENT	MSB (DATA ADDR)	LSB (DATA ADDR)	8X	STATUS
EXECUTE	PAGE SEGMENT	MSB (PROGRAM ADDR)	LSB (PROGRAM ADDR)	CX	-

Note: The "-" symbol is used in this table as "don't care". In column R3, the commands are represented as "shorthand" hexadecimal values; see figure 3-2 for a description of the command code structure.

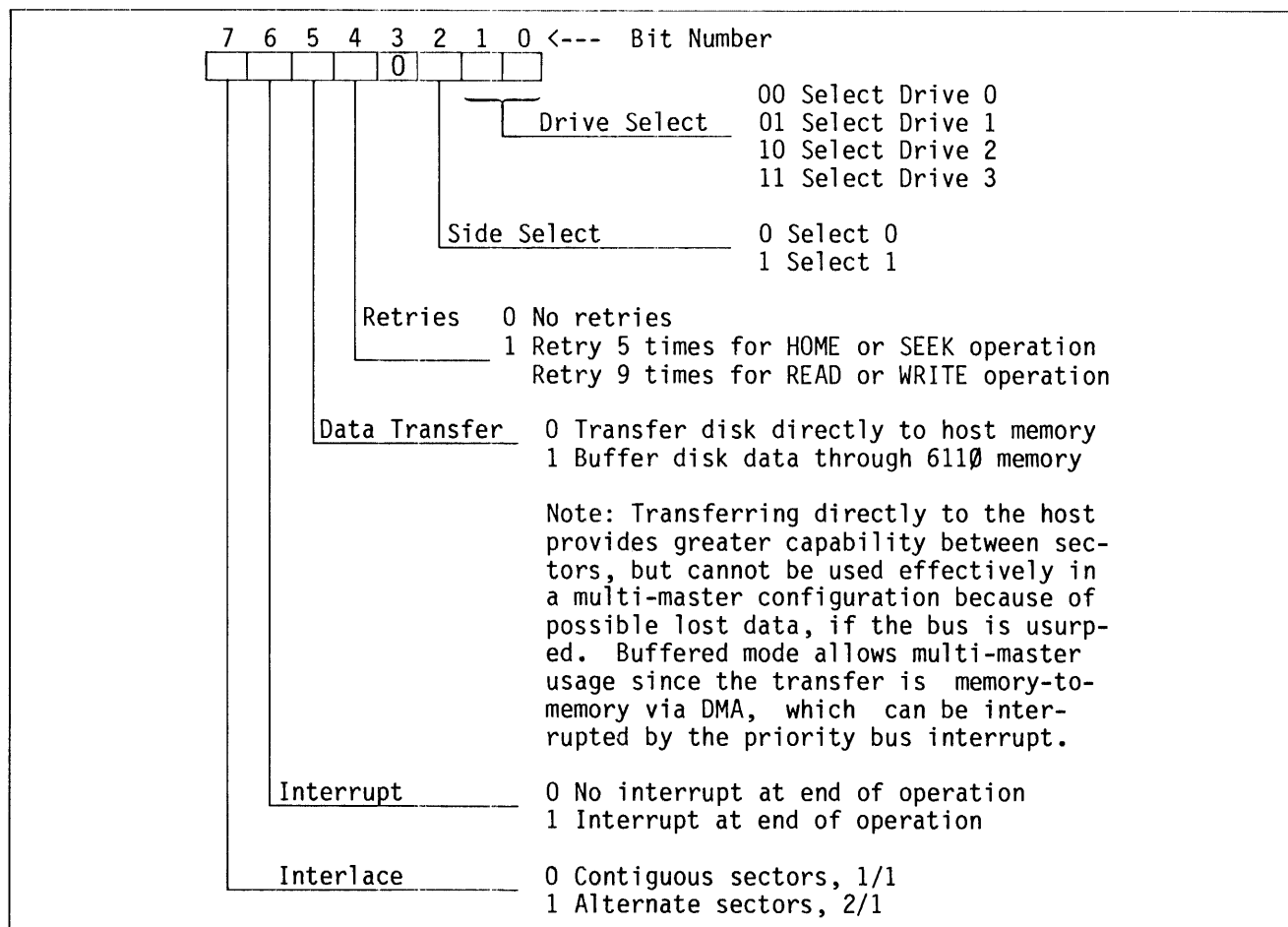


Figure 3-1. Unit Code.

then the data is transferred from buffer memory to disk; or 128 bytes of data are transferred from disk to buffer memory, then under a single DMA bus request transferred to master memory.

Interrupt: specifies whether the operation complete function will generate an INTERRUPT REQUEST on the MULTIBUS.

Interlace: specifies the sequence in which the sectors are selected when a multi-sector transfer is requested.

3-9. Track Select Code

The track select code specifies the floppy disk track to be accessed. Seven bits are used to specify a value from 0 to 76. Bit 0 is the least significant bit.

3-10. Sector Select Code

The sector select code specifies the starting sector in the selected track. Five bits are used to specify a value from 1 through 26. Bit 0 is the least significant bit.

3-11. Command Code

The command code specifies the command to be performed. This consists of a one-byte value. The value is listed in table 3-2. The READ and WRITE commands contain additional information to specify a sector count for the data transfer. The EXECUTE command contains additional information to specify a memory block count (64-byte blocks).

Figure 3-2 illustrates the construction of the command code.

3-12. Page Segment Code

The page segment code specifies the memory segment to be used for a data

transfer. The code extends the memory address from 16 bits to 20 bits. Page code values may be from 00 to FFH. The derivation of a 20-bit DMA address is illustrated in figure 3-3.

3-13. MSB Data Address Code

The MSB data address code is an 8-bit value representing the high-order byte of the main memory address where the first byte of data to be transferred is located. This is applicable to the READ and WRITE commands.

3-14. LSB Data Address Code

This is also an 8-bit value to be used as the low-order byte of the data address.

3-15. MSB Program Address

This is an 8-bit code similar to the MSB data address code. Together with the LSB program address code it represents the first byte of data in master memory to be transferred to the on-board memory for execution by the on-board CPU.

3-16. LSB Program Address

This is an 8-bit value used as the low-order byte of the program address. This address is applicable to the EXECUTE command.

3-17. Status Byte

The status byte is returned to register R4 upon completion of an operation. This mail-box register may be read by the host CPU. The format of the status byte is illustrated in figure 3-4. When a command does not use a particular bit of the status byte, a zero is returned at that bit position.

BASIC COMMANDS 7 6 5 4 3 2 1 0 0 0 0 0 0 n n n	<u>nnn</u> 0 1 2 3 4 5 6 7	<u>command</u> HOME SET PARAMETERS STATUS CLRINT INIDSK INTUNT INTRK INTSEC
READ COMMAND 7 6 5 4 3 2 1 0 0 1 s s s s s s		ssssss = sector count -1, from 0 through 63 to specify from 1 through 64 sectors, respectively.
WRITE COMMAND 7 6 5 4 3 2 1 0 1 0 s s s s s s		ssssss = sector count -1 as defined for read.
EXECUTE COMMAND 7 6 5 4 3 2 1 0 1 1 b b b b b b		bbbbbbb = count of 64-byte blocks of memory -1, from 0 through 63 to specify from 1 through 4096 (64 x 64) bytes, respectively.

Figure 3-2. Command Codes.

3-18. COMMAND DESCRIPTIONS

3-19. HOME COMMAND

This command positions the read/write head of a selected drive unit over track zero.

Call Sequence: R0 Unit code
 R1 not used
 R2 not used
 R3 0

Processing:

The head restore function is performed by the selected drive. The restore is retried according to the retry bit (unit code bit 4) until successful.

Returns:

The operation status is placed in R4. If bit-6 of the unit code was set, an interrupt is generated.

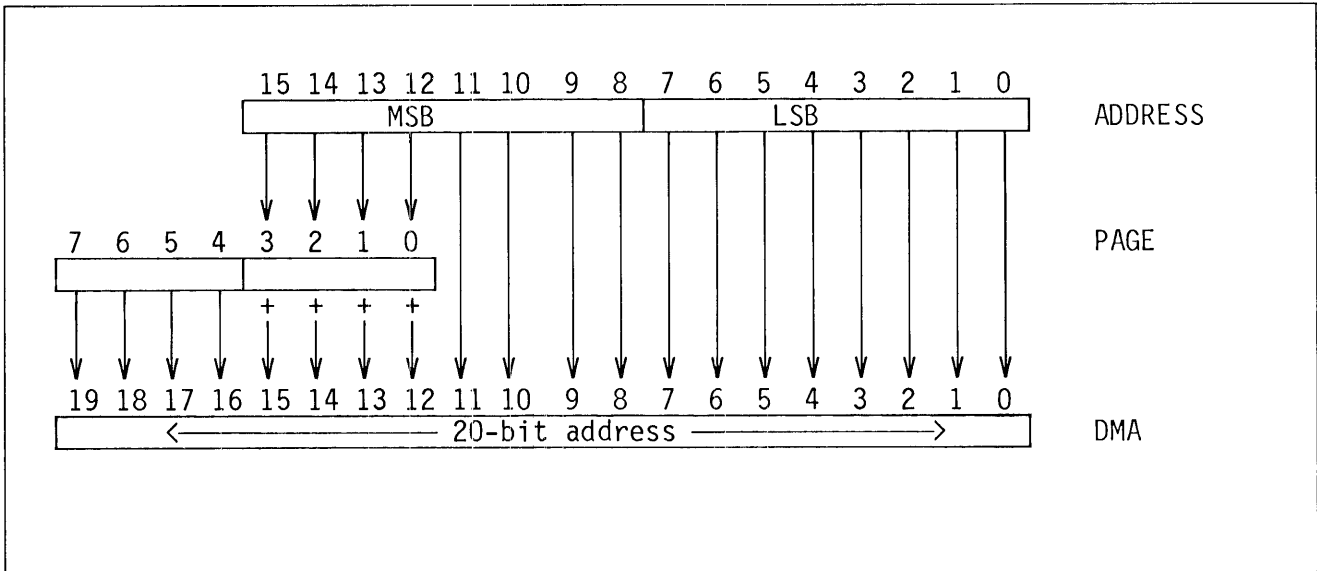


Figure 3-3. Page Segment Code.

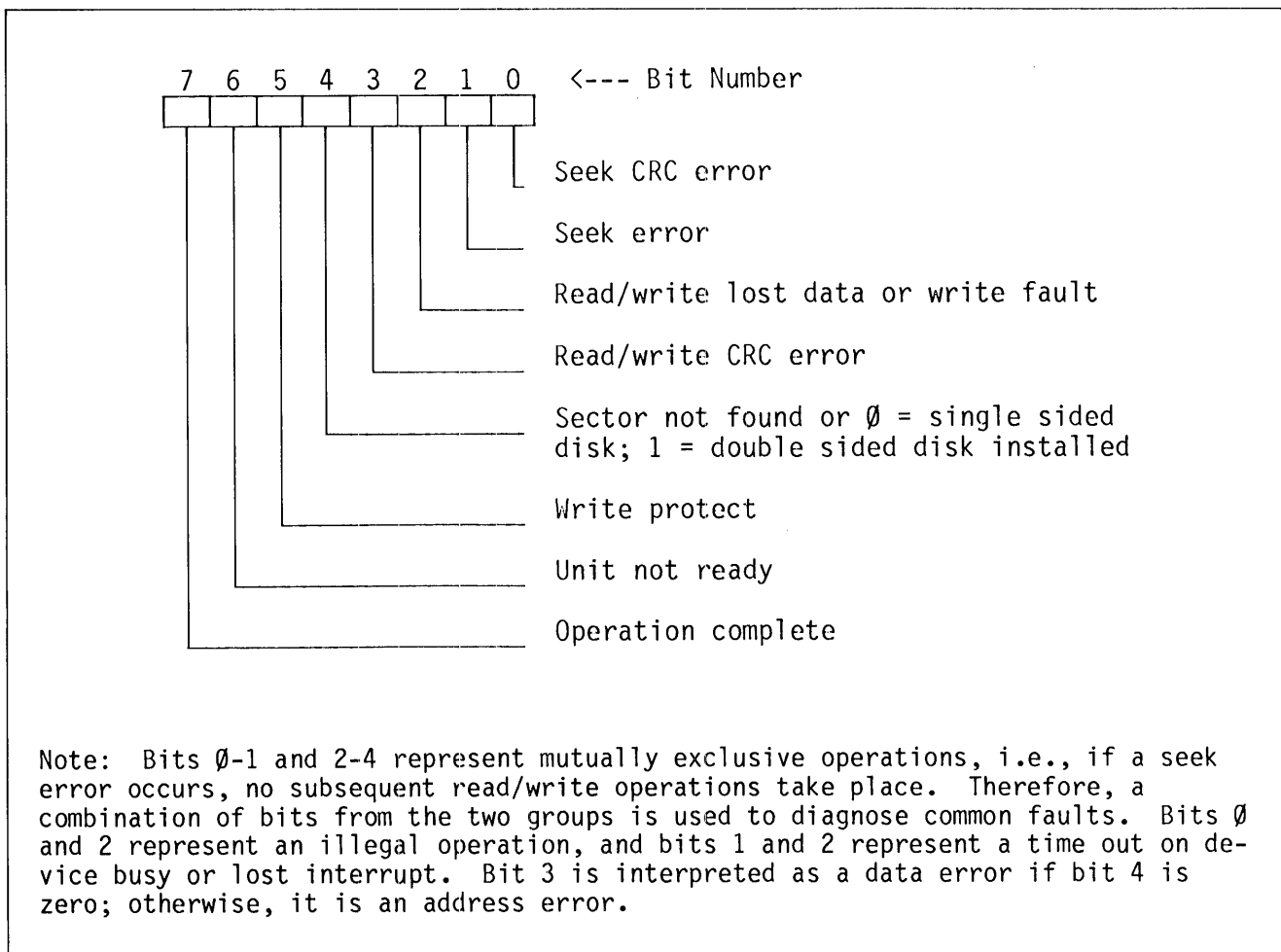


Figure 3-4. Status Byte.

3-20. SET PARAMETERS COMMAND

This command sets the device address information for a subsequent READ or WRITE operation.

Call Sequence: R0 Unit Code
R1 Track Select Code
R2 Sector Select Code
R3 1

Processing: The parameters are stored for later use; the unit is selected.

Returns: R4 contains a value of 80H. If bit-6 of the unit code was set, an interrupt will be generated.

3-21. STATUS COMMAND

This command causes R4 to be loaded with the selected device status.

Call Sequence: R0 Unit Code
R1 not used
R2 not used
R3 2

Processing: The designated drive unit is selected and its status read into R4.

Returns: R4 contains status bits 4-7. The other bits are undefined. If bit-6 of the unit code was set, an interrupt will be generated.

3-22. CLEAR INTERRUPT COMMAND

This command clears the interrupt latch set at the completion of a previous operation.

Call Format: R0 not used
R1 not used

R2 not used
R3 3

Processing: The interrupt latch is cleared.

Returns: R4 contains a value of 80H.

3-23. INITIALIZE DISK COMMAND

This command writes track and sector address information to all tracks and sectors. The data areas are written with a hexadecimal E5 code; the bit pattern of E5H is 11100101.

Call Format: R0 Unit Code
R1 not used
R2 not used
R3 4

Processing: The disk unit is homed and all sectors are written with initialize information (E5H) to permit normal use of the disk. The format is IBM 3740, 128 bytes per sector, single sided, single density. Completion of this operation leaves the read/write head position over track 76.

Returns: R4 contains the status byte. If bit-6 of the unit code was set, an interrupt will be generated.

3-24. INTERROGATE UNIT COMMAND

This command returns unit information for the currently selected disk.

Call Format: R0 not used
R1 not used
R2 not used
R3 5

Processing: The unit code, except for the interlace bit, is returned to the user, and a clear interrupt is performed.

Returns: R4 contains the unit code, except for bit-7, which is used for the status bit-7 function (operation complete).

3-25. INTERROGATE TRACK COMMAND

This command returns the track select code previously requested or as updated by the intervening I/O.

Call Format: R0 not used
R1 not used
R2 not used
R3 6

Processing: The track code currently existing in the controller is returned to the user. This value, together with the Current Sector code, can be used, when an error condition occurs, to determine the track and sector in error. A clear interrupt operation is also performed.

Returns: R4 contains the track code in bits 0-6 and the operation-complete status bit in bit-7.

3-26. INTERROGATE SECTOR COMMAND

This command returns the sector select code previously requested or as updated by the intervening I/O.

Call Format: R0 not used
R1 not used
R2 not used
R3 7

Processing: The sector code currently existing in the controller is returned to the user. This value, together with the current track code, may be used when an error condition occurs, to determine the track and sector in error. A clear interrupt operation is also performed.

Returns: R4 contains the sector code in bits 0-4, bits 5 and 6 have values of zero, and bit 7 has a value of 1.

3-27. READ COMMAND

This command reads from 1 to 64 consecutive sectors beginning at the previously selected unit, track, and sector. The command is normally preceded by a SET PARAMETER command. However, when the prior values are known to be correct, the SET PARAMETERS command is not required.

Call Format: R0 Page Segment
R1 Data Address MSB
R2 Data Address LSB
R3 Command Code (4X)
(figure 3-2)

Processing: One through 64 consecutive sectors can be read into the host address, either directly or sector buffered depending on the unit code, bit 4. The head location is automatically incremented to the next sector/track address. If end of disk occurs during the transfer, the transfer is prematurely terminated with no indication, other than loss of data.

If an unrecoverable error occurs, operations are prematurely terminated with an error status. The value x in the command code is six bits where 0-63 represent the number of sectors to be read (1-64). Internally, the host memory address page is shifted 12 bits and added to the R1-R2 address to determine the host absolute address. During the transfer, the host address is advanced by sector length but the page is not. Therefore, an offset wraparound may occur if the number of sectors times sector length plus offset address exceeds 16 bit capacity. The host must determine when this will occur and issue multiple commands to update the page as necessary.

Returns: R4 contains the status byte. If bit-6 of the unit code was set, an interrupt will be generated.

3-28. WRITE COMMAND

This command writes from one to sixty-four consecutive sectors beginning at the previously stored unit, track, and sector. The command is normally preceded by a SET PARAMETER command to designate unit, track, and sector. However, when the prior values are known to be correct, the SET PARAMETERS command is not required.

Call Format: R0 Page Segment
R1 Data Address MSB
R2 Data Address LSB
R3 Command Code (8X)
(figure 3-2)

Processing: One through sixty-four consecutive sectors can be written from the host memory address, either directly or sector buffered depending on the unit code bit 4. End of disk, error considerations, and addressing considerations are the same as READ.

3-29. EXECUTE PROGRAM COMMAND

This command can transfer from 64 to 4096 bytes of program code from a host memory address to the 6110 RAM, starting address of 0C20H and begin execution at this same address. However, the standard 6110 RAM capacity is 1024 bytes. Since the starting address in RAM is 0C20H and ending at 1000H, the usable capacity is 992 bytes. Also, since transfers are made in 64 byte groups, 15 groups would comprise 960 bytes. To use the full capability of the command, the off board RAM extension memory capability would have to be employed.

Call Format: R0 Page Segment
R1 Program Address MSB
R2 Program Address LSB
R3 Command Code (CX)
(figure 3-2)

Processing: One through 64 blocks of 64 bytes of program data are transferred from the host memory to the 6110 RAM and executed. This function is used to execute controller programs that are located in the 6110 ROM. The controller firmware uses addresses 0F00-0FFF as a sector buffer during buffered I/O transfers. The value x in the command is 6 bits 0-63 representing 1-64 blocks

of 64 bytes. A user program may be terminated by transferring to the firmware location a 39 hexadecimal (the normal command loop). The program stack, on entry to the user program, is 10 bytes in length and empty. It should be left empty on return to location 39. The user program must provide any R4 response required by the host following the completion of transfer and start of execution.

Return: No return code is provided. One may be provided by the user program.

3-30. FIRMWARE INSTRUCTIONS

Table 3-2 is a listing of the Am95/6110 firmware instructions stored in the FDC board E-PROMs. Included with the listing are appropriate comments.

3-31. PROGRAMMING INTRODUCTION

The previous paragraphs describe the firmware that is installed in the standard Am95/6110 board and how each command is implemented. Included on the FDC board are programmable devices that are controlled by the firmware. When and if the factory supplied firmware is modified, the user must realize the interrelationships to these programmable chips. Therefore, the following paragraphs provide some operation and programming information to aid user understanding of these devices. When greater detailed descriptions are required, consult the data sheet for the specific device. The programmable devices on the AMC 95/6110 FDC board are: Am9085 CPU, Am9517 DMA, and FD 1771 FDC.

3-32. Am9085A MICROCOMPUTER

The Am9085A is an 8-bit general-purpose microcomputer capable of accessing up to 64K bytes of memory and executing code byte-by-byte. The code executed by the Am9085 resides in the FDC on board E-PROMs, memory locations 0000-0BFF. The CPU chip is controlled exclusively by the firmware and the system CPU does not have access to control this device. Because of the complexity of the Am9085 and the various ways it can be used, and because many books and descriptions are currently in publication, it would be redundant to repeat that data here. If detailed information on the Am9085A CPU chip is required, consult the Am9080 user's manual. However, table 3-3, Am9085A Instruction Set, is provided for user convenience.

3-33. MULTIMODE DIRECT MEMORY ACCESS (DMA) CONTROLLER Am9517A

The Am9517 DMA controller provides the FDC board with the capability to transfer data to/from the FDC board and main memory and to route data on the board using four separate channels. The data channels can be programmed to perform single transfer mode or block transfer mode.

3-34. SINGLE TRANSFER MODE

When in the single transfer mode, the Am9517 is programmed to make a single byte transfer. The word count is decremented/incremented following each transfer. A terminal count (TC), reached when the word count is zero, causes an autoinitialize when the channel is so programmed.

3-35. BLOCK TRANSFER MODE

When using the block transfer mode, the Am9517 is programmed to continue making

TABLE 3-3. Am9085 Instruction Set.

Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic	Function
40	MOV B,B	58	MOV E,B	70	MOV M,B	1A	LDAX D	DATA
41	MOV B,C	59	MOV E,C	71	MOV M,C	2A	1HLD	
42	MOV B,D	5A	MOV E,D	72	MOV M,D	3A	LDA	TRANSFER
43	MOV B,E	5B	MOV E,E	73	MOV M,E	02	STAX B	
44	MOV B,H	5C	MOV E,H	74	MOV M,H	12	STAX D	
45	MOV B,L	5D	MOV E,L	75	MOV M,L	22	SHLD	
46	MOV B,M	5E	MOV E,M	77	MOV M,A	32	STA	
47	MOV B,A	5F	MOV E,A	78	MOV A,B	01	LXI B	
48	MOV C,B	60	MOV H,B	79	MOV A,C			
49	MOV C,C	61	MOV H,C	7A	MOV A,D	21	LXI H	
4A	MOV C,D	62	MOV H,D	7B	MOV A,E	31	LXI SP	
4B	MOV C,E	63	MOV H,E	7C	MOV A,H	F9	SPHL	
4C	MOV C,H	64	MOV H,H	7D	MOV A,L	E3	XTHL	
4D	MOV C,L	65	MOV H,L	7E	MOV A,M	EB	XCHG	
4E	MOV C,M	66	MOV H,M	7F	MOV A,A	D3	OUT	
4F	MOV C,A	67	MOV H,A	06	MVI B	DB	IN	
50	MOV D,B	68	MOV L,B	0E	MVI C	C5	PUSH B	
51	MOV D,C	69	MOV L,C	16	MVI D	D5	PUSH D	
52	MOV D,D	6A	MOV L,D	1E	MVI E	E5	PUSH H	
53	MOV D,E	6B	MOV L,E	26	MVI H	F5	PUSH PSW	
54	MOV D,H	6C	MOV L,H	2E	MVI L	C1	POP B	
55	MOV D,L	6D	MOV L,L	36	MVI M	D1	POP D	
56	MOV D,M	6E	MOV L,M	3E	MVI A	E1	POP H	
57	MOV D,A	6F	MOV L,A	0A	LDAX B	F1	POP PSW	
80	ADD B	C6	ADI	9E	SBB M	3C	INR A	ARITHMETIC
81	ADD C	CE	ACI	9F	SBB A	03	INX B	
82	ADD D	90	SUB B	D6	SUI	13	INX D	
83	ADD E	91	SUB C	DE	SBI	23	INX H	
84	ADD H	92	SUB D	09	DAD B	33	INX SP	
85	ADD L	93	SUB E	19	DAD D	05	DCR B	
86	ADD M	94	SUB H	29	DAD H	0D	DCR C	
87	ADD A	95	SUB L	39	DAD SP	15	DCR D	
88	ADC B	96	SUB M	27	DAA	1D	DCR E	
89	ADC C	97	SUB A	04	INR B	25	DCR H	
8A	ADC D	98	SBB B	0C	INR C	2D	DCR L	
8B	ADC E	99	SBB C	14	INR D	35	DCR M	
8C	ADC H	9A	SBB D	1C	INR E	30	DCR A	
8D	ADC L	9B	SBB E	24	INR H	0B	DCX B	
8E	ADC M	9C	SBB H	2C	INR L	1B	DCX D	
8F	ADC A	9D	SBB L	34	INR M	2B	DCX H	
						3B	DCX SP	

TABLE 3-3. Am9085 Instruction Set. (Cont.)

Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic	Hex	Mnemonic	Function	
A0	ANA B	A9	XRA C	B2	ORA D	BB	CMP E	LOGICAL	
A1	ANA C	AA	XRA D	B3	ORA E	BC	CMP H		
A2	ANA D	AB	XRA E	B4	ORA H	BD	CMP L		
A3	ANA E	AC	XRA H	B5	ORA L	BE	CMP M		
A4	ANA H	AD	XRA L	B6	ORA M	BF	CMP A		
A5	ANA L	AE	XRA M	B7	ORA A	FE	CPI		
A6	ANA M	AF	XRA A	F6	ORI	07	RLC		
A7	ANA A	EE	XRI	BB	CMP B	0F	RRC		
E6	ANI	B0	ORA B	B9	CMP C	17	RAL		
A8	XRA B	B1	ORA C	BA	CMP D	1F	RAR		
						2F	CMA		
C3	JMP	E9	PCW L	CD	CAL L	C9	RET		BRANCHING
C2	JNZ	C7	RST 0	C4	CNZ	C0	RNZ		
CA	JZ	CF	RST 1	CC	CZ	C8	RZ		
D2	JNC	D7	RST 2	DA	CNC	D0	RNC		
DA	JC	DF	RST 3	DC	CC	D8	RC		
E2	JPO	E7	RST 4	E4	CPO	E0	RPO		
EA	JPE	EF	RST 5	EC	CPE	E8	RPE		
F2	JP	F7	RST 6	F4	CP	F0	RP		
FA	JM	FF	RST 7	FC	CN	F8	RM		
00	NOP	F3	DI	37	STC	3F	CMC	CONTROL	
76	HLT	FB	EI						

transfers upon activation of the DREQ signal until a terminal count, caused by the word count going to zero, or an external end of process signal.

3-36. ADDRESSING

The Am9517 DMA controller uses 16 consecutive addresses (10H through 1FH) for reading and writing to the twelve internal registers. The port addresses and their functions are listed in table 3-4.

3-37. REGISTERS

The Am9517 DMA controller's twelve addressable registers are listed in table 3-5. These register addresses are listed in table 3-4 and their functions are described in the following paragraphs.

3-38. Command Register

This 8-bit register controls the operation of the Am9517. It is programmed by the Am9085 and is cleared by Reset. The port address of the command register is 18H and IOW active. The function of each command bit is illustrated in figure 3-5.

3-39. Mode Register

Each of the four channels has its own 6-bit mode register. When the Am9085 is writing into this register, bits 0 and 1 determine which channel mode register is to be written. The port address of the mode registers is 1BH and IOW active. The bit assignment and definition are shown in figure 3-6.

TABLE 3-4. DMA (Am9517) I/O PORT ADDRESSES.

I/O Port	Input Function (IOW)	Output Function (IOR)
10	Channel 0 Address	
11	Channel 0 Word Count	
12	Channel 1 Address	
13	Channel 1 Word Count	
14	Channel 2 Address	
15	Channel 2 Word Count	
16	Channel 3 Address	
17	Channel 3 Word Count	
18	STATUS REGISTER	Command Register
19	Not used	Request Register
1A	Not used	SET/RESET
1B	Not used	MODE REGISTER
1C	Not used	CLEAR FIRST/LAST FLIP-FLOP
1D	Temporary Register	MASTER CLEAR
1E	Not used	Not used
1F	Not used	MASK REGISTER FOUR BITS

TABLE 3-5. Am9517 INTERNAL REGISTERS.

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

3-40. Request Register

The Am9517 can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the four bit register. Each register bit is set or reset separately under software control or as cleared on generation of a terminal count or end of process. The port address of the request register is 19H and IOR active.

To set or reset a bit, the software loads the proper form of the data word, shown in figure 3-7.

3-41. Mask Register

Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit sets when its associated channel produces an end of process and the channel is not programmed for autoinitialization.

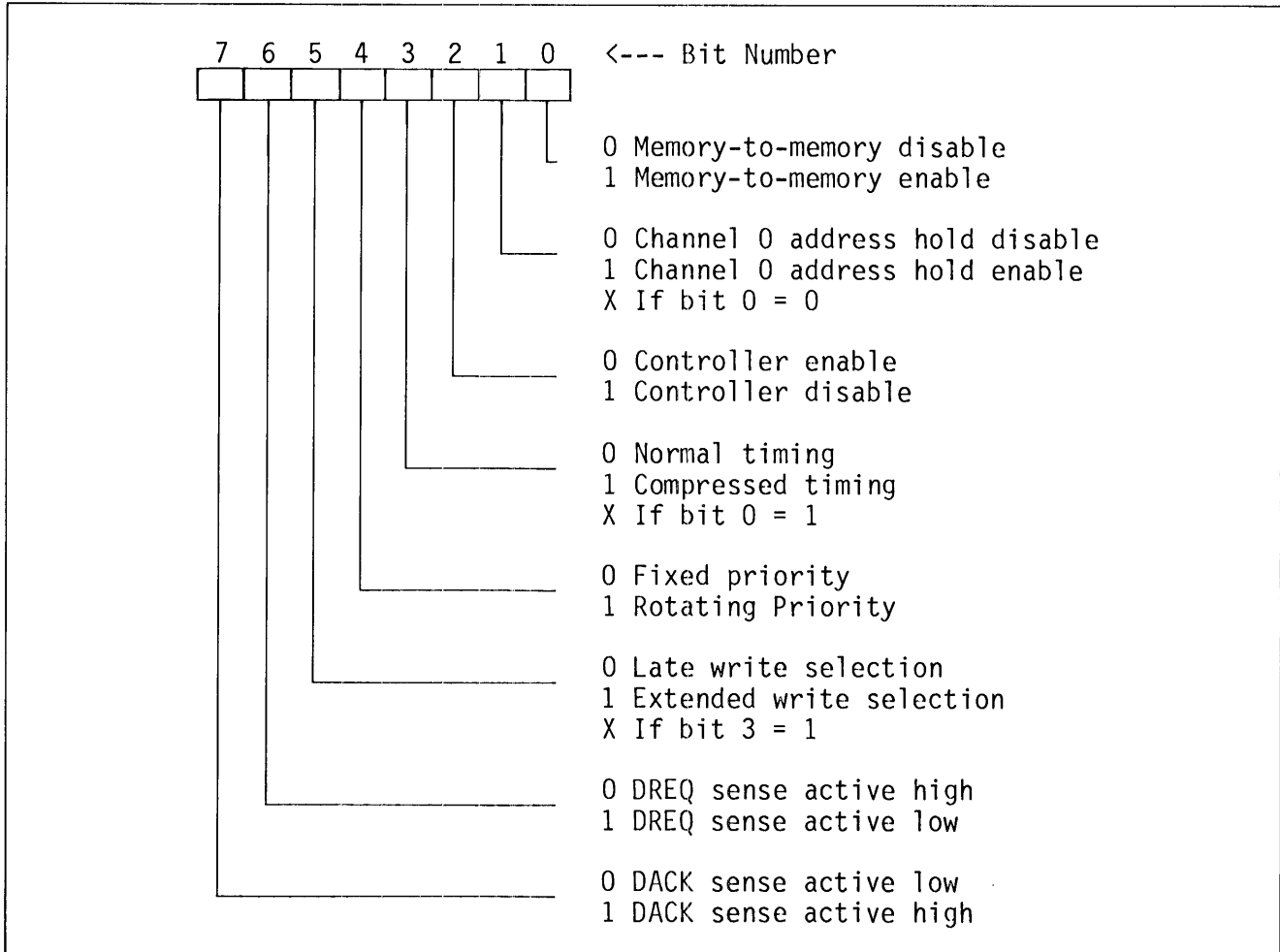


Figure 3-5. Am9517 Command Register.

Each bit of the four bit mask register can be set or cleared separately under software control.

The entire register is set by Reset, which disables all DMA requests until a clear mask register instruction allows them to occur. The port address to set individual bits is 1AH with IOR active and when all four bits are written with a single command, address port 1FH and IOW active. The bit configuration and definitions are shown in figure 3-8.

3-42. Status Register

The status register contents are available to be read out by addressing port 18 and activating IOR. It contains the

device status which includes the channels that have reached a tunnel count and which channels have pending DMA requests. Bits 0-3 are set each time a terminal count is reached by the appropriate channel. These bits are cleared upon Reset and on each Status Read. Bits 4-7 are set when the corresponding channel request services. Figure 3-9 shows the bit configuration of the Status Register.

3-43. Temporary Register

The temporary register resides at address port 1D and holds data during memory-to-memory transfers. When the transfer is complete, the last word moved can be read by the microproces-

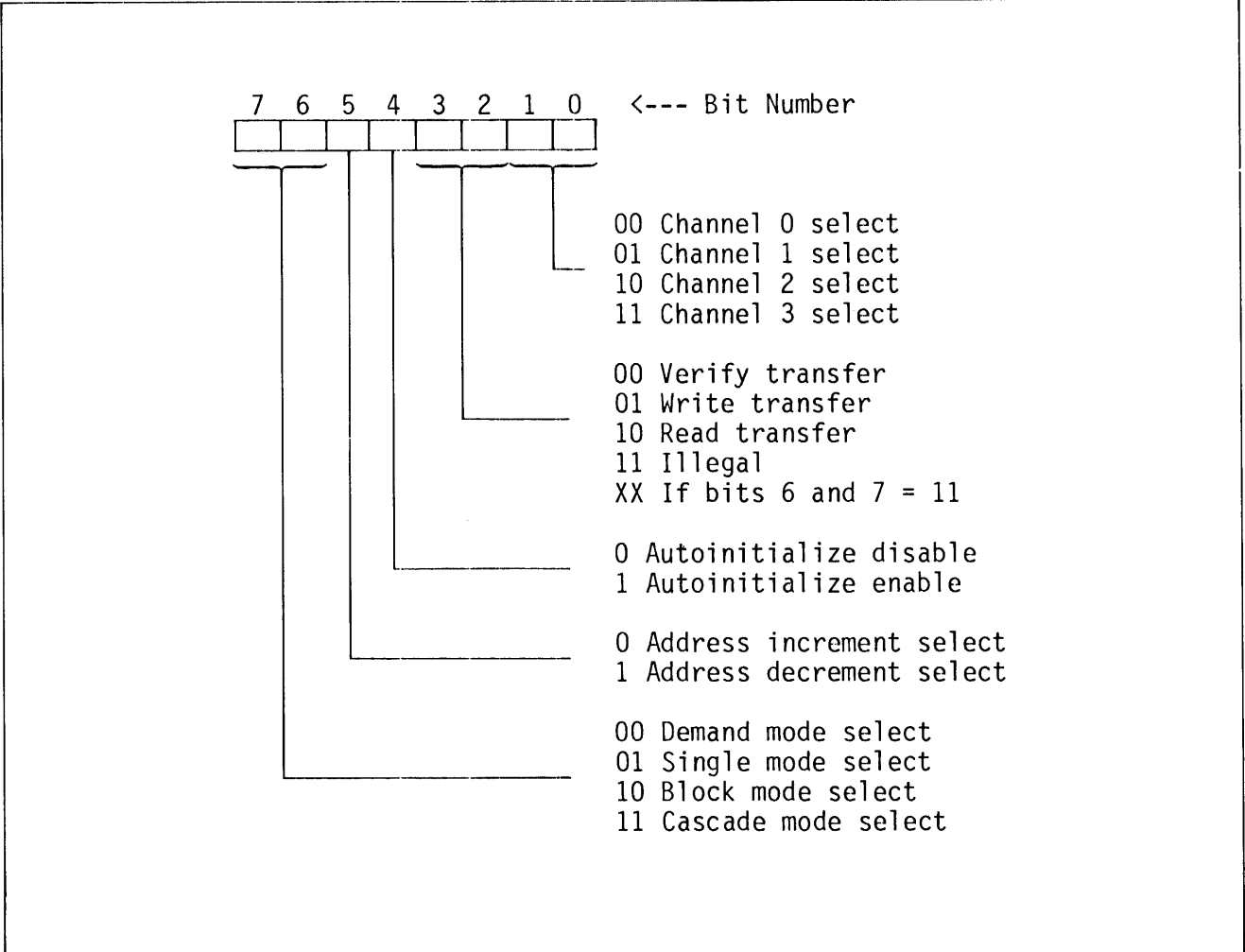


Figure 3-6. Am9517 Mode Register Bit Assignments.

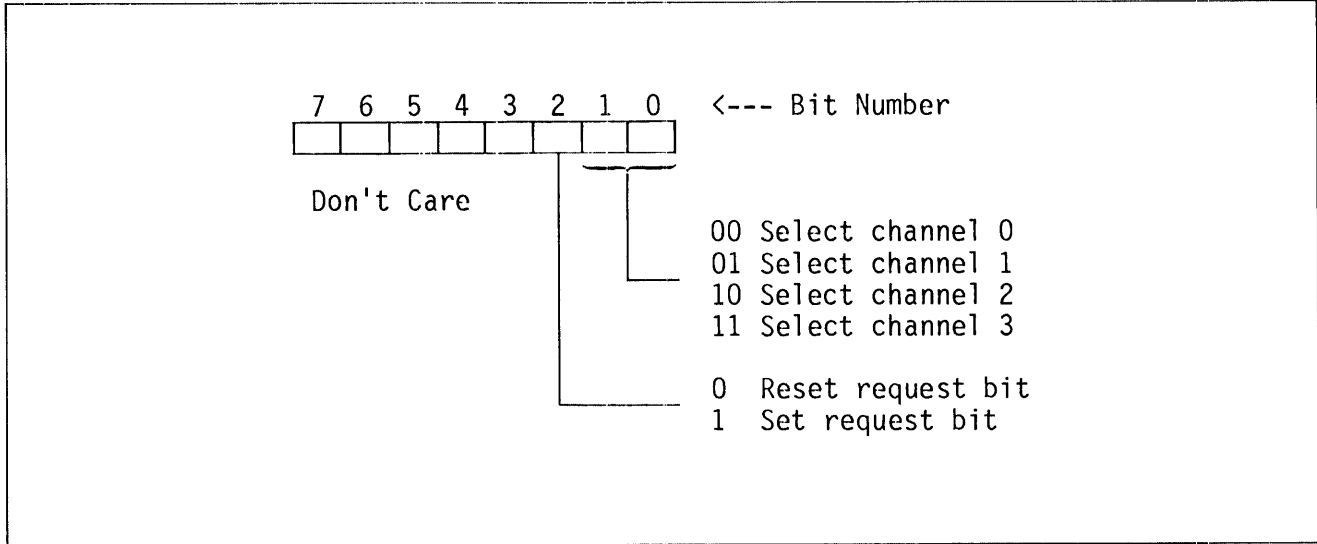


Figure 3-7. Am9517 Request Register.

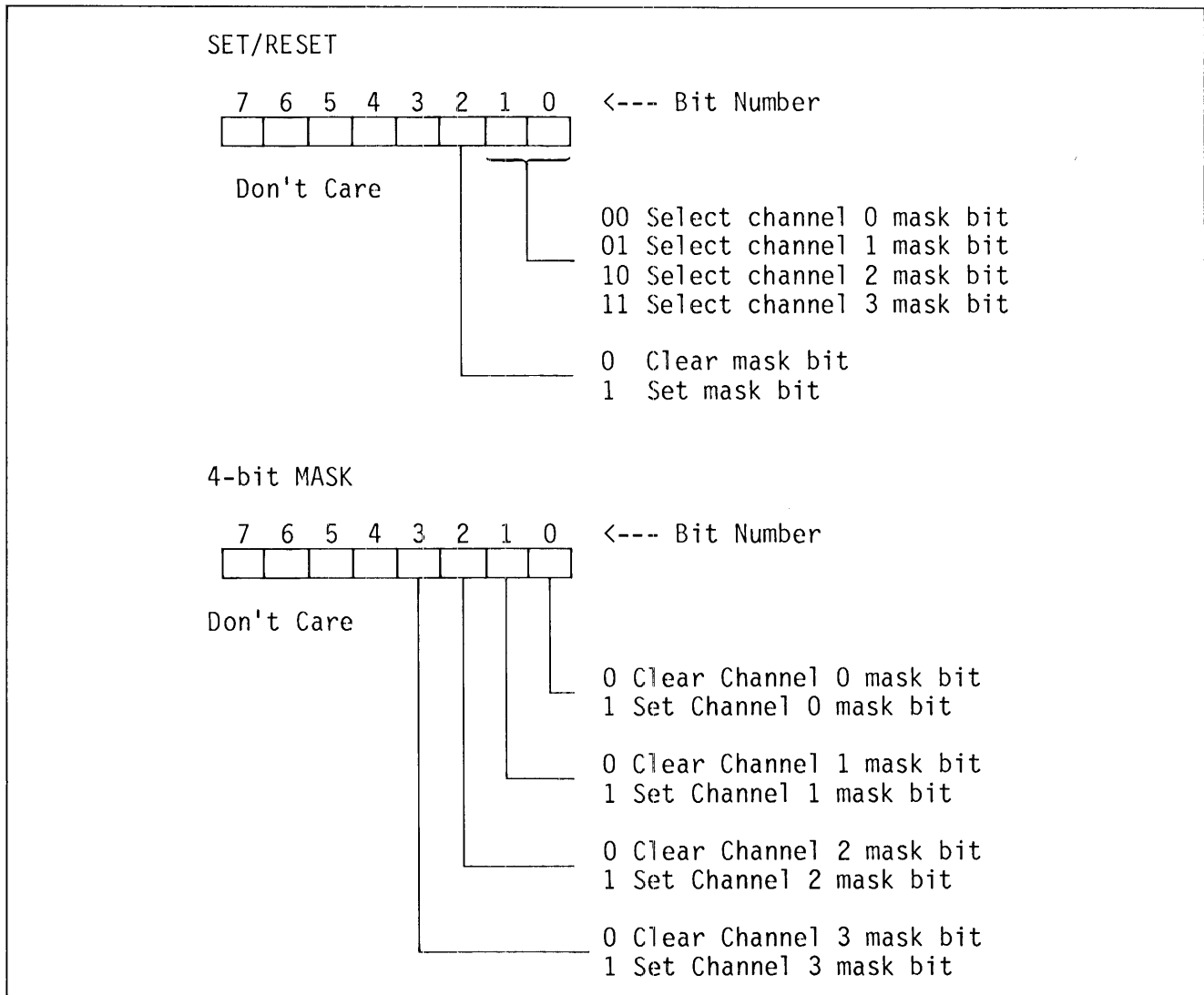


Figure 3-8. Am9517 Mask Register.

sor. This register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

3-44. SOFTWARE COMMANDS

There are two additional software commands that can be executed on the Am9517 that do not depend on any specific bit pattern on the data bus. These two commands are described in the following paragraphs and the address codes are shown in table 3-6.

3-45. Clear First/Last Flip/Flop

This command is executed prior to writing or reading new address or word count information to the Am9517. This initializes the flip/flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

3-46. Master Clear

This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary,

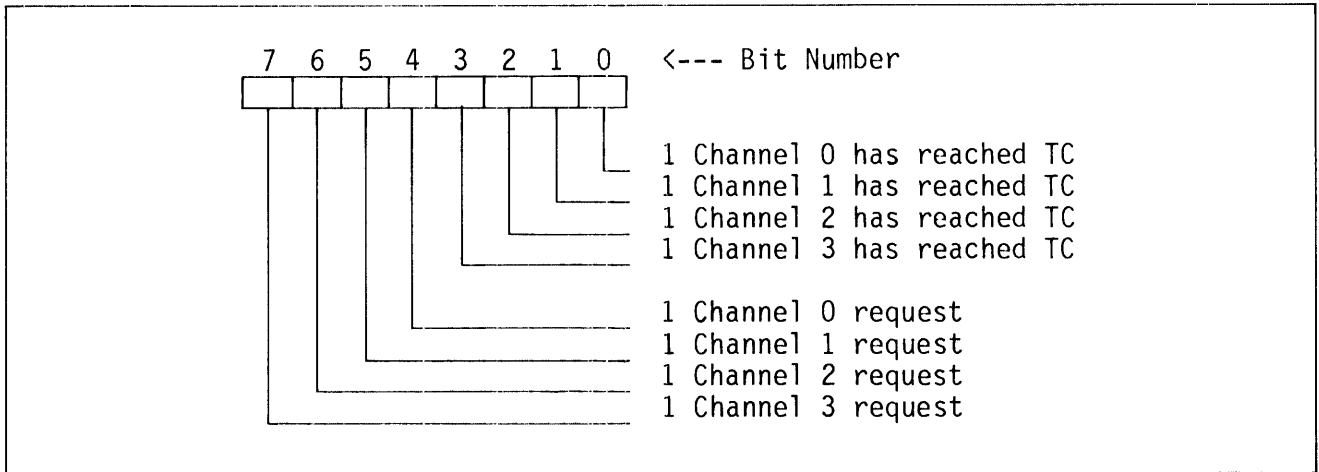


Figure 3-9. Am9517 Status Register Configuration.

TABLE 3-6. SOFTWARE COMMAND CODES.

Operation	Registers Affected	Signals							
		CS	IOR	IOW	A3	A2	A1	A0	
Clear FF	Internal First/Last Flip/Flop	0	1	0	1	1	0	0	
Master Clear	Clear: Command Status Request Temporary Internal First/Last Flip/Flop Set: Mask	0	1	0	1	1	0	1	

and Internal First/Last Flip/Flop registers are cleared and the Mask register is set. The Am9517 will enter the Idle cycle.

3-47. FLOPPY DISK FORMATTER/CONTROLLER FD1771

The FD1771 is a MOS/LSI device that performs the functions of a floppy disk controller/formatter. The device is included in the floppy disk controller board, and contains a flexible interface organization that accomodates the firmware interface and the disk drive interface.

The firmware/processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The device operates on a multiplexed bus with other bus-oriented devices.

3-48. PROCESSOR INTERFACE

The FD1771 to Am9085 processor interface is accomplished through the eight Data Access Lines (DAL) and associated control signals. Data, status, and control words out of or into the FD1771 use the DAL. The DAL contains three state buffers, which are

enabled as output drivers when Chip Select and Read Enable are active, and enabled as input receivers when Chip Select and Write Enable are active.

When data transfer through the FD1771 is required by the Am9085, the device address is decoded making the Chip Select (CS) line active. The four address parts on the FD1771 and the accessed registers are listed in table 3-6. The least significant address bits A₀ and A₁ are coded to select the registers listed.

During DMA types of transfers between the FD1771 Data Register and the buffer or main memory, the Data Request (DRQ) output is used in Data Transfer Control. This signal also appears as status bit 1 during read and write operations.

3-49. FLOPPY DISK INTERFACE

The floppy disk interface consists of head positioning controls, write gate controls, and data transfer lines. A 2.0MHz +1% squarewave clock is required at the $\overline{\text{CLK}}$ input for internal control timing. Commands read into the FD1771 from the Am9085 are implemented and the appropriate signals are sent to a selected disk drive.

3-50. COMMAND DESCRIPTION

The FD1771 accepts and executes eleven commands. The command words should be loaded into the command register only when the busy status bit is off (Status Bit 0). An exception is the Force Interrupt command. When a command is being executed, the busy status bit is set. When a command is completed, an interrupt is generated and the Busy Status bit is reset. The status register indicates whether a command is computed or an error occurred. The commands are divided into four types and are explained in the following paragraphs.

3-51. Restore (Seek Track 0)

When this command is read into the command register and execution is implemented, the track 00 (TR00) input is sampled. If TR00 is active, indicating the Read/Write head is positioned over track 0, the track register is filled with zeroes and an interrupt is generated. If TR00 is not active, stepping pulses, at a rate specified by bits 0 and 1, are sent to the drive unit until TR00 is activated. At this time the TR is filled with zeroes and an interrupt is generated. If the TR00 does not activate after 255 stepping pulses, the operation is terminated automatically, the interrupt is set, and the seek error status bit is set. A verification operation occurs if bit 2 of the command is set. The Restore command is implemented automatically when the master reset occurs. Figure 3-10 illustrates the bit configuration of the command register for a RESTORE command.

3-52. SEEK

This command assumes the track register contains the current Read/Write head track position and the data register contains the desired track number. The FD1771 updates the track register and issues stepping pulses in the proper direction, positioning the Read/Write head, until the contents of the track register equal the data register. At this point the Read/Write head is positioned over the desired track. An interrupt is generated at the end of this operation. Figure 3-11 illustrates the command register bit configuration for a SEEK command.

3-53. STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is determined by a previously issued STEP IN or STEP OUT command. An

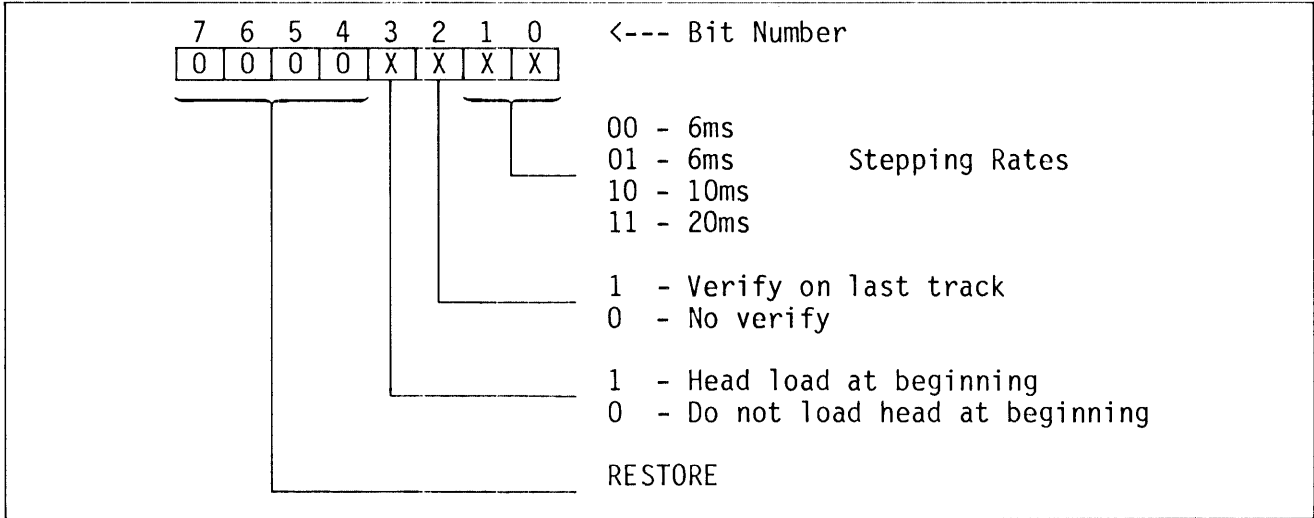


Figure 3-10. FD1771 RESTORE Command.

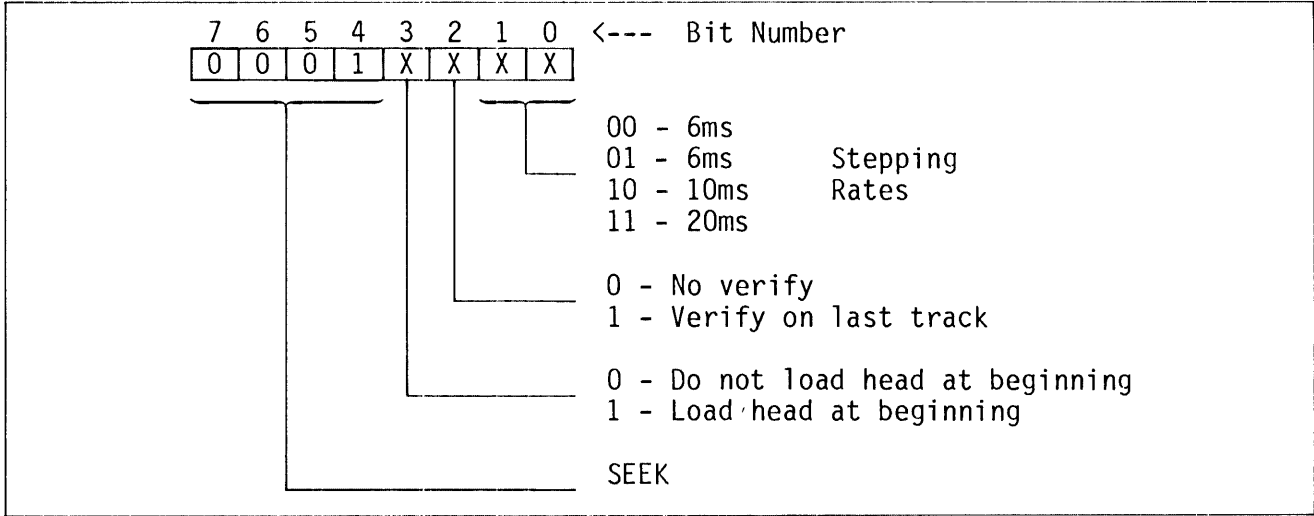


Figure 3-11. FD1771 SEEK Command.

interrupt is generated at the completion of this command. Figure 3-12 illustrates the command register bit configuration for a STEP command.

3-54. STEP-IN

The STEP-IN command causes the FD1771 to issue one stepping pulse such that the Read/Write head moves one track toward track 76. An interrupt is generated at the completion of this

command. Figure 3-13 illustrates the command register bit configuration for a STEP-IN command.

3-55. STEP-OUT

The STEP-OUT command causes the FD1771 to issue one stepping pulse such that the Read/Write head moves one track toward track 0. An interrupt is generated at the completion of this command. Figure 3-14 illustrates the command register bit configuration for a STEP-OUT command.

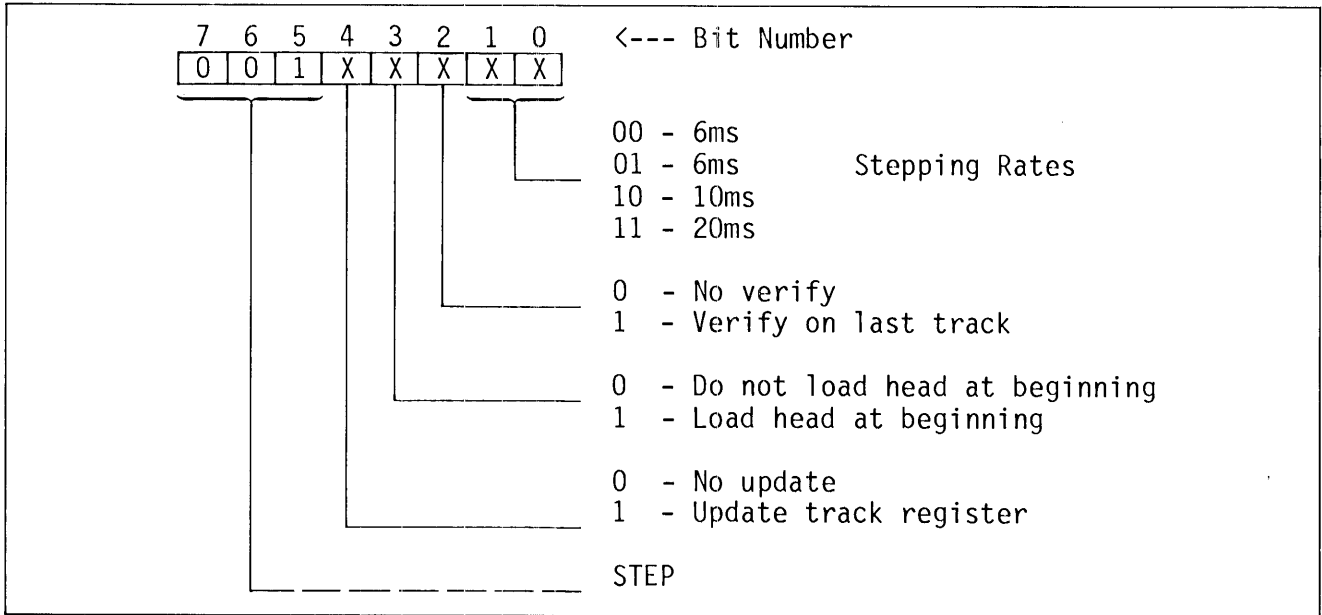


Figure 3-12. FD1771 STEP Command.

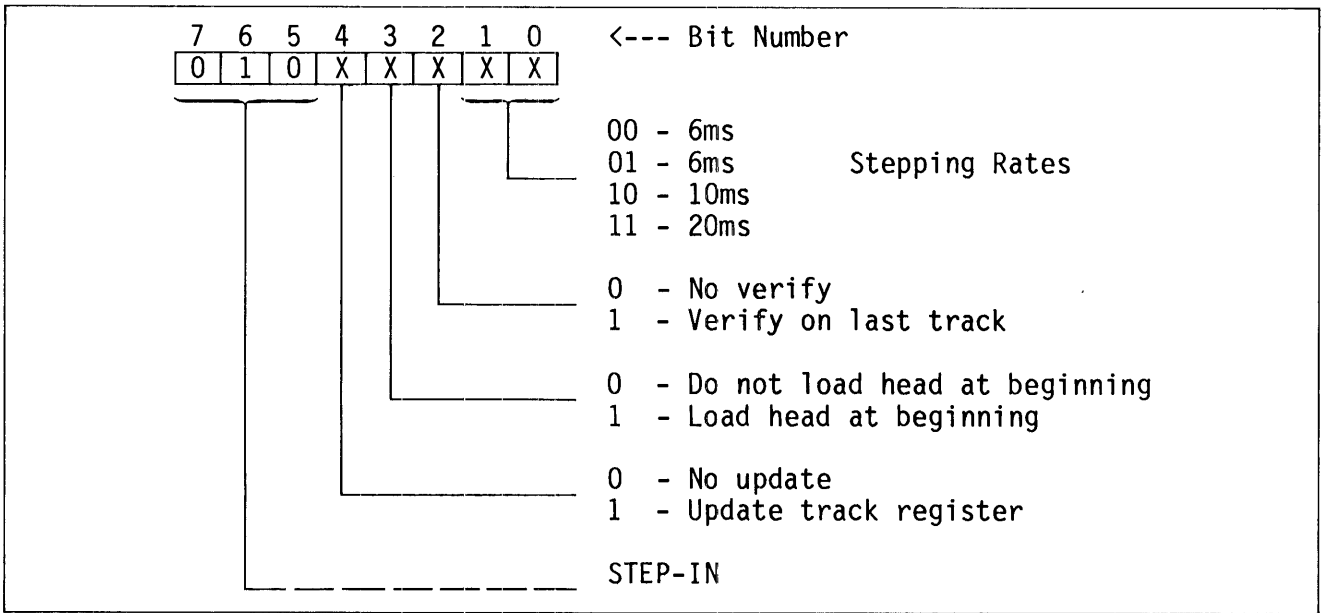


Figure 3-13. FD1771 STEP-IN Command.

3-56. READ

When the READ command is issued to the FD1771, the following events occur. The Read/Write head is loaded, the Busy status bit is set; and when the ID field (with the correct track number, sector number, and CRC) is encountered, the data read from the disk data field

is transferred to the DMA controller for routing. The Data Address Mark (AM) must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of data is shifted through the Data Shift Register (DSR), it is transferred to the Data Register

(DR) and DRQ is generated. When the next byte is encountered in the Data Shift Register (DSR), it is transferred to the DR and another DRQ is generated. If the DMA has not read the previous contents of the DR before a new character is transferred, that character is lost and the Last Data status bit is set. This sequence is repeated until the entire data field is read. If a CRC error occurs at the end of the data

field, the CRC error Status bit is set and the command is terminated.

When the read operation is complete, the type of Data Address Mark read in the data field is recorded in the Status Register. For a definition of the bits affected, see the Status Register description. Figure 3-15 illustrates the command register bit configuration for a READ command.

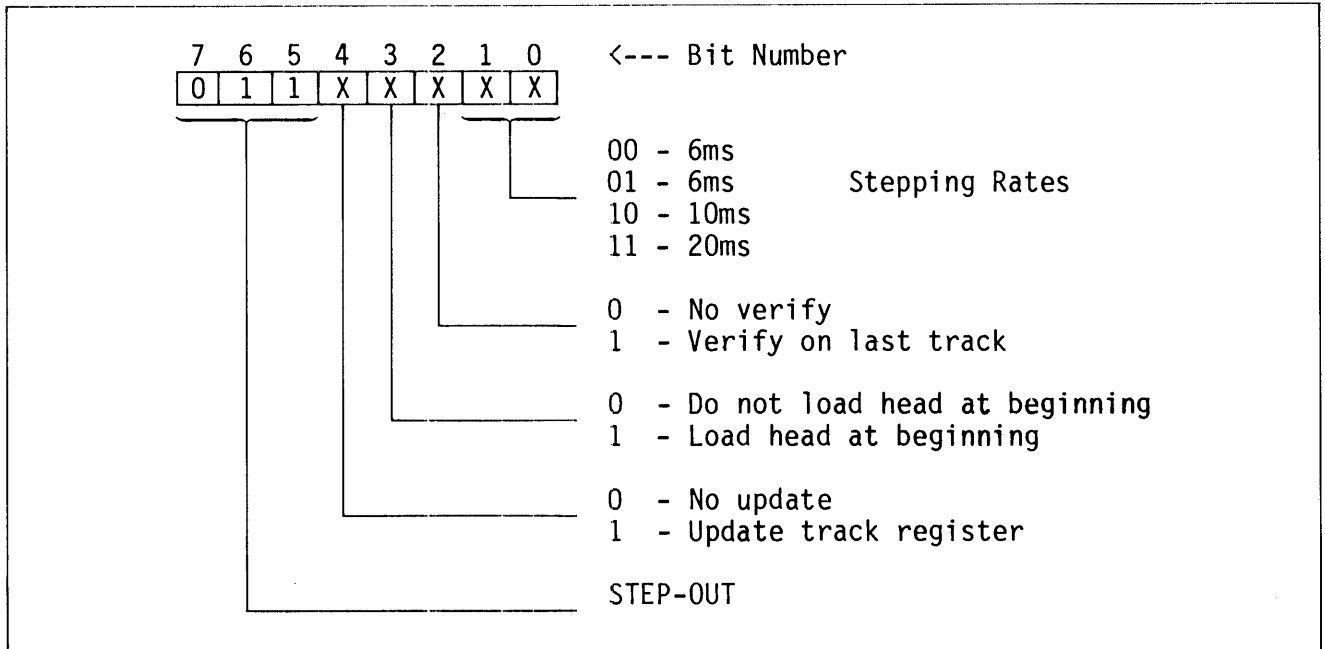


Figure 3-14. FD1771 STEP-OUT Command.

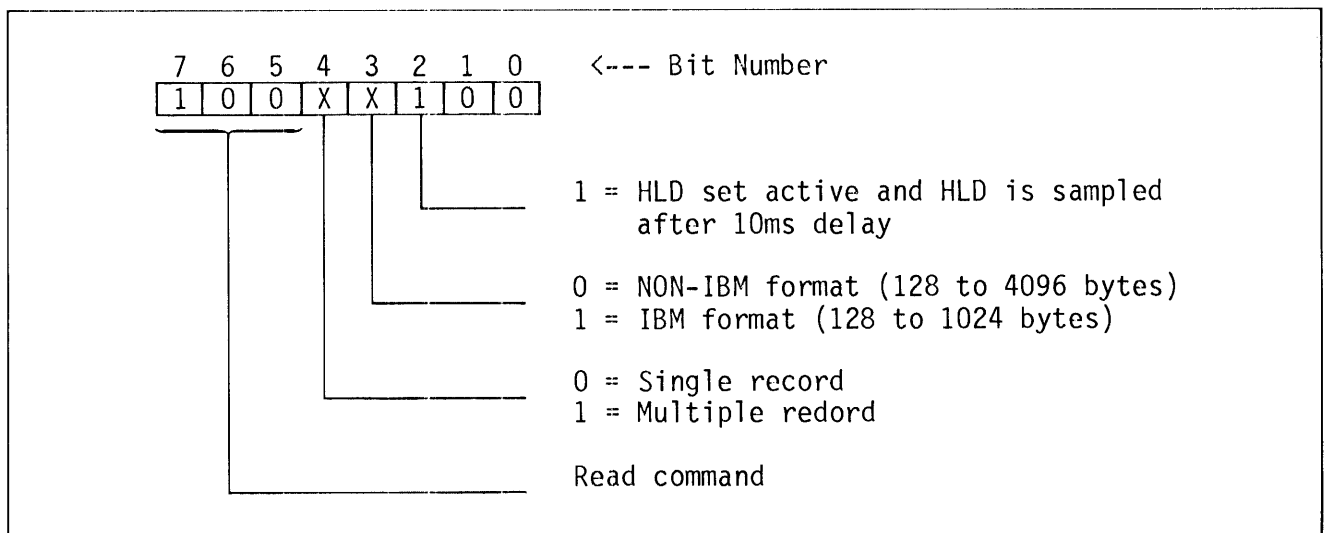


Figure 3-15. FD1771 READ Command.

3-57. WRITE

Upon receipt of the WRITE command, the Read/Write head is loaded (HLD active) and the Busy status bit is set. When the correct ID field is located, a DRQ is generated. After 11 bytes of the CRC field, Write Gate (WG) activates if the DRQ is serviced. If the Data Register has not been loaded, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, WG activates and six bytes of zeroes are written on the diskette.

The FD1771 proceeds to write the data field and generate DREQ to the DMA. If a Data request is not serviced in time for continuous writing, the Lost Data Status bit is set and a byte of zeros is written on the diskette, but the command is not terminated. When the last data byte is written, the two-byte CRC is computed internally and written, followed by a one byte gap of logic ones. The command is then terminated. Figure 3-16 illustrates the command register bit configuration for a WRITE command.

3-58. Read Address

When the Read Address command is issued, the read/write head is loaded and the Busy status bit set. The first ID field encountered is read and the six data bytes in this field are assembled and transferred to the data register. A DRQ is generated for each byte. The ID address field is shown in figure 3-17.

The FD1771 checks for validity and sets the CRC error status bit when a CRC error is detected. The sector address of the ID field is written into the sector register. When the operation is complete, an interrupt is generated and the Busy status bit reset. Figure 3-18 illustrates the command register bit configuration for a READ ADDRESS command.

3-59. Read Track

The Read Track command is implemented in the same manner as the Read Address command except the Read Enable signal

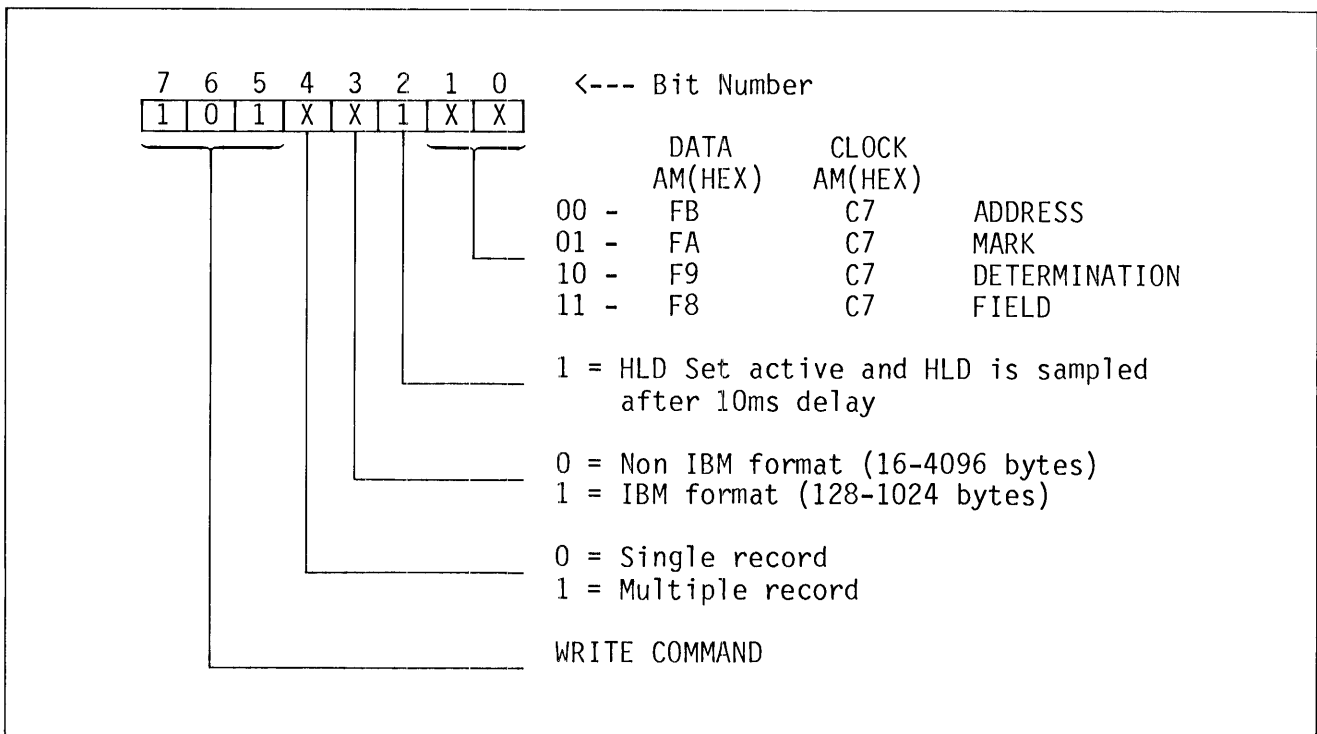


Figure 3-16. FD1771 WRITE Command.

activates coincident with the leading edge of the first Index Pulse detected. Reading continues until the next Index pulse (indicating a complete disk revolution has occurred) and then deactivates. Each byte read is assembled and transferred to the Data Register and a DRQ is generated. When bit 0 of the command is 0, the accumulation of bytes is synchronized to each address mark read. Interrupt is activated at the completion of the command. The command register bit configuration for a READ TRACK command is shown in figure 3-19.

3-60. Write Track

The Write Track command is initiated by loading the Read/Write head and setting the Busy status bit. Writing on the disk occurs coincident with the leading edge of the index pulse and terminates at the next index pulse. Data Request is activated with the receipt of the Write Track command, but no writing occurs until the first byte is read into the Data Register. If the Data Register is not loaded by the arrival of the first index pulse, the operation is terminated and interrupt activated.

BYTE #	1	2	3	4	5	6
ID ADDRESS FIELD	Track Address	Zeroes	Sector Address	Sector Length	CRC 1	CRC 2

Figure 3-17. ID Address Field Data Bytes.

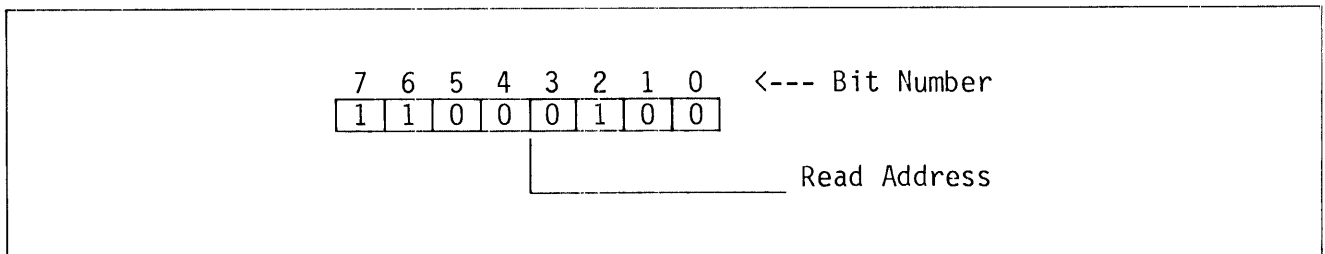


Figure 3-18. FD1771 READ ADDRESS Command.

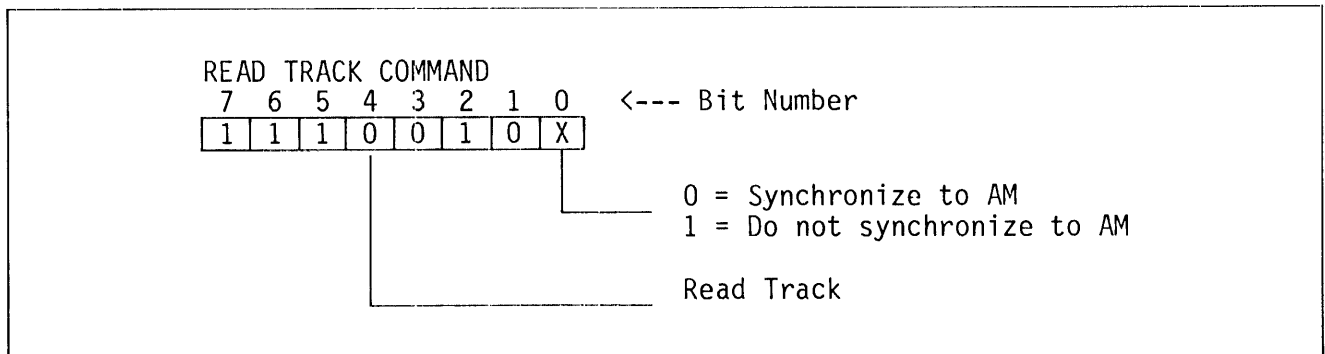


Figure 3-19. FD1771 READ TRACK Command.

If, once writing is instituted, a byte is not present in the Data Register when required, a byte of zeros is substituted. Address marks and CRC characters are written on the disk by detecting certain data patterns in the write data stream as shown in table 3-7. The CRC generator is initialized when any data byte from F7 to FE is about to be transferred from the Data Register to the Data Shift Register.

TABLE 3-7. DATA PATTERN.

Data Pattern (HEX)	Interpretation	Clock Mark
F7	Write CRC Character	FF
F8	Data Address Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7

3-61. Force Interrupt

This command can be loaded into the command register at any time. If a command is being executed (Busy Status Bit set), that command is terminated and an interrupt generated upon the selected condition programmed by bits 0 through 3. Figure 3-20 illustrates the command register for a FORCE INTERRUPT command.

3-62. STATUS REGISTER

The Status Register is located at address port 00, and at the receipt of any command, except Force Interrupt, the Busy status bit is set. Also, the rest of the status bits are updated or cleared for the new command. When the Force Interrupt Command is received and a command is being executed, the Busy status bit is reset and the other status bits remain unchanged. If no command is being executed when a Force Interrupt is received, the Busy status bit is reset and the other status bits are updated or cleared. Figure 3-21 illustrates the bit configuration of the Status Register.

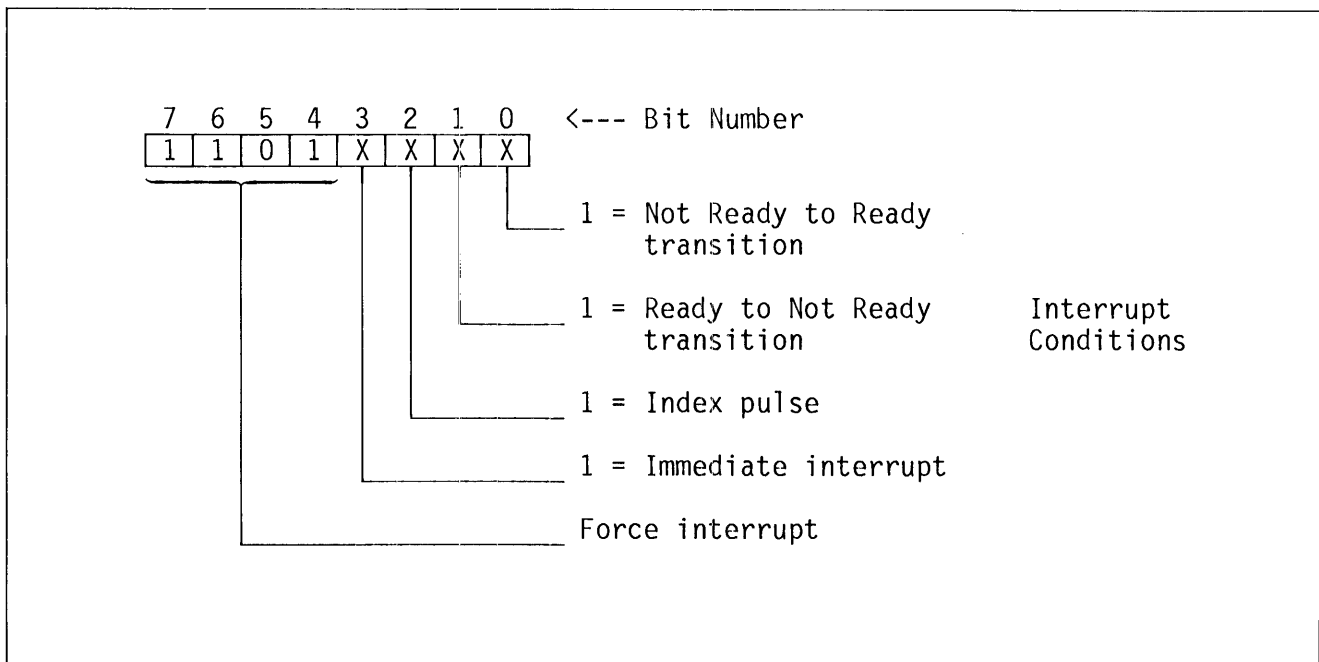


Figure 3-20. FD1771 FORCE INTERRUPT Command.

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Bit	All Type I Commands	Read Address	Read	Read Track	Write	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
A0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

FIGURE 3-21. FD1771 Status Register.

CHAPTER 4 THEORY OF OPERATION

4.1 GENERAL INFORMATION

The FDC board accepts commands and parameters from the host system, interprets the commands and produces control signals to initiate operations in the LSI circuits (FD1771A Floppy Disk Formatter/Controller and Am9517 Multimode DMA Controller), outputs operating signals to the disk units, interfaces disk data between the disk units and FD1771, and inputs status information from the disk units.

The functions to format disk data, transfer data between the FDC board and disk units, control disk unit operations, and transfer data between the FDC and Host memory are performed by the DMA controller. Functional descriptions of these operations are not included herein. Refer to the appropriate data sheets. (See references at the front of this manual).

All operations are under control of the on-board CPU and firmware. A block diagram of the Am95/6110 FDC board is shown in figure 4-1.

4-2. INSTRUCTION EXECUTION

Operations on the FDC board are the result of recognizing the command and implementing on-board firmware routines. One command is described in detail. The remaining commands are executed in a similar manner and the detailed descriptions are not included.

4-3. READ A SECTOR OPERATION

The host CPU sends the page segment parameter to R0, the MSB of the data address (in master memory) to R1, and

the LSB of the data address to R2. The command and sector count is then sent to R3.

The receipt of data into R3 causes the COMMAND-IN flip-flop (U7) to set. The status register is cleared; the board is in busy state. When in its idle state, the on-board CPU polls the state of this flip-flop. When the flip-flop sets, the on-board CPU inputs the command from R3 and determines the required operation.

In this case, a READ operation is found. The data in R0, R1, and R2 are retrieved and used to set-up the DMA controller. The DMA controller can be set to transfer either single bytes or blocks of 128 bytes for each DMA request. For this example, the DMA controller is set for single-byte DMA.

The on-board CPU then loads the track, sector, and command into the FD1771 controller. Unit, track, and sector parameters are sent from the host CPU during a previous SETPAR command.

When the sector is reached and a byte is assembled, the DREQ signal is raised. This is converted into the DMA REQUEST signal for the Am9517 DMA controller. The Am9517 sends an HREQ to the on-board CPU and a bus request is sent to the host system. When the master bus is obtained, the DMA controller generates a DMA acknowledge. This signal is also the chip select signal for the FD1771. The byte of data is transferred to main memory. When the byte is transferred, the DREQ signal is dropped and the Am9517 controller releases the CPU from HOLD.

Following transfer of the whole sector, the FD1771 generates an INTRQ to the on-board CPU. The on-board CPU is

interrupted and it then retrieves the drive status information from the FD1771 and places this information in mail-box register R4. Also, bit-7 of R4 is sent to signify that the

controller is no longer busy. If bit-6 of the previous Unit Code received was set, an interrupt request is sent to the host system. The on-board CPU returns to the Idle State.

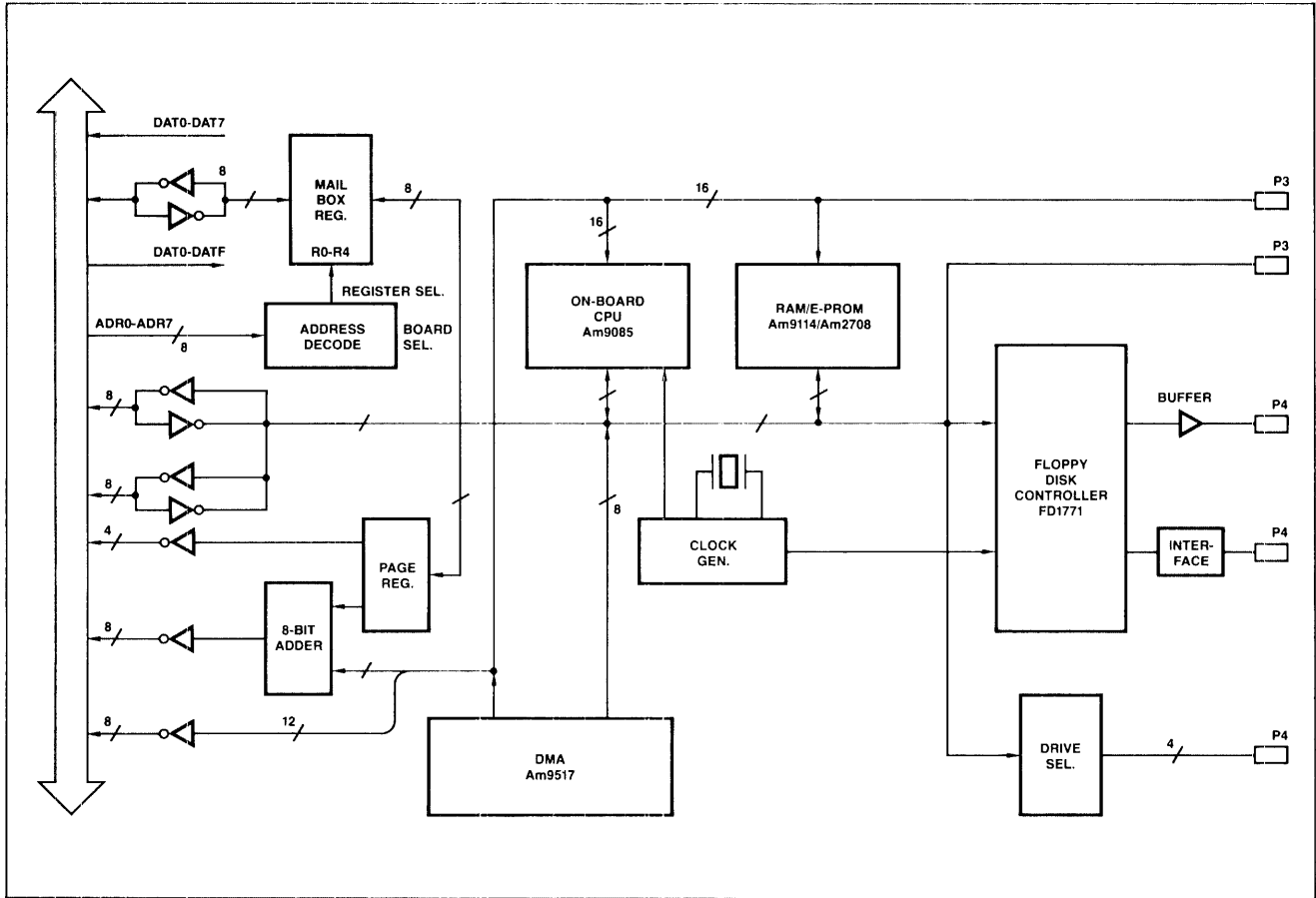


FIGURE 4-1. Floppy Disk Controller Functional Block Diagram (Control Signals are not Shown).

CHAPTER 5 SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides information on service and repair assistance, user replacement parts and service diagrams for the AMC 95/6110 Single Density Floppy Disk Controller.

5-2. SERVICE AND REPAIR ASSISTANCE

If it is necessary to return the AMC 915/6110 Floppy Disk Controller board to Advanced Micro Computers for service or repair, contact the Service Manager for OEM Products at the telephone number listed below. A Return Material Authorization number must be obtained prior to shipment. When the reshipment is due to the board being damaged during shipment from AMC, or the board is out of warranty, a purchase order is required to complete the repair.

Repackage the board in the original packing material or an equivalent substitute, and enclose in a corrugated carton suitable for shipping. Seal the shipping carton securely, mark it FRAGILE, and address to:

Advanced Micro Computers
Service Manager, OEM Products
3340 Scott Boulevard
Santa Clara, California 95051

TELEPHONE: (408) 988-7777

TOLL FREE:
800-672-3548 California
800-538-9791 U.S.A. (except
California)

5-3. USER REPLACEABLE PARTS

Listings of all user replaceable parts is provided in table 5-1. Figure 5-1 is the component location diagram.

5-4. SERVICE DIAGRAMS

The Floppy Disk Controller component locations are shown on the assembly drawing, figure 5-1. Part numbers for the components shown on the assembly drawing are listed in table 5-1.

Schematic diagrams of the Floppy Disk Controller are shown in figures 5-2 through 5-6. Active-low (logical 0) signals are specified by an asterisk (*) following the signal name.

TABLE 5-1. USER REPLACEABLE PARTS.

AMC Part Number	Description	Location
200032	Integrated circuit, Type 74LS04	U1, 10, 62
200081	Integrated circuit, Type 74LS164	U2, 5
200018	Integrated circuit, Type 74LS244	U3, 27, 34
200084	Integrated circuit, Type 74LS109	U4
200045	Integrated circuit, Type 74LS00	U6
200004	Integrated circuit, Type 74LS74	U7, 13,38, 39, 44, 68
200001	Integrated circuit, Type 74LS08	U8, 17, 61
200003	Integrated circuit, Type 74LS32	U9, 18, 19, 55, 64
210008	Integrated circuit, Type 7407	U12, 63
200021	Integrated circuit, Type 74LS253	U14, 15
220027	Integrated circuit, Type 74S257	U16
200057	Integrated circuit, Type 74LS11	U20
220022	Integrated circuit, Type 74S05	U21
220017	Integrated circuit, Type 74S04	U22
200052	Integrated circuit, Type 74LS138	U23, 24, 45
200075	Integrated circuit, Type 74LS373	U25, 35
280006	Integrated circuit, Type 8304	U26
200078	Integrated circuit, Type 74LS273	U28, 29
210007	Integrated circuit, Type 7483A	U30, 36
200016	Integrated circuit, Type 74LS240	U31, 37, 41
260028	Integrated circuit, Type 8085	U32
200080	Integrated circuit, Type 74LS260	U33
260009	Integrated circuit, Type 9517	U40
200020	Integrated circuit, Type 25LS2521	U42
230012	Integrated circuit, Type 9114E	U49, 50
280011	Integrated circuit, Type 8303	U51, 52, 58, 67
200085	Integrated circuit, Type 25LS2518	U53
220005	Integrated circuit, Type 74S139	U54
200082	Integrated circuit, Type 74LS670	U56, 57
260014	Integrated circuit, Type FD1771	U60
200083	Integrated circuit, Type 74LS123	U65
200041	Integrated circuit, Type 25LS2520	U66
200042	Integrated circuit, Type 74LS193	U69
200035	Integrated circuit, Type 74LS163	U70
220016	Integrated circuit, Type 74S240	U59
220002	Integrated circuit, Type 74S00	U11
450019	24 Pin I.C. Socket	U46, 47, 48
450021	40 Pin I.C. Socket	U32, 40, 60
690022	Switch, Recess Rocker, 6 POS.	U43
340011	Capacitor, Ceramic .1 ^μ f, 50V, 20%	C2, 3, 4
340002	Capacitor, Tantalum, 22 ^μ f, 15V, 20%	
340047	Capacitor, Tantalum, 4.7 ^μ f, 16V, 20%	C25, 26
310002	Diode, IN914	CR1, CR2
630029	Resistor, Carbon, 1K, 1/4W, 5%	R1, 6, 7 14
630017	Resistor, Carbon, 4.7K, 1/4W, 5%	R2, 3, 4, 10, 11
630033	Resistor, Carbon, 10K, 1/4W, 5%	R5, 8, 9, 15
630065	Resistor, Carbon, 27K, 1/4W, 5%	R12
630063	Resistor, Carbon, 47K, 1/4W, 5%	R13

TABLE 5-1. USER REPLACEABLE PARTS (Cont.).

AMC Part Number	Description	Location
630014	Resistor, Network, 4.7K, 8 Pos.	RP1, 4, 5
630057	Resistor, Network, 4.7K, 6 Pos.	RP2
630056	Resistor, Network, 4.7K, 10 Pos.	RP3, 6, 7
630500	Resistor, Network, 10K, 6 Pos.	RP9
630508	Resistor, Network, 1K, 6 Pos.	RP8
480011	8MHz Clock, OSC	Y1

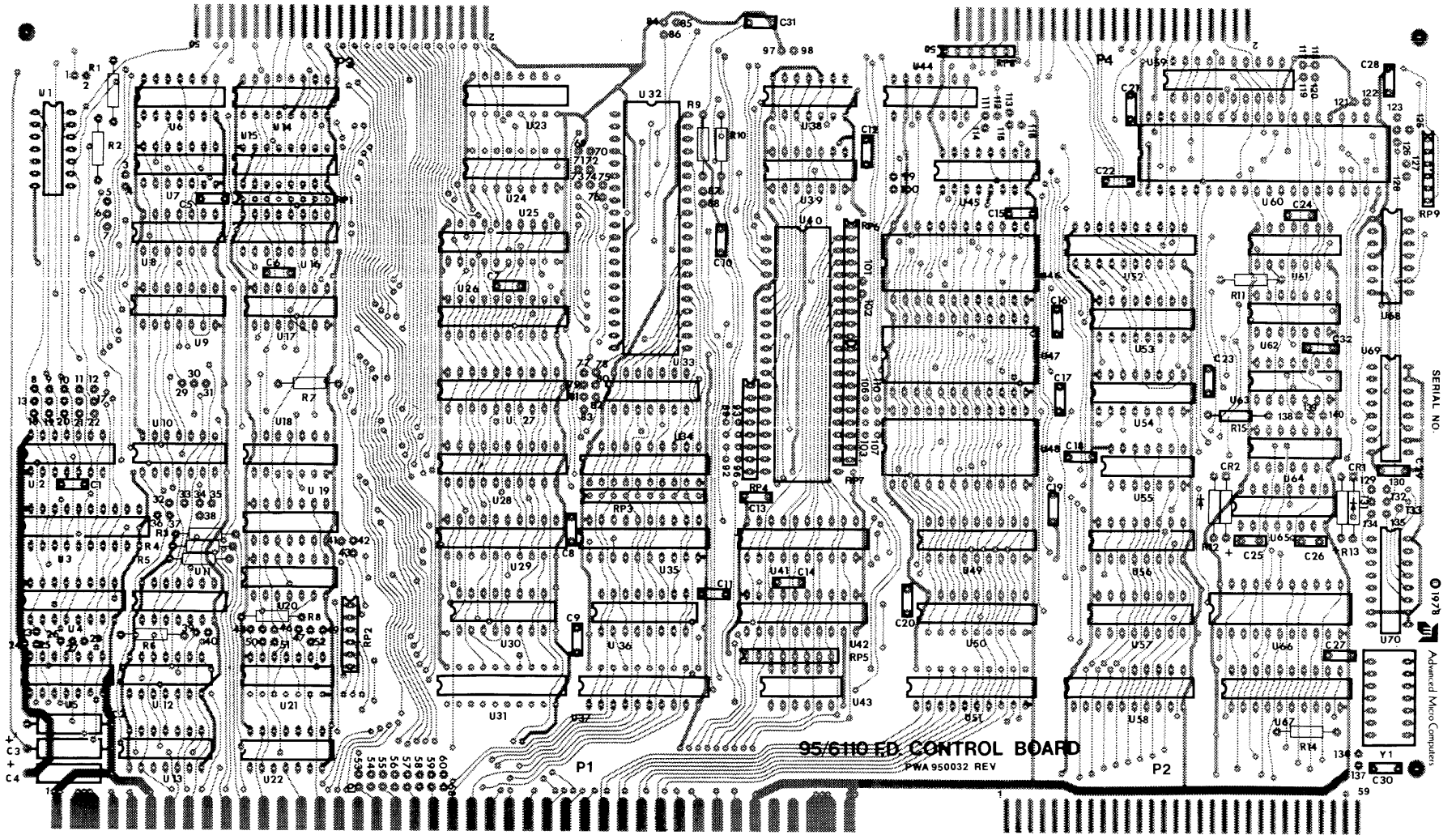
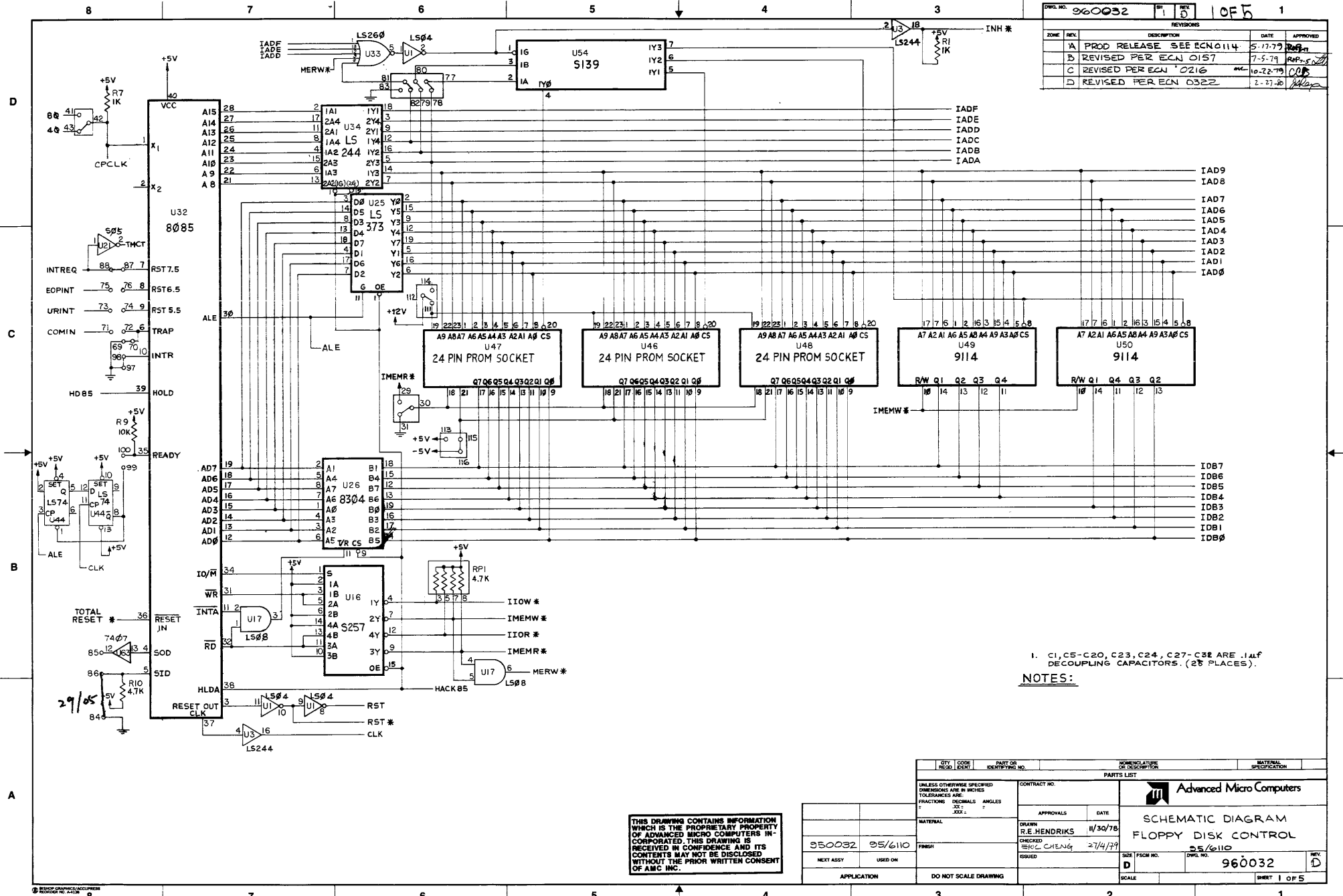


Figure 5-1. Am95/6110 Components Location.



REV. NO.		REV. NO.		REV. NO.	
ZONE	REV.	DESCRIPTION	DATE	APPROVED	
A	1	PROD RELEASE SEE ECN 0114	5-17-79	<i>[Signature]</i>	
B	2	REVISED PER ECN 0157	7-5-79	<i>[Signature]</i>	
C	3	REVISED PER ECN 0216	10-22-79	<i>[Signature]</i>	
D	4	REVISED PER ECN 0322	2-27-80	<i>[Signature]</i>	

1. C1, C5-C20, C23, C24, C27-C32 ARE .1uF DECOUPLING CAPACITORS. (28 PLACES).

NOTES:

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QTY	CODE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES			CONTRACT NO.	
MATERIAL			APPROVALS DATE	
NEXT ASSY			DRAWN R.E.HENDRIKS 11/30/78	
USED ON			CHECKED S.H.CHEUNG 2/7/79	
APPLICATION			ISSUED	
DO NOT SCALE DRAWING			SIZE FROM NO. 35/6110	
			DWG. NO. 960032	
			SCALE	
			SHEET 1 OF 5	

Figure 5-2. Am95/6110 Schematic Sheet 1.

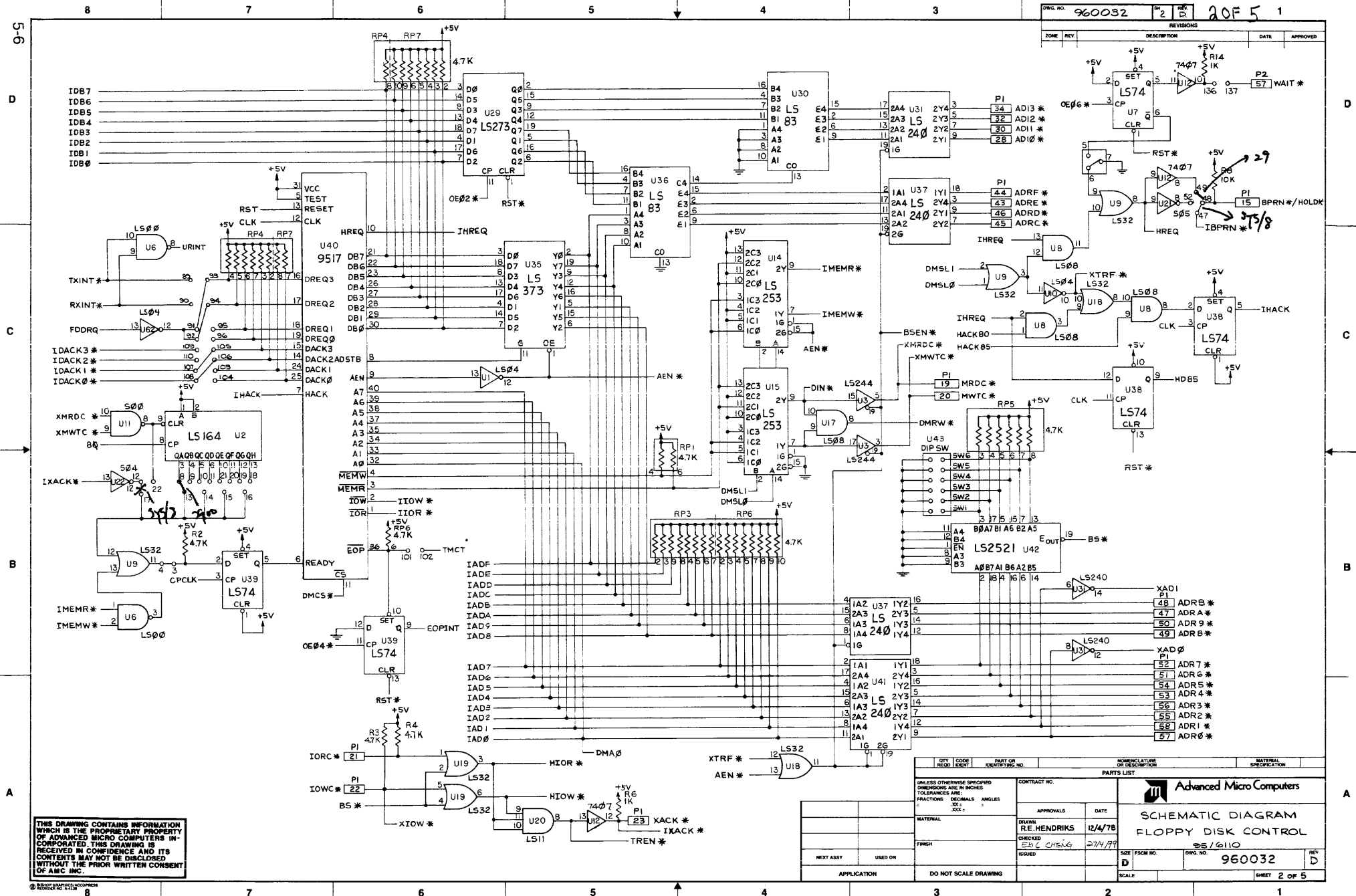
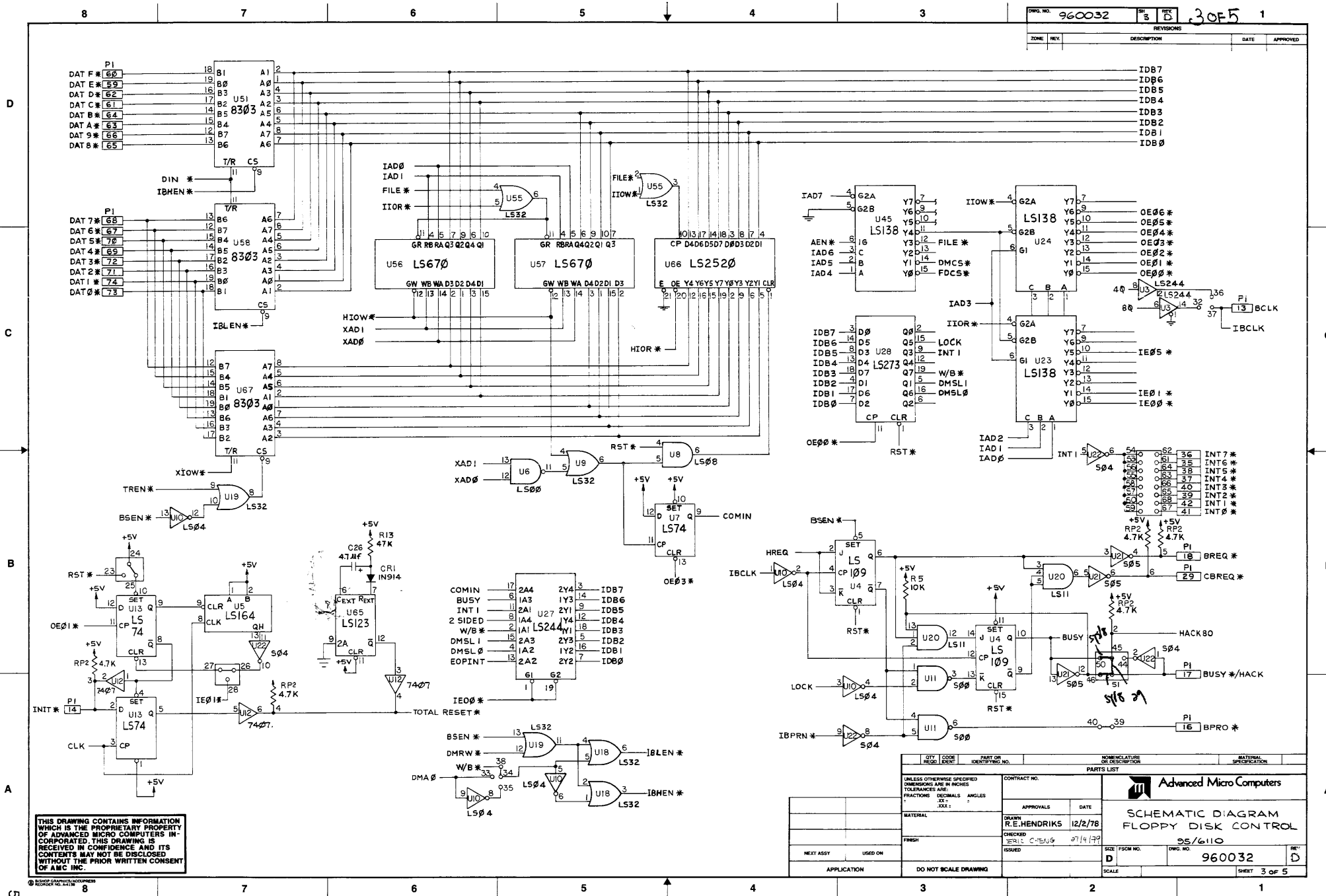


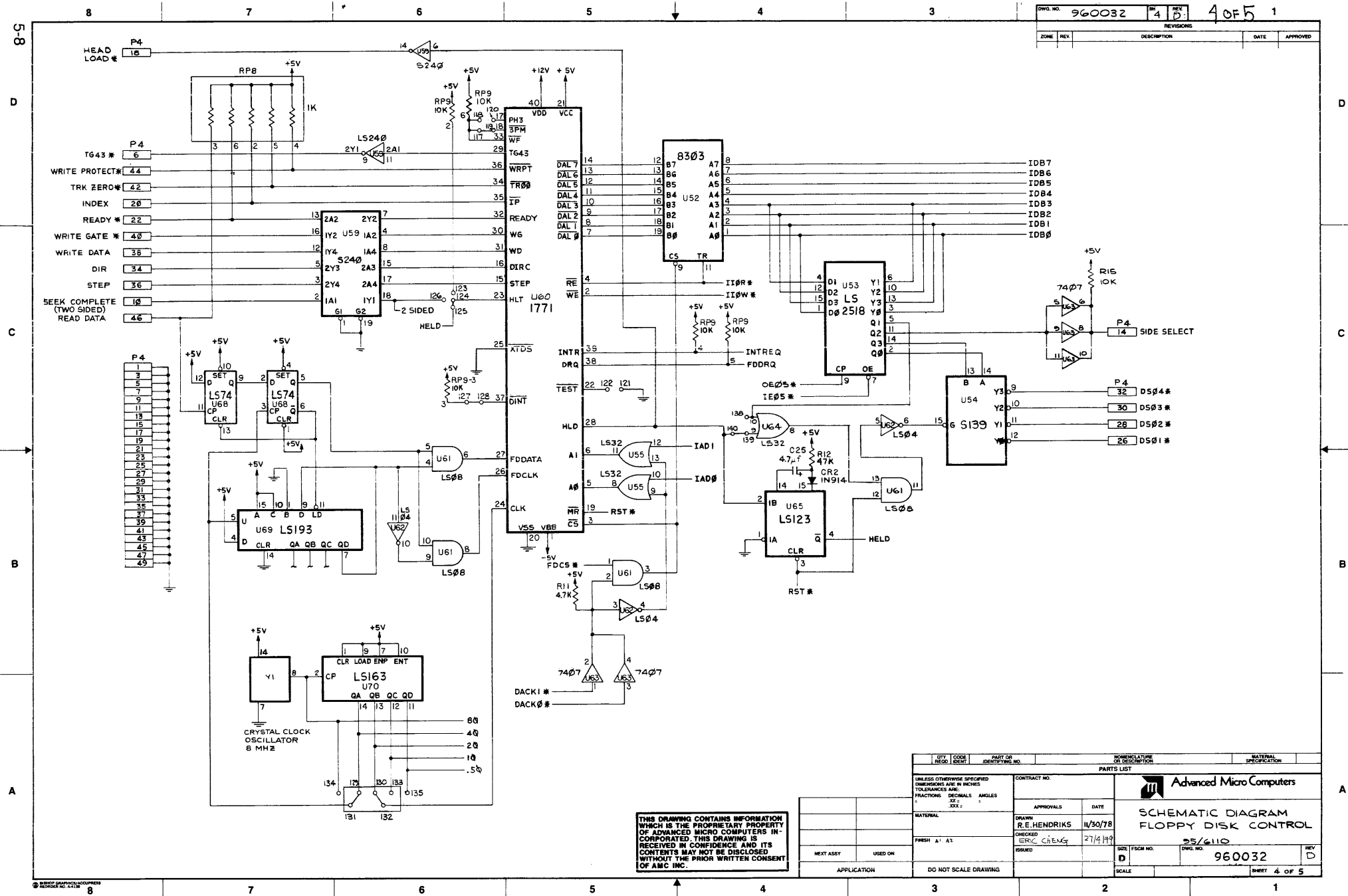
Figure 5-3. Am95/6110 Schematic Sheet 2.



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QTY		CODE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION
PARTS LIST						
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES			CONTRACT NO.		Advanced Micro Computers	
XXX .XXX .			APPROVALS		DATE	
MATERIAL			DRAWN		12/2/78	
FINISH			CHECKED		9714/199	
NEXT ASSY			ISSUED		95/6110	
USED ON			SIZE		DWG. NO. 960032	
APPLICATION			SCALE		SHEET 3 OF 5	
DO NOT SCALE DRAWING						

Figure 5-4. Am95/6110 Schematic Sheet 3.

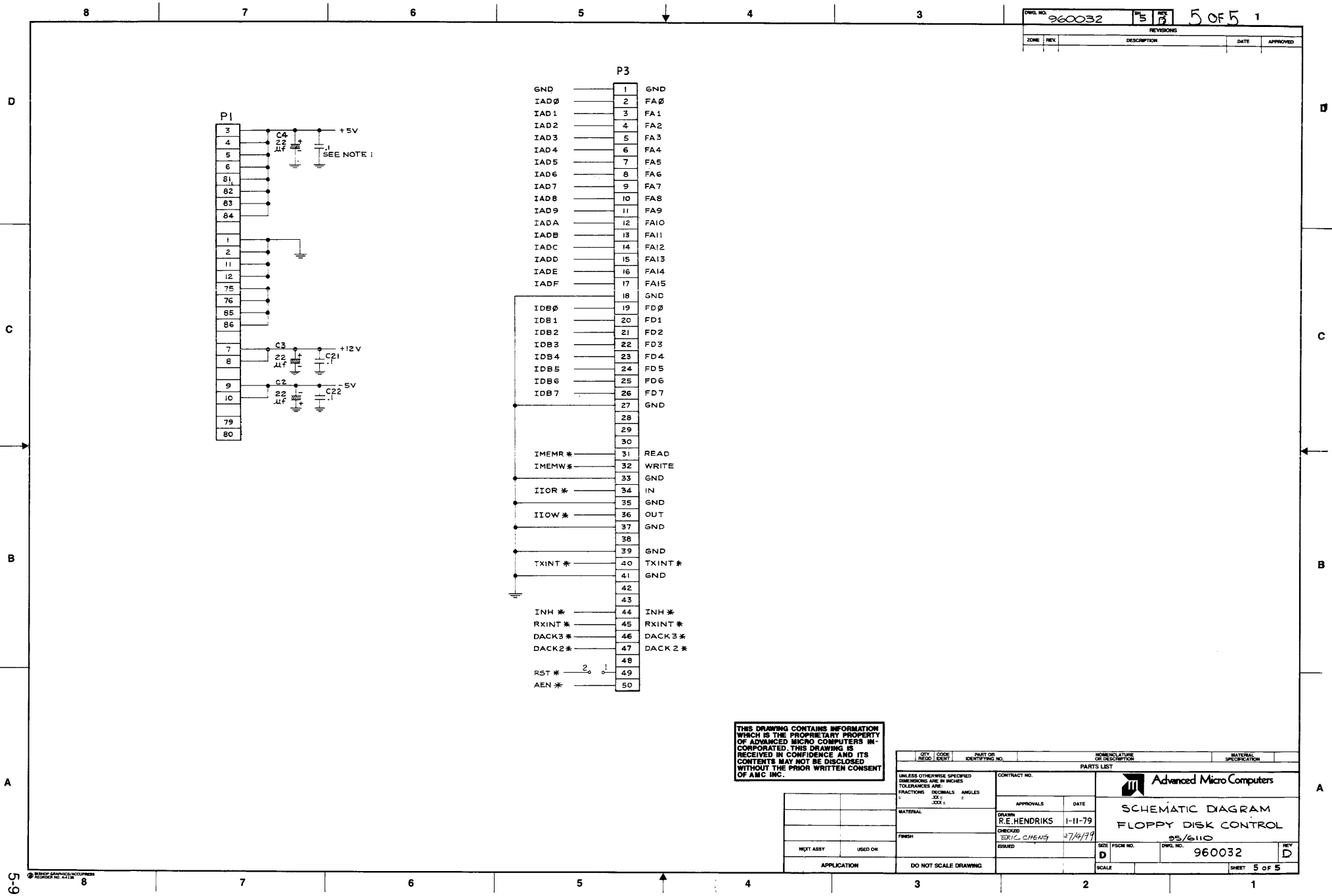


DWG. NO. 960032		REV. 4	REV. 4 OF 5
REVISIONS		DATE	APPROVED
ZONE	REV.	DESCRIPTION	

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UTL. CODE	PART OR IDENTIFYING NO.	QUANTITY	DESCRIPTION	MATERIAL SPECIFICATION
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES		CONTRACT NO.		
FRESH A1 A1		APPROVALS DATE		
NEXT ASSY USED ON		DRAWN R.E.HENDRIKS 11/30/78		
APPLICATION		CHECKED ERIC CHENG 2/14/79		
DO NOT SCALE DRAWING		ISSUED		
SCALE		SIZE FROM NO. 95/6110		
D		DWG. NO. 960032		
REV. D		SHEET 4 OF 5		

Figure 5-5. Am95/6110 Schematic Sheet 4.



DWG. NO. 960032		REV. 1		SHEET 5 OF 5	
ZONE	REV.	DESCRIPTION	DATE	APPROVED	

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CITY CODE PART OR IDENTIFYING NO.		NOMENCLATURE OR DESCRIPTION		MATERIAL SPECIFICATION	
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:		CONTRACT NO.		Advanced Micro Computers	
FRACTIONS	DECIMALS	ANGLES	APPROVALS	DATE	SCHEMATIC DIAGRAM FLOPPY DISK CONTROL 25/6110 DWG. NO. 960032 REV. D
		DRAWN R.E.HENDRIKS		1-11-79	
		CHECKED TREV. CHENS		27/4/79	
NEXT ASSY USED ON		ISSUED		SIZE PSCN NO.	D
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Figure 5-6. Am95/6110 Schematic Sheet 5.

COMMENT SHEET

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