UNIMAP
Preliminary
User's Guide

10143X07

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CHAPTER 1

How To Use This Manual

Congratulations on your purchase of a UNIMAP from ABLE Computer. We are sure that it will provide you with years of satisfactory service. We have prepared this manual to help you maximize the effectiveness of the UNIMAP in your system.

This manual is provided to assist you with the installation, use and care of the UNIMAP; it does not provide repair information. If you have problems with your UNIMAP, we prefer that you let us repair it in our factory.

This manual asssumes that you are familiar with the PDP-11 Unibus and LSI-11 Q Bus architecture. For information about these architectures, refer to the following DEC documents:

* Microcomputers and Memories Handbook
* PDP-11 Peripherals Handbook
* PDP-11 Terminals and Communications Handbook

This manual is organized into the following chapters:

* Chapter 2 provides a general description, a functional description and a list of the primary features of UNIMAP. It also includes electrical, physical, and environmental specifications.
* Chapter 3 describes the installation procedure for UNIMAP. This includes unpacking information, as well as information on setting the upper and lower mapping limits, selecting the pin connector for map enable input, and enabling the LTC. It also provides installation verification information.
* Chapter 4 tells who to call for service and how to contact them.
* Chapter 5 provides applications information.

* Chapter 6 contains programming information, which includes information on the I/O map registers and the clock status register.

* Appendix A supplies backplane modification information to acheive 22-bit addressing on the Q bus.

* Appendix B describes how to patch RSTS/E v7.Ø to run with 22-bit parity memories.

CHAPTER 2

What Is UNIMAP?

2.1 GENERAL DESCRIPTION

The UNIMAP is a quad-width board (see Figure 2-1) which performs the following three main functions:

* Serves as a Q Bus to Unibus convertor.

* Increases the addressing capability of the Unibus up to 4 megabytes on the Q bus.

* Provides a KW11-L compatible line time clock.

With UNIMAP, memories and interrupt devices may reside on the Q Bus. DMA and interrupt devices may reside on the Unibus. The 18-bit addresses of NPR devices are mapped through the UNIMAP onto the 22-bit Q bus.

UNIMAP installs into a quad slot of an LSI-11 backplane and interfaces to the Q bus via the A and B connectors on the board. A pair of Unibus connectors on the UNIMAP provide connection to a Unibus cable (not supplied). The physical arrangement is specifically designed to allow users easy connection of a Unibus cable for external Unibus devices. UNIMAP also provides one end of Unibus termination.

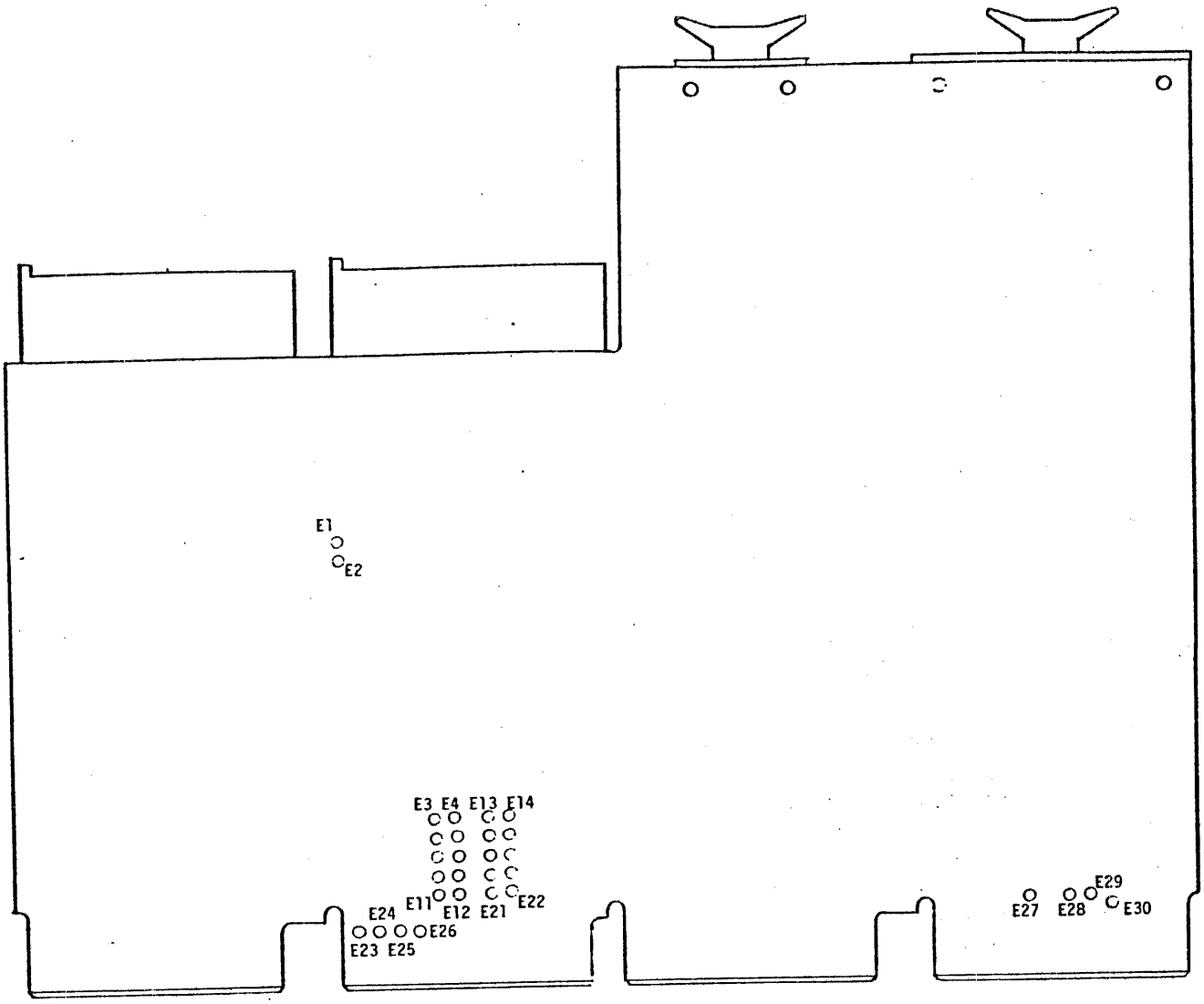

Figure 2-1: UNIMAP Board Layout

2.2 FEATURES

* UNIMAP supplies -11/23 systems with the I/O mapping capability of -11/70's, -11/44's, or PAX-enhanced -11/24's with up to 4 megabytes of main memory fully available for optimization of CPU, Q Bus and/or Unibus operations.

* Provides Line Time Clock (LTC) function to maintain software compatibility with existing operating systems.

* Adds I/O map (IOM) functions providing software compatible 4 megabyte addressing for 18-bit DMA devices.

* Supports the addition of up to 19 bus loads to any existing -11/23 system.

* Provides front-end Unibus termination.

* Special memory implementations, like Unibus bus window and Unibus dual port memory are allowed.

* UNIMAP is software compatible with RSTS/E, RSX-11 and UNIX.

2.3 SPECIFICATIONS

2.3.1 Electrical Specifications

Q Bus Loading	1 DC Load 2 AC Loads
Drive Capability	19 Unibus loads
Power Required	5.1 amps @ +5V, $\pm$12V not required
Priority Level	The LTC has a fixed interrupt level of 6.
Vector Setting	The LTC has a fixed vector setting of 100 (octal).

2.3.2 Physical Specifications

Size	Standard quad-width module measuring 10.45 x 8.40 inches (excluding handles).
External Connection	Two connectors compatible with a standard Unibus extender cable.

2.3.3 Environmental Specifications

Operating Temperature	5 C to 40 C (41 F to 104 F). Derate maximum temperature by one degree Celsius for each 1,000 feet of altitude above 8,000 feet.
Storage Temperature	-40 C to 65 C (-40 F to 149 F)
Relative Humidity	10% to 90% non-condensing
Altitude	To 15,000 feet

2.4 FUNCTIONAL DESCRIPTION

UNIMAP converts accesses on the Q bus into Unibus accesses. Q bus lines BDAL13 through BDAL21 and BBS7 are monitored for addresses in the range 3840K to 4096K bytes. Master sync is asserted in the Unibus only for accesses in that range.

Interrupt cycles on the Unibus are converted into interrupt cycles on the Q bus at the same level. For example, BR4 is converted to BIRQ4. The UNIMAP adheres to the position independent priority rules of the Q bus.

DMA cycles on the Unibus are converted to cycles on the Q bus. This includes mapping from 18-bit Unibus addresses to 22-bit Q bus addresses. BSYNC is asserted on the Q bus only for Unibus cycles in the range 0K to 248K bytes. This range may be changed in 8K byte increments within 0 to 248K by upper/lower limit straps on the UNIMAP.

Mapping of Unibus DMA devices is enabled by bit 5 of SR3 in the Memory Management Unit of the -11/23. This bit is present as a low true signal at pin AR2 of the

processor board. As this pin is normally used as BDMGI on the Q bus, and cannot be bussed into other slots, the UNIMAP is designed to take the Map Enable signals from pin AF1, pin AH1, or pin BH1.

A programmable Line Time Clock (LTC) is provided on the UNIMAP. When interrupts are enabled in its CSR, an interrupt to 100 (octal) is generated at BR6 for every clock tick. The clock signal is received from the BEVNT line of the Q bus. This line is generally sourced by the power supply, but may also be generated by an MXV11. The frequency is generally 50 or 60 Hz. The LTC may be disabled by removing a strap on the UNIMAP. If the LTC is used, the BEVNT interrupt of the -11/23 processor should be disabled.

CHAPTER 3

How To Install UNIMAP

3.1 UNPACKING UNIMAP

UNIMAP is shipped in a special container to prevent any damage during shipment. Unpack it carefully and verify that no damage has occurred. If there is damage, notify the carrier immediately. Save the shipping carton to show proof of damage or in case the product requires shipment.

3.2 VERIFY THAT YOU RECEIVED WHAT YOU ORDERED

Be sure that you have received what you ordered by checking the product number on the component side of the board near the handles. The UNIMAP product number is 10142. (See photo in Figure 2-1).

If you have not received the correct equipment, notify our factory immediately.

3.3 EQUIPMENT NEEDED TO USE UNIMAP

To incorporate UNIMAP in an LSI-11/23 or PDP-11/23 system, the following user-supplied equipment is needed:

* Unibus cable
* M930 Unibus terminator or equivalent
* Unibus backplane for installation of controllers

* Appropriate power source
* Q bus backplane which provides for 22-bit addressing

NOTE

Refer to Appendix A, Backplane Modification, for directions on modifying a backplane for 22-bit addressing.

3.4 E POINT INFORMATION

The UNIMAP board contains 30 E points which provide for various user-selectable functions. Refer to Figure 2-1 for the location of these E points and to Table 3-1 for a brief listing of their functions. The following sections provide more detail.

E POINTS	FUNCTION
E1, E2	LTC Enable/Disable
E3 through E12	Set lower limit of mapping
E13 through E22	Set upper limit of mapping
E23 through E26	Pass bus grant signals (DMG, IAK)
E27 through E30	Pick up map enable signal from backplane

Table 3-1: E Point Functions

3.5 LTC ENABLE/DISABLE

The LTC is enabled by installing a jumper from E1 to E2. It is normally enabled. If you desire to disable the LTC, simply remove the jumper.

3.6 I/O MAP LIMITS

3.6.1 Lower I/O Map Limits

The lower I/O mapping limit is set using points E3 through E12. Refer to Table 3-2 to determine how to achieve your desired setting.

Unibus Memory Start Address	E3-E4	E5-E6	E7-E8	E9-E10	E11-E12
0KB	I	I	I	I	I
8KB	I	I	I	I	-
16KB	I	I	I	-	I
24KB	I	I	I	-	-
32KB	I	I	-	I	I
40KB	I	I	-	I	-
48KB	I	I	-	-	I
56KB	I	I	-	-	-
64KB	I	-	I	I	I
72KB	I	-	I	I	-
80KB	I	-	I	-	I
88KB	I	-	I	-	-
96KB	I	-	-	I	I
104KB	I	-	-	I	-
112KB	I	-	-	-	I
120KB	I	-	-	-	-
128KB	-	I	I	I	I
136KB	-	I	I	I	-
144KB	-	I	I	-	I
152KB	-	I	I	-	-
160KB	-	I	-	I	I
168KB	-	I	-	I	-
176KB	-	I	-	-	I
184KB	-	I	-	-	-
192KB	-	-	I	I	I
200KB	-	-	I	I	-
208KB	-	-	I	-	I
216KB	-	-	I	-	-
224KB	-	-	-	I	I
232KB	-	-	-	I	-
240KB	-	-	-	-	I
248KB*	-	-	-	-	-

"I" = Jumper Installed; "-" = Jumper Removed
* = Factory Setting

Table 3-2: I/O Map Lower Limit Jumper Settings

3.6.2 Upper I/O Map Limits

The upper I/O mapping limit is set using points E13 through E22. Refer to Table 3-3 to determine how to achieve your desired setting.

Unibus Memory End Address	E13-E14	E15-E16	E17-E18	E19-E20	E20-E21
8KB	I	I	I	I	I
16KB	I	I	I	I	-
24KB	I	I	I	-	I
32KB	I	I	I	-	-
40KB	I	I	-	I	I
48KB	I	I	-	I	-
56KB	I	I	-	-	I
64KB	I	I	-	-	-
72KB	I	-	I	I	I
80KB	I	-	I	I	-
88KB	I	-	I	-	I
96KB	I	-	I	-	-
104KB	I	-	-	I	I
112KB	I	-	-	I	-
120KB	I	-	-	-	I
128KB	I	-	-	-	-
136KB	-	I	I	I	I
144KB	-	I	I	I	-
152KB	-	I	I	-	I
160KB	-	I	I	-	-
168KB	-	I	-	I	I
176KB	-	I	-	I	-
184KB	-	I	-	-	I
192KB	-	I	-	-	-
200KB	-	-	I	I	I
208KB	-	-	I	I	-
216KB	-	-	I	-	I
224KB	-	-	I	-	-
232KB	-	-	-	I	I
240KB	-	-	-	I	-
248KB*	-	-	-	-	I

"I" = Jumper Installed; "-" = Jumper Removed
* = Factory Setting

Table 3-3: I/O Map Upper Limit Jumper Settings

3.7 BUS GRANT SIGNALS

Jumpers from E23-E24 and E25-E26 are implemented in etch and perform the following functions:

E23-E24	Passes DMG to devices located behind the UNIMAP
E25-E26	Passes IAK to devices located behind the UNIMAP

NOTE

These jumpers may need to be removed if connectors C and D are used for something other than the Q bus.

3.8 MAP ENABLE

The Unibus Map Enable signal is not bussed on any backplanes. It is sourced by the -11/23 processor at pin AR2, which is normally BUS-DMG-IN-L.

The UNIMAP may receive this signal on pin AF1, pin AH1, or pin BH1. The user must wrap his backplane from pin AR2 of the processor slot to one of three pins in the UNIMAP board slot. Refer to Table 3-4.

E27 TO	USES CONNECTOR PIN
E28	BH1
E29	AH1
E30	AF1

Table 3-4: Map Enable Input

3.9 INSTALLING UNIMAP

UNIMAP may be installed in any quad-slot of an -11/23. Every empty slot between the UNIMAP and the processor must contain a Q bus grant card. If grant cards are not available, there must be no empty slots between boards.

UNIMAP follows the position independent priority rules of the Q bus. LSI-11 interfaces and memories can be located either ahead of or behind the UNIMAP. Devices located behind UNIMAP have a lower priority than Unibus devices of the same level attached to the UNIMAP. Refer to Chapter 12 of the Microcomputers and Memories Handbook for further information.

Unibus peripherals are installed in a Unibus backplane which must be supplied with the appropriate power. An M930 terminator (or equivalent) must be installed in connectors A and B of the last slot of the last Unibus backplane. The Unibus backplane is connected to UNIMAP with a standard Unibus extender cable connected between the first Unibus connectors in the Unibus backplane and the connectors on the top end of the UNIMAP board.

3.10 INSTALLATION VERIFICATION

UNIMAP may be used under DECX/11 using the "E" monitor. The KWA module may be included to exercise the LTC.

The UNIMAP is totally software transparent to the -11/23 system. Therefore, any diagnostic appropriate for the device attached through UNIMAP to the arbitrating system bus may be used to verify proper installation.

NOTE

Certain device/memory diagnostics may not be completely computer independent. Consult the diagnostic listing for the applicable devices and computer(s).

With UNIMAP installed, the computer system is provided with a second bus structure: Unibus. The arbitration of the two buses is performed by the -11/23 processor.

CHAPTER 4

What to Do if UNIMAP Does Not Work

4.1 HOW TO CARE FOR UNIMAP

ABLE products are designed to provide years of service with a minimum of care. Here are a few tips to help you avoid problems.

* If a printed circuit board is frequently inserted and removed, it tends to build up a gum-like residue on the contacts. Clean this off using alcohol or freon. Use of a pencil eraser can remove some of the gold on the contacts, so if you choose to use one, go easy.

* Every six months remove each printed circuit board and clean off any accumulated dust. Dust can impede air flow. While the board is out, inspect it for any visual evidence of a potential problem such as damaged components, loose connections, etc.

* If a problem arises with the operation of your UNIMAP, follow the steps outlined below.

4.2 WHO TO CALL FOR SERVICE WITHIN THE UNITED STATES

Able's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

If your UNIMAP does not function properly and you are within the United States, contact our Product Support Center before sending it for repair. Have serial numbers available when calling.

ABLE Computer
1732 Reynolds Avenue
Irvine, California 92714
(714) 979-7030
TWX 910-595-1729

If your product requires repair, we prefer that you return it to the factory. Use the original container(s) or a corregated cardboard carton with at least one inch of cushioning material on all sides. Include a description of the problem and a hard copy of the failure mode or diagnostic printout when available. Be sure to include your name, address, and telephone number. Ship it to the above address.

4.3 WHO TO CALL FOR SERVICE OUTSIDE THE UNITED STATES

Able's goal is to provide each customer with a product that works well in his system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to quickly and efficiently solve it.

If your UNIMAP does not function properly, contact your local distributor or telex ABLE Computer for the name and address of your local distributor:

TWX 910-595-1729

In England telex our London office at:

Telex 848715 ABLE G

In Germany, telex our Haar, (near Munich) office at:

Telex 5213883 ABLE D

CHAPTER 5

How To Use UNIMAP

UNIMAP allows the wide range of PDP-11 Unibus peripherals to address 4 megabytes of Q bus memory. The UNIMAP can be installed in any quad slot of the LSI-11/23 and PDP-11/23 systems. Other LSI-11 interfaces and memories can be located either ahead of or behind the UNIMAP. Devices located behind UNIMAP have a lower priority than the Unibus devices of the same level attached to the UNIMAP.

Unibus peripherals are installed in a Unibus backplane which must be supplied with the appropriate power. An M930 terminator (or equivalent) must be installed in connectors A and B of the last slot of the last Unibus backplane. The Unibus backplane is connected to UNIMAP with a standard Unibus extender cable connected between the first Unibus connectors in the Unibus backplane and the connectors on the top end of the UNIMAP.

UNIMAP provides the LSI-11/23 system with a second bus structure, Unibus. The LSI-11/23 processor controls the arbitration of both buses.

CHAPTER 6

How To Program UNIMAP

UNIMAP provides the LSI-11/23 system of which it is a part with a second bus structure: Unibus. The UNIMAP is completely software transparent to the host computer. Note that UNIMAP is designed to operate with a single computer performing bus arbitration; it is not intended to be used as an interprocessor coupler.

Since UNIMAP is software transparent to the host computer, any diagnostic appropriate for the device(s) being connected through UNIMAP to the system may be used to verify system operation. Note that certain device/memory diagnostics may not be completely computer independent. Consult the diagnostic listing for the applicable devices and computer(s).

NOTE

A KEY CONSIDERATION IS TO INSURE THAT ADDRESS ASSIGNMENTS OF DEVICES ON THE UNIBUS AND Q BUS DO NOT CONFLICT.

6.1 I/O MAP REGISTERS

The 32 I/O map registers provide direct memory access (DMA) address offset. Each I/O map register is a 22-bit, 2 word register. The low order word contains the 16 least significant bits (15-0) and the high order word contains the 6 most significant bits (21-16). The contents of these registers are user programmable via software control.

DMA address offset is accomplished as follows:

* The upper five bits (17-13) of the DMA virtual address select one of 32 I/O map registers. If this address is outside of the limit switches, the cycle is not passed to the Q bus.

* Bits 12-1 of the DMA virtual address are added to bits 21-1 of the I/O map register and the sum placed in bits 21-1 of the physical address.

* Bit Ø of the DMA virtual address is placed directly into bit Ø of the physical address.

Figure 6-1 illustrates the DMA memory offset. Table 6-1 provides addressing information for the map registers.

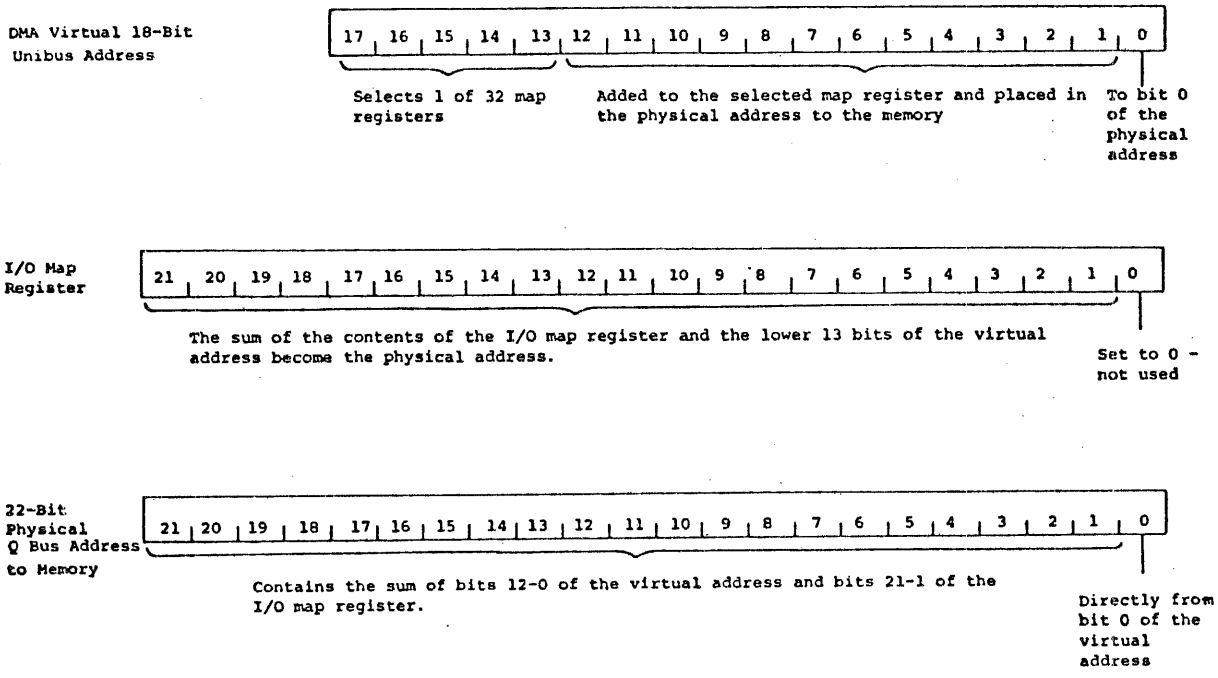

Figure 6-1: DMA Memory Offset

Map Register Number	Physical Address Low Word	High Word	DMA Virtual Address
0	17770200	17770202	00XXXX
1	17770204	17770206	02XXXX
2	17770210	17770212	04XXXX
3	17770214	17770216	06XXXX
4	17770220	17770222	10XXXX
5	17770224	17770226	12XXXX
6	17770230	17770232	14XXXX
7	17770234	17770236	16XXXX
10	17770240	17770242	20XXXX
11	17770244	17770246	22XXXX
12	17770250	17770252	24XXXX
13	17770254	17770256	26XXXX
14	17770260	17770262	30XXXX
15	17770262	17770264	32XXXX
16	17770270	17770272	34XXXX
17	17770274	17770276	36XXXX
20	17770300	17770302	40XXXX
21	17770304	17770306	42XXXX
22	17770310	17770312	44XXXX
23	17770314	17770316	46XXXX
24	17770320	17770322	50XXXX
25	17770324	17770326	52XXXX
26	17770330	17770332	54XXXX
27	17770334	17770336	56XXXX
30	17770340	17770342	60XXXX
31	17770344	17770346	62XXXX
32	17770350	17770352	64XXXX
33	17770354	17770356	66XXXX
34	17770360	17770362	70XXXX
35	17770364	17770366	72XXXX
36	17770370	17770372	74XXXX
37	17770374	17770376	76XXXX

Table 6-1: I/O Map Register Addressing

6.2 CLOCK STATUS REGISTER (17777546)

The Clock Status Register (CLKS) controls the line time clock. Figure 6-2 supplies the register format for the clock status register.

Bit	Description
15-Ø8	Not used.
Ø7	Monitor. This read/write Ø only bit is set by the clock and cleared by the program.
Ø6	Interrupt Enable. When set, the clock will generate an interrupt at PR6 through location 1ØØ (octal). This bit is Read/Write.
Ø5	Maintenance. When set, processor reads to the Unibus address space selected for mapping will return, as data, the relocated address.
Ø4-ØØ	Not used.

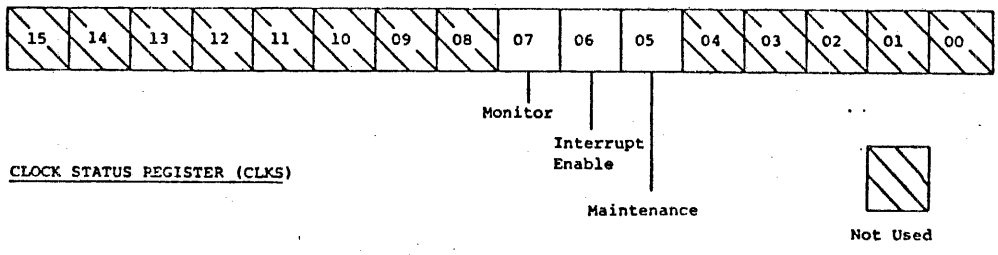

Figure 6-2: Clock Status Register Format

APPENDIX A

BACKPLANE MODIFICATION

This appendix describes how to modify a backplane for 22-bit addressing on the Q bus.

22-bit addressing on the Q bus is provided only by the DEC H9275-A backplane. Other backplanes do not provide for 22-bit addressing.

To use backplanes other than the H9275-A, the user may need to bus the upper address lines. They are found on the following pins:

BUS-DAL18-L	BC1
BUS-DAL19-L	BD1
BUS-DAL20-L	BE1
BUS-DAL21-L	BF1

Older memories, such as 16 or 18 address bit memories, will not function properly with the UNIMAP.

APPENDIX B

PATCHING RSTS/E V7.Ø

This appendix describes how to patch RSTS/E v7.Ø to run with 22-bit parity memories.

INIT v7.0 does not initialize all memory when run on a 22-bit system. This may cause problems with RSTS after a power-up due to random data and parity left in memory. The following patch allows INIT to correct all parity bits.

```
OPTION: PATCH INIT.SYS
BASE ADDRESS? DEFAULT
OFFSET ADDRESS? 4602
  BASE  OFFSET   OLD      NEW?
XXXXXX  004602   012701?  401
XXXXXX  004604   000002?  ↑C

OPTION:
```